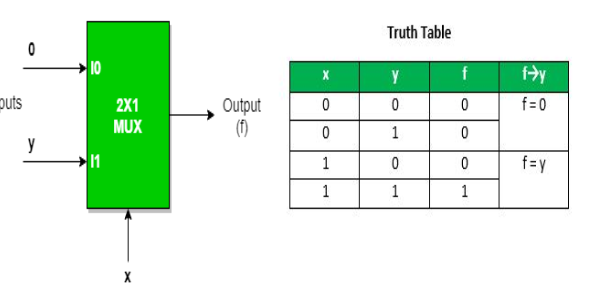
**COA**

**DCSE, UET Peshawar**

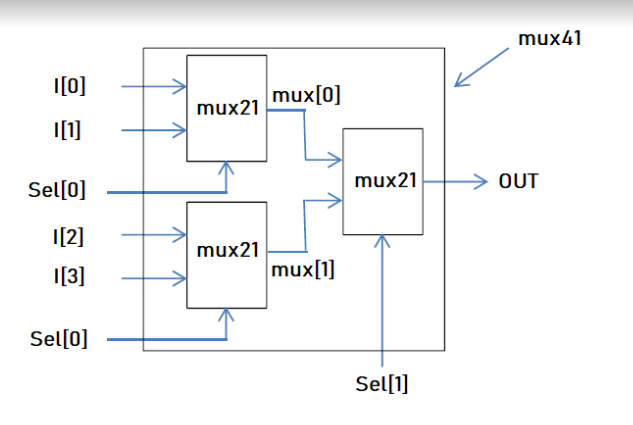
**LAB 7**

**MULTIPLEXER IN VERILOG:**

Q NO 1: implement 2X1 MUX in Verilog.



Q NO 2: Implement 4X1 MUX using 2X1 MUX.



QNO 3: Design MUX where if the select to a MUX is 00 it will output A , 01 the output will be B , for 10 the output will be A+B and for 11 the output will be A-B.