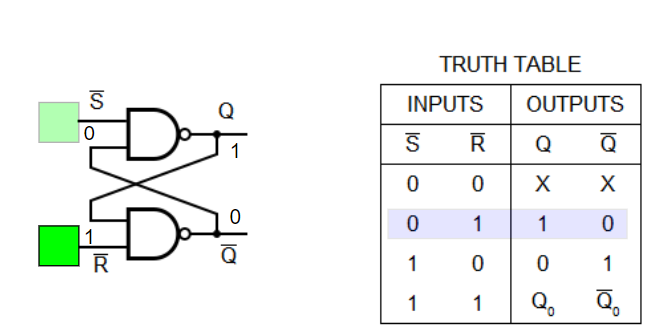
**COA**

**DCSE, UET Peshawar**

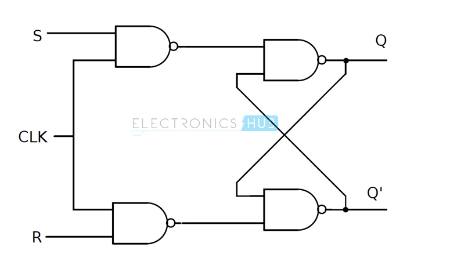
**LAB 9**

**FLIP FLOP AND LATCHES IN VERILOG:**

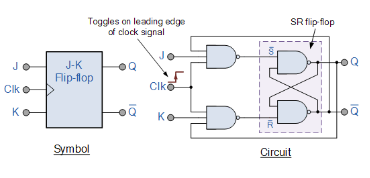
Q NO 1: Write a Verilog code to implement S R latch.



Q NO 2: Implement SR flip flop in Verilog .

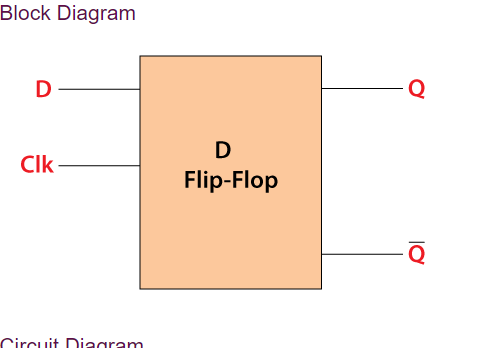


QNO 3: implement JK Flip Flop in Verilog

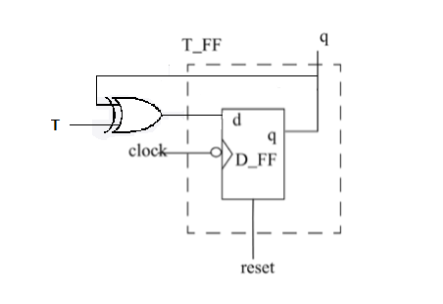


Q NO 4: Design D Flip Flop in Verilog

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Q NO 5: Design T Flip Flop using D Flip Flop in Verilog.

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