An Optimized Topology for Next-to-Next Balancing of Series-Connected Lithium-ion Cells

Thanh Hai Phung, Alexandre Collet, and Jean-Christophe Crebier

***Abstract*—Voltage balancing between series-connected cells of rechargeable lithium-ion batteries is important for battery life, autonomy, and safety. Active balancing is the designated choice for applications that are sensitive to energy losses and maximized autonomy. First, a well-known next-to-next balancing technique is presented and its design and operating limitations are analyzed. Then, the paper focuses on an evolution of the converter's architecture offering better performances while being more compact, requiring fewer and smaller filtering needs and still, being simple to implement. The experimental results of the balancing operation of a pack of eight cells connected in series show demonstrative and satisfactory results.**

***Index Terms*—Active balancing, batteries, lithium-ion, next-to-next balancing, power integrated circuits.**

I. Introduction

A. Necessity for Balancing Li-ion Battery Stack

LI-ION cells are very susceptible to damage outside the allowed operating voltage range. If the upper or lower voltage limits (e.g., 2 and 3.6 V at 25 °C for LiFePO4 chemistry) are exceeded, the cells may be damaged irreversibly, reducing their storage capacity and increasing their internal impedance [1].

When implemented in series in a battery stack, the cells are charged and discharged with the same current hundreds to thousands of cycles. As this occurs, the cell's characteristics and more specifically their capacities become slightly different due to aging, process tolerances, and differences in the operating conditions especially with respect to the temperature [2], [3]. In a complementary manner, their leakage currents may also vary, introducing charge imbalances among the cells. The increasing imbalance prevents from using the full capacity of the pack if the operation is forbidden as soon as one of the cells reaches the border of the allowed operating range (see Fig. 1). The passive balancing techniques are used to compensate aging imbalances and to guarantee that the weakest element of the battery stack will be fully used to store or supply energy. However, the passive balancing techniques are not useful to take advantage of the energy capacities available in all the other cells, thus lowering significantly the battery storage capabilities as function of the capacity distribution of the battery cell. With an appropriate active balancing circuit, the charge capability of the weakest cells can be sustained with the strongest cells of the battery making possible to keep them into safe operating conditions, limiting heat generation during balancing operation, and allowing to extend the global capacity of the battery. To reach this goal, energy must be exchanged among the cells from the strongest to the weakest, whenever the voltages of any cells in the stack begin to differ from the others. High energy active balancing converters are required to perform real-time balancing and to maximize the access to all possible stored energy in the battery. Besides being efficient, the converters used to perform active balancing must be compact and reliable.

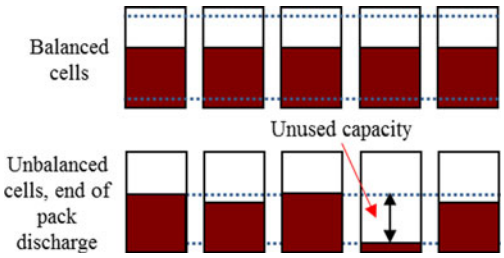

Fig. 1. Energy levels in series-connected cells.

B. Passive and Active Balancing

Many balancing systems have been developed in order to equalize the charge among the different cells connected in series in battery packs [4]–[23], usually divided in passive or active balancing systems. Besides some assumptions related to the temperature and the series impedance, it can be stated that the lithium cell voltage is related to its state of charge, especially after a large relaxation time. As a result, equalizing voltages among cells connected in series is a good solution to equalize charge levels and to prevent any cell from operating outside its nominal charge levels.

The passive balancing solutions are dissipative techniques that operate only under charging conditions to equalize the charge level among the cells. Resistors are used to bypass a part of the charging current or even to discharge the cells already fully charged. The equalization times are long because this method operates under low bypass currents to limit the heat generation. The pack performances are determined by the

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T. H. Phung and J.-C. Crebier are with the Grenoble Electrical Engineering Laboratory (G2elab), BP 46—38402 Saint Martin d'Hères Cedex—Grenoble, France (e-mail: Thanh-Hai.Phung@g2elab.grenoble-inp.fr; jean-christophe.crebier@grenoble-inp.fr).

A. Collet is with the FREEMENS SAS—1 place Notre Dame—38000 Grenoble, France (e-mail: alexandre.collet@freemens.fr).

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weakest cell and the energy is wasted during the bypass balancing process.

The active cell balancing techniques are based on the energy exchange among cells, equalizing the charge differences by taking energy from the most charged cells and transferring it to the less charged cells. The operation is possible and advantageous at any time or operating conditions. The energy is not anymore entirely wasted during the equalizing process but is redistributed among the cells. If the active balancing system has been designed for large current ratings, it can also operate during the battery discharge to support the weakest elements of the battery. In such a way, charging or discharging the battery can be supported in real time with large transfer of capacity balancing devices, making possible the global energy stored in the cells to be accessed and furnished to the load. This real-time balancing capability is then a question of design and ratings of the balancing converter versus the cell capacity differences. The higher the current rating of the balancing converter, the higher the cell capacity differences that will be balanced by the system. This clearly points out the interest in having high current ratings in the active balancing converters.

The energy transfer is usually carried out using a temporary storage unit between two or more cells. It can be either an inductor or a capacitor. Using a capacitor [6], [7] is inefficient because the transferred current level is determined by the parasitic series resistors in the circuit. In such balancing systems, when high energy exchange rates are desired, arrays of large transistors with very small R_{DSon} that operate under high switching frequencies are required. This approach is efficient and simple to implement but must be limited to low current level active balancing applications.

In terms of ratings, it is usually more flexible and much more favorable to design converters able to store temporary energy in magnetic devices such as inductors or HF transformers with leakage inductors in order to exchange energy between voltage sources. Today, most of the commercial topologies and circuits are low current level equalizers, which are not adapted to perform real-time active balancing as presented earlier. Besides, they are more complex topologies than passive or capacitive balancing converters, requiring more and bigger components [23]. The secondary multiple winding topology includes the difficulty of implementing a multiple secondary winding in a single transformer [9], [10]. The equalizers using selective switches can reduce the number of passive components, the size can be reduced but the control scheme for these type of equalizers is more complex [11], [12]. Simple equalizers that can operate with a few switches and open-loop control have been proposed in [13], [14], and [15] but these topologies are not suitable for the monolithic integration on CMOS technology. This limits the interest of their use and the emergence of balancing solutions efficient, compact, and simple to implement.

It is then an issue to try to improve their characteristics, volume, and ease of implementation. Many active balancing solutions are based on next-to-next balancing techniques [4], [6], [23]. This paper presents an evolution for one of them, including improved integration level, downsized passive components, and decreased filtering requirements. All these improvements make possible great increases in the current capabilities and higher power densities allowing to fully take advantage of the active balancing approach to manage energy and power stored or delivered by the battery. First, we recall the basic operation of the considered "next-to-next" balancing topology, its operating principle, control strategy, and limitations. Then, an improved architecture is proposed with a two-step enhanced approach. The advantages and drawbacks are underlined and illustrated with experiments on a battery containing eight cells connected in series. If the topology is an issue, it is also the case for the control. A specific care is given to outline how this converter topology can be controlled in an efficient way.

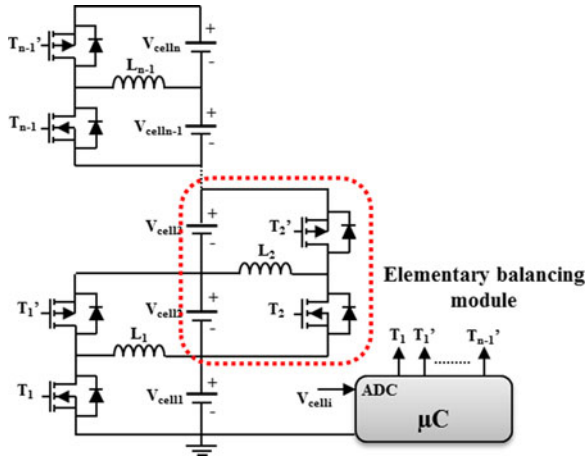


Fig. 2. Basic topology and converter stacking.

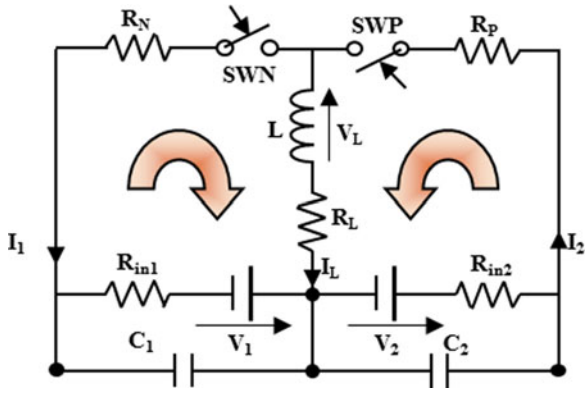


Fig. 3. Equivalent schematic of advanced basic topology.

II. The Original Topology

A. Presentation

The balancing system depicted in Fig. 2 is based on the well-known buck–boost chopper [5], [8]. The next-to-next elementary modules are implemented in such a way that the power can flow in either direction from one cell to the other. The staggering of the balancing units or modules creates a multicell next to next balancing system as depicted in Fig. 3.

The elementary balancing module also shown on Fig. 2 (dashed circle) is composed of two transistors (bidirectional current flow and unidirectional voltage capability) and an inductor L_N. A balancing module is connected across two adjacent cells to allow next-to-next energy transfer from the cell with higher voltage (or higher state of charge) to the cell with lower voltage (or lower state of charge).

The number of modules must be equal to the number of cells minus one. TN and TN' are activated with a pulsewidth modulation signal (PWM). By adjusting the duty cycle of this signal and/or considering the voltage differences between two adjacent cells, the current through LN can flow in either direction with the desired magnitude.

In a commercial solution [21], the converter is operated in discontinuous mode with constant duty cycle or maximum current clamping to ease the current control and to minimize the unit control complexity. The current direction is defined by the battery management system (BMS) after sensing the voltage difference between two adjacent cells. If this approach simplifies the implementation, it requires to oversize the inductor (LI^2) operated in discontinuous mode as well as the transistors and the filtering elements which in turns lead to low converter power densities and nonoptimized device design factors. In addition, if the freewheeling operation is carried out by the body diode of the transistors, the converter is simple to drive but inefficient at these voltage ratings.

The same converter architecture can be operated in continuous mode to reduce the storage and the filtering needs. In such a case, the control strategy of the converter must be developed in order to keep the balancing current under a maximum level no matter what the operating conditions of the balancing module. As in discontinuous mode operation, two simple strategies can be used, either the converter is operated under fixed duty cycle or under maximum current clamping. In the first case, the converter duty cycle can be set to 0.5 and both transistors are driven. As a result, the balancing current flows naturally from the cell with the higher voltage to the cell with the lower voltage level. The current can be continuous in the inductor and its level becomes dependent on the parasitic and the voltage mismatch between the two cells. Especially, the series resistors in the circuit such as the R_{DSon} of the transistors are critical elements in the current ratings. In this case, the greater is the voltage mismatch between the two cells, the higher will be the balancing current. This is an interesting functionality, especially around the edge of the safe operating area of the cells where the voltage slope increases greatly as function of the charge. This approach is very simple to implement and can even operate without interactions with the BMS to define the current flow direction. However, the balancing current ratings remain low and it is usually preferred to operate the balancing unit under variable duty cycle as a function of the given order by the associated BMS. In this case, the duty cycle is set slightly above or below 0.5 as function of the desired current flow direction. The balancing current rating can be much higher in this case. However, in both cases, a current clamping protection must be added to keep the balancing current at maximum allowed level in the active and passive power devices.

B. Operating Principle

1) Description: The elementary balancing module shown on Fig. 2 is composed of one P channel MOSFET, one N channel MOSFET, and an inductor. The MOSFETs are driven by a microcontroller, by applying on both gates the same PWM driving signals for complementary operation, for example 0.5 duty cycle. A special care must be taken to optimize the switching transitions of the complementary chopper to prevent the short-circuit occurrences at each commutation. In this case, the energy is transferred naturally from one cell to the other. Operated under continuous current mode and making the assumption that the voltage unbalances remain within a maximum range, this topology is simple to control. It can offer high transfer current levels and improved efficiency because only MOSFET operation is allowed since they are operated in synchronous rectification mode, reducing the voltage drop across the diode and consequently the losses of the converter.

2) Equivalent Schematic Diagram: To estimate the value of the charge and discharge current levels in the cells as function of the converter elements and cell charge levels, the equivalent electrical circuit depicted in Fig. 3 is used: $R_{\mathrm{in}1}, R_{\mathrm{in}2}$ are the internal resistance of the battery cells, R_L is the internal resistance of the coil, R_P, R_N are the ON state resistances of the CMOS devices N and P, respectively.

Assuming that from [0; αT], the P-MOSFET is closed (N is open) and from [αT; T], the N MOSFET is closed (P is open) and applying the averaging model technique, we can deduce the average current levels $\langle I_L\rangle$, $\langle I_1\rangle$, and $\langle I_2\rangle$ corresponding respectively the average currents flowing through the coil, and the ends of two adjacent cells from the following formula:

$$\text{For [0; } \alpha\text{T]: } \langle V_L\rangle = \alpha V_2 - \alpha\langle I_L\rangle(R_{\mathrm{in}2} + R_P + R_L) \tag{1}$$

$$\text{For [}\alpha\text{T; T]: } \langle V_L\rangle = -(1-\alpha)V_1 - (1-\alpha)\langle I_L\rangle(R_{\mathrm{in}2} + R_P + R_L). \tag{2}$$

For a period: $\langle V_L\rangle = 0$, we deduce

$$\langle I_L\rangle = \frac{\alpha V_2 - (1-\alpha)V_1}{\alpha(R_{\mathrm{in}2} + R_P + R_L) + (1-\alpha)(R_{\mathrm{in}1} + R_P + R_L)} \tag{3}$$

$$\langle I_1\rangle = (1-\alpha)\langle I_L\rangle;\ \langle I_2\rangle = \alpha\langle I_L\rangle;\ I_{1\mathrm{rms}} = \sqrt{1-\alpha}\langle I_L\rangle \quad I_{2\mathrm{rms}} = \sqrt{\alpha}\langle I_L\rangle. \tag{4}$$

Based on this current estimation, it is possible to estimate the converter's total conduction losses based on the following formula:

$$P_C = \langle I_L\rangle^2.R_L + (1-\alpha)\langle I_L\rangle^2.(R_N + R_{\mathrm{in}1}) + \alpha\langle I_L\rangle^2.(R_P + R_{\mathrm{in}2}). \tag{5}$$

The converter efficiency evolution based only on conduction losses can also be estimated with the following formula:

$$\eta(\%) = \begin{cases} \dfrac{V_2.\alpha.\langle I_L\rangle - P_C}{V_2.\alpha.\langle I_L\rangle} * 100 & \text{if } I_L > 0 \\ \dfrac{V_2.\alpha.|\langle I_L\rangle|}{V_2.\alpha.|\langle I_L\rangle| + Pc} * 100 & \text{if } I_L. \end{cases} \tag{6}$$

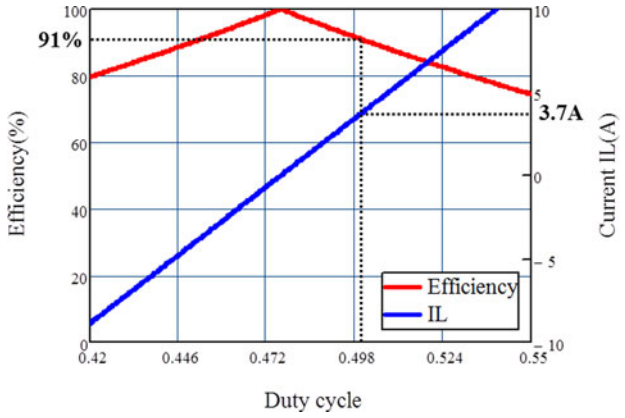


Fig. 4. Average inductor current and efficiency (switching and driving losses not included).

The reader will notice that the switching losses were not considered in this estimation because they are greatly dependent on the converter's practical implementation as well as the transistor driving conditions. Nevertheless, the proposed efficiency estimation gives an interesting evolution to be discussed.

The energy flow and the conduction losses levels depend on the values of V_1, V_2, the parasitic resistances, and the duty cycle. Fig. 4 below presents the evolution of the inductor current and the converter efficiency for the following computation conditions ($V1 = 3$ V, $V2 = 3.3$ V, L $= 30$ μH, RN $=$ RP $= 20$ mΩ, RL $= 10$ mΩ, Rin1 $=$ Rin2 $= 10$ mΩ) as function of the duty cycle.

The currents' orientations and magnitude depend on the voltage difference across each battery cell and duty cycle. It can be seen that the current evolution is almost linear which makes it possible to clamp its magnitude as a function of the duty cycle and the voltage mismatch. Even if the secondary elements may modify the current magnitude such as the value of the internal battery cell, impedance, or the temperature of the transistor acting on the value of their $\mathrm{RD_{Son}}$, it is possible to define an optimal and maximal duty cycle operation. This is possible because two battery cells with extremely stable characteristics at converter switching period time scale are placed on each side of the cell balancing converter.

This result presents as expected that the greater the current, the larger the losses. In particular, it can be observed that the operating point at duty cycle equal to 0.5 exhibits a balancing current in the range of 3.7 A with 91% efficiency. Forced balancing with variable duty cycle is also possible. Especially, it is interesting to notice that very small duty cycle variations are able to generate large increase in the current flow. As an example, considering the previous operating conditions, a fixed duty cycle of 0.53 will make possible to double the balancing current level. This means that for the design of the inductor, the duty cycles in the range of 0.5 must be considered, which represents the worst duty cycle for the ripple current clamping. In addition, it clearly appears that increasing the current flow induces larger RMS currents, larger needs for filtering, and much lower efficiency. Not all these points are bringing this converter topology in good track for implementation success.

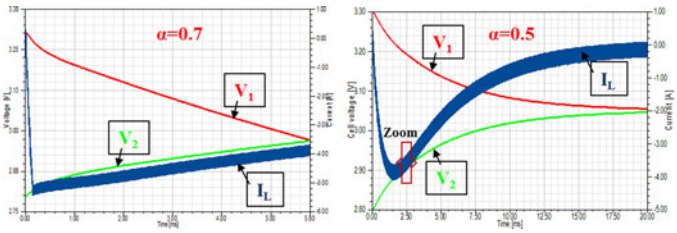


Fig. 5. Cell voltages (V_1, V_2) and current in the coil (I_L) in the case of forced and natural balancing.

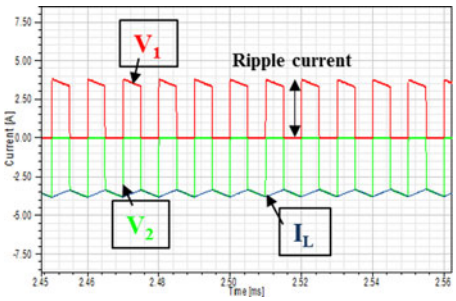


Fig. 6. Cell (I_1, I_2) and coil currents.

3) Simulation Results: After this functional analysis, we present the simulation results for forced and natural balancing based on the studied topology applied to two cells connected in series. The simulations are carried out using the simulation tool SIMPLORER.

The battery cells are modeled to represent the nonlinear electrical charge characteristic versus the voltage level behavior of a regular LiFePO4 battery. The charge capacity is set to 1 mAh to limit the duration of the switched mode simulation time.

The simulation parameters are:

1) voltages of the two cells: $V_1 = 3.3$ V, $V_2 = 2.8$ V, Rin1 $=$ Rin2 $= 10$ mΩ;
2) inductance coil L $= 30$ μH, RL $= 10$ mΩ;
3) switching frequency $F_d = 100$ kHz;
4) MOSFETs P,N with low R_{ds} (20 mΩ);
5) schottky diodes D_1 and D_2.

The simulation results depicted on Figs. 5 and 6 provide interesting data on the balancing technique that effectively fit the functional analysis. It can be seen that the cell voltages are completely balanced after a certain time.

The value of the current through the coil is increased at the beginning of the balancing sequence. Then, it decreases exponentially at the end of the balancing sequence operated under 0.5 duty cycle. The forced balancing (e.g., $\alpha = 0.7$) may be used to speed up the balancing action. The voltages of the two cells converge immediately and then an action must be taken to stop the balancing process before the voltages start to diverge. In forced balancing, the power transfer level is higher but a specific care must be taken to keep the current level within nominal range.

In both cases, the coil is the main component to be reduced since its size and cost are directly related to the current that it carries and the energy that is stored. Moreover, as shown in Fig. 6, the current applied to the cells is highly discontinuous. It

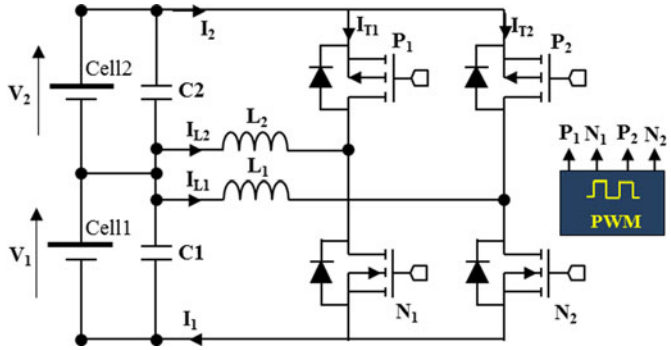


Fig. 7. Second proposed topology.

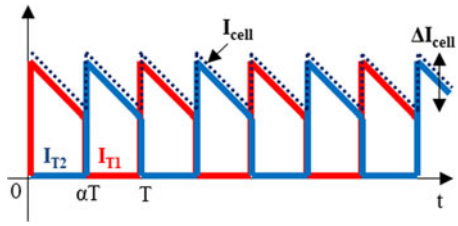


Fig. 8. Shape of one cell current with two interleaved conversion units for 0.5 duty cycle.

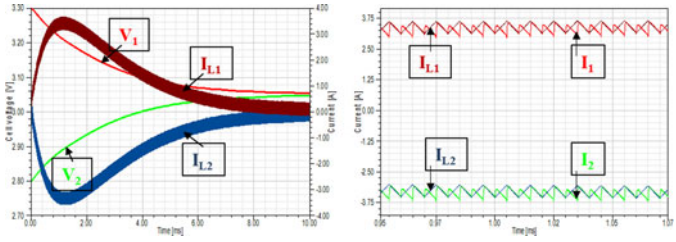


Fig. 9. Cell voltages (V_1, V_2), cell (I_1, I_2), and coil current (I_L) with the improved topology.

may require the addition of a capacitor filter with high ac current capability, as a function of the cell response to high frequency currents or its physical distance to the balancing converter. Indeed, the introduction of long wires between the converter and the balancing cell without adequate filtering on the PCB board would be greatly damageable for the converter operation, especially at each switching transition. Finally, the overall passive device values and sizes increase drastically with the current level of this active balancing technique no matter which control strategy is used.

To improve these limitations, the following sections of the paper present the evolutions of the topology.

III. Proposed Topologies and Control Approach

In this section of the paper, we are going to present two consecutive evolutions of the conventional topology allowing to drastically reduce the size of the passive components and to consequently increase its power density. These changes are intended to ease the integration and the implementation of the initial next-to-next active balancing technique while offering the possibility to greatly increase the balancing current levels. The paper focuses on the natural balancing with duty cycle equal or close to 0.5 but all improvements can be applied to the force balancing control with variable duty cycles of any value.

A. Improved Topology: Reduced Capacitor Filtering Needs

At first, we propose an improved topology that corresponds to a basic interleaved topology with two coils in parallel as shown in Fig. 7 and considering 180° phase shift angle driving orders between the two converter arms.

1) Description: A second coil with its own CMOS arm is added to the first topology. The switches P_1 and N_1 operate in synchronous rectification mode and the two arms are 180° phase shifted from each other. The two conversion units are interleaved under a duty cycle of ideally 0.5 but duty cycles close to 0.5 are also very favorable to increase the current levels. Therefore, the input and output currents of the cells are "the sum" of the currents flowing in both coils as it is represented in Fig. 8.

As it can be seen, the ripple current applied to the filtering caps is greatly reduced compared to the one depicted on Fig. 6. Therefore, this approach allows reducing the filtering needs, and thus the size of the capacitors $C1$ and $C2$. The implementation of two converters in parallel will either double the balancing current level if both interleaved units are designed at initial design ratings. Otherwise, the design of each conversion unit will have to consider current ratings divided by a factor of two. In such way, the main limitation of this approach becomes clearly the increase of the number of the components, especially the active devices. This issue will be addressed in a following section.

2) Simulation Results: The resulting balancing converter was simulated under the following conditions and the obtained results are depicted on Fig. 9.

The simulation parameters are:

1) voltages of the two cells: $V_1 = 3.3$ V, $V_2 = 2.8$ V, Rin1 = Rin2 = 10 mΩ;
2) inductance coil $L_1 = L_2 = 30\ \mu$H, RL1 = RL2 = 10 mΩ;
3) switching frequency $F_d = 100$ kHz;
4) MOSFETs P,N with low $R_{\rm ds}$ (20 mΩ);
5) schottky diodes D_1, D_2, D_3, D_4.

As shown in Fig. 9, the voltages of the two cells (initially $V_1 > V_2$) converge faster in comparison to Fig. 5, since the two coils transfer now twice the initial power to the cell. The main advantage of this topology is the significant reduction of the capacitive filtering requirements. The disadvantage is that two coils and two CMOS inverters are now required, which may appear more complex to implement. As far as the two CMOS inverter arms are concerned, their monolithic integration in CMOS technology can easily be carried out as it has been presented in [24]. In such a way, the possible occurrence of CMOS arm short circuit is managed internally in the integrated circuit thanks to integrated drivers supplied by the dc bus created by the sum of the two cells. The gate driving signals are optimized as well as the electrical interconnections. Considering the magnetic devices, their coupling corresponds to the second evolution of the converter topology.

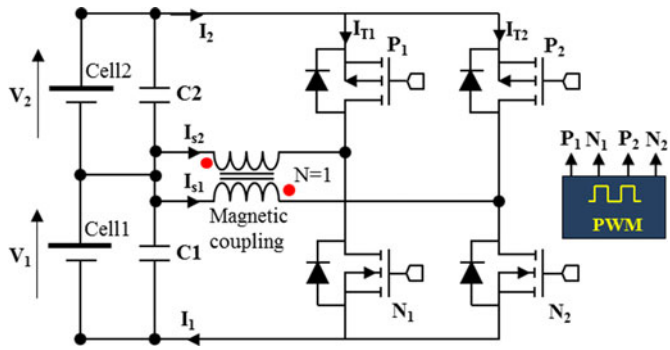


Fig. 10. Third topology.

B. Third Topology: Downsizing the Coils

1) Description: In order to improve the topology previously proposed, the two coils can be winded on the same iron core as it is shown on Fig. 10. This double-winded coil replaces the two discrete coils of the second topology, maximizing the compactness of the overall inductor. The currents flowing in the two windings have symmetrical dc levels. Therefore, the windings are connected in order to compensate the flux generated by each of them into the magnetic core.

Almost perfect magnetic compensation is obtained, offering great size reductions of the magnetic device no matter the value of the duty cycle. If the converter is always operated under fixed 0.5 duty cycle, the coupled inductor can be optimized with a minimum leakage inductance. Nevertheless, it is also possible to operate the converter with coupled inductors under variable duty cycle, designing the magnetic device to exhibit the required leakage inductance. As it has been underlined earlier in the paper, only small variations of the duty cycle are necessary to enlarge greatly the balancing current. As a result, the leakage inductance needed to filter the coil currents remains very small. As an example, for a duty cycle variation of 10% above and below 0.5, the leakage inductance necessary to moderate the inductor current ripple to 0.5 A over a dc level of 5 A per coil is 6 μH which is a realistic value compared to the magnetizing inductance value of 30 μH. It is this expected design and optimization result based on the fact that the application only requires small duty cycle variations around 0.5 and that the CMOS arms and their associated drivers can operate at high frequency and under very small duty cycle mismatch that evident the contribution of this work.

In addition, this third topology provides the same advantages as the second one, which is to ensure the continuity of the charge or discharge currents in the cells, thus reducing the size of the filtering capacity and increasing the balancing speed. Furthermore, the current compensation at the magnetic device level is an opportunity to manage short overcurrent levels in the balancing converters, which may simplify the implementation. Indeed, the magnetic flux level in the magnetic core has become independent from the average current flow in both windings. As function of the heat removal capabilities, the short converter overload is made possible without the immediate magnetic core saturation. The modeling and analysis of the topology with respect to the operation characteristics will be presented in the following section.

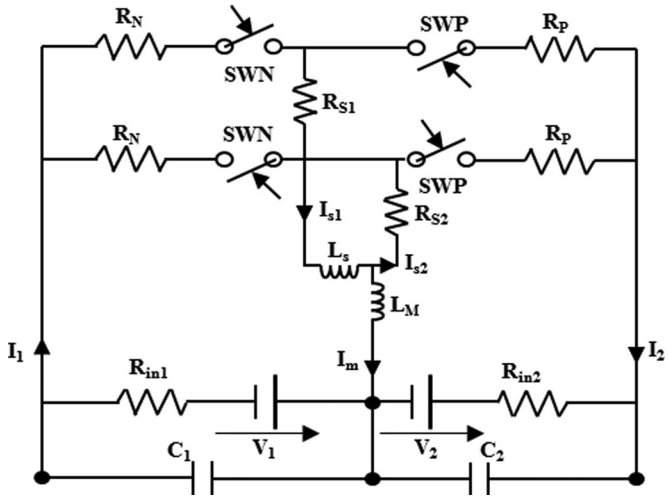


Fig. 11. Equivalent schematic of the third topology.

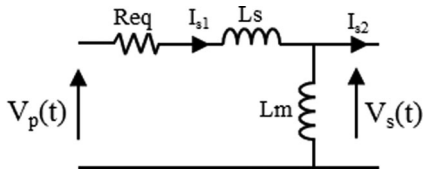


Fig. 12. Coupled inductor simplified schematic diagram.

2) Equivalent Schematic Diagram Allowing to Calculate the Load Currents: In a similar manner as for the initial topology, the next-to-next balancing topology with coupled inductors equivalent circuit only takes into account main resistive and inductive elements (see Fig. 11).

To simplify the calculation, we use the following model for the coupled inductor, which is based on an equivalent transformer model where the ideal coupling element has been neglected (see Fig. 12).

$R_{\rm eq}$ is the equivalent conduction resistance of the magnetic coupling, MOSFETs, and cells with the following relationship:

$$R_{\rm eq} = R_P + R_N + R_{\rm in1} + R_{\rm in2} + R_{S1} + R_{S2}. \qquad (7)$$

L_s, L_m are, respectively, the leakage and magnetizing inductances of the coupled magnetic device.

$V_p(t), V_s(t)$ are the voltages applied to the primary and secondary winding, respectively

$$V_p(t) = \begin{cases} V_1 & 0 \le t \le \alpha T \\ -V_2 & \alpha T \le t \le T \end{cases} \quad V_s(t) = \begin{cases} V_2 & 0 \le t \le \alpha T \\ -V_1 & \alpha T \le t \le T \end{cases} \qquad (8)$$

$$\Rightarrow V_p(t) - V_s(t) = (V_1 - V_2) > 0. \text{ (Assuming } V_1 > V_2)$$

By applying Kirchhoff's voltage law, the obtained result is

$$L_s \frac{dI_{s1}}{dt} + R_{\rm eq}.I_{s1} = V_p(t) - V_s(t) = (V_1 - V_2). \qquad (9)$$

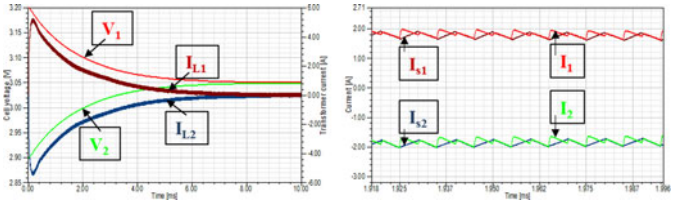


Fig. 13. Cell voltage and current in the coil.

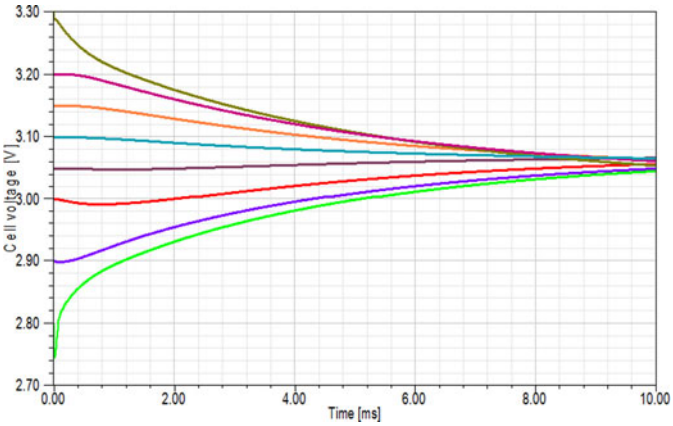


Fig. 14. Balancing of eight cells.

Solving (9), the current flowing through the circuit can be expressed as

$$I_{s1} = \frac{V_1 - V_2}{R_{\text{eq}}}(1 - e^{\frac{-t}{\tau}}) \text{ where } \tau = \frac{L_s}{R_{\text{eq}}}. \quad (10)$$

After some periods, $I_{s1} = (V_1 - V_2)/R_{\text{eq}}$

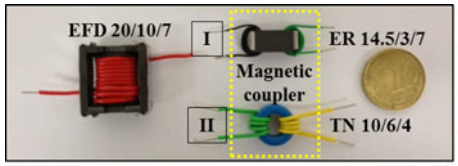
$$I_{s2} = I_{s1} + I_m \approx I_{s1}. \quad (11)$$

Where the deduced value of the current cell is

$$|\langle I_1 \rangle| = |\langle I_2 \rangle| = |I_{s2}| + |I_{s1}| = 2\,|I_{s1}|\,. \quad (12)$$

Here again, the balancing current level is twice of that of the initial topology due to the interleaved topology. However, significant improvements can be identified. Considering the losses in the filtering capacitors, the ac current levels are greatly reduced, minimizing the losses. Considering the magnetic device, the reduction of the magnetic core sizes and volume as well as the induction level reduces the iron losses. Moreover, the winding length is minimized leading to minimized copper losses. Finally, interleaved converters offer the opportunity to manage at best the active devices, optimizing their use and operation with the use of smaller and more efficient devices.

3) Simulation Results: The simulation results presented in Fig. 13 are in accordance to those of the second topology, the flowing current being very regular. However, in this case, the design of the magnetic devices is greatly optimized. This improved next-to-next balancing system is smaller, more efficient, and easier to integrate. Fig. 14 shows a demonstrative result of the balancing operation applied to a pack of eight cells in series with great voltage imbalances. The seven converters with coupled inductors are operated under natural control technique with fixed duty cycles all equal to 0.5. In this case, the system automatically finds the balanced point and sets the balancing currents in the good direction.



Magnetic device	DC resistance
Inductor	10mΩ
Coupler I	1.2mΩ
Coupler II	9.3mΩ

Fig. 15. Picture of the inductor and coupled magnetics with their corresponding dc resistance.

As far as the simulation of the eight cells pack is concerned, the battery cells are initially charged under various voltages from 2.8 up to 3.3 V with a total stored energy of 91.6 Wh. Initially, with one cell almost fully discharged, no energy can be delivered by the battery pack. After the balancing action, the mean voltage level accord of all the cells is 3.05 V and the total available energy is: 86.6 Wh. As it can be seen, over 5 Wh have been lost, but about 86.6 Wh are now available and can be used to supply a charge with the battery. In the following section, the experimental work will demonstrate the interest of the converter and will validate our analysis. We will now present with more details what can be expected from the magnetic devices in terms of design and performances.

4) Reducing the Size of the Magnetic Core: Considering that each winding is wound on the same magnetic core, a magnetic coupling is created. Depending on the inverter leg phase shift and duty cycle and depending on the coupling directions in the magnetic core, it is possible to create a flux compensation allowing to reduce the needs of the magnetic material. Indeed, if the currents flowing in the two coils are similar in magnitude, the dc components of the created fluxes can be cancelled. If the ac part of the inductive current is small compared to the dc part, substantial reduction in the cross section of the magnetic core can be obtained [25]–[27].

Based on our previous design, the current ripple was set at 10% of the dc nominal current. Considering that the dc part of the fluxes created by each winding cancel each other, the resulting coupled inductor can be optimized.

Based on this design approach, it is then possible to improve even more the coupled inductor design. Since the magnetic core is smaller, the windings are shorter, making the dc and HF winding resistance values smaller. As far as the natural balancing technique is concerned, this gain in series resistance directly affects the current capabilities of the next-to-next balancing topology. For this specific and advantageous operating condition at fixed 0.5 duty cycle, the designed magnetic coupler is shown in Fig. 17. It can be observed a significant volume reduction of the magnetic core relative to the separated inductor in the case of the basic interleaving topology. Besides, it has to be considered that two inductors are required in the classical interleaved topology. The inductor on the left side of Fig. 15 is the regular 30-μH inductor 5 A dc. The coupled inductor on the top right part of the figure is designed with a 6-μH leakage inductor necessary to moderate the inductor current ripple to 0.5 A for a duty cycle variation of 10% above and below 0.5. This coupler

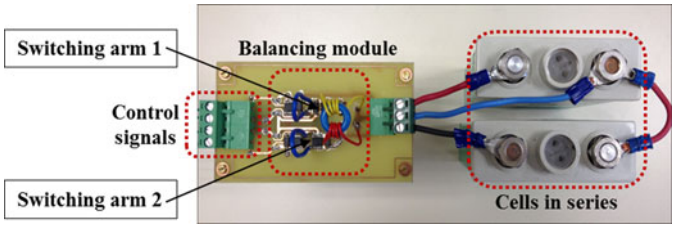


Fig. 16. Next to next coupled inductor balancing system implemented across two 10 Ah cells in series.

is designed according to conventional rules with reference to previous work on the couplers and has been optimized in terms of the value of the leakage inductance. The bottom inductor is a toroidal inductor with minimum leakage inductor for an operation at fixed 0.5 duty cycle, again for 5 A dc. Both coupled inductors are designed to withstand a dc current mismatch of 0.5 A between the two windings. This picture clearly demonstrates the gain in terms of magnetic device volume that can be obtained thanks to the proposed topology. The dc winding resistances for the three magnetic devices are presented in the table Fig. 15 below.

IV. Experimental Results

An experimental implementation has been carried out to validate the analytical work and to check the compliance with the simulation results. The first measurements were made operating the converter based on the coupled inductor between two independent battery cells having a large voltage mismatch. The basic PCB board with special region dedicated for the voltage and current measurements is depicted on Fig. 16, connected to two 10 Ah LiFePO4 batteries. The power transistors have low conduction resistance (about 25 mΩ at the operating point at 25 °C); the internal resistance of each cell is estimated at 10 mΩ. Fig. 17 shows the time domain response of the experiment while operated under fixed 0.5 duty cycle and with an initial voltage mismatch of 0.24 V. It can be seen that within 25 min, the voltage mismatch has been reduced below 50 mV and that within 46 min, the mismatch is below 20 mV, which is usually the accuracy range of the BMS voltage monitoring.

For the operation of the converter at the switching period scale, it can be seen on Fig. 17(b) that the currents within the two coils are very comparable with less than 0.1-A mismatch without regulation needs. Besides, the ripple current is well maintained in the range of 0.5 A as defined in the design specifications. On Fig. 17(c), the battery current, being the sum of the two inverter currents 180° phase shifted, appears also with a minimum ac part, in the range of 0.5-A peak to peak compared to the 2 A of a single arm. This second set of waveforms clearly demonstrates the impact of the topology on the passive devices.

To characterize the performance of each conversion unit with coupled inductor, an accurate estimate of the efficiency can be carried out by using a constant voltage source 3 V with a variable resistor instead of using the two cells. The experimental tests performed at different power levels help us to evaluate the efficiency of the balancing converter. It can be observed in

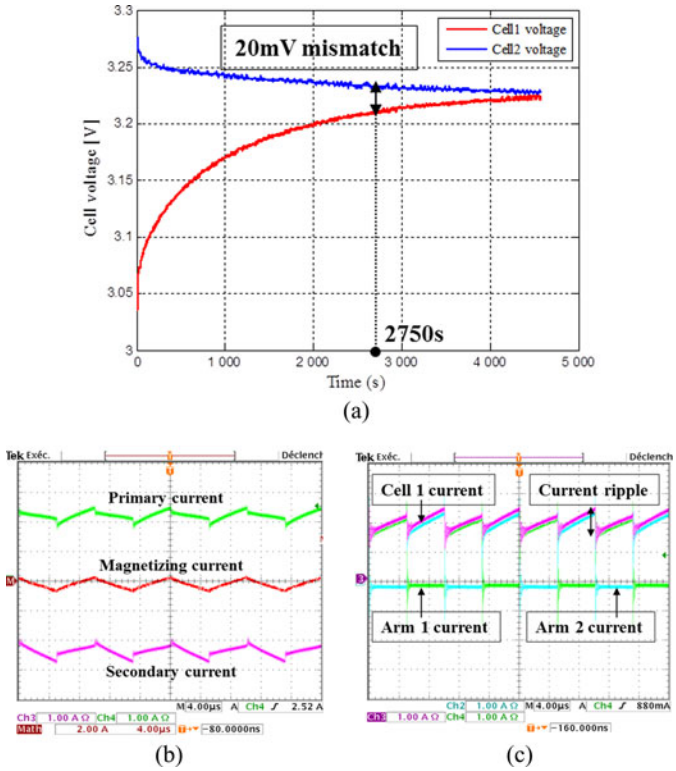


Fig. 17. (a) Evolution of the cells voltage. (b) Winding and magnetizing currents. (c) Arm currents and cell 1 current.

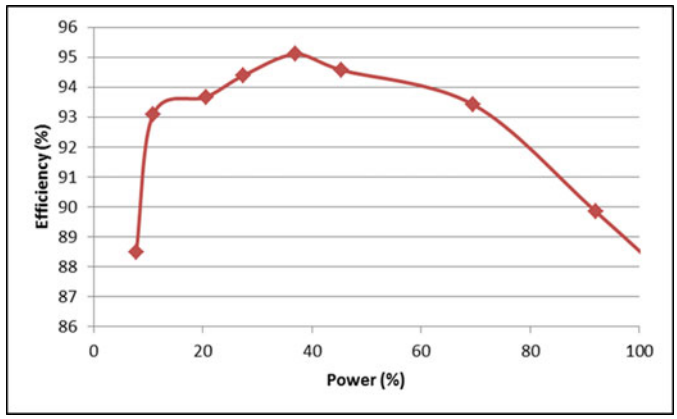


Fig. 18. Efficiency of coupled inductor converter.

Fig. 18, the converter efficiency in the range of rated power (10–100% Pmax, Pmax = 15 W) is always greater than 88%, the maximum value reaches up to 95% at 35% Pmax.

Equalizing the voltages across two cells in series has proven the interest of the proposed topology with respect to the reduction of the current ripples, converter effectiveness, and compacity. Fig. 19 below presents now the experimental setup with two active balancing circuits implemented on the same type of PCB board. One of them is connected with seven inductors (original topology) and the other is connected with seven coupled inductors (third topology) to equalize the cell charge of eight battery cells when operated under fixed 0.5 duty cycle. To make the comparison as realistic as possible, the two switching arms

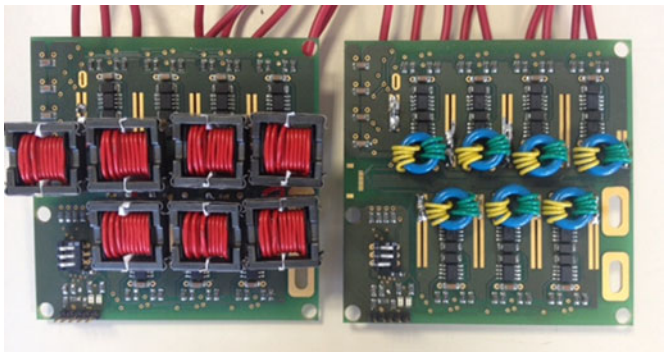


Fig. 19. Two systems balancing of eight cells in series.

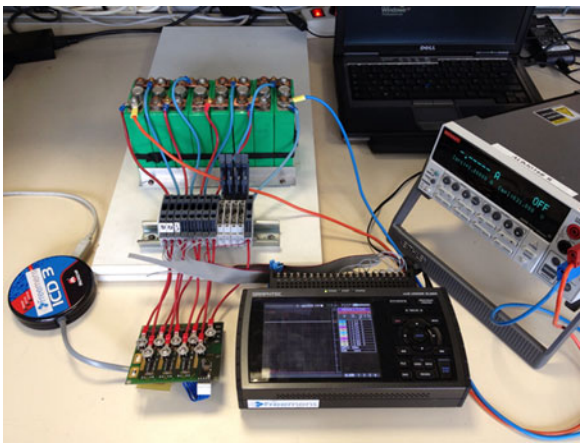


Fig. 20. Experimental test bench.

used in the interleaved architecture are simply placed in parallel to implement the single arm of each converter unit of the original topology. This provides comparable current transfer capability as well as comparable PCB design (identical parasitic, copper traces, and so on). This implementation allows to compare the performance of the proposed structure with the original based on the magnetic volume and speed balancing.

The battery pack, which is the same in two cases, is composed of eight LiFePO4 10 Ah cells connected in series with different initial voltages. The setup is depicted on Fig. 20. The converters are designed to operate at 5-A maximum dc current in each magnetic device. In practice, this current level is reached at the maximum voltage difference of 0.5 V between two adjacent cells. The switching frequency is set to 100 kHz, and the MOSFETs present a low on state resistance from 15 to 25 mΩ as a function of temperature. The DSPIC33FJ06GS202 T—microcontroller is used to generate the control signals.

Fig. 21(a), (b), and (c) presents the evolution of the voltages across each battery cell when discharged under a constant battery current of 1 A and with identical initial conditions. In the first case, the battery is discharged without the help of the active balancing converters whereas in the second and the third plots below, the battery is discharged but the weakest elements are supported by the strongest ones thanks to the operation of balancing units. It clearly appears that thanks to the operation of the balancing units, all cell voltages converge and that the weaker cells are supported by the stronger one. Furthermore, it can be observed that the discharge time is slightly longer in case the proposed topology is used compared to the initial one.

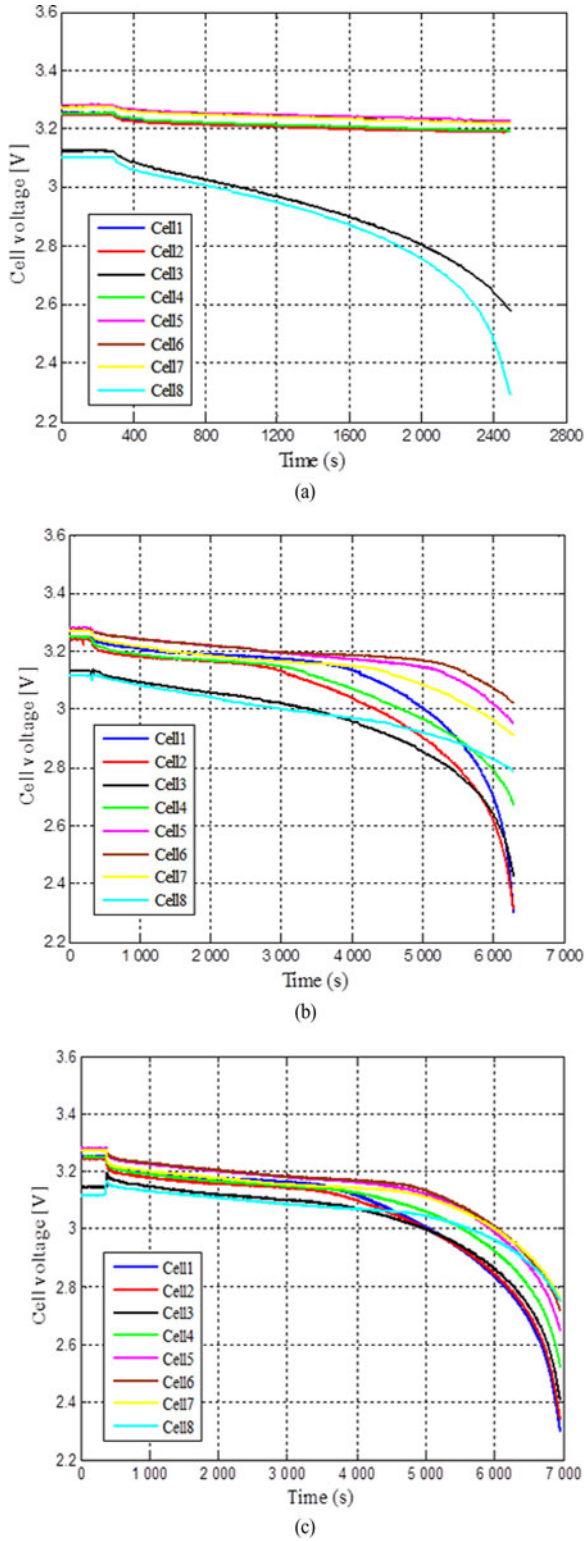


Fig. 21. (a) Battery discharge characteristics under voltage mismatch and 1-A dc current. (b, c) Battery discharge characteristics under the same conditions and with the operation of the active balancing conversion units.

TABLE I
COMPARISON OF THE PROPOSED TOPOLOGY WITH THE ORIGINAL

	Filtering capacity	Magnetic volume	Discharge time
Original topology	1000µF	10.22cm^3	6350s
Proposed topology	100µF	1.316cm^3	7000s

This is because the second topology is slightly more efficient, with lower parasitic resistances and lower RMS currents in the capacitors.

It is interesting to see on the plot of Fig. 21(b) that the voltage mismatch remains within 100 mV range among the cells, while in Fig. 21(c), this mismatch is about 50 mV, this until the battery is almost completely discharged. These voltage mismatches caused by the difference value of the balancing current in both cases, is the decisive reason for the discharge time of the pack. This clearly demonstrates the operation of the conversion units and the interest of the real-time active balancing approach. At the end of the discharge characteristics, the voltage mismatch increases due to the internal cell resistance increase. The three lower cells 1, 2, and 3 are the most discharged ones because they are used to supply the microcontroller and the drivers on the PCB board (about 0.5 W in total). Increasing the balancing current can be achieved by the use of the forced balancing with specific and controlled duty ratio on each converter balancing unit. To implement this strategy, a decentralized approach can be used based on independent balancing modules, each of them being connected to two adjacent cells. Table I presents a set of experimental results allowing to compare and to demonstrate clearly the interest of the proposed topology compared to the original one. It also clearly demonstrates the interest of implementing an active balancing system to perform real-time equalization and maximize the energy availability to the load.

V. CONCLUSION AND FUTURE WORK

This paper has presented and validated an enhanced active cell balancing topology built upon a popular next-to-next topology. The purpose of this paper was to investigate a more effective and more compact topology that can best meet the application requirements for integration, performance, and cost, addressing applications such as electric vehicles. The practical implementation presented in the paper has shown the interest of the converter based on significant design optimizations. The reduction of the magnetic coil based on a flux compensation approach is effective. In addition, the filtering needs are substantially reduced and optimized. The balancing operation of the new equalization converter has been checked. The integration of the active parts of the balancing converter, integrating the sensors, and the control units allowing to make this conversion topology fully autonomous will be further investigated and presented.

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Thanh Hai Phung received the graduation degree in engineering from the Hanoi University of Technology, Hanoi, Vietnam, in 2009, and the M.S. degree in electrical engineering from the Grenoble Institute of Technology, Grenoble, France, in 2010. He is currently working toward the Ph.D. degree in the Grenoble Electrical Engineering Laborary, University of Grenoble, France.

His current research interests include the control strategy for system balancing, micro converter networks, and hybrid integration applying an isolated bidirectional dc–dc converter.

Alexandre Collet received the graduation degree from the Grenoble Institute of Technology, Grenoble, France, in 2010.

From 2010 to 2011, he was a Research Engineer with the French National Center for Scientific Research, France, and is currently the CEO of Freemens since October 2011. His area of expertise include power electronics and battery management systems.

Jean-Christophe Crebier received the B.S. degree in electrical engineering from the National Polytechnic Institute of Grenoble, Grenoble, France, in 1995, and the Ph.D. degree in power electronics, electromagnetic compatibility, and power factor correction from Laboratoire d'Electrotechnique de Grenoble, Institut National Polytechnique de Grenoble, Grenoble, France, in 1999.

In 1999, he was working as a Postdoctoral Student in the Center for Power Electronics Systems, Blacksburg, VA, USA, doing research in system integration. In 2001, he was hired by the National Center for Scientific Research, France, as a Full-Time Researcher in power electronics. He is currently with Grenoble Electrical Engineering Laboratory, Grenoble. Today, his main research fields include system and functional, hybrid and monolithic integration and packaging for medium-to-high-voltage active devices, and applications to the management of multicellular systems such as photovoltaic, batteries, and distributed systems.