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Verification Report

[Amba 3 AHB-LITE protocol spec]

Introduction to the Device-Under-Test (DUT)

AMBA AHB-Lite addresses the requirements of high-performance synthesizable designs. It is a bus interface that supports a single bus master and provides high-bandwidth operation.
AHB-Lite implements the features required for high-performance, high clock frequency systems including:
• *burst transfers*
• *single-clock edge operation*
• *non-tristate implementation*
• *wide data bus configurations, 64, 128, 256, 512, and 1024 bits.*
The most common AHB-Lite slaves are internal memory devices, external memory interfaces, and high bandwidth peripherals. Although low-bandwidth peripherals can be included as AHB-Lite slaves, for system performance reasons they typically reside on the AMBA Advanced Peripheral Bus (APB). Bridging between this higher level of bus and APB is done using a AHB-Lite slave, known as an APB bridge.

Verification Plan

No.	Feature	Test Description	Ref.	Type	Result	Comments
1 a	Apply HCLK, HADDR, HWRITE=1,HSIZE= WORD SIZE,HTRANS=NON SEQ AND HW DATA=ANY RANDOM DATA OF WORD SIZE And wait for HRESPONSE=OKAY	We will write random 32 bit word to HADDR in memory	Amba 3 Ahb lite v 1 chapters 3 and 5	TR		
1 b	(Clock is being applied throughout that's why I am not writing it again) Apply same HADDR, HWRITE=0,HSIZE= WORD SIZE,HTRANS=IDLE And check HREAD after HRESPONSE=OKAY	Verifying idle vs non sequential	Amba 3 Ahb lite v 1 chapters 3 and 5	TR		
1 c	Again apply same HADDR, HWRITE=0,HSIZE= WORD SIZE,HTRANS=NON SEQ AND And check HREAD after waiting one clock cycle, i-e	Verifying idle vs non sequential and also that data has been written correctly	Amba 3 Ahb lite v 1 chapters 3 and 5	TR		

	HRESPONSE=OKAY (of HREAD not of non seq) . Repeat above three steps 4 to 5 times and then go for random testing					
2	Apply some sequence of signals such that HTRANS is applied as non sequential and then is not applied for next 3 cycles and then applied again but other signals are applied meanwhile and check for HRESPONSE if HRESPONSE = 1 , assert error	Checking error message	Amba 3 Ahb lite v 1 sect 5.1.3	A		
3	Apply some signals such that HTRANS is applied as non sequential for first cycle and then is applied as a random sequence of sequential, idle and busy for next cycles and other signals including HPROT, HADDR(according to	Verifying behaviour of HBURST and that data has been written correctly	Amba 3 Ahb lite v 1 sect 3.5.3 and ch 5	TR		

	burst type and size), HWDATA, HBURST(type of burst) and HSIZE are also applied and check for HRESPONSE					
3 a	APPLY same set of signals as in 3 except HTRANS HWRITE AND HWDATA. now HWRITE=0 and not writing any data to HWDATA.HTRANS will be according to sequential busy and idle according to previous section(3) Wait for HRESPONSE to be 0(for data) Read data from HRDATA. Repeat above (3 and 3a) multiple times.	Same as above	Same as above			

Explanation of Different Fields

No. The serial number of the test.

Feature The feature which the current test is verifying in full or partially. The feature is usually on the abstraction level of a user.

Test Description	A detailed description of the test case being performed. You can be as verbose as you want.
Ref.	Reference to the section in the related standard document. The section number as well as page numbers should be described here.
Type	Type of the test. Whether the test is an assertion (A) or a transaction (T) type.
Result	Pass (P) or Fail (F).
Comments	Any other comments about the test or its results that you want to mention.