Verification of Kirchhoff's Voltage Law (KVL) using Breadboard

LAB # 6

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CIRCUIT AND SYSTEMS 1 LAB

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"On my honor, as a student of the University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work.'

Submitted to:

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Experiment # 6

Verification of Kirchhoff's Voltage Law (KVL) using Breadboard

Objective:

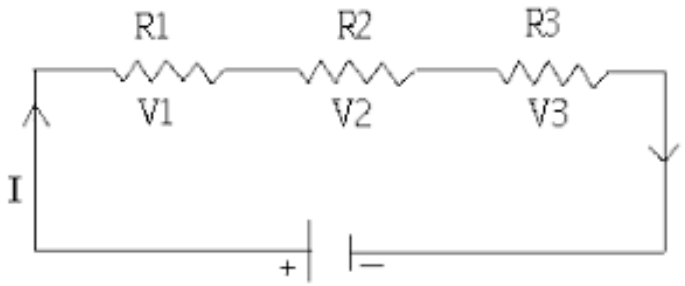
To verify Kirchhoff's Voltage Law (KVL) on Breadboard and know relationship between varying resistors and applied voltage.

Kirchhoff's Voltage Law (KVL):

Statement:

The algebraic sum of all voltage differences around any closed loop is zero.

Diagram:



Mathematically:

$$\sum V = 0$$

$$V1 + V2 + V3 = 0$$

PSPICE Simulator:

PSPICE is a computer-aided simulation program that enables you to design a circuit and then simulate the design on a computer. As this is one of its main purposes, it is used extensively by electronic design engineers for building a circuit and then testing out how that circuit will simulate.

Apparatus:

1. DMM
2. Resistors
3. DC power supply

Procedure:

4. Design the following circuit on breadboard

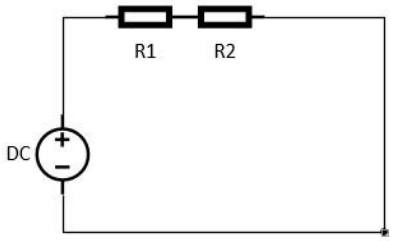


Figure 1 Circuit diagram

5. Using DMM find resistance of the resistors and note down in the table.
6. Find voltage of DC source and voltage drop on each resistor and note down in the table.
7. Add the voltage drops and compare with the source voltage by finding the percentage error.

Observation:

S.no	Vs (actual) (V)	V1 (Measured) (V)	V2 (Measured) (V)	V1+V2 (V)	Error	Percentage Error (%)
1.	5	0.89	4.30	5.19	0.19	3.8%
2.	10	1.7	8.2	9.9	0.1	1%
3.	15	2.6	12.5	15.1	0.1	0.67%
4.	20	3.4	16.7	20.1	0.1	0.5%
5.	30	5.2	24.9	30.1	0.1	0.3%

Analysis:

From the observation in any closed-loop network, the total voltage around the loop is equal to the sum of all the voltage drops within the same loop which is also equal to zero. In other words, the algebraic sum of all voltages within the loop must be equal to zero.