Homework 4 **Due: Tuesday, January 10, 2023**

- This homework is due on Tuesday, January 10, 2023.
- Hand in your completed handwritten homework to me during our Tuesday lecture.
- There is a 50% penalty per day for late submission.
- Copied homework will be awarded 0 marks.

Problem 1.

Determine the Q output waveform if the inputs shown in Figure 1 are applied to a gated S-R latch (shown in Figure 2) that is initially RESET.

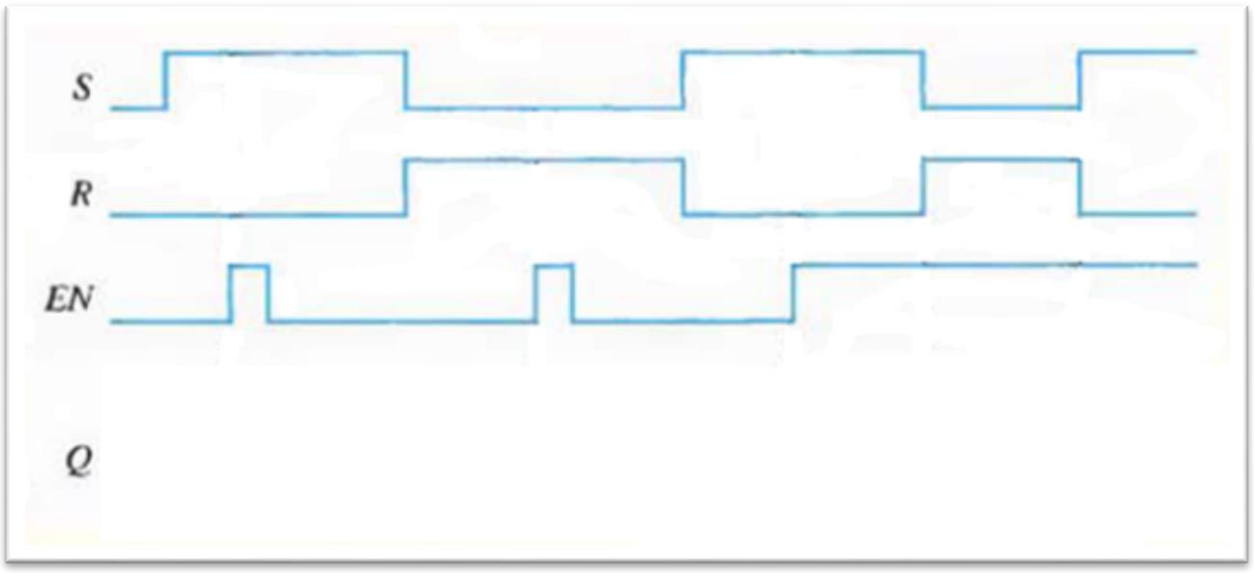


Figure 1. Input waveforms.

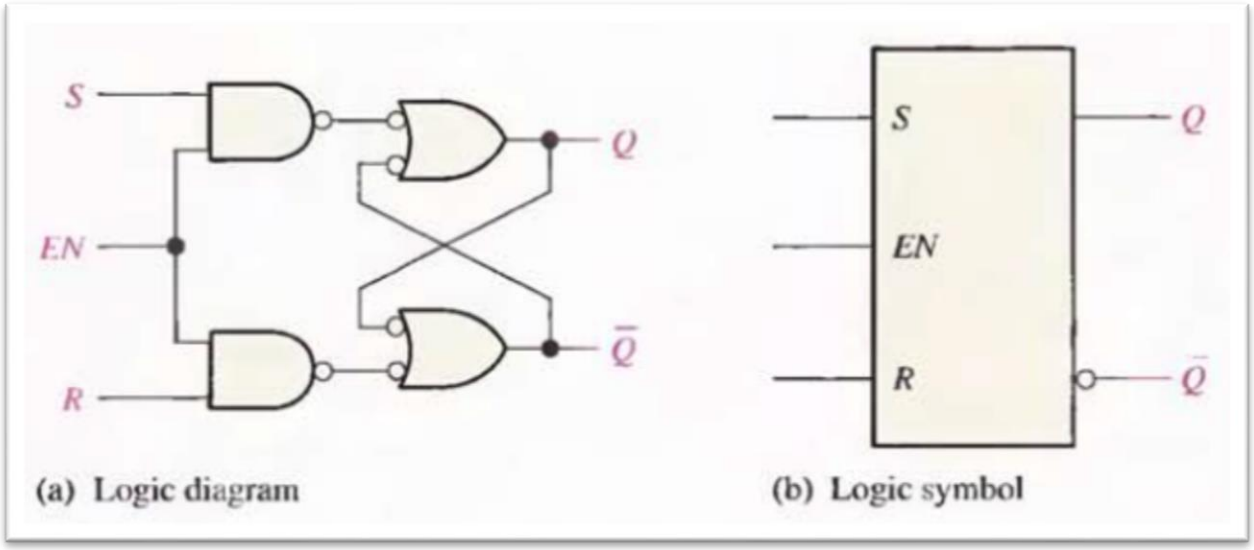


Figure 2. A gated S-R latch.

Problem 2.

Determine the Q output waveform if the inputs shown in Figure 3 are applied to a gated D latch (shown in Figure 4), which is initially RESET.

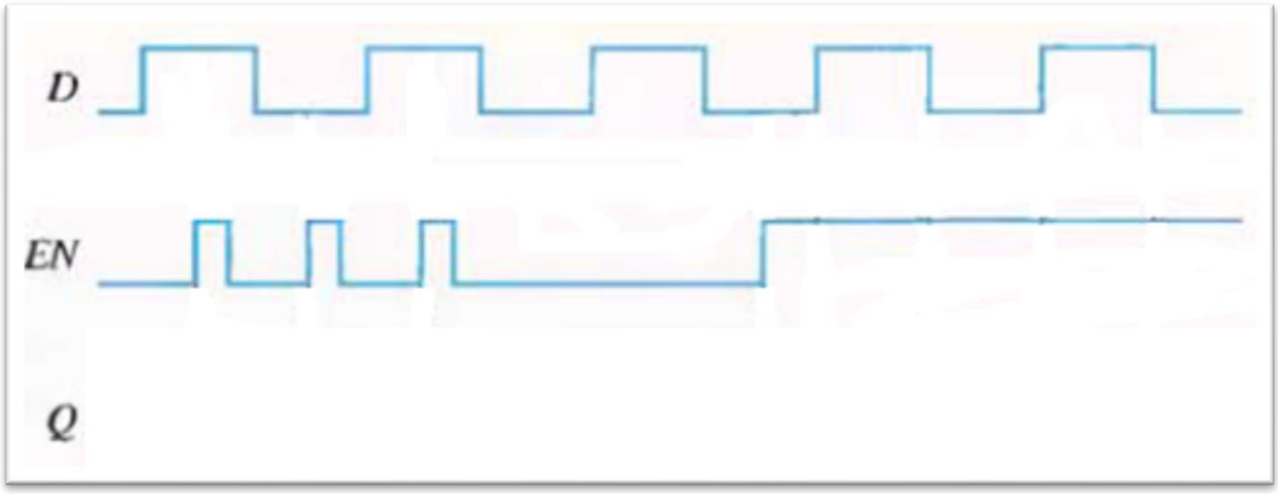


Figure 3. Input waveforms.

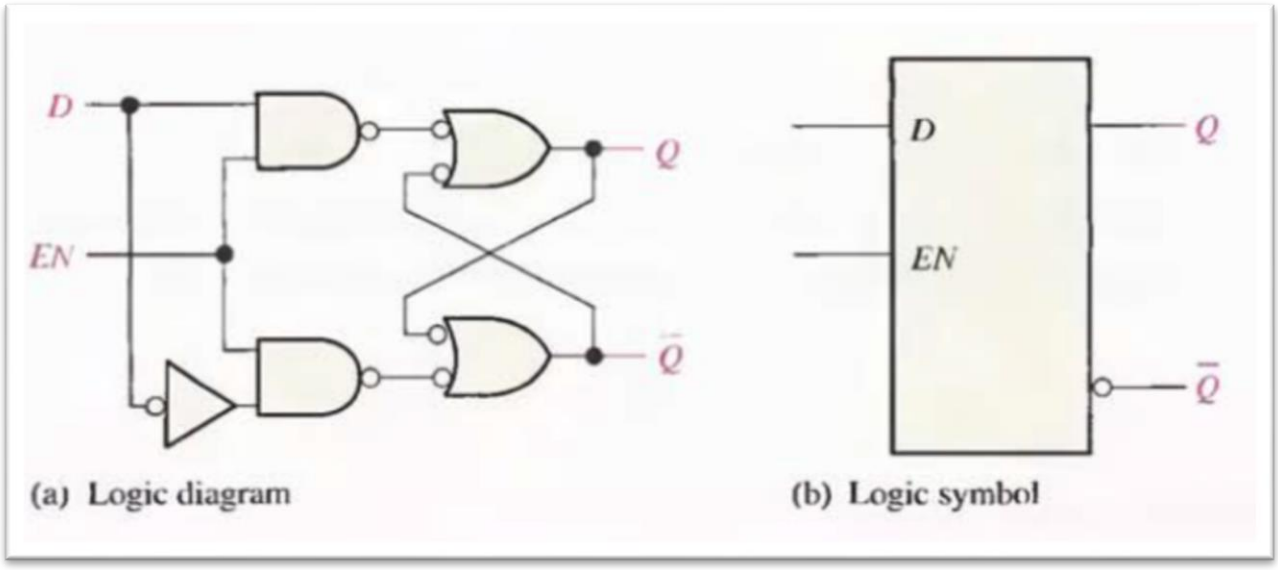


Figure 4. A gated D latch.

Problem 3.

Determine the Q and Q' output waveforms for the positive edge-triggered S-R flip-flop in Figure 6 for the S, R, and CLK inputs in Figure 5. Assume that the flip-flop is initially RESET.

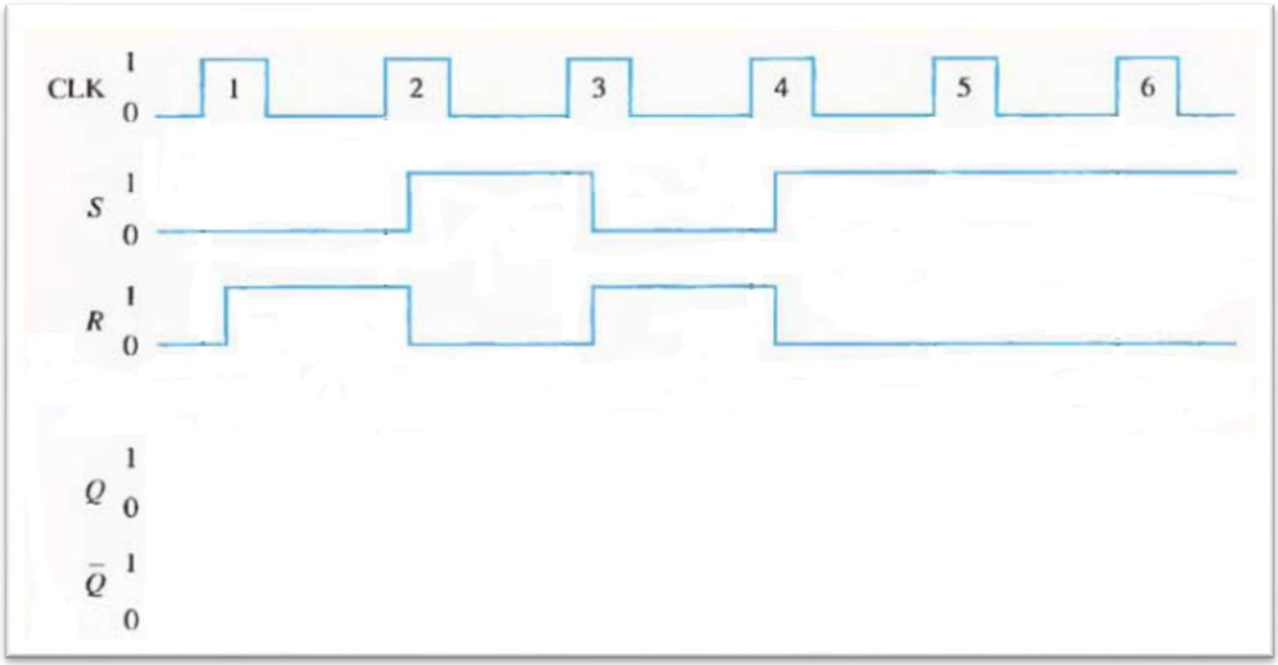


Figure 5. Input waveforms.

INPUTS S	R	CLK	OUTPUTS Q	$\overline{Q}$	COMMENTS
0	0	X	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	?	?	Invalid

↑ = clock transition LOW to HIGH

X = irrelevant ("don't care")

Q_0 = output level prior to clock transition

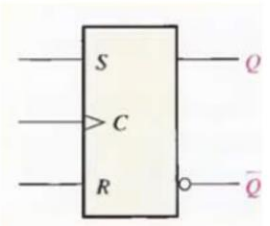


Figure 6: Truth table (left) and logic symbol (right) for a positive edge-triggered S-R flip-flop.

Problem 4.

Determine the Q output waveform for the positive edge-triggered D flip-flop in Figure 8 for the D and CLK inputs in Figure 7. Assume that the flip-flop starts out RESET.

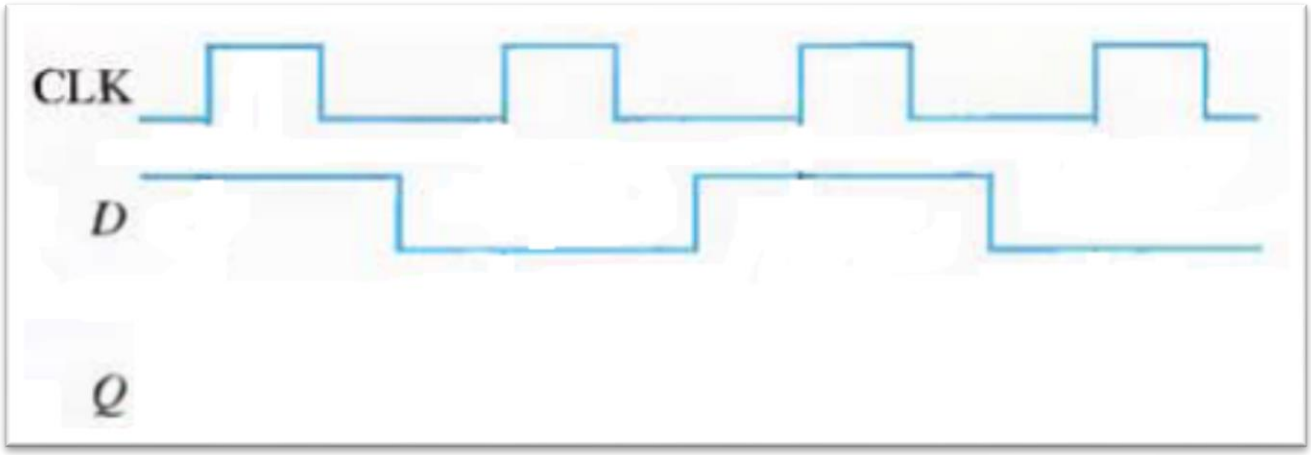
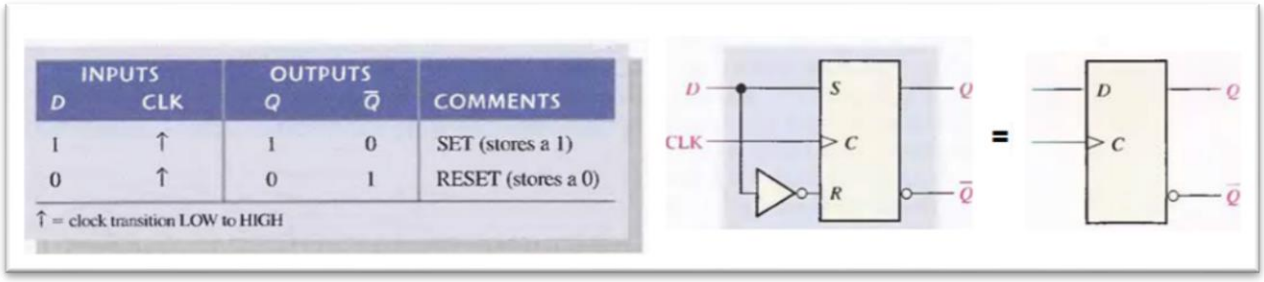


Figure 7. Input waveforms.



INPUTS		OUTPUTS		
D	CLK	Q	$\overline{Q}$	COMMENTS
1	↑	1	0	SET (stores a 1)
0	↑	0	1	RESET (stores a 0)

↑ = clock transition LOW to HIGH

Figure 8. Truth table (left) and logic symbols (right) for a positive edge-triggered D flip-flop.

Problem 5.

The waveforms in Figure 9 are applied to the J, K, and CLK inputs of the negative edge-triggered J-K flip-flop shown in Figure 10. Determine the Q output, assuming that the flip-flop is initially RESET.

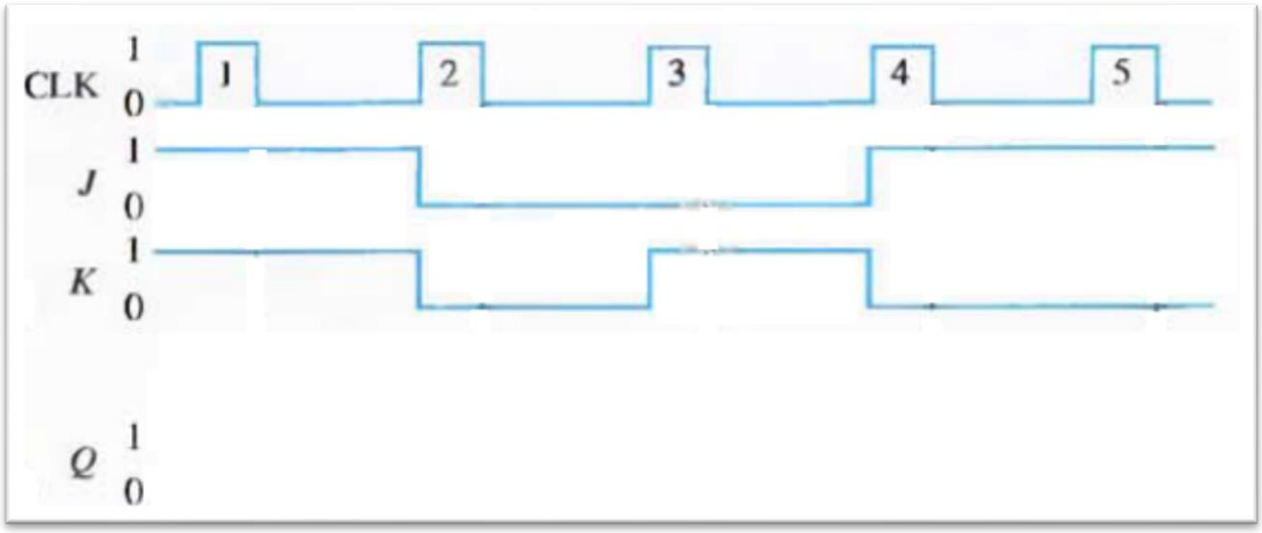


Figure 9. Input waveforms.

INPUTS			OUTPUTS		
J	K	CLK	Q	$\overline{Q}$	COMMENTS
0	0	↓	Q_0	$\overline{Q}_0$	No change
0	1	↓	0	1	RESET
1	0	↓	1	0	SET
1	1	↓	$\overline{Q}_0$	Q_0	Toggle

↓ = clock transition HIGH to LOW

Q_0 = output level prior to clock transition

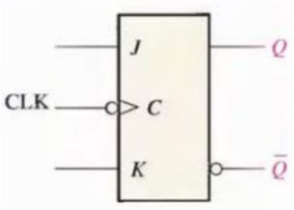


Figure 10. Truth table (left) and logic symbol (right) for a negative edge-triggered J-K flip-flop.

Problem 6.

The waveforms in Figure 11 are applied to the J, K, and CLK inputs of the positive edge-triggered J-K flip-flop shown in Figure 12. Determine the Q output, starting in RESET state.

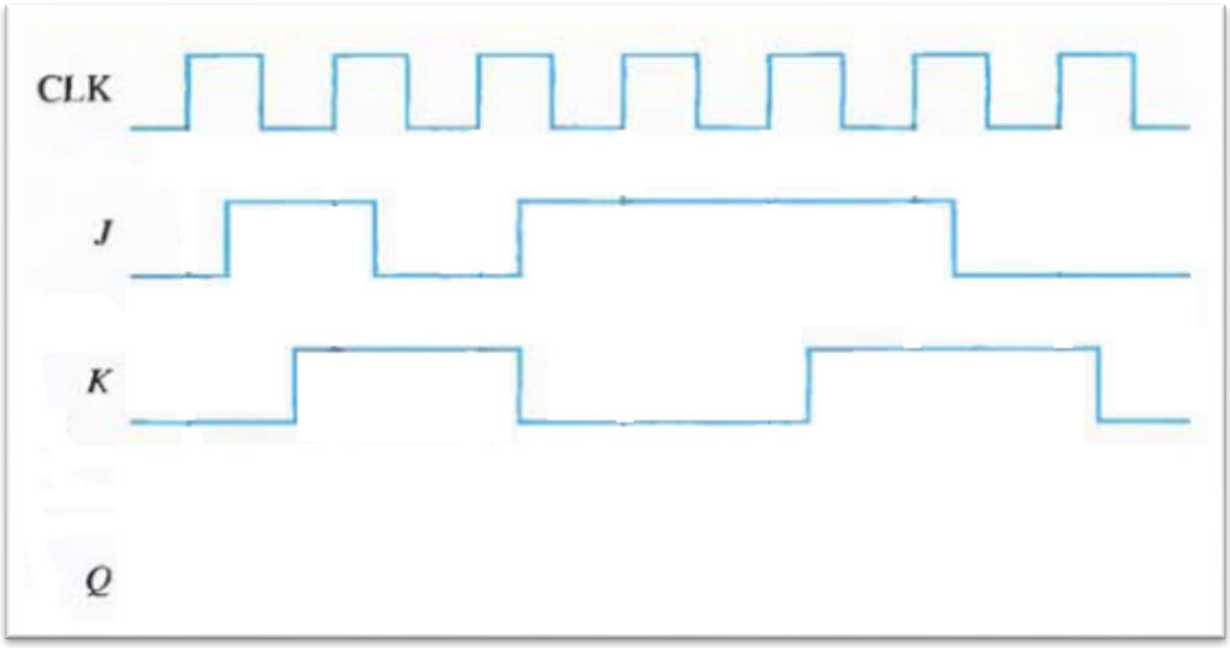
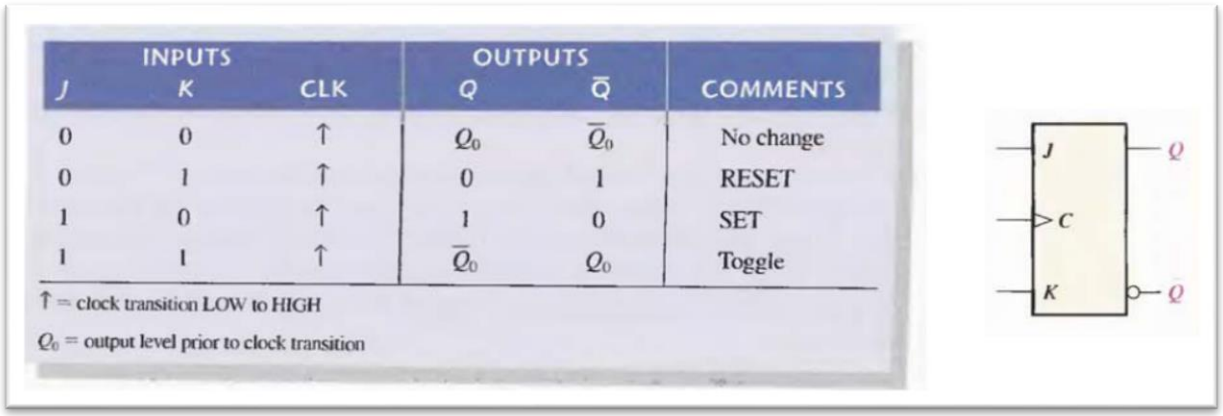


Figure 11. Input waveforms.



INPUTS			OUTPUTS		
J	K	CLK	Q	$\overline{Q}$	COMMENTS
0	0	↑	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\overline{Q}_0$	Q_0	Toggle

↑ = clock transition LOW to HIGH

Q_0 = output level prior to clock transition

Figure 12. Truth table (left) and logic symbol (right) for a positive edge-triggered J-K flip-flop.

Problem 7.

The J, K, CLK, PRE, and CLR waveforms in Figure 13 are applied to the negative edge-triggered J-K flip-flop in Figure 14. Determine the Q output waveform.

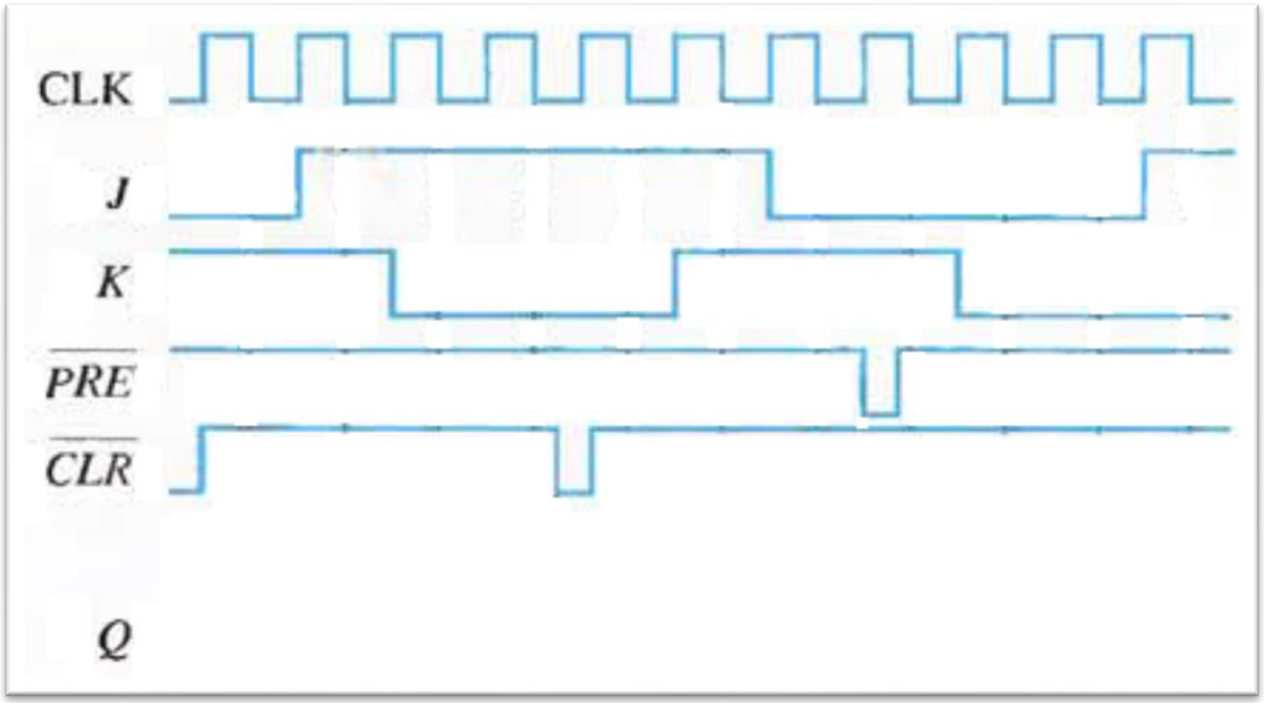


Figure 13. Input waveforms.

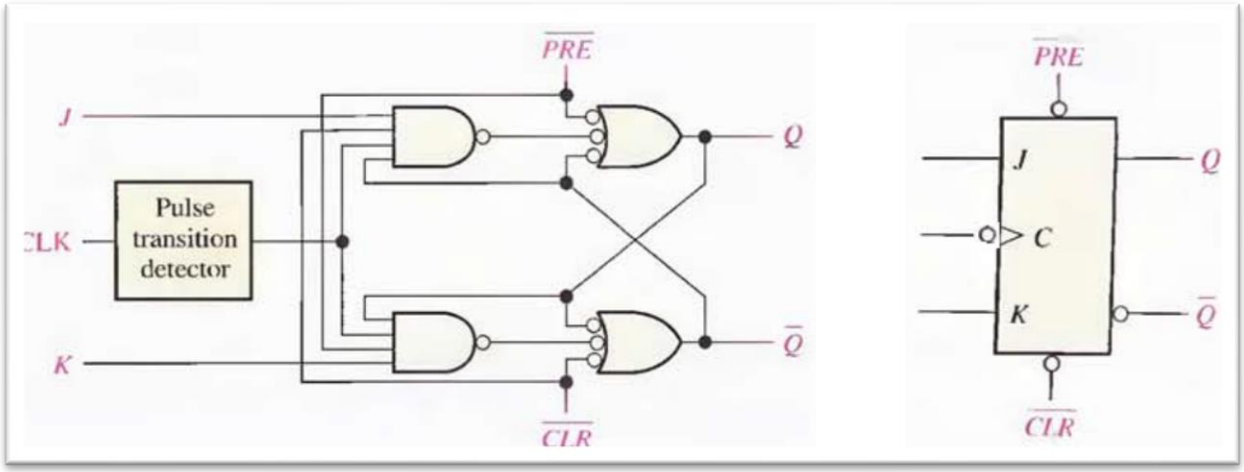


Figure 14. Logic circuit (left) and logic symbol (right) for a negative edge-triggered J-K flip-flop with active-LOW PRESET and CLEAR inputs.

Problem 8.

For the positive edge-triggered J-K flip-flop with active-LOW PRESET and CLEAR inputs and J-K inputs tied to a HIGH input (Figure 16), determine the Q output for the inputs shown in the timing diagram in Figure 15 if Q is initially LOW.

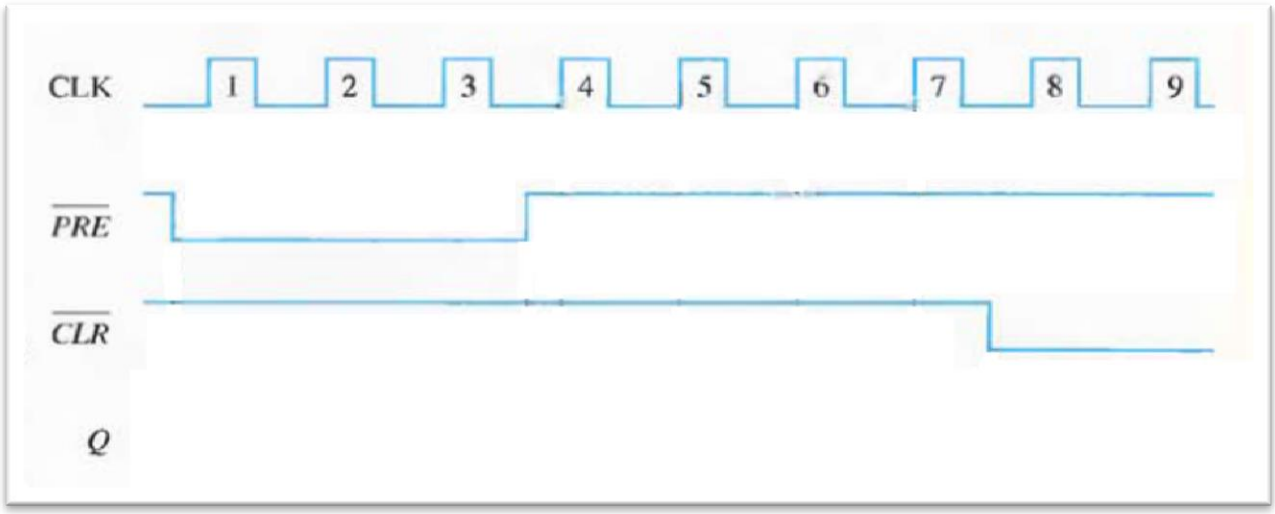


Figure 15. Input waveforms.

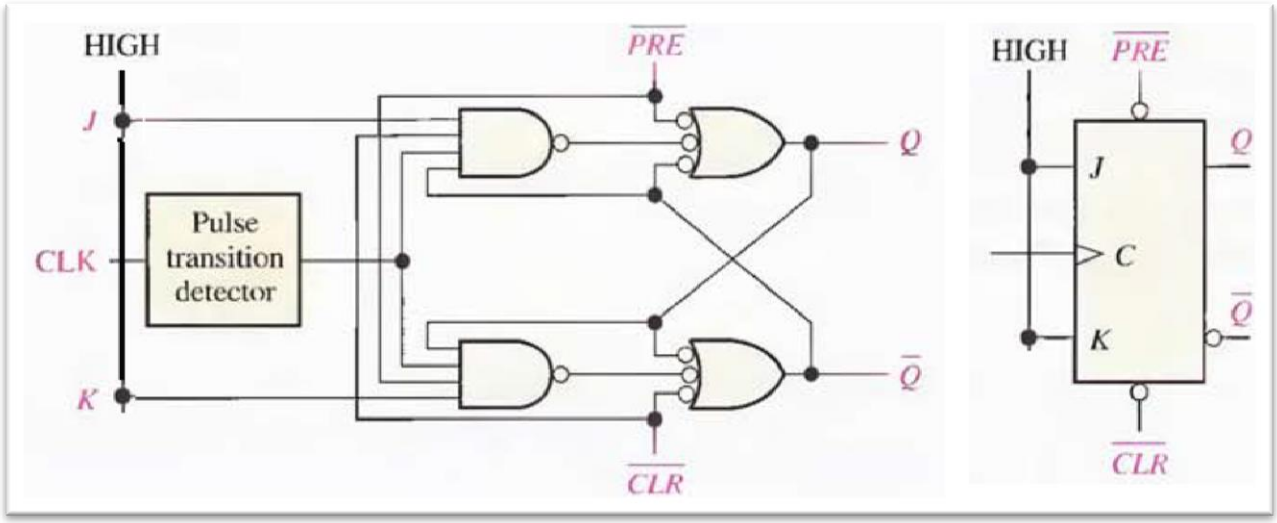


Figure 16. Logic circuit (left) and logic symbol (right) for a positive edge-triggered J-K flip-flop with active-LOW PRESET and CLEAR inputs and J-K inputs tied to a HIGH input.