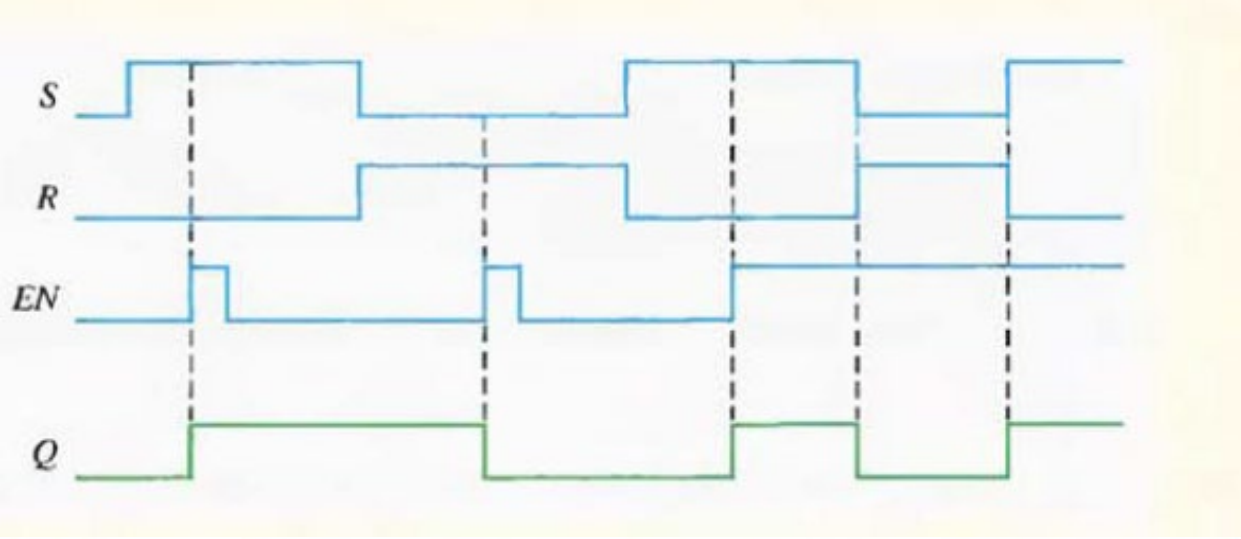
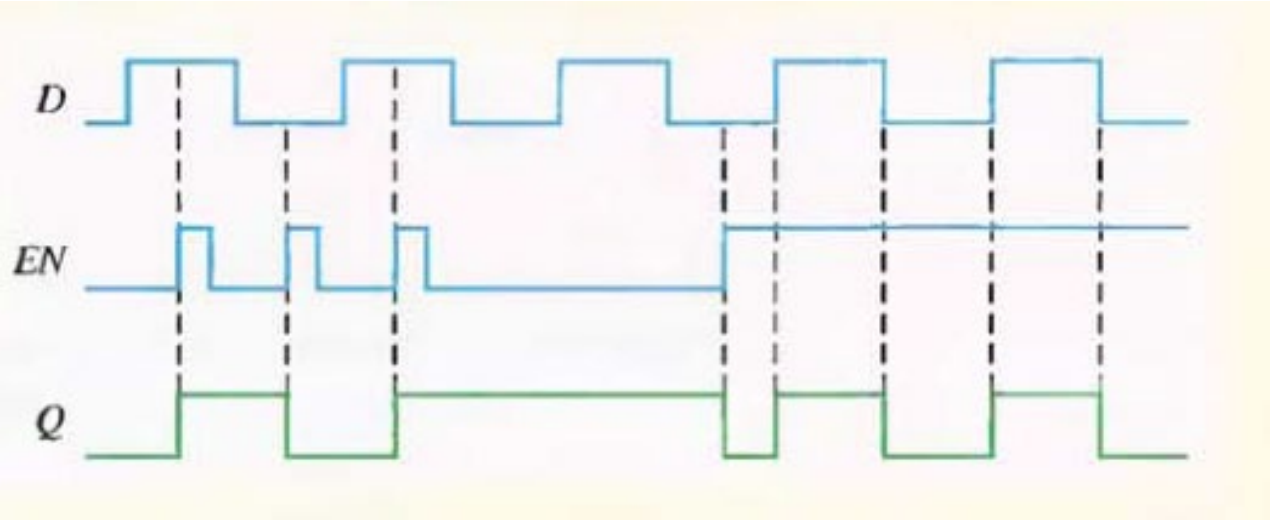
Homework 4 Solution

Problem 1.



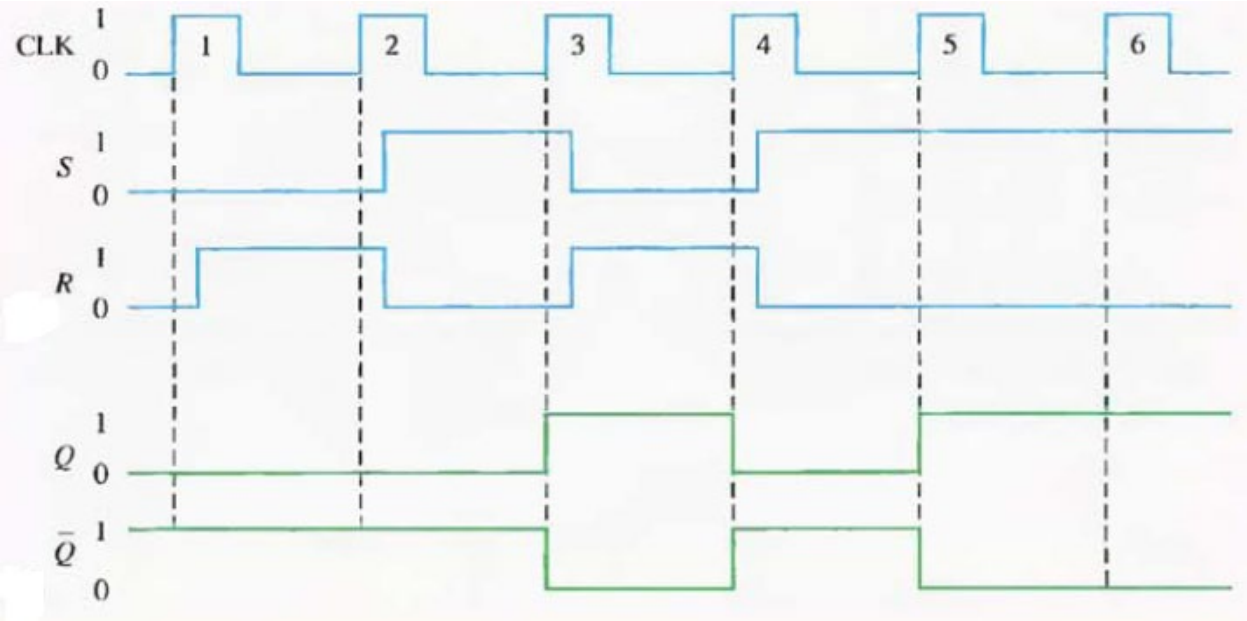
When S is HIGH and R is LOW, a HIGH on the EN input sets the latch. When S is LOW and R is HIGH, a HIGH on the EN input resets the latch.

Problem 2.



When D is HIGH and EN is HIGH, Q goes HIGH. When D is LOW and EN is HIGH, Q goes LOW. When EN is LOW, the state of the latch is not affected by the D input.

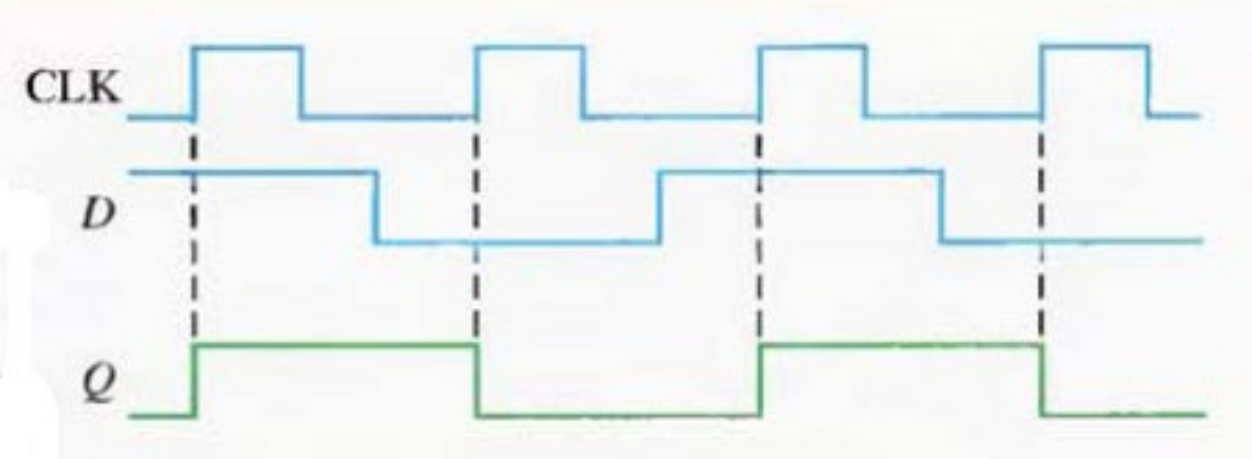
Problem 3.



1. At clock pulse 1, S is LOW and R is LOW, so Q does not change.
2. At clock pulse 2, S is LOW and R is HIGH, so Q remains LOW (RESET).
3. At clock pulse 3, S is HIGH and R is LOW, so Q goes HIGH (SET).
4. At clock pulse 4, S is LOW and R is HIGH, so Q goes LOW (RESET).
5. At clock pulse 5, S is HIGH and R is LOW, so Q goes HIGH (SET).
6. At clock pulse 6, S is HIGH and R is LOW, so Q stays HIGH.

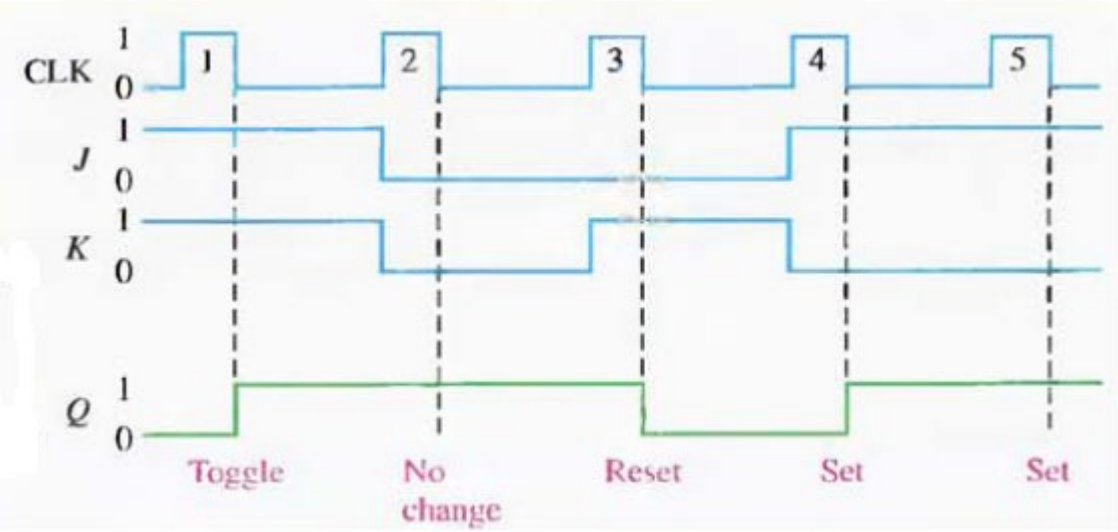
Once Q is determined, $\overline{Q}$ is easily found since it is simply the complement of Q.

Problem 4.



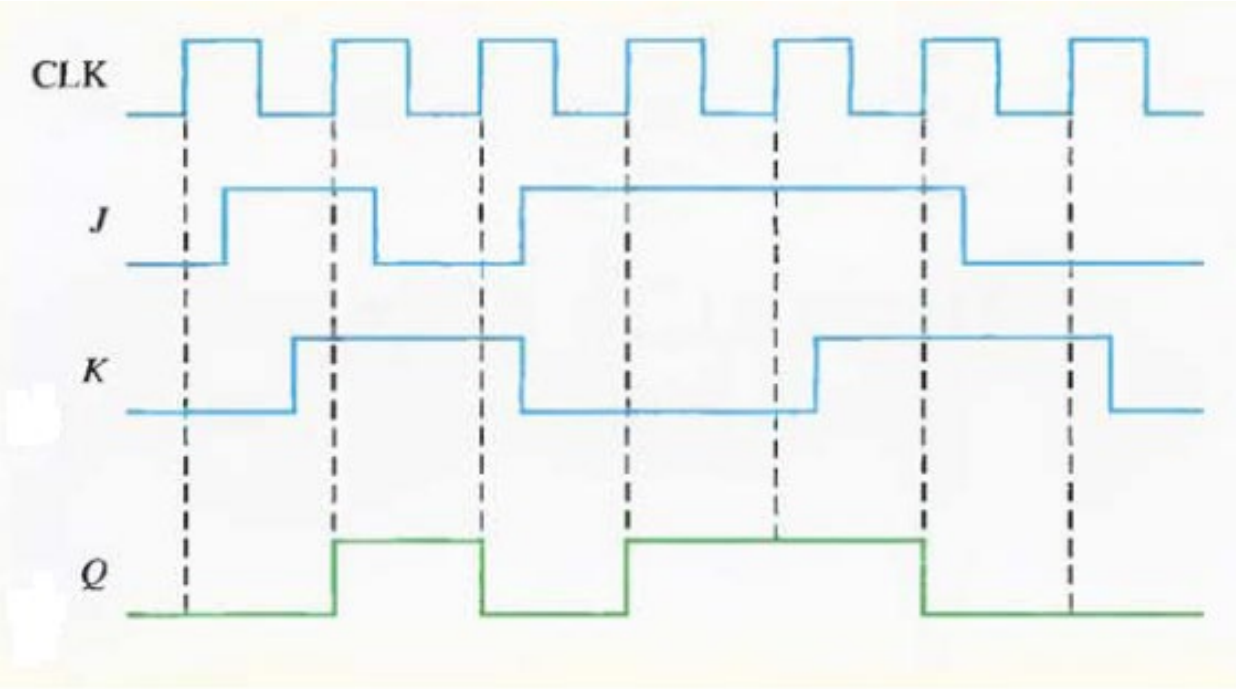
The Q output goes to the state of the D input at the time of the positive-going clock edge.

Problem 5.



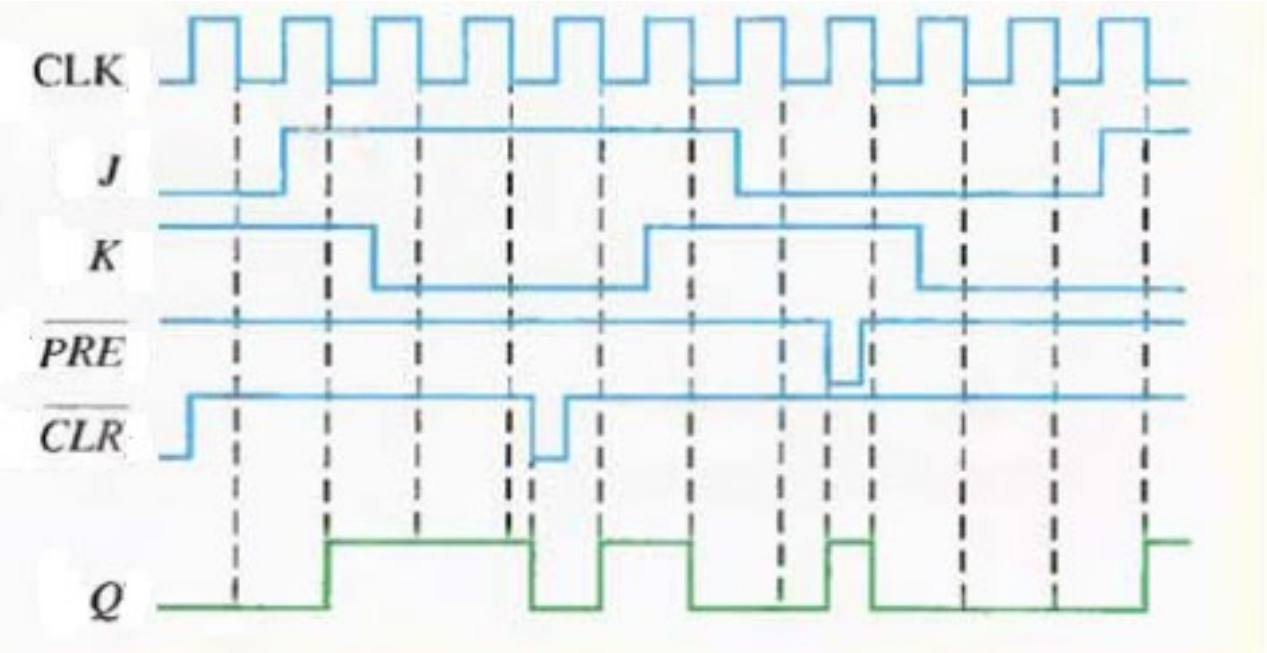
1. First, since this is a negative edge-triggered flip-flop, as indicated by the "bubble" at the clock input, the Q output will change only on the negative-going edge of the clock pulse.
2. At the first clock pulse, both J and K are HIGH; and because this is a toggle condition, Q goes HIGH.
3. At clock pulse 2, a no-change condition exists on the inputs, keeping Q at a HIGH level.
4. When clock pulse 3 occurs, J is LOW and K is HIGH, resulting in a RESET condition; Q goes LOW.
5. At clock pulse 4, J is HIGH and K is LOW, resulting in a SET condition; Q goes HIGH.
6. A SET condition still exists on J and K when clock pulse 5 occurs, so Q will remain HIGH.

Problem 6.



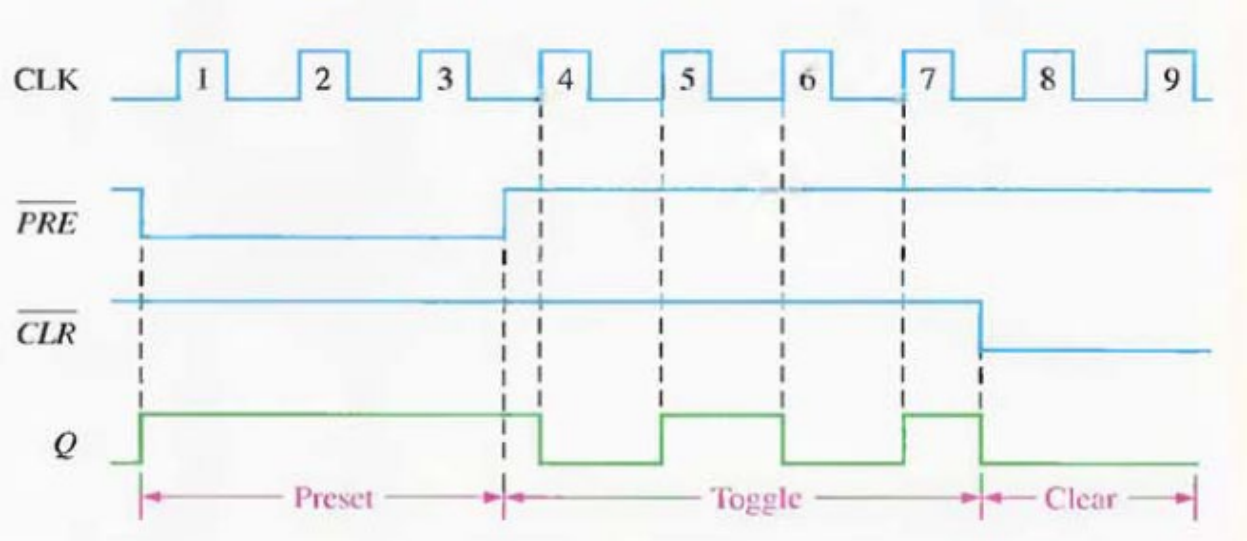
The Q output assumes the state determined by the states of the J and K inputs at the positive-going edge (triggering edge) of the clock pulse. A change in J or K after the triggering edge of the clock has no effect on the output, as shown in Figure

Problem 7.



Notice that each time a LOW is applied to the $\overline{PRE}$ or $\overline{CLR}$, the flip-fiop is set or reset regardless of the states of the other inputs.

Problem 8.



1. During clock pulses 1, 2, and 3, the preset ($\overline{PRE}$) is LOW, keeping the flip-flop SET regardless of the synchronous J and K inputs.

2. For clock pulses 4, 5, 6, and 7, toggle operation occurs because J is HIGH, K is HIGH, and both $\overline{PRE}$ and $\overline{CLR}$ are HIGH.

3. For clock pulses 8 and 9, the clear ($\overline{CLR}$) input is LOW, keeping the flip-flop RESET regardless of the synchronous inputs.