TI Designs: TIDA-01606

10-kW, Three-Level, Three-Phase Grid Tie Inverter Reference Design for Solar String Inverters

Description

This reference design provides an overview on how to implement a three-level, three-phase, SiC-based DC/AC grid-tie inverter stage. A higher switching frequency of 50 kHz reduces the size of magnetics for the filter design and as a result a higher power density. SiC MOSFETs with switching loss ensures higher DC bus voltages of up to 1000 V and lower switching losses with a peak efficiency of 99%. This design is configurable to work as a two-level or three-level inverter.

Resources

TIDA-01606	Design Folder
ISO5852S	Product Folder
UCC5320	Product Folder
TMDSCNCD28379D	Tool Folder
AMC1306M05	Product Folder
OPA4340	Product Folder
LM76003	Product Folder
PTH08080W	Product Folder
TLV1117LV	Product Folder
OPA350	Product Folder
UCC27211	Product Folder

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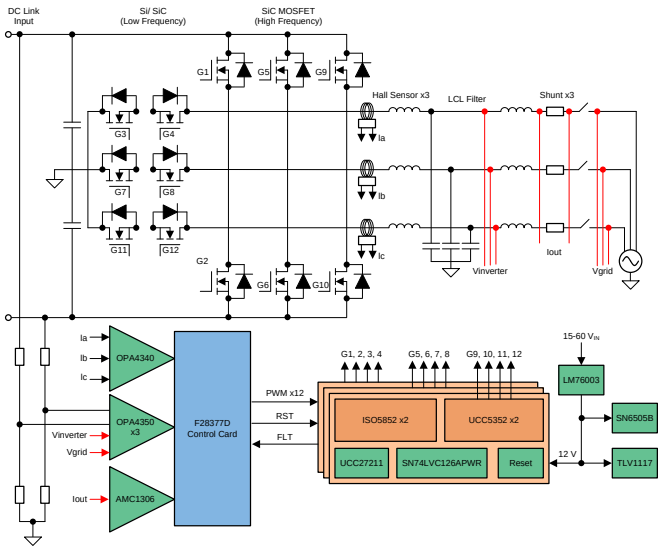
Features

- Rated Nominal and Max Input Voltage at 800-V and 1000-V DC
- Max 10-kW/10-kVA Output Power at 400-V AC 50- or 60-Hz Grid-Tie Connection
- Operating Power Factor Range From 0.7 Lag to 0.7 Lead
- High-Voltage (1200-V) SiC MOSFET-Based Full-Bridge Inverter for Peak Efficiency of 98.5%
- Compact Output Filter by Switching Inverter at 50 kHz
- <2% Output Current THD at Full Load
- Isolated Driver ISO5852S With Reinforced Isolation for Driving High-Voltage SiC MOSFET and UCC5320S for Driving Middle Si IGBT
- Isolated Current Sensing Using AMC1301 for Load Current Monitoring
- TMS320F28379D Control Card for Digital Control

Applications

- Solar String Inverters
- Solar Central Inverters



1 System Description

Modern commercial scale solar inverters are seeing innovation on two fronts, which lead to smaller, higher efficiency products on the market:

1. The move to higher voltage solar arrays
2. Reducing the size of the onboard magnetics

By increasing the voltage to 1000-V or 1500-V DC from the array, the current can be reduced to maintain the same power levels. This reduction in current results in less copper and smaller power conducting devices required in the design. The reduction in di/dt also reduces the stress on electrical components. However, sustained DC voltages of > 1 kV can be difficult to design to, or even find components that can survive it.

To compensate for the voltage stresses generated by high-voltage solar arrays, new topologies of solar inverters have been designed. Traditional half bridges block the full input voltage on each switching device. By adding additional switched blocking and conduction components, the overall stress on the device can be significantly reduced. This reference design shows how to implement a three-level converter. Higher level converters are also possible, further increasing the voltage handling capability.

Additional power density in solar electronics is also being enabled by moving to higher switching speeds in the power converters. As this design shows, even a modestly higher switching speed reduces the overall size requirement of the output filter stage—a primary contributor to the design size.

Traditional switching devices have a limit in how quickly they can switch high voltages, or more appropriately, the dV/dt ability of the device. This slow ramp up and down increases conduction loss because the device spends more time in a switching state. This increased switch time also increases the amount of dead time required in the control system to prevent shoot-through and shorts. The solution to this has been developed in newer switching semiconductor technology like SiC and GaN devices with high electron mobility. This reference design uses SiC MOSFETs alongside TI's SiC gate driver technology to demonstrate the potential increase in power density.

1.1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Output power	10 kW	Section 2.3
Output voltage	Three-phase 400-V AC	Section 2.3
Output frequency	50 or 60 Hz	Section 2.3
Output current	18 A (max)	Section 2.3
Nominal input voltage	800-V DC	Section 2.3
Input voltage range	600-V to 1000-V DC	Section 2.3
Inverter switching frequency	50 kHz	Section 2.3
Efficiency	99%	Section 2.3.1.5
Power density	1 kW/L+	

2 System Overview

2.1 Block Diagram

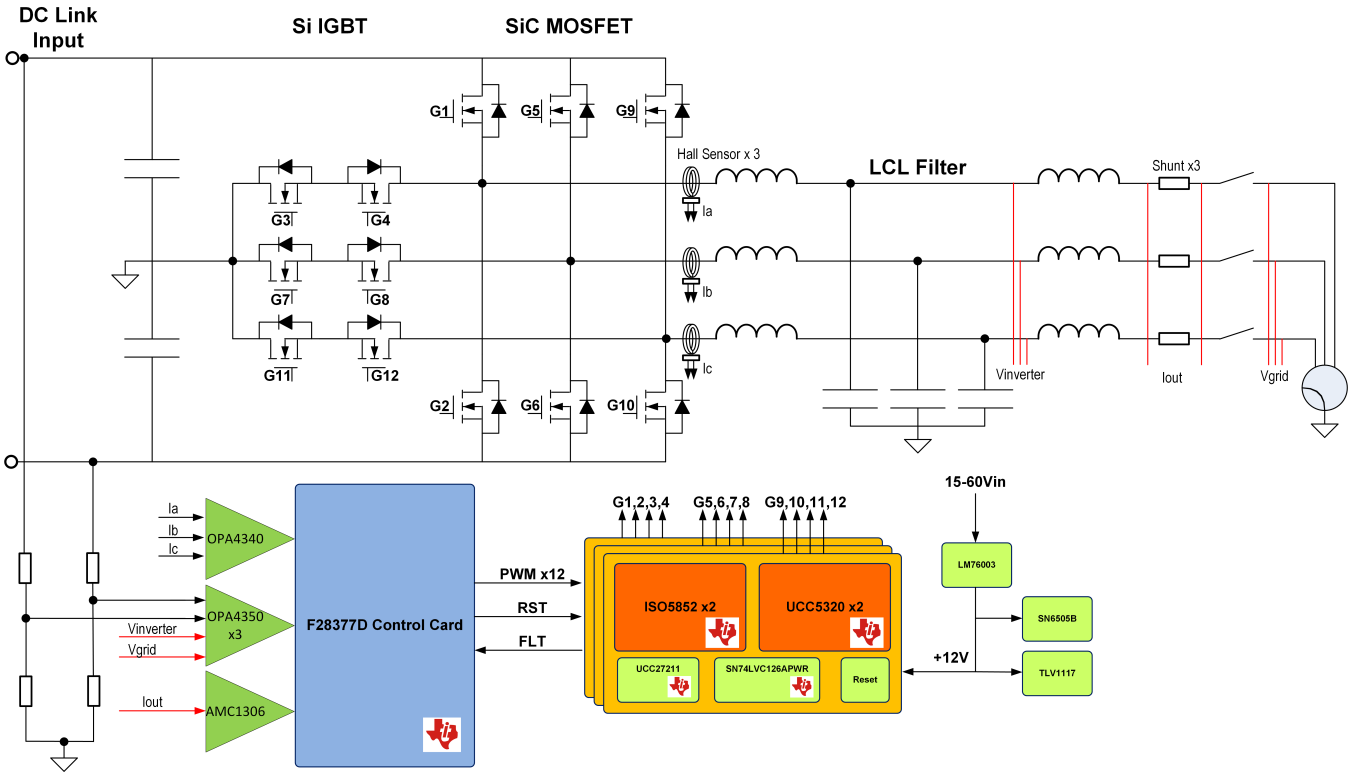


Figure 1. TIDA-01606 Block Diagram

This reference design is comprised of three separate boards that intercommunicate. The following boards work in tandem to form this three-phase inverter reference design:

- A power board, comprising all of the switching device, LCL filter, sensing electronics, and power structure
- A TMS320F28377D Control Card to support the DSP
- Three gate driver cards, each with two ISO5852S and two UCC5320 gate drivers

2.2 Highlighted Products

2.2.1 ISO5852S

The ISO5852S device is a 5.7-kV_{RMS}, reinforced isolated gate driver for IGBTs and MOSFETs with split outputs, OUTH and OUTL, providing 2.5-A source and 5-A sink current. The input side operates from a single 2.25-V to 5.5-V supply. The output side allows for a supply range from minimum 15 V to maximum 30 V. Two complementary CMOS inputs control the output state of the gate driver. The short propagation time of 76 ns provides accurate control of the output stage.

- 100-kV/μs minimum common-mode transient immunity (CMTI) at V_{CM} = 1500 V
- Split outputs to provide 2.5-A peak source and 5-A peak sink currents
- Short propagation delay: 76 ns (typ), 110 ns (max)
- 2-A active Miller clamp
- Output short-circuit clamp
- Soft turnoff (STO) during short circuit
- Fault alarm upon desaturation detection is signaled on FLT and reset through RST

- Input and output undervoltage lockout (UVLO) with Ready (RDY) pin indication
- Active output pulldown and default low outputs with low supply or floating inputs
- 2.25-V to 5.5-V input supply voltage
- 15-V to 30-V output driver supply voltage
- CMOS compatible inputs
- Rejects input pulses and noise transients shorter than 20 ns
- Operating temperature: –40°C to +125°C ambient
- Isolation surge withstand voltage of 12800-V_{PK}

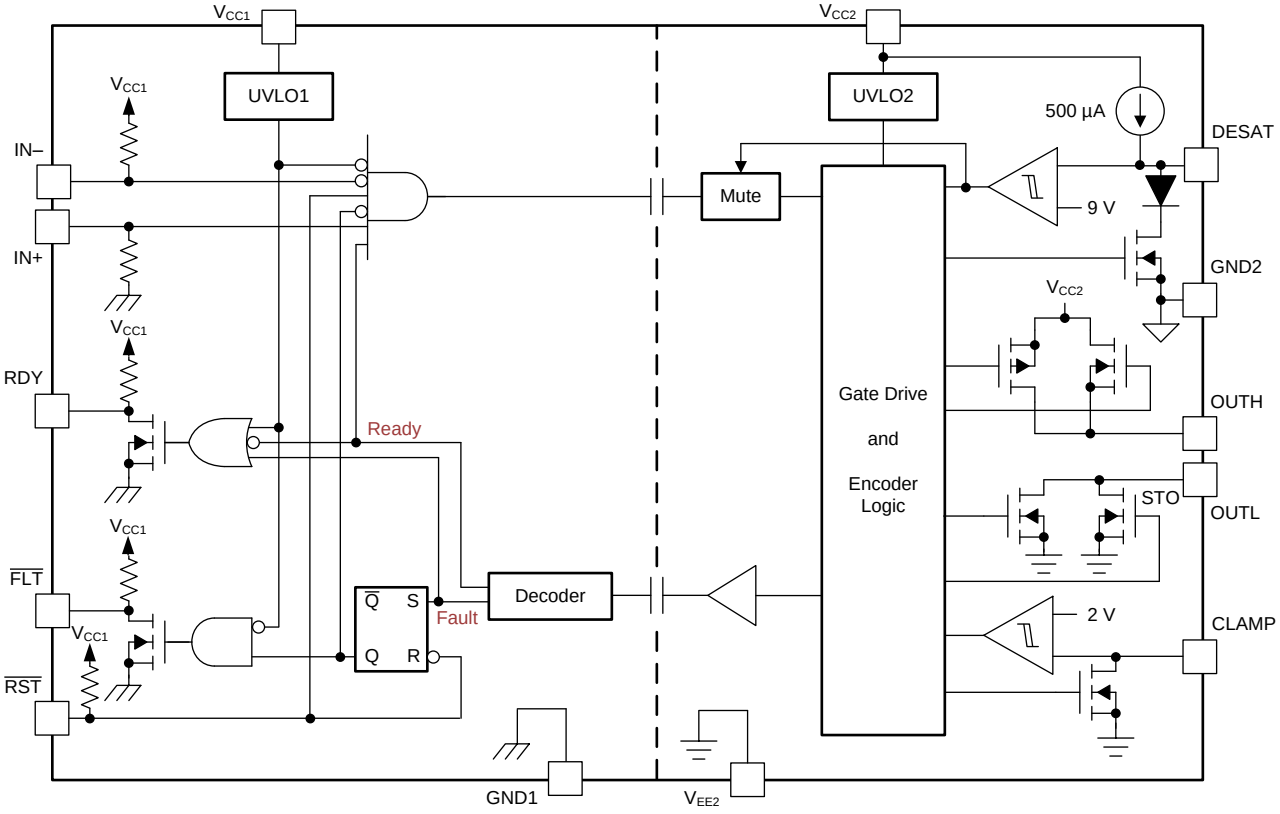


Figure 2. ISO5852S Functional Block Diagram

2.2.2 UCC5320

The UCC53x0 is a family of compact, single-channel, isolated IGBT, SiC, and MOSFET gate drivers with superior isolation ratings and variants for pinout configuration, and drive strength.

The UCC53x0 is available in an 8-pin SOIC (D) package. This package has a creepage and clearance of 4 mm and can support isolation voltage up to 3 kV_{RMS}, which is good for applications where basic isolation is needed. With these various options and wide power range, the UCC53x0 family is a good fit for motor drives and industrial power supplies.

- 3-V to 15-V input supply voltage
- 13.2-V to 33-V output driver supply voltage
- Feature options:
  - Split outputs (UCC5320S and UCC5390S)
  - UVLO with respect to IGBT emitter (UCC5320E and UCC5390E)
  - Miller clamp option (UCC5310M and UCC5350M)

- Negative 5-V handling capability on input pins
- 60-ns (typical) propagation delay for UCC5320S, UCC5320E, and UCC5310M
- 100-kV/µs minimum CMTI
- Isolation surge withstand voltage: 4242 V_{PK}
- Safety-related certifications:
  - 4242-V_{PK} isolation per DIN V VDE V 0884-10 and DIN EN 61010-1 (planned)
  - 3000-V_{RMS} isolation for 1 minute per UL 1577 (planned)
  - CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 61010-1 End Equipment Standards (Planned)
  - CQC Certification per GB4943.1-2011 (Planned)
- 4-kV ESD on all pins
- CMOS inputs
- 8-pin narrow body SOIC package
- Operating temperature: –40°C to +125°C ambient

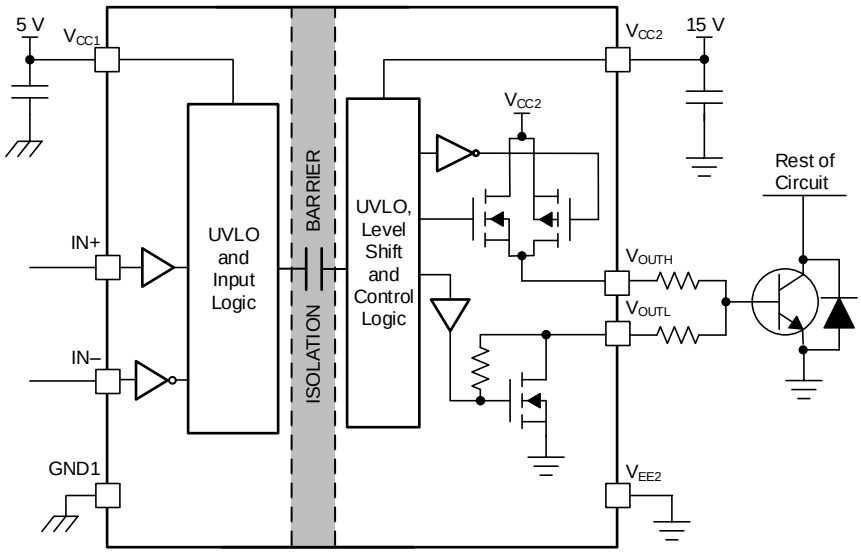


Figure 3. UCC5320 Functional Block Diagram (S Version)

2.2.3 TMS320F28379D

The Delfino™ TMS320F2837xD is a powerful 32-bit floating-point microcontroller unit (MCU) designed for advanced closed-loop control applications such as industrial drives and servo motor control; solar inverters and converters; digital power; transportation; and power line communications. Complete development packages for digital power and industrial drives are available as part of the powerSUITE and DesignDRIVE initiatives. While the Delfino product line is not new to the TMS320C2000™ portfolio, the F2837xD supports a new dual-core C28x architecture that significantly boosts system performance. The integrated analog and control peripherals also let designers consolidate control architectures and eliminate multiprocessor use in high-end systems.

- Dual-core architecture:
  - Two TMS320C28x 32-bit CPUs
  - 200 MHz
  - IEEE 754 single-precision floating-point unit (FPU)
  - Trigonometric math unit (TMU)
  - Viterbi/complex math unit (VCU-II)

- Two programmable control law accelerators (CLAs)
  - 200 MHz
  - IEEE 754 single-precision floating-point instructions
  - Executes code independently of main CPU
- On-chip memory
  - 512KB (256 kW) or 1MB (512 kW) of Flash (ECC-protected)
  - 172KB (86 kW) or 204KB (102 kW) of RAM (ECC-protected or parity-protected)
  - Dual-zone security supporting third-party development
- Clock and system control:
  - Two internal zero-pin 10-MHz oscillators
  - On-chip crystal oscillator
  - Windowed watchdog timer module
  - Missing clock detection circuitry
- 1.2-V core, 3.3-V I/O design
- System peripherals:
  - Two external memory interfaces (EMIFs) with ASRAM and SDRAM support
  - Dual six-channel direct memory access (DMA) controllers
  - Up to 169 individually programmable, multiplexed general-purpose input/output (GPIO) pins with input filtering
  - Expanded peripheral interrupt controller (ePIE)
  - Multiple low-power mode (LPM) support with external wakeup
- Communications peripherals:
  - USB 2.0 (MAC + PHY)
  - Support for 12-pin 3.3-V compatible universal parallel port (uPP) interface
  - Two controller area network (CAN) modules (pin-bootable)
  - Three high-speed (up to 50-MHz) SPI ports (pin-bootable)
  - Two multichannel buffered serial ports (McBSPs)
  - Four serial communications interfaces (SCI/UART) (pin-bootable)
  - Two I^2C interfaces (pin-bootable)
- Analog subsystem:
  - Up to four analog-to-digital converters (ADCs):
    - 16-bit mode
      - 1.1 MSPS each (up to 4.4-MSPS system throughput)
      - Differential inputs
      - Up to 12 external channels
    - 12-bit mode
      - 3.5 MSPS each (up to 14-MSPS system throughput)
      - Single-ended inputs
      - Up to 24 external channels
    - Single sample-and-hold (S/H) on each ADC
    - Hardware-integrated post-processing of ADC conversions:
      - Saturating offset calibration
      - Error from setpoint calculation
      - High, low, and zero-crossing compare, with interrupt capability
      - Trigger-to-sample delay capture
  - Eight windowed comparators with 12-bit digital-to-analog converter (DAC) references

  - Three 12-bit buffered DAC outputs
- Enhanced control peripherals:
  - 24 pulse width modulator (PWM) channels with enhanced features
  - 16 high-resolution pulse width modulator (HRPWM) channels:
    - High resolution on both A and B channels of eight PWM modules
    - Dead-band support (on both standard and high resolution)
  - Six enhanced capture (eCAP) modules
  - Three enhanced quadrature encoder pulse (eQEP) modules
  - Eight sigma-delta filter module (SDFM) input channels, two parallel filters per channel:
    - Standard SDFM data filtering
    - Comparator filter for fast action for out of range

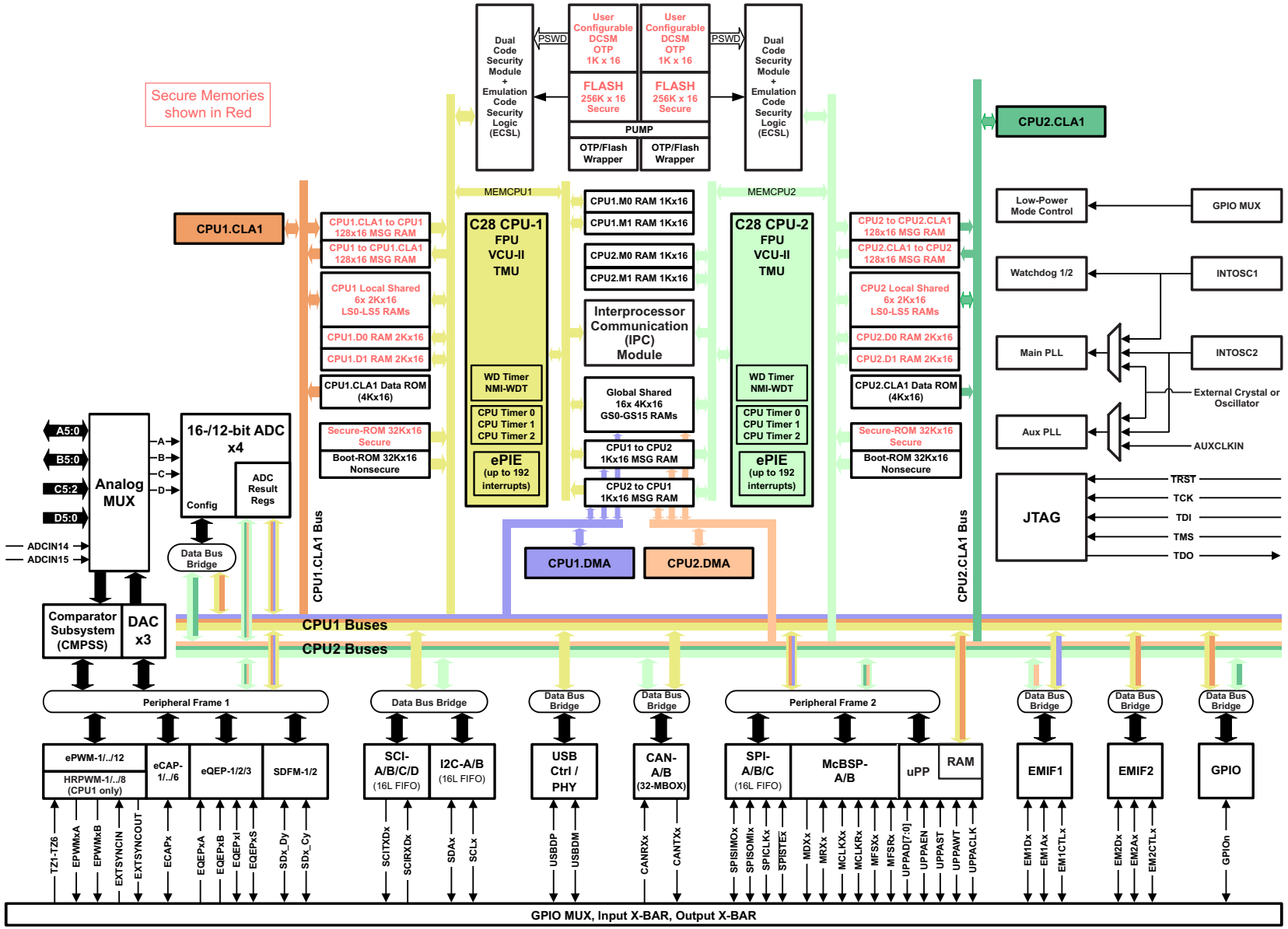


Figure 4. TMS320F28377D Functional Block Diagram

2.2.4 AMC1305M05

The AMC1305 device is a precision, delta-sigma (ΔΣ) modulator with the output separated from the input circuitry by a capacitive double isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced isolation of up to 7000 V_{PEAK} according to the DIN V VDE V 0884-10, UL1577, and CSA standards. Used in conjunction with isolated power supplies, the device prevents noise currents on a high common-mode voltage line from entering the local system ground and interfering with or damaging low voltage circuitry.

- Pin-compatible family optimized for shunt-resistor-based current measurements:
  - ±50-mV or ±250-mV input voltage ranges
  - CMOS or LVDS digital interface options
- Excellent DC performance supporting high-precision sensing on system level:
  - Offset error: ±50 µV or ±150 µV (max)
  - Offset drift: 1.3 µV/°C (max)
  - Gain error: ±0.3% (max)
  - Gain drift: ±40 ppm/°C (max)
- Safety-related certifications:
  - 7000-V_{PK} reinforced isolation per DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12
  - 5000-V_{RMS} isolation for 1 minute per UL1577
  - CAN/CSA No. 5A-Component Acceptance Service Notice, IEC 60950-1, and IEC 60065 End Equipment Standards
- Transient immunity: 15 kV/µs (min)
- High electromagnetic field immunity (see *ISO72x Digital Isolator Magnetic-Field Immunity*)
- External 5-MHz to 20-MHz clock input for easier system-level synchronization
- Fully specified over the extended industrial temperature range

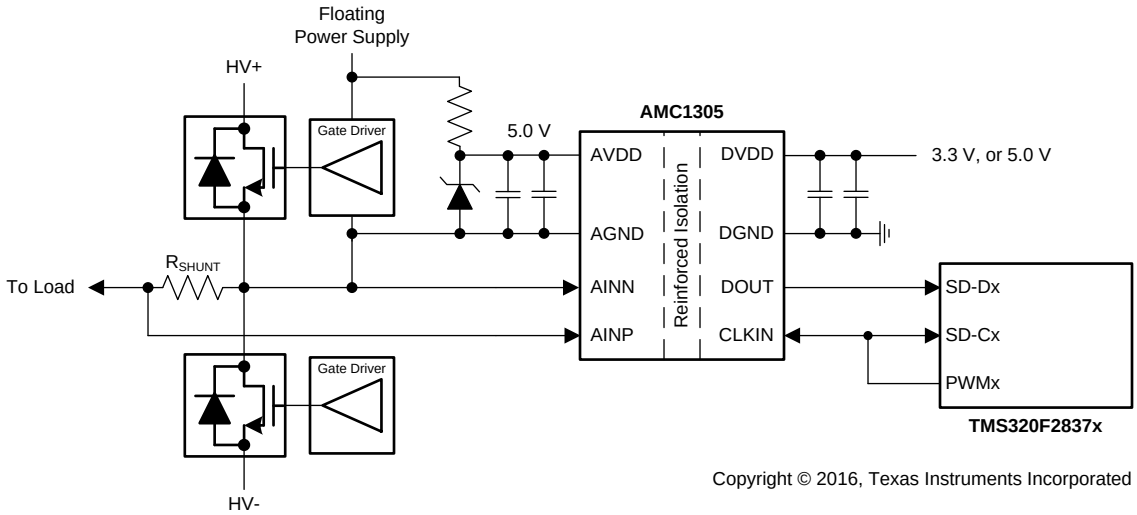


Figure 5. AMC1305M05 Simplified Schematic

2.2.5 OPA4340

The OPA4340 series rail-to-rail CMOS operational amplifiers are optimized for low-voltage, single-supply operation. Rail-to-rail input and output and high-speed operation make them ideal for driving sampling ADCs. These op amps are also well-suited for general purpose and audio applications as well as providing I/V conversion at the output of DACs. Single, dual, and quad versions have identical specifications for design flexibility.

- Rail-to-rail input
- Rail-to-rail output (within 1 mV)
- MicroSize packages
- Wide bandwidth: 5.5 MHz
- High slew rate: 6 V/µs
- Low THD + noise: 0.0007% (f = 1 kHz)
- Low quiescent current: 750 µA/channel
- Single, dual, and quad versions

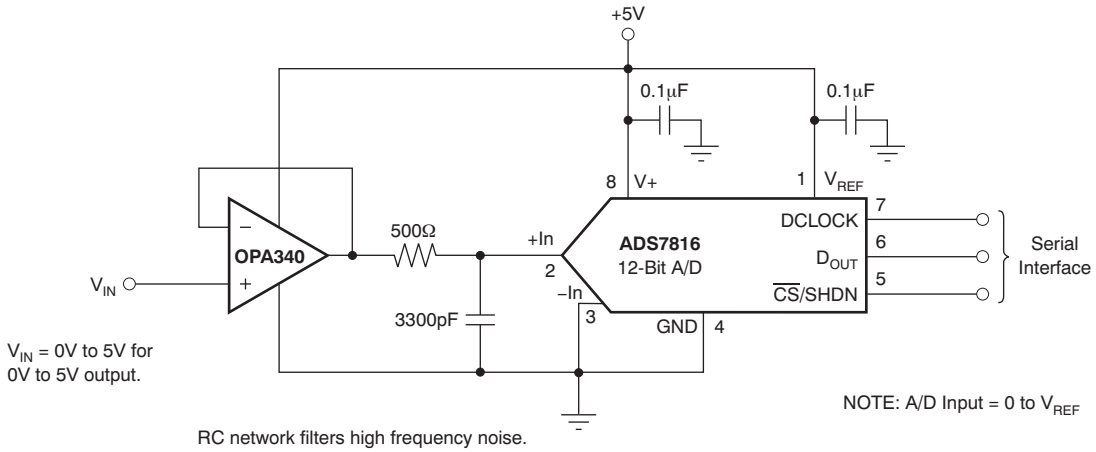


Figure 6. OPA4340 in Non-Inverting Configuration

2.2.6 LM76003

The LM76002/LM76003 regulator is an easy-to-use synchronous step-down DC/DC converter capable of driving up to 2.5 A (LM76002) or 3.5 A (LM76003) of load current from an input up to 60 V. The LM76002/LM76003 provides exceptional efficiency and output accuracy in a very small solution size. Peak current-mode control is employed. Additional features such as adjustable switching frequency, synchronization, FPWM option, power-good flag, precision enable, adjustable soft start, and tracking provide both flexible and easy-to-use solutions for a wide range of applications. Automatic frequency foldback at light load and optional external bias improve efficiency. This device requires few external components and has a pinout designed for simple PCB layout with best-in-class EMI (CISPR22) and thermal performance. Protection features include thermal shutdown, input UVLO, cycle-by-cycle current limit, and short-circuit protection. The LM76002/LM76003 device is available in the WQFN 30-pin leadless package with wettable flanks.

- Integrated synchronous rectification
- Input voltage: 3.5 V to 60 V (65 V maximum)
- Output current:
  - LM76002: 2.5 A
  - LM76003: 3.5 A
- Output voltage: 1 V to 95% V_{IN}
- 15-µA quiescent current in regulation
- Wide voltage conversion range:

  - t_{ON-MIN} = 65 ns (typical)
  - $t_{OFF-MIN}$ = 95 ns (typical)
- System-level features:
  - Synchronization to external clock
  - Power-good flag
  - Precision enable
  - Adjustable soft start (6.3 ms default)
  - Voltage tracking capability
- Pin-selectable FPWM operation
- High-efficiency at light-load architecture (PFM)
- Protection features:
  - Cycle-by-cycle current limit
  - Short-circuit protection with hiccup mode
  - Overtemperature thermal shutdown protection

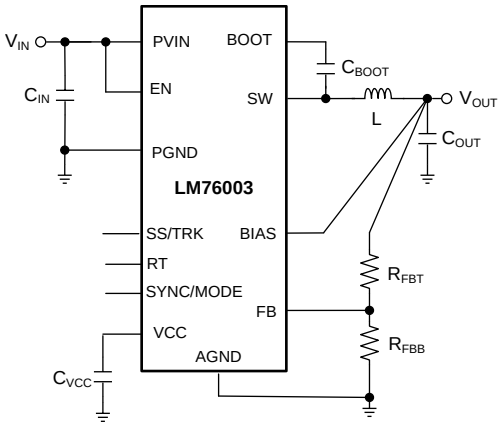


Figure 7. LM76003 Simplified Schematic

2.2.7 PTH08080W

The PTH08080W is a highly integrated, low-cost switching regulator module that delivers up to 2.25 A of output current. The PTH08080W sources output current at a much higher efficiency than a TO-220 linear regulator, thereby eliminating the need for a heat sink. Its small size (0.5 × 0.6 in) and flexible operation creates value for a variety of applications.

- Up to 2.25-A output current at 85°C
- 4.5-V to 18-V input voltage range
- Wide-output voltage adjust (0.9 V to 5.5 V)
- Efficiencies Up To 93%
- On/off inhibit
- UVLO
- Output overcurrent protection (non-latching, auto-reset)
- Overtemperature protection
- Ambient temperature range: –40°C to +85°C
- Surface-mount package
- Safety agency approvals: UL/CUL 60950, EN60950

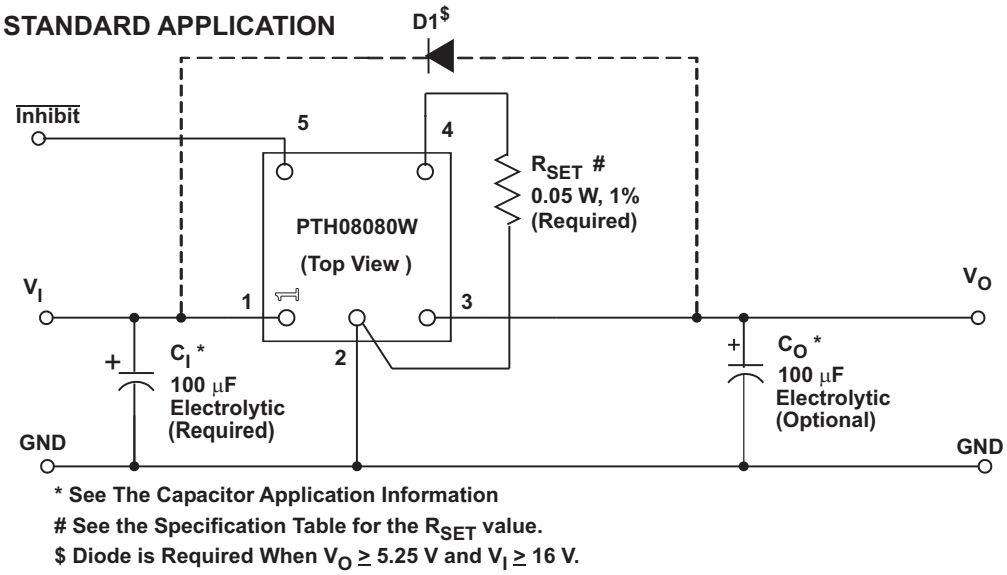


Figure 8. PTH08080W Standard Application

2.2.8 TLV1117

The TLV1117 device is a positive low-dropout voltage regulator designed to provide up to 800 mA of output current. The device is available in 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V, and adjustable-output voltage options. All internal circuitry is designed to operate down to 1-V input-to-output differential. Dropout voltage is specified at a maximum of 1.3 V at 800 mA, decreasing at lower load currents.

- 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V, and adjustable-output voltage options
- Output current: 800 mA
- Specified dropout voltage at multiple current levels
- 0.2% line regulation maximum
- 0.4% load regulation maximum

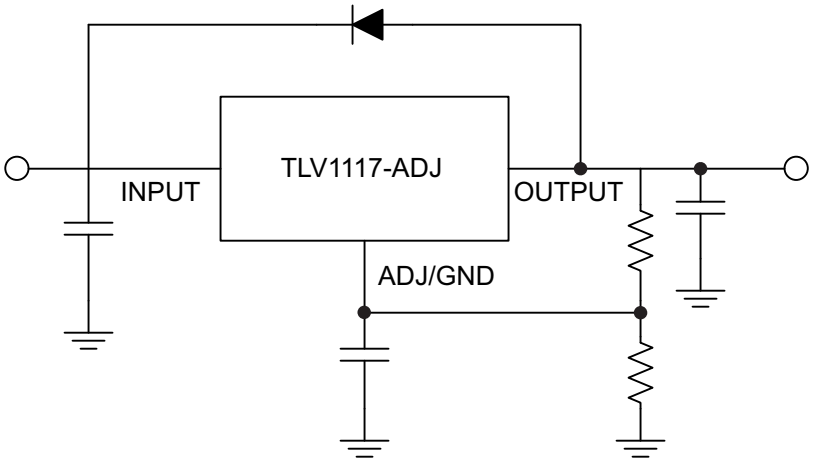


Figure 9. TLV1117 Simplified Schematic

2.2.9 OPA350

The OPA350 series of rail-to-rail CMOS operational amplifiers are optimized for low voltage, single-supply operation. Rail-to-rail input and output, low noise (5 nV/√Hz), and high speed operation (38 MHz, 22 V/µs) make the amplifiers ideal for driving sampling ADCs. They are also suited for cell phone PA control loops and video processing (75-Ω drive capability), as well as audio and general purpose applications. Single, dual, and quad versions have identical specifications for maximum design flexibility.

- Rail-to-rail input
- Rail-to-rail output (within 10 mV)
- Wide bandwidth: 38 MHz
- High slew rate: 22 V/µs
- Low noise: 5 nV/√Hz
- Low THD+noise: 0.0006%
- Unity-gain stable
- MicroSize packages
- Single, dual, and quad

2.2.10 UCC27211

The UCC27210 and UCC27211 drivers are based on the popular UCC27200 and UCC27201 MOSFET drivers, but offer several significant performance improvements. Peak output pull-up and pull-down current has been increased to 4-A source and 4-A sink, and pull-up and pull-down resistance have been reduced to 0.9 Ω, thereby allowing for driving large power MOSFETs with minimized switching losses during the transition through the Miller Plateau of the MOSFET. The input structure is now able to directly handle –10 VDC, which increases robustness and also allows direct interface to gate-drive transformers without using rectification diodes. The inputs are also independent of supply voltage and have a maximum rating of 20-V.

- Drives two N-channel MOSFETs in high-side and low-side configuration with independent inputs
- Maximum boot voltage: 120-V DC
- 4-A sink, 4-A source output currents
- 0.9-Ω pullup and pulldown resistance
- Input pins can tolerate –10 V to +20 V and are independent of supply voltage range
- TTL or pseudo-CMOS compatible input versions
- 8-V to 17-V VDD operating range (20-V absolute maximum)
- 7.2-ns rise and 5.5-ns fall time with 1000-pF load
- Fast propagation delay times (18 ns typical)
- 2-ns delay matching
- Symmetrical UVLO for high-side and low-side driver
- All industry standard packages available (SOIC-8, PowerPAD™ SOIC-8, 4-mm × 4-mm SON-8 and 4-mm × 4-mm SON-10)
- Specified from –40°C to +140°C

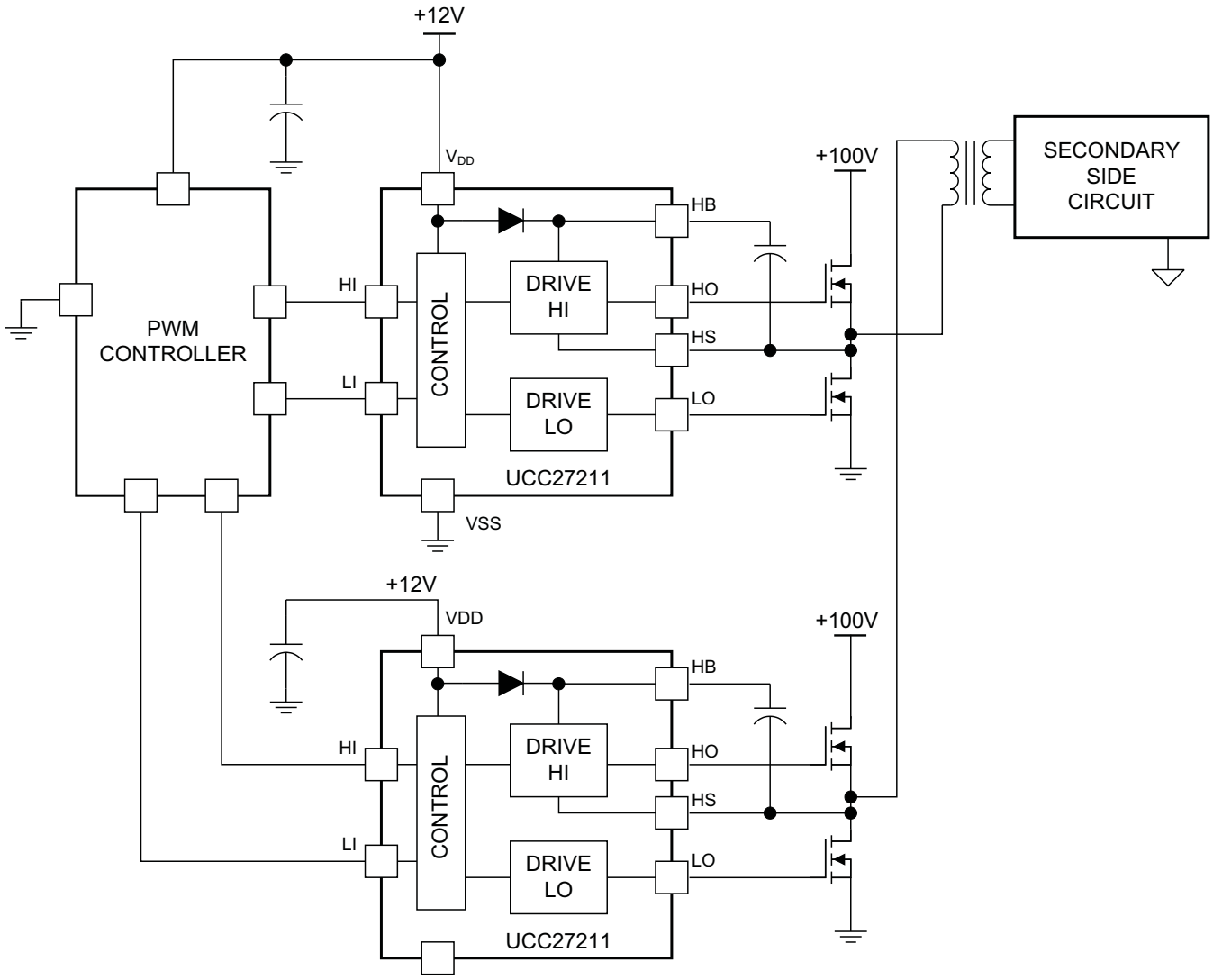


Figure 10. UCC27211 Typical Application

2.3 System Design Theory

2.3.1 Three-Phase T-Type Inverter

2.3.1.1 Architecture Overview

To understand the impetus behind a three level t-type inverter, some background on a traditional two-level inverter is required. A typical implementation of this architecture is shown in Figure 11.

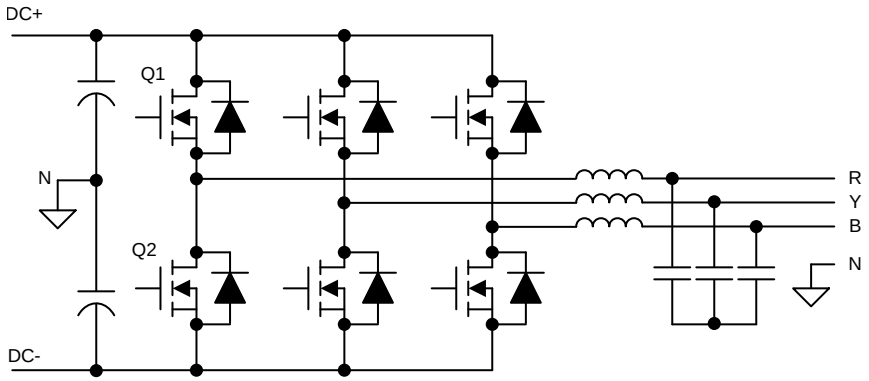


Figure 11. Two-Level, Three-Phase Inverter Architecture

To simplify the analysis, a single leg can be isolated.

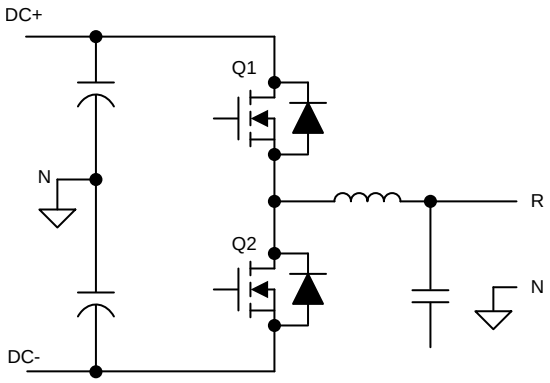


Figure 12. Two-Level, Single-Phase Inverter Leg

In this example, the two switching devices as a pair have four possible conduction states, independent of the other phases:

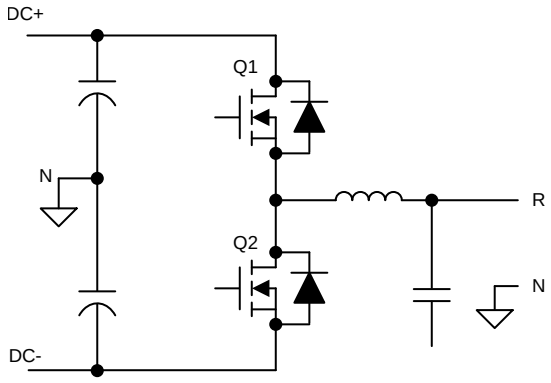


Figure 13. Q1 and Q2 off

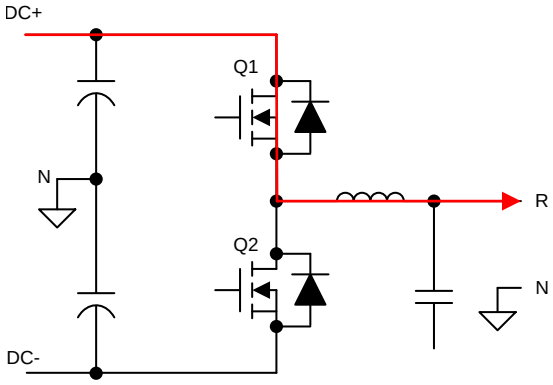


Figure 14. Q1 on, and Q2 off

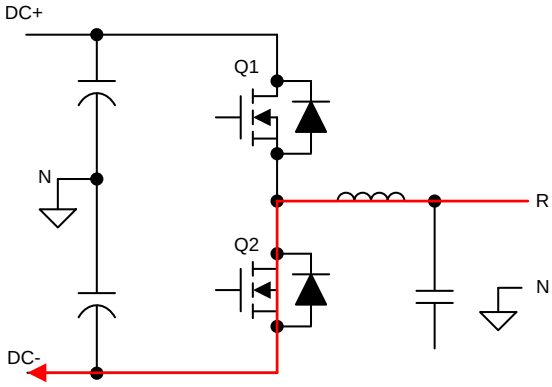


Figure 15. Q1 off, and Q2 on

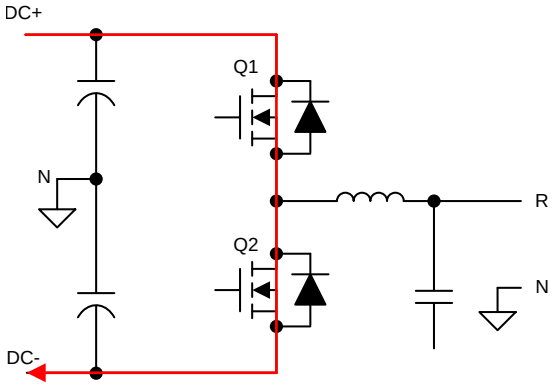


Figure 16. Q1 and Q2 on (Invalid)

By observing the current path through the inverter, each switching device must be capable of blocking the full DC link voltage present between DC+ and DC–. In traditional low-voltage systems (< 600 V), this capability is fairly trivial with common off-the-shelf IGBTs. However, if the DC link voltage is pushed higher to increase the power throughput without increasing current, as is a common trend in power electronics, this limitation puts an upper level on the supported voltage ranges.

Additionally, the increased voltage does result in increased switching losses in the traditional IGBTs. The low dV/dt exacerbates itself in these devices, even if they are able to support the higher voltages. This dV/dt is what determines how quickly one device can transition from on to off (or vice versa), thus dictating the dead time between each of these states. An elongated switch time or dead time means the switches spend less time at full conduction, resulting in decreased efficiency.

These two primary drawbacks of a two-level inverter are what drives the implementation in this design.

The next step up from a standard two-level inverter is a T-type three-level inverter. This type is implemented by inserting two back-to-back switching devices between the switch node and the neutral point of the DC link created by the bulk input capacitors. These two switch devices are placed in a common emitter configuration so that current flow can be controlled by switching one or the other on or off. This configuration also enables both of them to share a common bias supply as the gate-emitter voltage is identically referenced. Figure 17 shows a simplified view of the implementation.

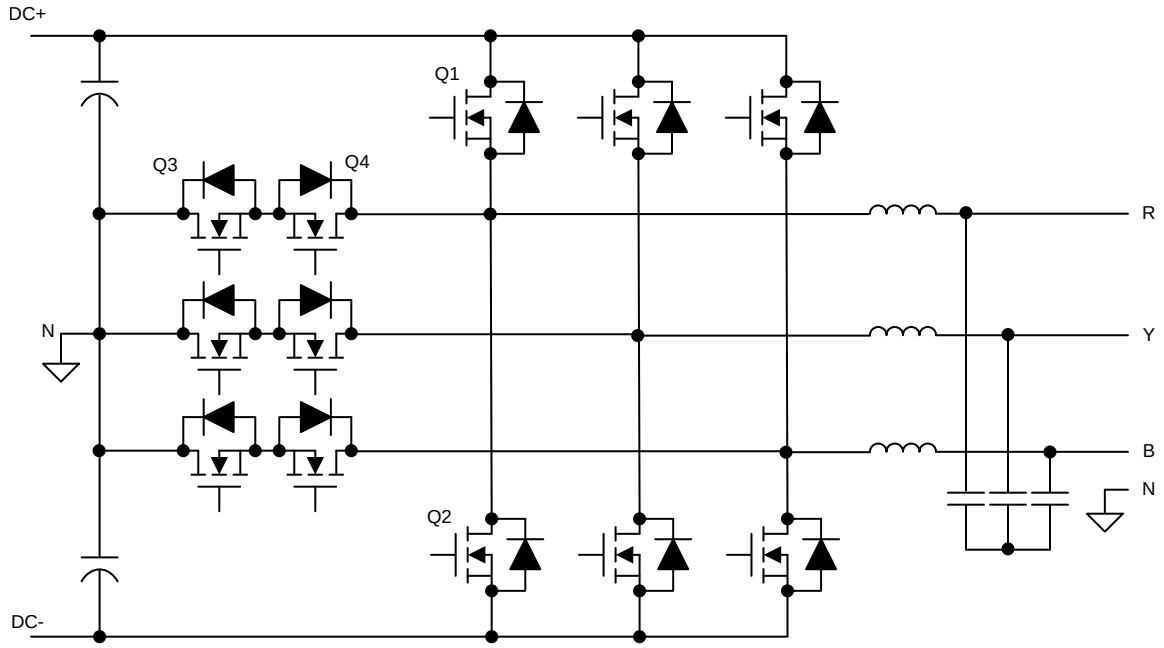


Figure 17. Three-Level T-Type, Three-Phase Inverter Architecture

To assist in understanding the benefits of the architecture, the inverter is again reduced to a single leg.

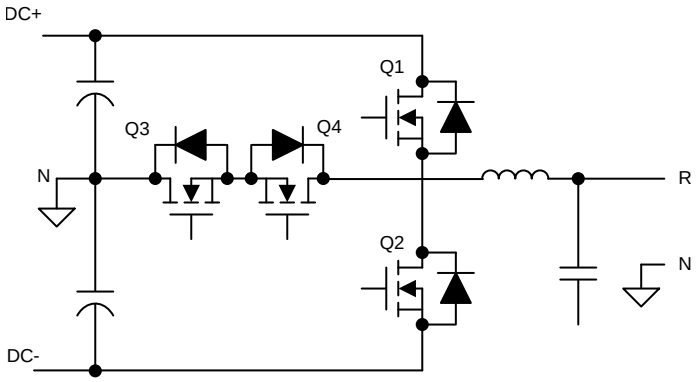


Figure 18. Three-Level T-Type, Single-Phase Inverter Leg

Adding two extra switching devices complicates the control of the system, but the same process of evaluating current flow during various modulation points illustrates the architecture benefits. Additionally, a simplified commutation scheme can be demonstrated, illustrating that control of a T-type inverter is not substantially more difficult than a traditional two-level architecture.

A single leg has three potential connection states: DC+, DC–, or N. This connection can be accomplished by closing Q1, closing Q3 and Q4, and closing Q2, respectively. However, this scheme depends on the current path in the system. Rather, for a DC+ connection, Q1 and Q3 can be closed, Q2 and Q4 for a neutral connection, and Q2 and Q4 for a DC– connection. This scheme acts independent of current direction as shown in the following figures.

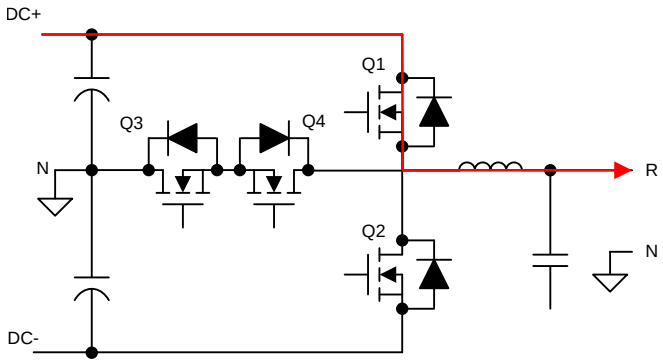


Figure 19. Q1 on, Q2 off, Q3 on, and Q4 off

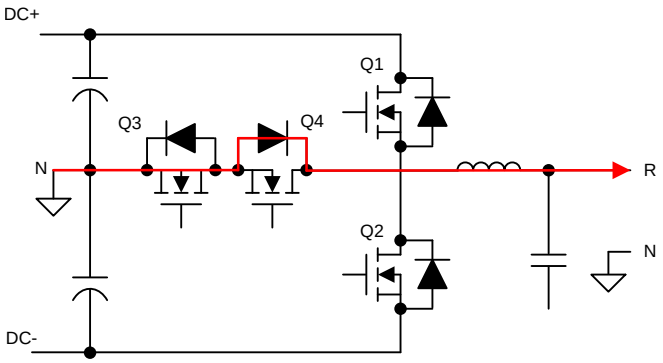


Figure 20. Q1 off, Q2 off, Q3 on, and Q4 off

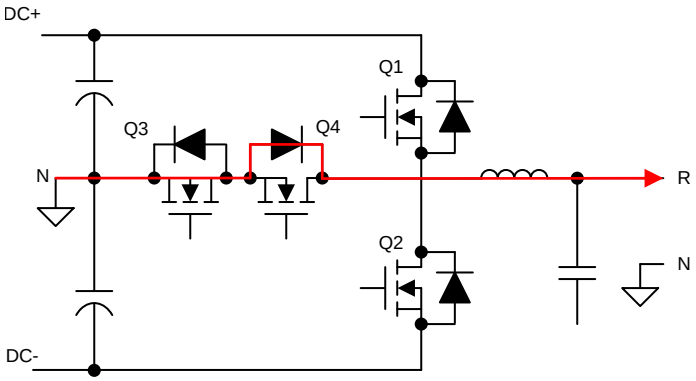


Figure 21. Q1 off, Q2 off, Q3 on, and Q4 on

This example starts with the output phase connected to DC+ by closing Q1 and Q3, resulting in current output from the system. To transition to an N connection, Q1 is opened and after a dead-time delay, and Q4 is closed. This setup allows current to naturally flow through Q3 and the diode of Q4.

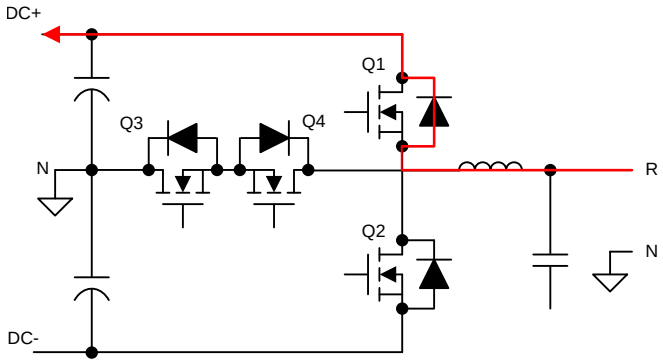


Figure 22. Q1 on, Q2 off, Q3 on, and Q4 off

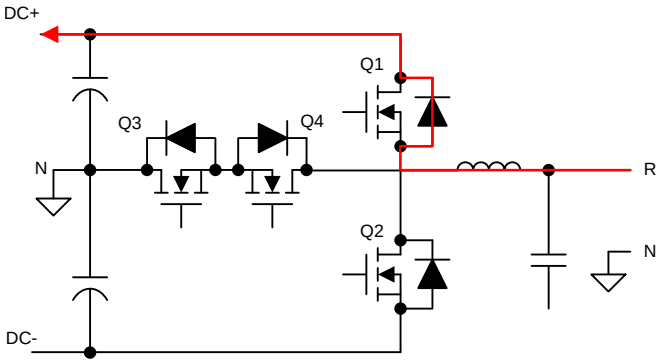


Figure 23. Q1 off, Q2 off, Q3 on, and Q4 off

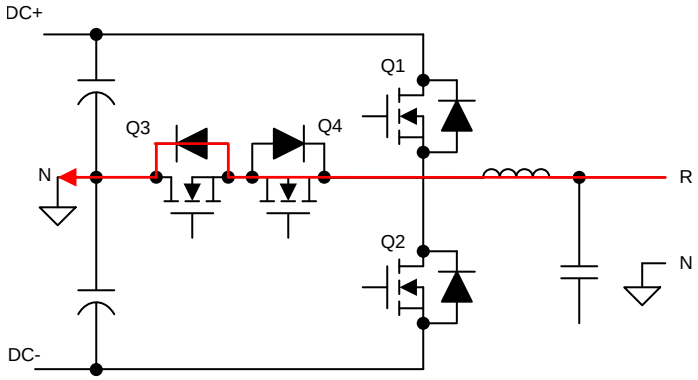


Figure 24. Q1 off, Q2 off, Q3 on, and Q4 on

For a negative current, the same sequence can be used. Once Q4 is closed, current then flows through it and the diode of Q3 rather than the diode of Q1.

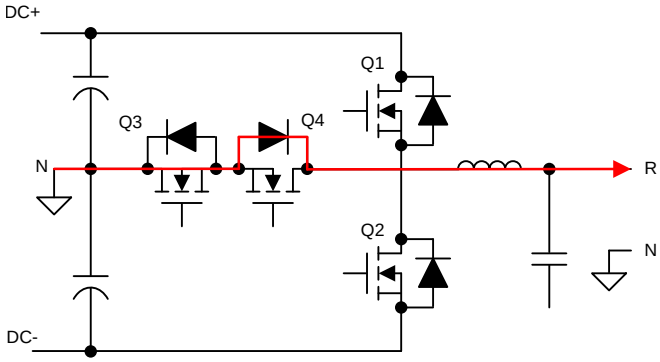


Figure 25. Q1 off, Q2 off, Q3 on, Q4 on

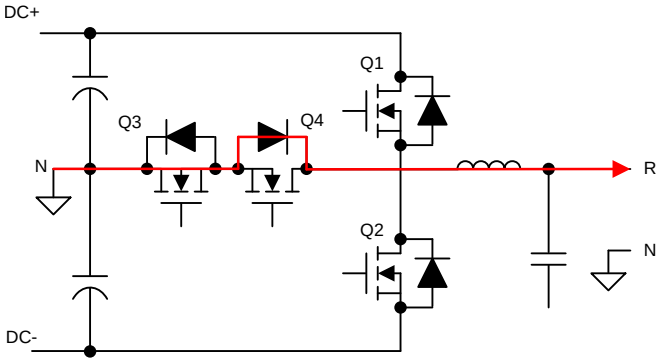


Figure 26. Q1 off, Q2 off, Q3 on, Q4 off

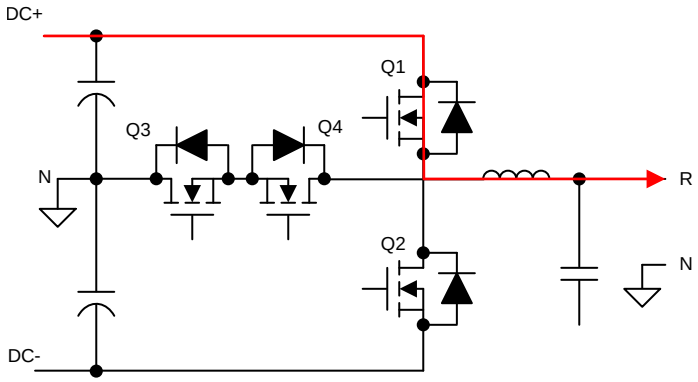


Figure 27. Q1 on, Q2 off, Q3 on, Q4 off

A similar natural current flow can be observed when connecting the output leg from N to DC+ with a positive current. Q3 and Q4 start closed with a full N connection. Q4 is switched off, but current still flows through its associated diode. Closing Q1 now naturally switches the current flow from N to DC+.

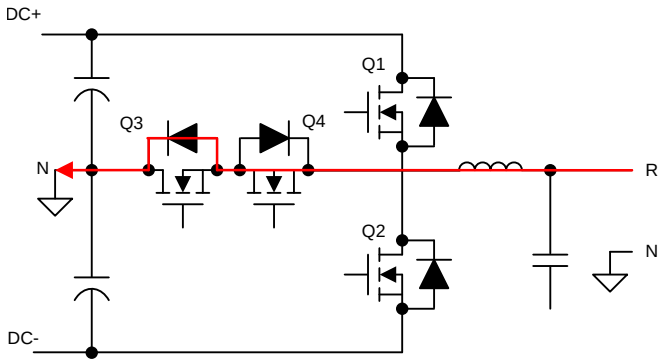


Figure 28. Q1 off, Q2 off, Q3 on, Q4 on

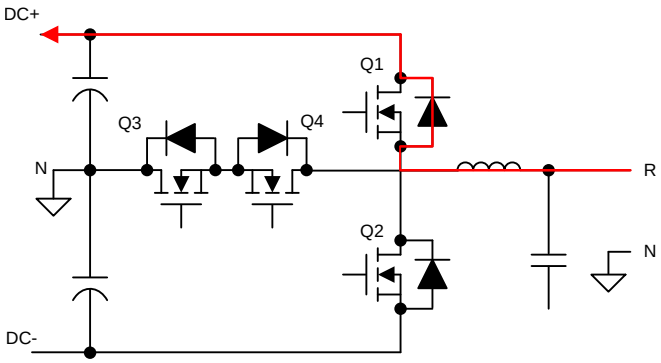


Figure 29. Q1 off, Q2 off, Q3 on, Q4 off

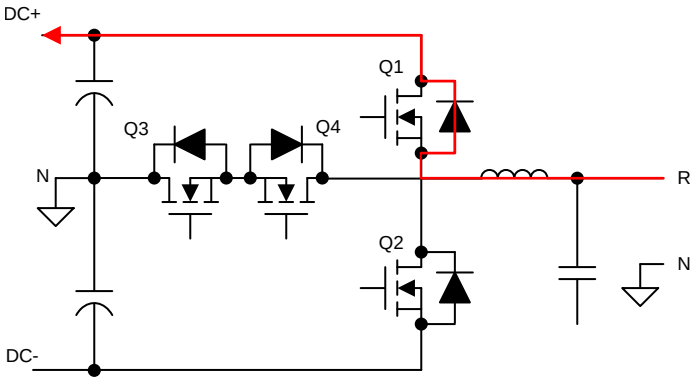


Figure 30. Q1 on, Q2 off, Q3 on, Q4 off

As in the earlier example when moving from a DC+ to N connection on a negative current, the same scheme can also be used here for a positive current. Q3 and Q4 begin closed, conducting current into N. Q4 is opened, causing current to flow through the diode of Q1. Lastly, Q1 is closed, and current remains flowing in the same direction.

All four of these transition states (DC+ to N, N to DC+, with both forward and reverse current) all share two simple switching schemes. This also holds true for transitions to and from DC– through Q2. By maintaining this scheme through all switching cycles, a simple dead-zone delay between switching events is all that is needed to avoid shoot-though; however, additional protection can be added in the control software with relative ease.

An additional benefit from this modulation scheme is that Q3 and Q4 never switch at the same time. This benefit reduces voltage stress on the devices as well as the power rating of the bias supply to drive these devices effectively. As mentioned earlier, Q3 and Q4 can share a single supply sized for one driver rather than two.

Q1 and Q2 still need to block the full DC link voltage as they would in the traditional architecture. To use a higher DC bus voltage, full-voltage FETs still need to be in place here; however, because they are back to back and do not switch at the same time, the two switches on the center leg can be at a lower rating.

2.3.1.2 LCL Filter Design

Any system of power transfer to the grid is required to meet certain output specifications for harmonic content. In voltage sourced systems like modern photo-voltaic inverters, a high-order LCL filter typically provides sufficient harmonic attenuation, along with reducing the overall design size versus a simpler filter design. However, due to the higher order nature, take some care in its design to control resonance. Figure 31 shows a typical LCL filter.

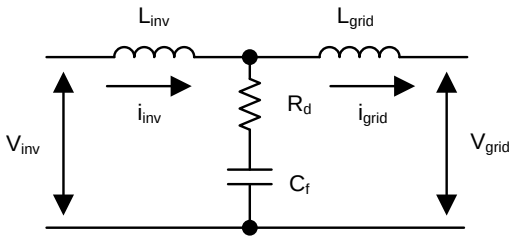


Figure 31. LCL Filter Architecture

One of the key benefits of using SiC MOSFETs (as this reference design does) is the ability to increase the switching frequency of the power stage significantly versus traditional Si-based switching elements. This increased switching frequency has a direct impact on the inverter's output filter resonant design, which needs to be accounted for. To ensure that the filter is designed correctly around this switch frequency, this known mathematical model is used in this design.

The primary component is the inverter inductor, or L_{inv}, which can be derived using Equation 1:

$$L_{inv} = \frac{V_{DC}}{8 \times f_{SW} \times I_{grid\_rated} \times \%ripple} \tag{1}$$

Using re-determined system specifications, one can easily calculate the primary inductor value:

$$L_{inv} = \frac{1000\ V}{8 \times 50\ kHz \times 18\ A \times 40\%} = 347\ \mu H \tag{2}$$

The sizing of the primary filter capacitor is handled in a similar fashion using Equation 3:

$$C_f = \frac{\%x \times Qrated}{2 \times \pi \times F_{grid} \times V_{grid}^{\ 2}} \tag{3}$$

Make some design assumptions to finalize the value of C_f, namely, limiting the total reactive power absorbed by the capacitor to 5%. Scaling the total system power by the per phase power results in a primary capacitor value of:

$$C_f = \frac{5\% \times \frac{10\ kW}{3}}{2 \times \pi \times 50\ Hz \times \left(\frac{400}{\sqrt{3}}\right)^2} = 9.947\ \mu F \tag{4}$$

For the remainder of the filter design, determine the values by defining the attenuation factor between the allowable ripple in grid inductor and the inverter inductor. This factor needs to be minimized while still maintaining a stable and cost effective total filter. By assuming an attenuation factor, an r value, which defines the ratio between the two inductors, is determined using Equation 5:

$$I_{att} = \frac{1}{\left|1 + r \times \left(1 - L_{inv} \times C_f \times \left(2 \times \pi \times f_{SW}\right)^2 \times x\right)\right|} \times 100 \tag{5}$$

To obtain an attenuation factor of 10%, and using the earlier derived values, the value of r can be evaluated by rewriting this to be:

$$r = \left| \frac{\frac{1}{10\%} - 1}{1 - 347\ \mu H \times 9.95\ \mu F \times \left(2 \times \pi \times 50\ kHz\right)^2 \times 5\%} \right| = 2.7\% \tag{6}$$

The resultant value for L_{grid} is then:

$$L_{grid} = r \times L_{inv} = 9.34\ \mu H \tag{7}$$

The filter design can be validated by determining its resonant frequency (F_{res}). A good criteria for ensuring a stable F_{res} is that it is an order of magnitude above the line frequency and less than half the switching frequency. This criteria avoids issues in the upper and lower harmonic spectrums. The resonant frequency of the filter is defined using Equation 8:

$$F_{res} = \frac{1}{\frac{\sqrt{\frac{L_{grid} \times L_{inv}}{L_{grid} + L_{inv}} \times C_f}}{2 \times \pi}} \quad (8)$$

Or, using the derived filter values:

$$F_{res} = \frac{1}{\frac{\sqrt{\frac{9.34\ \mu H \times 347\ \mu H}{9.34\ \mu H + 347\ \mu H} \times 9.95\ \mu F}}{2 \times \pi}} = 16.733\ kHz \quad (9)$$

This value for F_{res} meets the criteria listed earlier and validates the filter design.

The remaining value to determine is the passive damping that must be added to avoid oscillation. Generally, a damping resistor at the same relative order of magnitude as the C_f impedance at resonance is suitable. This impedance is easily derived using Equation 10:

$$R_d = \frac{1}{6 \times \pi \times F_{res} \times C_f} \quad (10)$$

$$R_d = \frac{1}{6 \times \pi \times 16.733\ kHz \times 9.95\ \mu H} = 0.316\ \Omega \quad (11)$$

For the final implementation in hardware, use real values for all of these components based on product availability and must be chosen to be appropriately close (±10% typically). When final values are determined, recalculate the resonant frequency to ensure the filter is still stable.

2.3.1.3 Inductor Design

With the filter being one of the major contributors to the size and weight of a solar inverter, ensure that the individual components are correctly sized. As seen in Section 2.3.1.2, the increase in the system switching speed provided by the SiC MOSFETs has already resulted in an inverter inductor that is of much smaller value than normal.

In Equation 1, the switching frequency is in the denominator. Any increase in switch frequency, all else being the same, results in an inverse relationship. Looking at the simplified equation for the inductance of a given inductor, there is a positive relationship between inductance and inductor cross sectional area by a number of turns. Both have a direct effect on the size of the component.

$$L = \frac{0.4 \times \pi \times \mu \times N^2 \times A \times 10^{-2}}{\ell} \quad (12)$$

where

- μ is core permeability
- N is the number of turns
- A is the cross sectional area
- l is the mean magnetic path length

The starting point for evaluating a solution to the variables in Equation 12 is to determine a valid core material and subsequent permeability. The core manufacturer typically has a range of suitable materials with selection criteria based on the design inductance and the inductor current. For this design, the nominal inductor current (with an overload factor of 105%) is defined as:

$$I_{ind\_nom} = \frac{KVA_{out} \times 105\%}{\sqrt{3}\ V_{grid}} \quad (13)$$

$$I_{ind\_nom} = \frac{10\ kVA \times 105\%}{\sqrt{3} \times 400} = 15.155\ A \quad (14)$$

Using a selection guide for a toroidal inductor core manufacturer, at 347 µH, the core permeability comes to 26 µH. The core also provides a value for the inductance factor, A_L, which enables a quick path to selecting the number of turns.

$$N = \sqrt{\frac{L \times 10^3}{A_L}} \quad (15)$$

$$N = \sqrt{\frac{347\ \mu H \times 10^3}{49}} = 84 \quad (16)$$

One last piece of information required for the inductor design is the winding wire size. This size is easily computed using the nominal inductor current rating. Using copper, with a current carrying density of 4 A/mm, this inductor requires a cross sectional area of:

$$A_w = \frac{I_{ind\_nom}}{4} = \frac{15.155}{4} = 3.789\ mm^2 \quad (17)$$

This area is an equivalent to American Wire Gauge #12, which has a cross sectional area of 3.309 mm^2. This slight derating is acceptable because the switching current allows a smaller gauge to be used when compared to a static DC bias current. For this inductor, flat winding is used to increase surface area for cooling and decrease potential skin depth effects.

Using the overall design of the core, with the flat 12 AWG winding, the total length of each winding is determined to be 64.87 mm. At this point, the DC resistance of the inductor can be calculated using Pouillet's Law:

$$R_{DC} = \rho \frac{\ell}{A} \quad (18)$$

$$R_{DC} = \left(17 \times 10^{-9}\right) \frac{84 \times 64.87\ mm \times 10^{-3}}{3.309\ mm^2 \times 10^{-6}} = 0.028\ \Omega \quad (19)$$

To determine the AC resistance, first calculate the skin depth at the inverter switching frequency:

$$S_d = 1000 \times \sqrt{\frac{\rho}{\pi \times f_{SW} \times \mu_o}} \quad (20)$$

$$S_d = 1000 \times \sqrt{\frac{17 \times 10^{-9}}{\pi \times 50\ kHz \times 4 \times \pi \times 10^{-7}}} = 0.293\ mm \quad (21)$$

R_{AC} is then determined by R_{DC}, S_d, and S_s, which is the equivalent square conductor width.

$$R_{AC} = R_{DC} \times \frac{1}{2} \times \left(\frac{S_s}{S_d}\right) \times \left(\frac{\sinh\left(\frac{S_s}{S_d}\right) + \sin\left(\frac{S_s}{S_d}\right)}{\cosh\left(\frac{S_s}{S_d}\right) - \cos\left(\frac{S_s}{S_d}\right)}\right) = 0.087\ \Omega \quad (22)$$

This determination of R_{AC} helps determine total system losses.

2.3.1.4 SiC MOSFET and IGBT Selection

As shown in the architecture overview, the main switching device needs to support the full switching voltage. To support the 1000-V DC link voltage of this design, use 1200-V FETs; however, at this voltage, the migration to SiC is necessitated by several factors:

- The switching speed of a 1200-V SiC MOSFET is significantly faster than a traditional IGBT, leading to a reduction in switching losses.
- The reverse recovery charge is significantly smaller in the SiC MOSFET, resulting in reduced voltage and current overshoot.
- A lower temperature dependence at due to reduced conduction loss increase at full load.

The middle switches are only exposed to half of the DC link voltage, or 500 V in this design. As such, a 650-V device is suitable. A full SiC solution provides the best performance due to these same features; however, the cost would be higher. To reduce overall system cost, traditional Si switching devices can be used. A few factors dictate the choice of device:

- Si MOSFETs have a resistive feature that helps to reduce conduction loss at light load conditions compared with IGBT, but the high reverse recovery of the body diode increases voltage and current overshoot. Because SiC MOSFETs switch much faster than Si devices, the reverse recovery is much more severe.

- Si IGBTs have higher conduction loss at light load, but the reverse recovery can be lower if a fast recovery diode is used as the antiparallel diode. Moreover, because an IGBT is a unidirectional device, the current always conducts through one anti-parallel diode in T-type topology. The light load efficiency will be reduced.

For this design, the reverse recovery loss and voltage overshoot limits the device selection. As such, a 1200-V SiC MOSFET + 650-V IGBT solution is used.

Conduction loss is mainly determined by the R_{DS_on} of the 1200-V SiC MOSFET and the on voltage drop of the 650-V IGBT. The 80-mΩ SiC devices have a good high-temperature performance, and the R_{DS_on} only increases 30% at 150°C junction temperature. With the high temperature I-V curve in the data sheet, calculate the conduction loss on the devices.

Switching loss is a function of the switching frequency and switching energy of each switching transient, the switching energy is related with device current and voltage at the switching transient. Using the switching energy curve in the data sheet, one can estimate the total switching loss. Note that the switching energy curve in the data sheet is measured with SiC diode freewheeling, but in a T-type converter, the freewheeling device is the Si diode in IGBT. The switching loss is expected to be higher than calculated result.

Similarly, the conduction loss and switching loss can be estimated for all the devices and efficiency can be estimated. With the thermal impedance information of the thermal system design, the proper device rating can be selected. The 1200-V/80-mΩ SiC MOSFET and 650-V/30-A IGBT is a good tradeoff among thermal, efficiency and cost.

2.3.1.5 Loss Estimations

The primary source of lost efficiency in any inverter is going to be a result of the losses incurred in the switching devices. These losses are broken into three categories for each device:

- Conduction loss: When the device is on and conducting normally
- Switching loss: When the device is switching between states
- Diode conduction loss: Related to voltage drop and current when in conduction

Each of these are dictated by their own equation, and can be determined from the device data sheet and design parameters that have already been set.

Conduction loss is driven by the on-time of the FET, the switched current, and the on-resistance:

$$P_{cond\_loss} = \frac{1}{T}\int_0^T V_{ce}(t) \times I_c(t) \times D_Q(t)dt$$

where

- V_{ce} is the conduction voltage drop
- I_c is the conduction current
- D_Q is the duty cycle
- T represents one modulation cycle (23)

Switching loss is determined by the switching energy of the device and the switching voltage at a selected test point. Determine the value of the switching energy from the device data sheet using the value of the designed external gate resistor. The remainder of the values needed were determined earlier in the design phase.

$$P_{sw\_loss} = \frac{(E_{on} + E_{off}) \times I_{peak} \times f_{SW} \times V_{DC}}{\pi \times I_{avg} \times V_{nom}} \quad (24)$$

Figure 32 shows an example of the graph used to extract the switching energy values from the device data sheet is shown for an LSIC1MO120E0080 SiC MOSFET. Note that at this time the switching energies of this SiC MOSFET are an order of magnitude lower than those of the IGBTs used in the system. Even at this stage, it is easy to see how the higher electron mobility in SiC results in reduced switch loss.

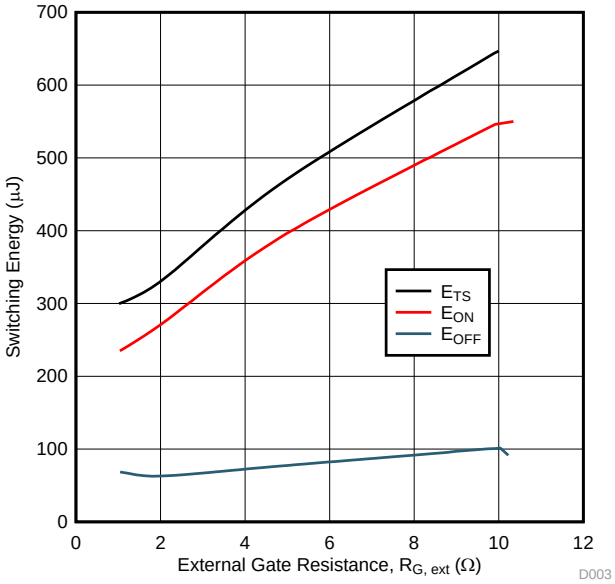


Figure 32. Switching Energy vs Gate Resistance for LSIC1MO120E0080

The diode conduction loss is similarly calculated using known values:

$$P_{sw\_diode} = \frac{1}{T}\int_0^T Vf(t) \times If(t) \times D_D(t)dt$$

where

- V_f is the voltage drop
- I_f is the diode current
- D_D is the duty cycle
- T represents one modulation cycle (25)

Using these three equations, the expected losses of the design are computed for both the SiC MOSFETs and IGBTs as shown in Table 2.

Table 2. Expected Losses of Switching Devices

PARAMETER	LSIC1MO120E0080 (Q1)	IKW20N60TFKSA1 (Q3)
Conduction loss	4.095 W	2.08 W
Switching loss	1.536 W	2.789 W
Diode loss	0 W	2.697 W
Total	5.631 W	7.566 W

The final piece of the total system loss estimation is the inductor losses. These losses are determined using the value of the inductor DC and AC resistance and expected inductor current from Section 2.3.1.3.

$$Pind\_loss = I_{ind\_ac\_rms}^2 \times R_{DC} + I_{ind\_ripple\_rms}^2 \times R_{AC} \quad (26)$$

$$P_{ind\_loss} = (0.81\,A)^2 \times 0.024\,\Omega + (15.155)^2 \times 0.076\,\Omega = 5.64\,W \quad (27)$$

The total major energy loss for this design is then:

$$P_{loss\_total} = 6 \times \left(P_{Q1\_total} + P_{Q3\_total}\right) + 3 \times P_{int\_loss} \quad (28)$$

$$P_{loss\_total} = 6 \times (5.631\,W + 7.56\,W) + 3 \times 5.64\,W = 96.102\,W \quad (29)$$

Equation 29 can then be used to determine the total expected inverter efficiency. Note that this is an estimation, but it will allow the design to be validated up to this point.

$$\eta = \frac{P_{out}}{P_{out} + P_{loss\_total}} \times 100 \quad (30)$$

$$\eta = \frac{10\ kW}{10\ kW + 96.102\ W} = 99.048\% \quad (31)$$

2.3.1.6 Thermal Considerations

The loss estimations can also allow the heat output of the design to be characterized. Any electrical loss in the system is converted to waste heat.

Thermal simulations where performed using the physical layout of the design, as well as the expected energy losses. An off the shelf heat sink from Wakefield-Vette (OMNI-UNI-18-50) was selected to simplify the design process and provide a starting reference point for understanding the thermal performance. This data should be used as a starting point for a thermal solution, and not a fully validated solution.

The system was simulated using a worse than calculated thermal output of 10 W per switching device. This meant 120 W of total power dissipation across all three phases. Figure 33 and Figure 34 show the thermal simulation results with no fans.

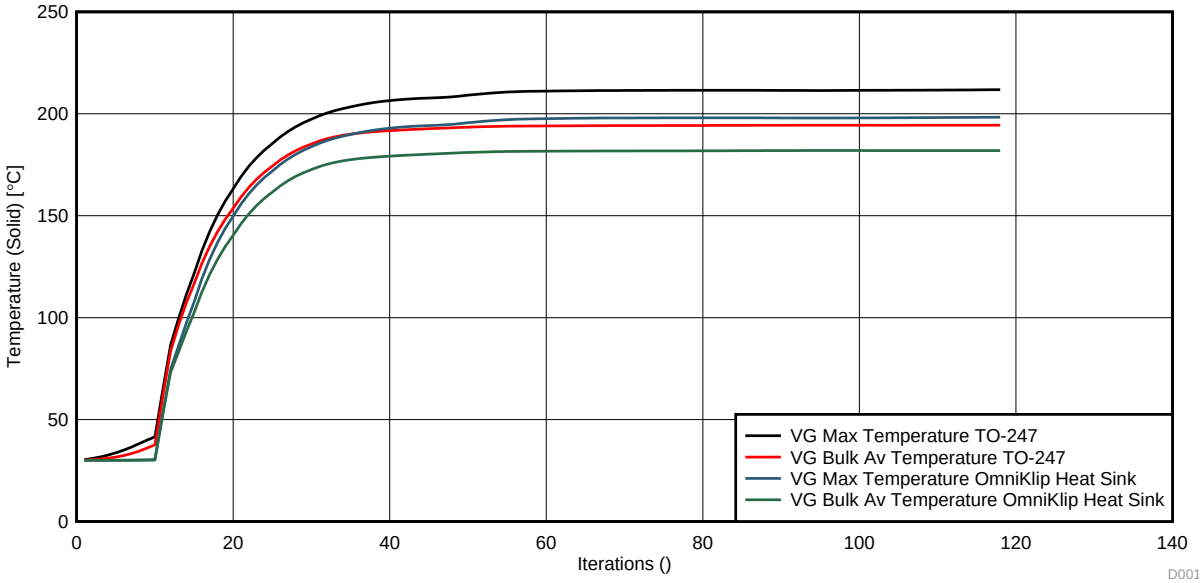


Figure 33. Simulated Temperature vs Time

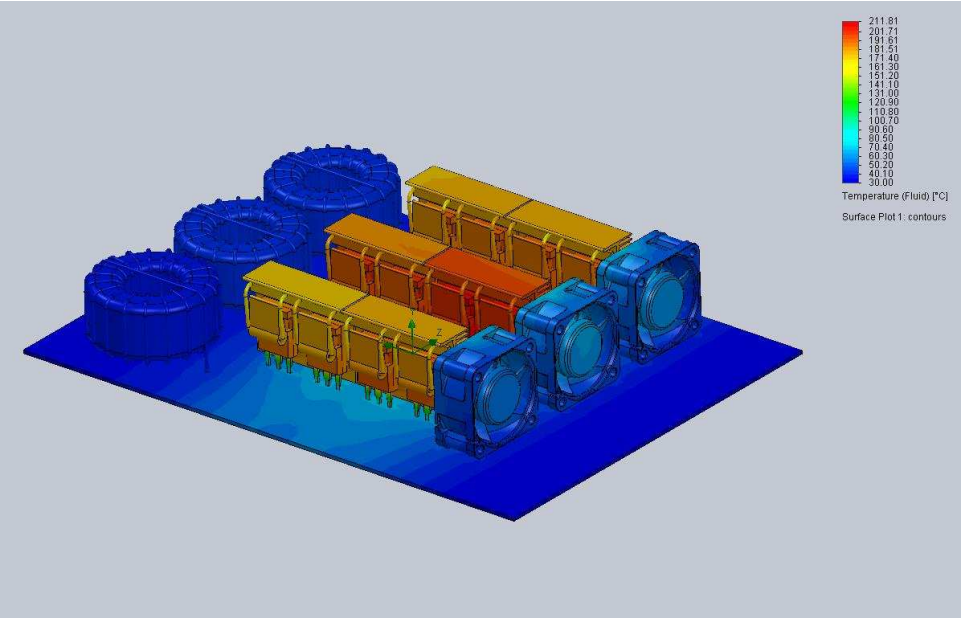


Figure 34. Passive Thermal Simulation Result

In this simulation, with only natural convection and small off the shelf heat sinks, the TO-247 package of the IGBTs reaches a maximum temperature of 215°C, and the SiC MOSFET reaches 197°C. These temperatures are both outside the maximum allowed temperature range of the devices.

Figure 35 shows the next simulation, which includes active airflow and full ducting of the heat generating devices. This airflow reduces the maximum temperature of the MOSFET under a 130% load to be 130°C. This temperature is within the design constraint of the 175°C junction temperature of the IKW20N60TFKSA1, which is the major heat generator.

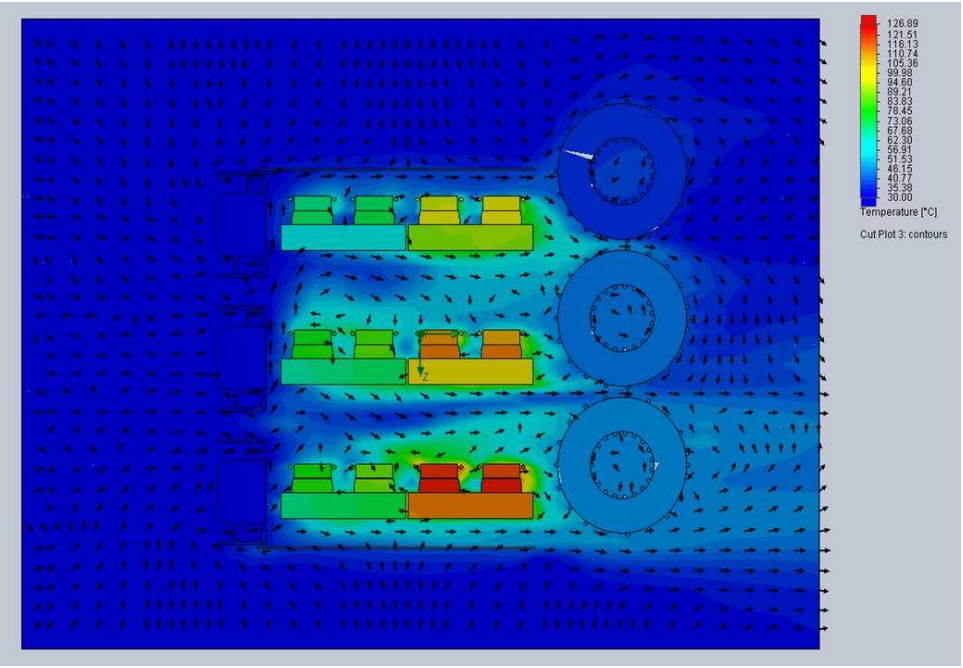


Figure 35. Active Ducted Thermal Simulation

2.3.2 Voltage Sensing

Voltage sensing happens at two points in the inverter signal path to aid in control: before and after the primary output relay. By enabling measurement on both sides of the relay, the control system can lock into the grid voltage and frequency before connecting, thus preventing any mismatch issues.

Both sensing topologies are similar. First, PGND is used as a virtual neutral using a resistor network. On the grid side of the relay, only neutral is used. The high voltage signal is attenuated using a series of large value resistances. An offset of 1.65 V is added to the attenuated neutral point to center the voltage signal in the middle of the input range of the OPA4350, and the attenuated value from the phase voltage is measured. Figure 36 shows this sensing arrangement.

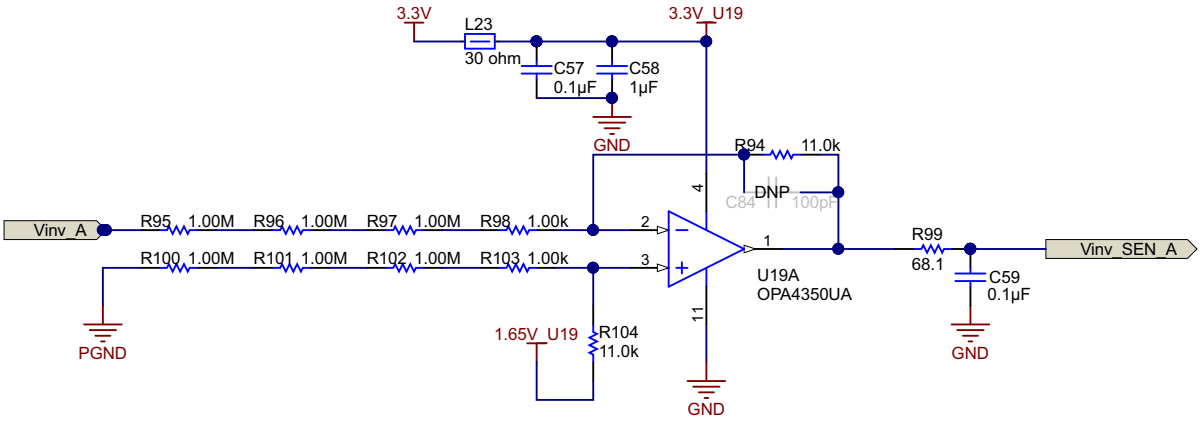


Figure 36. High-Voltage Sensing Signal Path

2.3.3 Current Sensing

Critical to getting a closed loop control system is accurate current measurement of the inverter. In this design, current measurement is done at two locations with different sensing technologies. The first location is on the grid output using shunt resistors. Because the output is high voltage and the controller needs to remain isolated, the AMC1306M05 reinforced modulator is used to measure the resistor voltage drop. To keep system losses low, the AMC1306M05 has a ±50-mV input range. When compared to other devices with a typical input range of ±250 mV, the total power loss across the shunt is significantly reduced.

Sizing the shunt resistor for this design is a trade-off between sensing accuracy and power dissipation. A 0.001-Ω shunt provides a ±20-mV output signal at the inverter's approximate ±20-A output but also only generates 0.4 W of heat at full load. When choosing an actual device, select a high accuracy value to eliminate the need to calibrate each sensor path.

The voltage across the shunt resistor is fed into the AMC1306M05 sigma-delta modulator, which generates the sigma-delta stream that is decoded by the SDFM demodulator present on the C2000™ MCU. The clock for the modulator is generated from the ECAP peripheral on the C2000 MCU, and the AMC1306M05 data is decided using the built-in SDFM modulator.

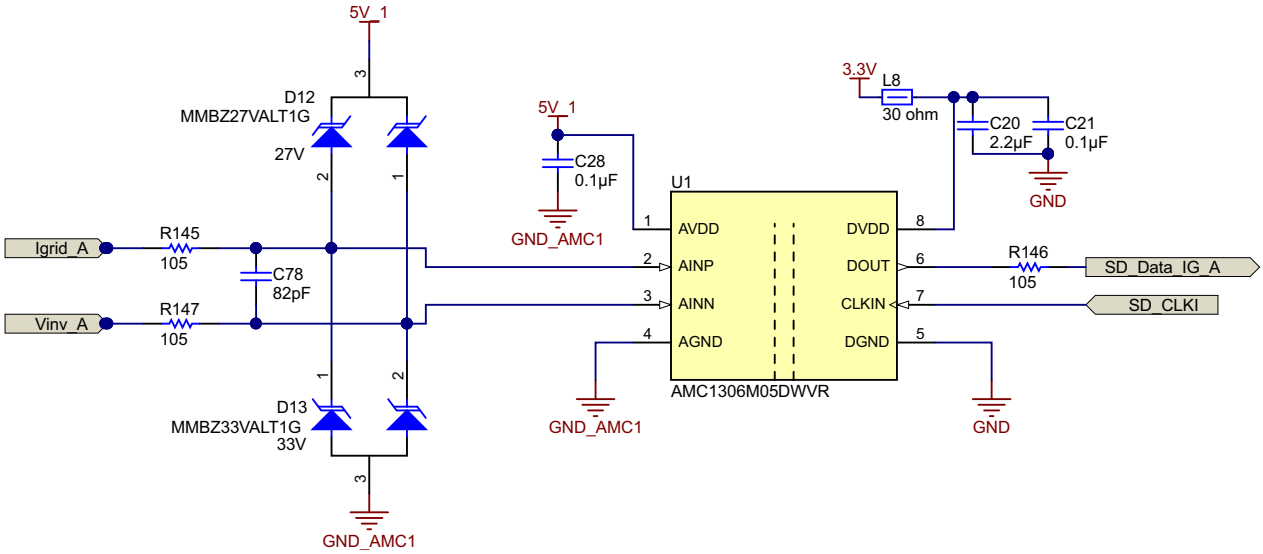


Figure 37. Isolated Shunt Sensing With AMC1305M05

The second location is a Hall effect sensor, which is used to sense the current through the inductor. The Hall effect sensor has a built-in offset, and the range is different than what ADC can measure. Therefore, the voltage is scaled to match the ADC range using the circuit shown in Figure 39 and Equation 32. Of note here, the OPA4340 is used over the OPA4350 in the voltage sense path due to the former's lower bandwidth. The low bandwidth helps to reduce accidental amplification of switching noise that might be picked up by long traces in the PCB.

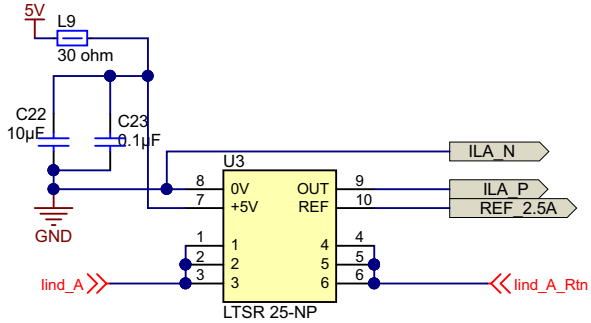


Figure 38. Isolated Hall Effect Current Sensing

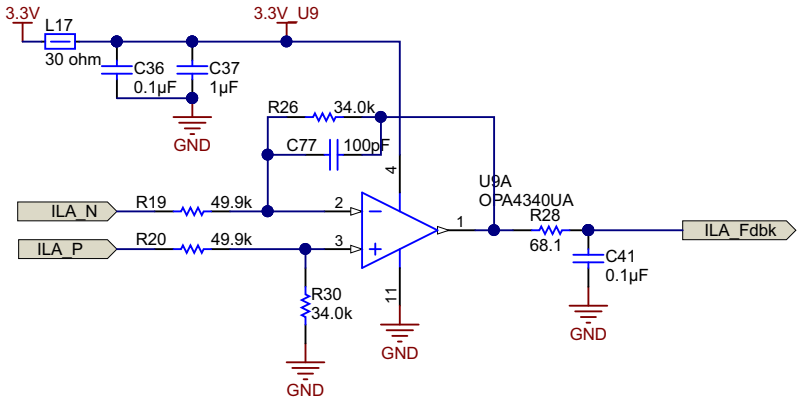


Figure 39. Hall Effect Sensor Matching

$$V_{out} = \frac{R_f}{R_e}\left(\frac{V_{nominal}}{I_{max}} + V_{offset}\right) \quad (32)$$

2.3.4 System Power Supplies

This reference design uses multiple voltage domains across the system:

- A primary high-voltage input to power the entire board (up to 60 V)
- 12 V to power the gate drive cards, further described in Section 2.3.5
- 5 V to power the control card and drive isolated supplies
- Non-isolated 3.3 V for analog sensing
- Isolated 3.3 V for current shunt sensing

Figure 40 shows the full tree for all of these domains.

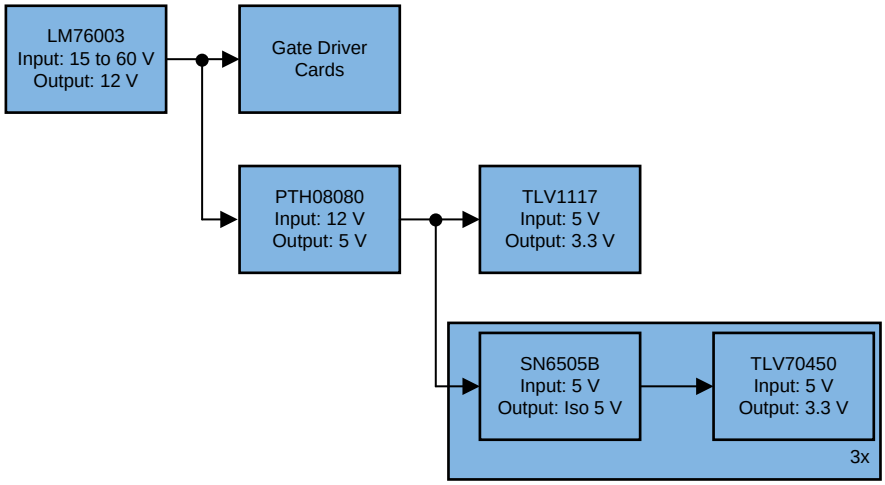


Figure 40. Power Tree

2.3.4.1 Main Input Power Conditioning

The primary voltage input for the design is rated for 15 V to 60 V. This wide V_{IN} enables the inverter to be powered from a variety of industrial voltage sources that might be used in a larger system. The range is enabled by the LM76003 synchronous step-down converter.

The converter is configured for a 12-V output using the R54 and R57 feedback resistor divider. This 12-V rail is then used to power the relays, fans, isolated gate drive bias supplies, and the remainder of the step-down converters in the system. The 3.5-A output support of the LM76003 is sufficient for this operation. The design also includes dual parallel output capacitors to reduce ESR and subsequent ripple and load transients and loads switch on an off.

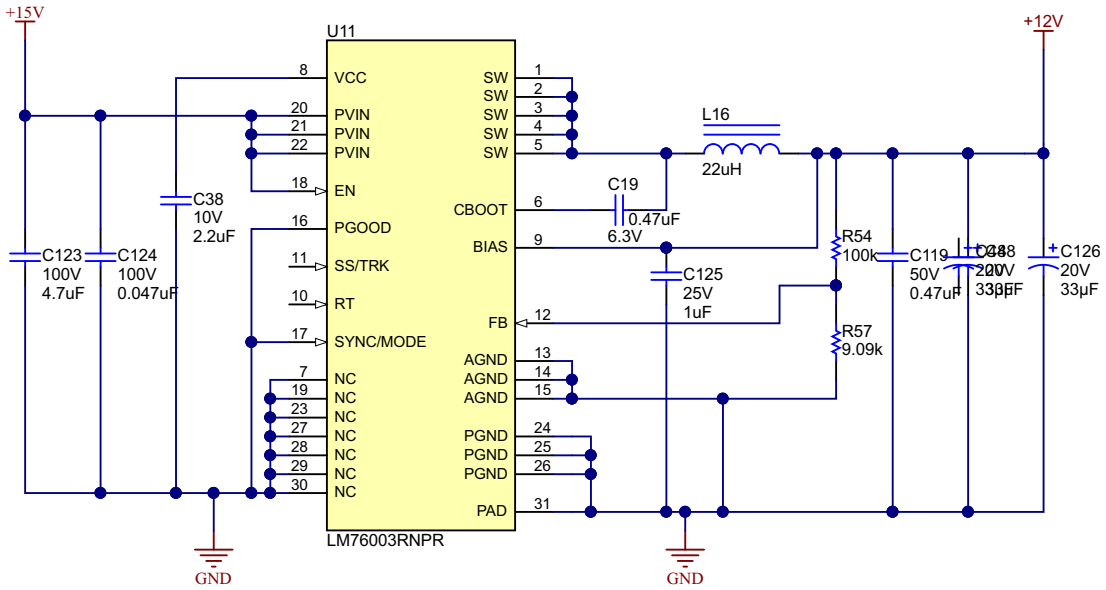


Figure 41. LM76003 12-V DC/DC Converter

2.3.4.2 Isolated Bias Supplies

To generate the isolated bias supplies for the AMC1306M05 isolated modulators, the SN6505B transformer driver is used to drive a Würth 750313638 transformer in a push-pull configuration. This is a recommended configuration from the SN6505B data sheet to build a 5-V → 6-V isolated supply.

The 6-V output is used to feed a TLV70450 LDO to generate a clean 5-V rail for the analog and digital circuitry of the AMC1306M05.

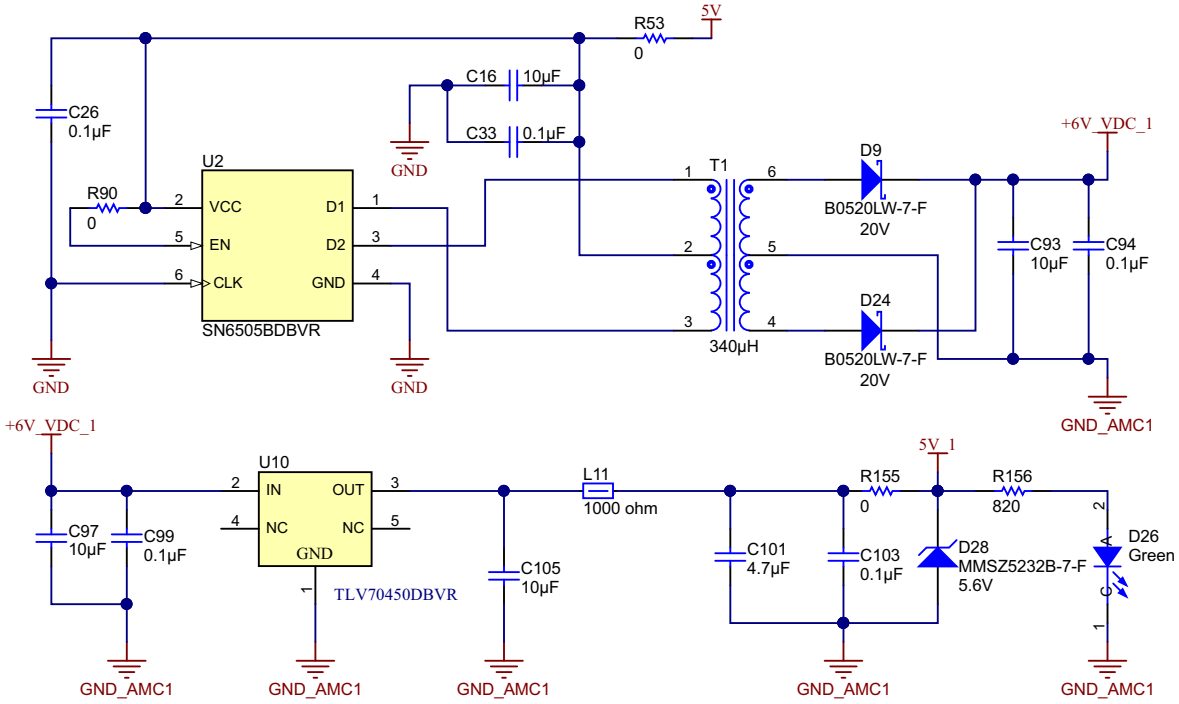


Figure 42. SN6505 Bias Voltage Supply

2.3.5 Gate Drivers

2.3.5.1 SiC MOSFETs

Figure 43 shows the schematic design of the isolated SiC MOSFET gate driver. VCC1 and GND1 are the supply pins for the input side of the ISO5852S device. The supply voltage at VCC1 can range from 3.0 V to 5.5 V with respect to GND1. VCC2 and GND2 are the supply pins for the output side of the ISO5852S device. VEE2 is the supply return for the output driver and GND2 is the reference for the logic circuitry. The supply voltage at VCC2 can range from 15 V up to 30 V with respect to VEE2. The PWM is applied across the IN+ and IN– pins of the gate driver.

On the secondary-side of the gate driver, gate resistors R29 and R30 control the gate current of the switching device. The DESAT fault detection prevents any destruction resulting from excessive collector currents during a short-circuit fault. To prevent damage to the switching device, the ISO5852S slowly turns off the SiC MOSFET in the event of a fault detection. A slow turnoff ensures the overcurrent is reduced in a controlled manner during the fault condition. The DESAT diode D9 conducts the bias current from the gate driver, which allows sensing of the MOSFET-saturated collector-to-emitter voltage when the SiC MOSFET is in the ON condition.

For more detailed design procedures for the ISO5852S, see *Isolated IGBT Gate Driver Evaluation Platform for 3-Phase Inverter System*

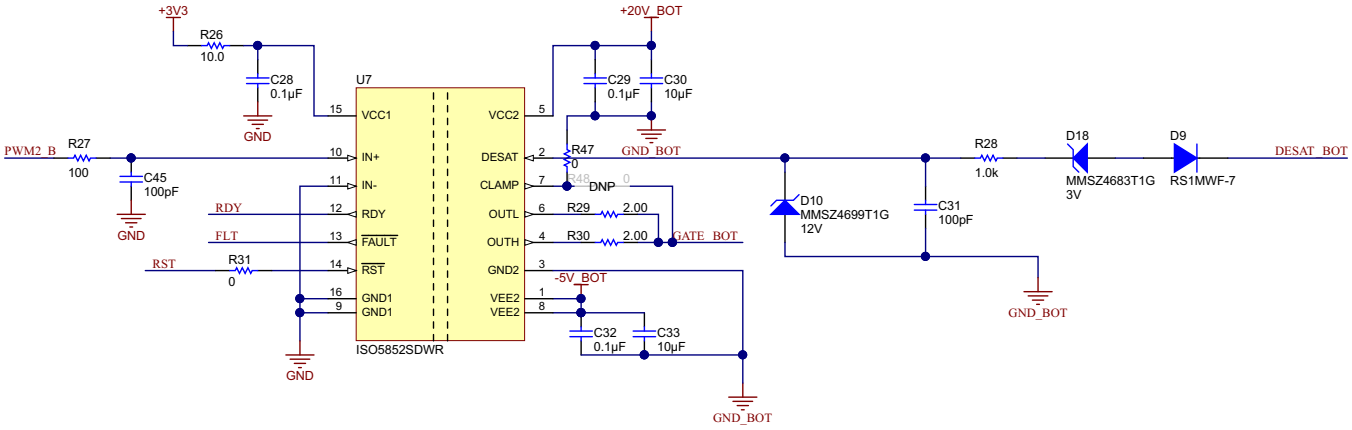


Figure 43. ISO5852S Gate Drive Circuit

2.3.5.2 IGBTs

Figure 44 shows the schematic design of the isolated IGBT gate driver. The UCC5320S primary side is powered by a 3.3-V rail. A 0.1-µF ceramic capacitor is placed close to the VCC1 pin for noise decoupling. The positive going UVLO threshold on the supply is 2.6 V and the negative going threshold is 2.5 V.

The PWM input to the gate driver is provided by the controller PWM output peripheral. Dead time must be inserted between the low-side and high-side PWM signals to prevent both switches turning on at the same time. The signal is single ended and is filtered by RC low-pass filter comprising of R35 and C46 before connecting to the gate driver input. The filter attenuates high-frequency noise and prevents overshoot and undershoot on the PWM inputs due to longer tracks from the controller to the gate driver. The inverting PWM input IN– is not used in the design and is connected to primary side ground.

The UCC5320S has split outputs that allows for controlling the turnon rise time and turnoff fall time of the IGBT individually. A 3.3-Ω gate resistor R36 is used for IGBT turnon. A 3.3-Ω IGBT turnoff resistor R12 allows for strong turnoff, helping reduce turnoff losses. The low value of the turnoff resistor also increases the immunity of the gate drive circuit to Miller induced parasitic turnon effects. A 10-kΩ resistor is connected across the IGBT gate to emitter pins close to the IGBT on the main power board. This connection ensures that the IGBT remains in the off state in case the gate driver gets disconnected from the IGBT due to faults.

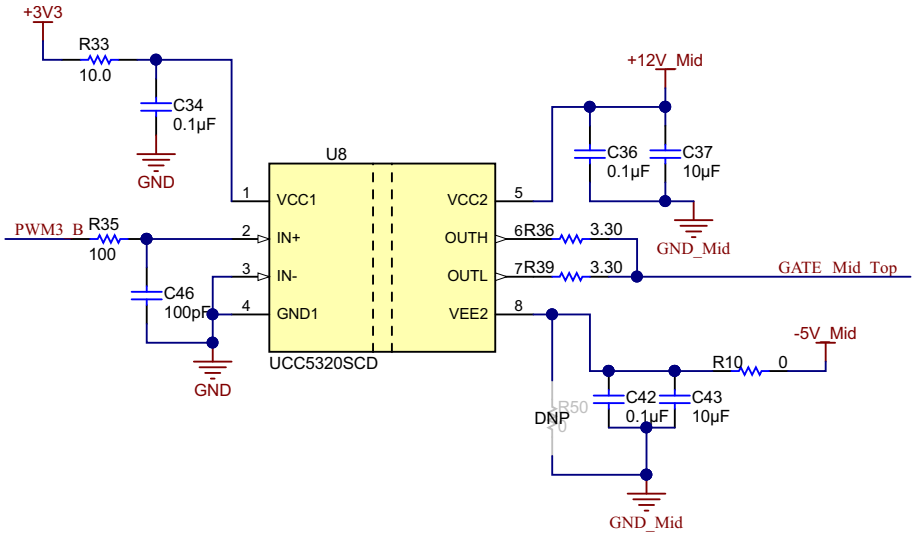


Figure 44. UCC5320 Gate Drive Circuit

2.3.5.3 Gate Driver Bias Supply

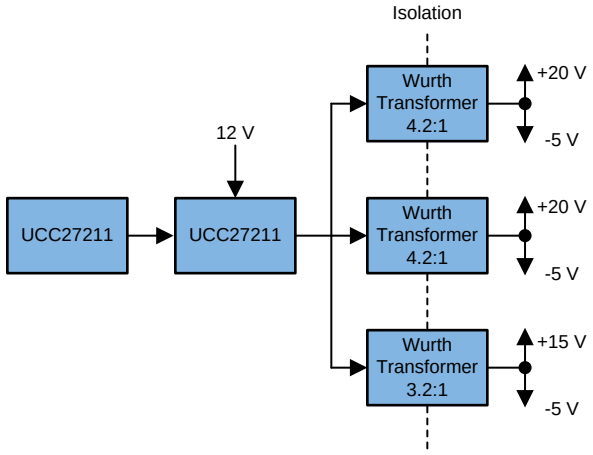


Figure 45. Gate Driver Bias Supply Architecture

Section 2.3.5.1 and Section 2.3.5.2 show that the gate drivers rely on isolated bias voltages to drive the gates across the high-voltage barrier. In this architecture, there are four drivers per phase, but only three isolated domains are needed as described in Section 2.3.1.1. These domains are:

1. +20 V and –5 V for high SiC MOSFET switch
2. +20 V and –5 V for low SiC MOSFET switch
3. +15 V and –5 V for both IGBTs in the neutral leg

The same architecture used in Section 2.3.4.2 could generate the domains individually. However, with the close proximity of all of the gates on the daughter cards, it makes more sense to use a central controller and distributed isolation transformers.

The UCC27211 uses a dual PWM input from the control card to drive a half bridge comprised of two CDS88537ND MOSFETs. These two FETs are capable of driving the 12-V source from the main power supply to the low side of all three isolation transformers. The transformers have been designed to operate with an open loop control signal of 500 kHz and have appropriate turn ratios to generate the required voltage rails for each gate driver. This architecture decreases system complexity, cost, and size.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

The DUT in this design is set up and operated in several pieces:

- One TIDA-01606 power board
- Three TIDA-01606 gate driver card
- TMS320F28379D Control Card
- Mini USB cable
- Laptop or other computer

The test equipment required to power and evaluate the design is as follows:

- 15-V/4-A bench style supply for primary board power
- >1000-V/10-A power supply for DC link input
- >10-kVA resistive load
- Four-channel, power quality analyzer

3.1.2 Software

- Code Composer Studio™ 7.x with TI C2000 powerSUITE

3.2 Testing and Results

3.2.1 Test Setup

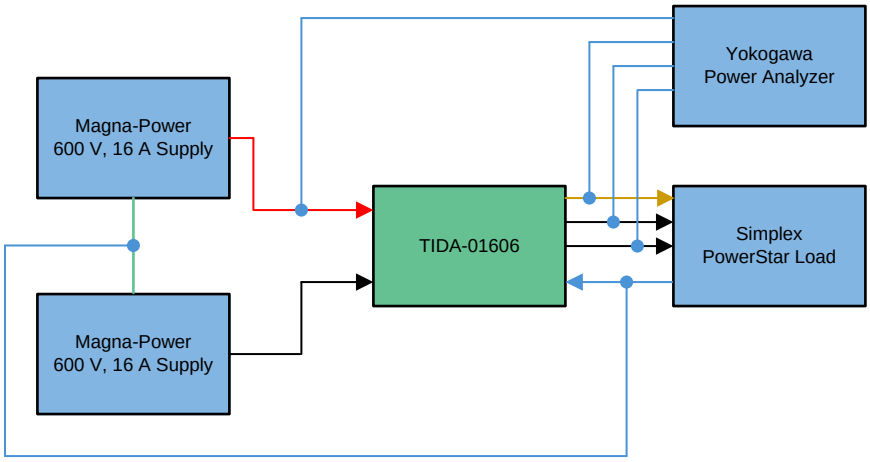


Figure 46. Test Setup for Efficiency

To test the efficiency of this reference design, use the following equipment:

- Two Magna-Power 600-V, 16-A power supplies placed in series to generate the 1000-V input maximum. The midpoint voltage of the supply configuration is used to stabilize the neutral leg in lieu of a true grid neutral in open loop testing.
- A 110-kW Simplex PowerStart load bank is used as a configurable load to test the design at various set points.
- A Yokogawa PX8000 Precision Power Scope is connected to the DUT input and output to perform efficiency measurements.
- An external BK precision bench power supply is used to provide a 15-V input to power the DUT.

The system is configured to operate in an open loop control mode, generating a static 400-V, 60-Hz output. The power demand is then modulated by the Simplex load bank to test the system at multiple load points.

Table 3 lists the system efficiency results from the power scope. The results demonstrate an inverter with a maximum efficiency of 99.08%.

The final design dimensions are outlined in Table 4 and show a total volume of 7 L. With a power rating of 10 kW, this results in a power density of 1.44 kW/L.

3.2.2 Test Results

Table 3. System Efficiency Results

POWER RATING	10%	20%	30%	40%	50%	60%	70%	80%	90%	100%
600-V input	95.6%	97.43%	97.74%	97.82%	97.79%	97.79%	97.79%	97.79%		
800-V input	92.64%	96.55%	97.87%	98.31%	98.42%	98.47%	98.51%	98.54%	98.7%	98.22%
1000-V input	92.37%	96.55%	97.95%	98.52%	98.77%	98.95%	99.01%	99.06%	99.08%	99.02%

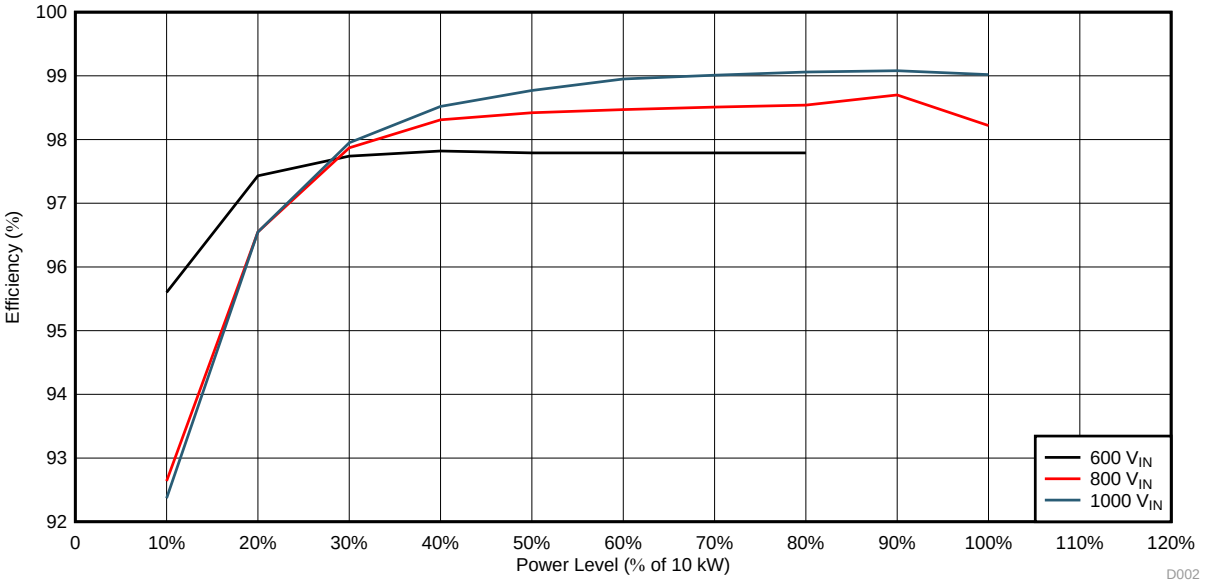


Figure 47. Inverter Efficiency

Table 4. System Dimensions

AXIS	DIMENSION
X	350 mm
Y	200 mm
Z	100 mm
Volume	7 liters

The total energy density of the design is 10 kW/7L, or 1.43 kW/L.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01606.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01606.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01606.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-01606.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01606.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01606.

5 Trademarks

6 About the Authors

BART BASILE is a systems architect in the Grid Infrastructure Solutions Team at Texas Instruments, where he focuses on renewable energy and EV infrastructure. Bart works across multiple product families and technologies to leverage the best solutions possible for system level application design. Bart received his bachelors of science in electronic engineering from Texas A&M University.

MURALI KRISHNA PACHIPULUSU is a systems engineer at Texas Instruments, where he is responsible for developing reference design solutions for the industrial segment. Murali brings to this role his experience in analog and digital power electronics converters design to this role. Murali earned his master of technology (M.Tech) from the Indian Institute of Technology in Delhi.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (March 2018) to A Revision	Page
• Updated block diagram Figure 1. *TIDA-01606 Block Diagram*: "F28004x Control Card" to "F28377D Control Card"	2

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