All Lecture Slides After Mid

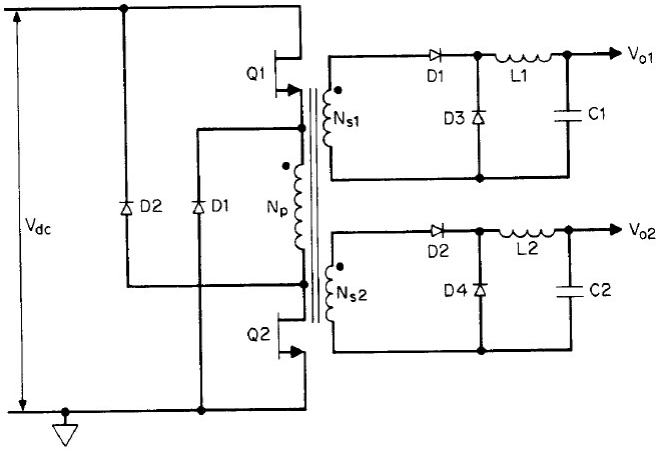
Switch Mode Power Supplies
Spring-2019

Double-Ended Forward Converter Topology

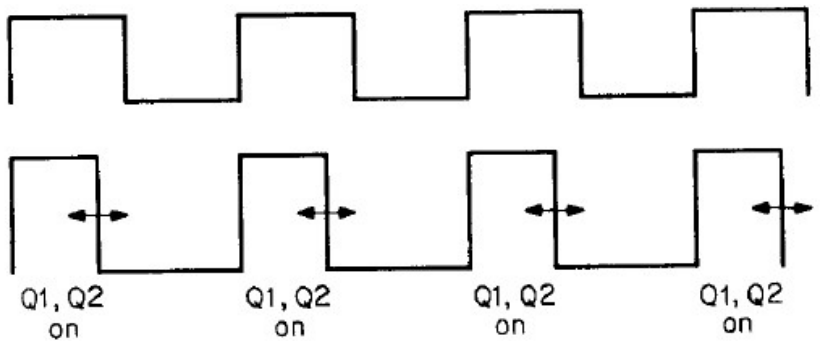
Switch Mode Power Supplies

Dr. Tahir Izhar

Basic Circuit



Waveforms



Basic Operation

- Transistors *Q*1 and *Q*2 are turned on and off simultaneously.
- Diodes *D*1 and *D*2 keep the maximum off-voltage stress on *Q*1, *Q*2 at V_{dc}.
- Compared with $2V_{dc}$ plus a leakage spike for the single-ended forward converter.
- There is no leakage inductance spike across the Transistors.

Basic Operation

- *Q*1 and *Q*2 are in series with the transformer primary.
- These transistors are turned on and off simultaneously.
- When they are "on," all primary and secondary dot ends are positive, and power is delivered to the loads. When they turn "off," current stored in the *T*1 magnetizing inductance reverses the voltage polarity of all windings.
- The negative-going dot end of *Np* is caught at ground by diode *D*1, and the positive-going no-dot end of *Np* is caught at V_{dc} by diode *D*2.

Basic Operation

- The emitter of *Q*1 can never be more than *V*dc below its collector.
- The collector of *Q*2 can never be more than *V*dc above its emitter.
- Leakage inductance spikes are clamped so that the maximum voltage stress on either transistor can never be more than the maximum DC input voltage.

Basic Operation

- The energy stored in the leakage inductance during the "on" time is fed back into V_{dc} via *D*1 and *D*2 when the transistors turn "off."
- The leakage inductance current flows out of the no-dot end of *Np,* through *D*2, into the positive end of V_{dc}, out of its negative end, and up through *D*1 back into the dot end of *Np.*

Basic Operation

- It is clear from the circuit that the core is always reset in a time equal to the “on” time.
- The reverse polarity voltage across *Np* when the transistors are “off” is equal to the forward polarity voltage across it when the transistors are “on.”
- Thus the core will always be fully reset with a 20% safety margin before the start of a succeeding half cycle if the maximum “on” time is no greater than 80% of a half period.

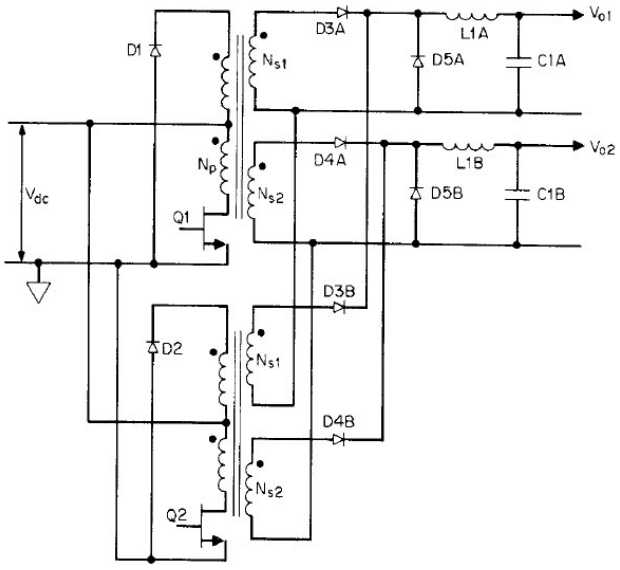
Output Power Limit

- This topology still yields only one power pulse per period, just like the single-ended forward converter.
- Thus the power available from a specific core is same for either the single- or double-ended configuration.
- The 200-W practical power limit for the single-ended forward converter does not hold for the double-ended forward converter.

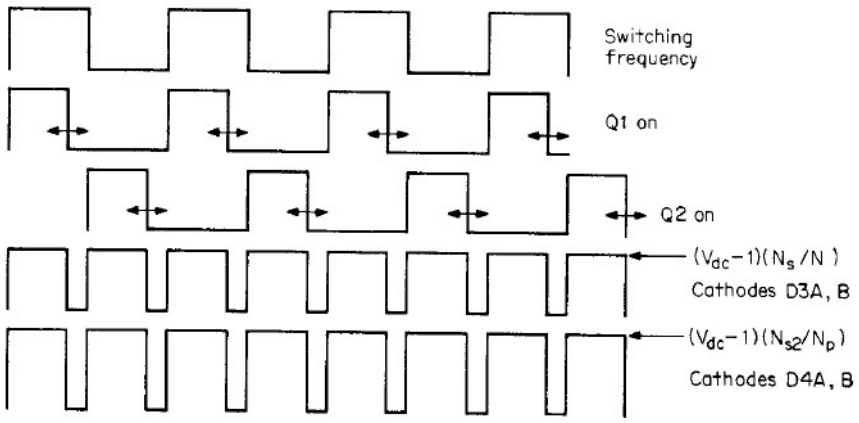
Output Power Limit

- With the reduced voltage stress, output powers of 400 to 500W are obtainable.

Interleaved Forward Converter



Waveforms



Operation

- Two identical single-ended forward converters operating on alternate half cycles with their secondary currents adding through rectifying “on” diodes.
- The advantage is that there are two power pulses per period, and each converter supplies only half the total output power.
- The transistor current is half that of a single forward converter at the same total output power.

Comparison

- One extra transistors is used with lower peak current rating and lower cost.
- Looking at it another way, two transistors of the same current rating used at the same peak current as one single-ended converter at a given output power in an interleaved converter would yield twice the output power of the single converter.

Comparison

- Compared to a push-pull, both are two-transistor circuits, the two transformers in the interleaved forward converter are probably more expensive and occupy more space than a single large one in a push-pull.
- There is no flux imbalance in the interleaved forward converter is probably the best argument for its use.

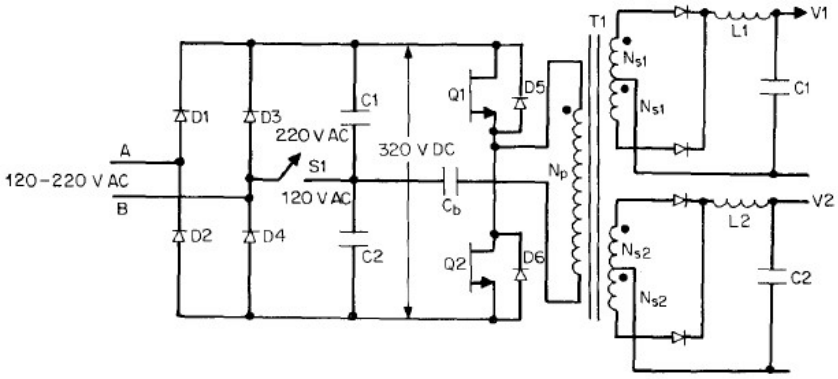
Bridge Converter Topologies

Switch Mode Power Supplies

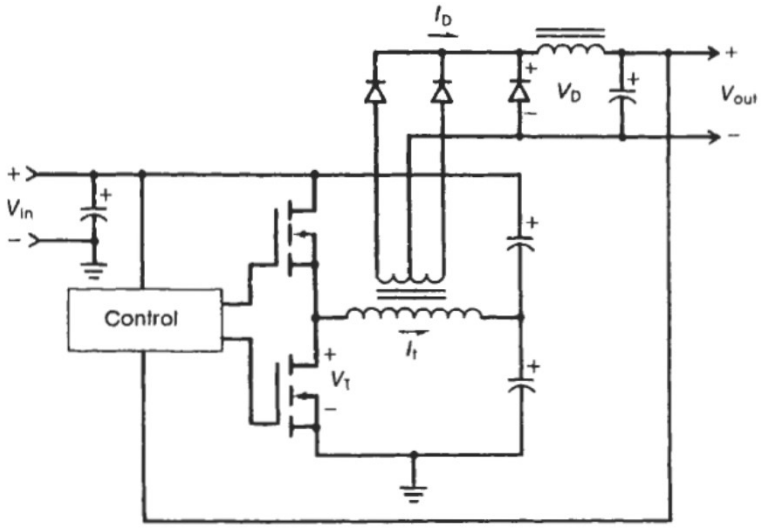
Dr. Tahir Izhar

Half-Bridge Converter

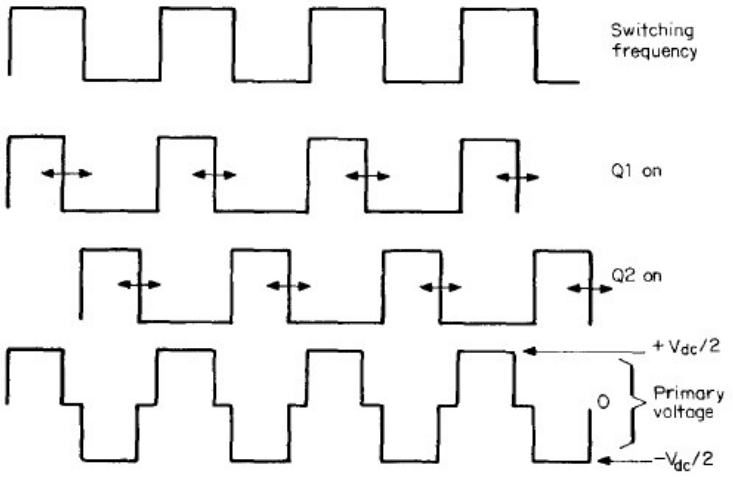
Half-Bridge Converter Circuit



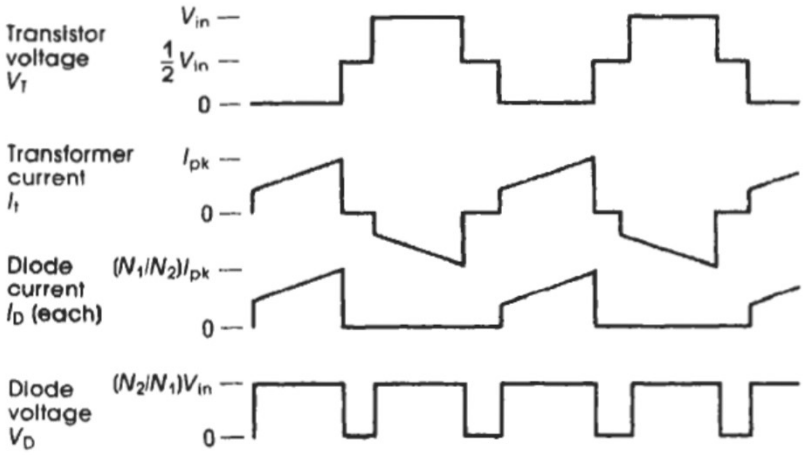
SMPS Circuit using Half Bridge



Waveforms



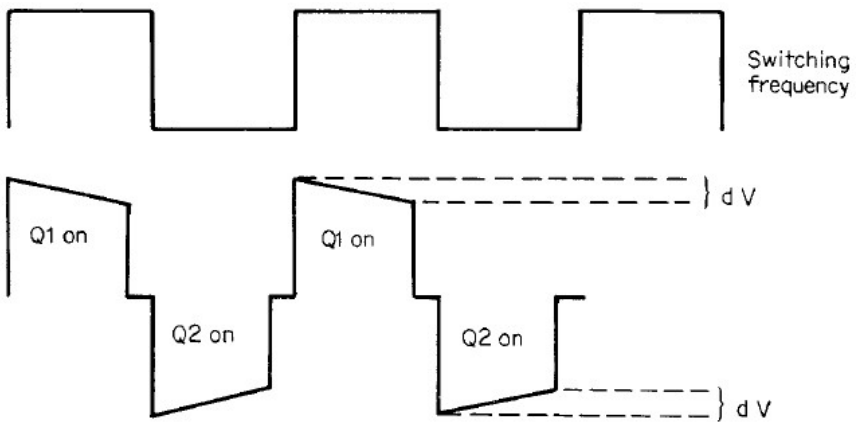
Waveforms



Blocking Capacitor

- If the junction of *C*1 and *C*2 is not at exactly half the supply voltage, the positive and negative voltage across the primary will differ, causing saturation and destroying the transistors.
- To avoid this flux imbalance, A small capacitor *Cb* is fitted in series with the primary.
- The capacitor charges up as the primary current *I*pft flows into it, robbing voltage from the flat-topped primary pulse as shown in the following Figure.

Effect of Blocking Capacitor



Value of Blocking Capacitor

Assume a permissible droop of *dV.*
The equivalent flat-topped current pulse that causes this droop is *I*pft
This current flows for 0.8*T*/2,
Thus the required capacitor magnitude is simply

$$C_b = \frac{I_{pft} \times 0.8T/2}{dV}$$

Value of Blocking Capacitor

At minimum DC input, the maximum "on" time in each half period will be set at 0.8*T*/2.

At primary voltage *V*dc/2, the input power is

$$1.25P_0 = \frac{V_{DC}}{2} \times I_{pft} \times \frac{0.8T}{T}$$

$$I_{pft} = \frac{3.13P_0}{V_{DC}}$$

Example

- A 150-W half bridge operating at 100 kHz from a nominal AC input of 230 V with 5% tolerance. Assume the efficiency of 80%. A tolerable droop in the flat-topped primary voltage pulse would be 10%.calculate the value of the Blocking Capacitor.

Solution

$$V_{DC} = \sqrt{2}\,(230 - 5\%) = 308V$$

$$I_{pft} = \frac{3.13P_0}{V_{DC}}$$

$$I_{Pft} = 3.13 \times 150/308 = 1.52A$$

10% of $V_{dc}/2$ is 15.4V

Solution

$$C_b = \frac{I_{pft} \times 0.8T/2}{dV}$$

$$C_b = \frac{I_{pft} \times 0.8}{dV \times 2 \times f}$$

$$C_b = \frac{1.52 \times 0.8}{15.4 \times 2 \times 100 \times 10^3} = 0.39\mu F$$

The capacitor must be a no polarized type.

Leakage Inductance in Half-Bridge

- Voltage spikes due to Leakage inductance are clamped to *V*dc by the diodes across transistors.
- When *Q*1 is "on," the load and magnetizing currents flow through it and through the primary leakage inductance through C_b and to the *C*1, *C*2 junction.
- The dot end of *Np* is positive with respect to its no-dot end.

Leakage Inductance in Half-Bridge

- When *Q*1 turns "off," the magnetizing inductance forces all winding polarities to reverse.
- The dot end of *T*1 try to become negative, however, it is clamped by diode *D*6 to the supply rail *V*dc and can not be more negative than the negative end of the supply.

Leakage Inductance in Half-Bridge

- Similarly, when Q_2 is "on," it stores current in the magnetizing inductance, and the dot end of *Np* is negative with respect to the no-dot end.
- When Q_2 turns "off," the magnetizing inductance reverses all winding polarities and the dot end of *Np* tries to go positive but is caught at V_{dc} by diode D_5.

Leakage Inductance in Half-Bridge

- Thus the energy stored in the leakage inductance during the “on” time is returned to the supply rail V_{dc} via diodes D_5, D_6.

Double-Ended Forward
vs.
Half Bridge

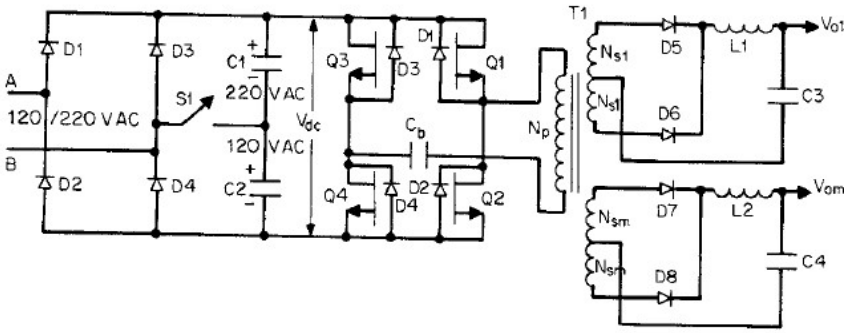
- Both are candidates for the universal off-line power supply.
- The most significant difference is that the half-bridge secondary provides full-wave output as compared with half-wave in the forward converter.

Double-Ended Forward
vs.
Half Bridge

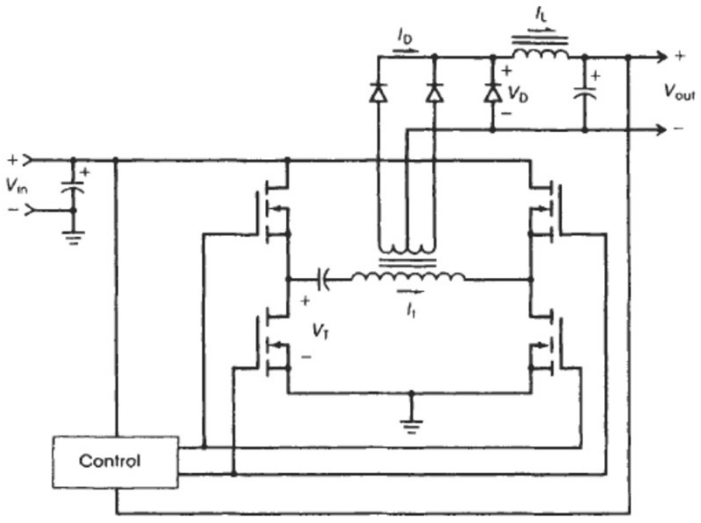
- Thus, the square-wave frequency in the half-bridge secondary is twice that in the forward converter.
- Hence, the output *LC* inductor and capacitor are smaller with the half bridge.

Full-Bridge Converter

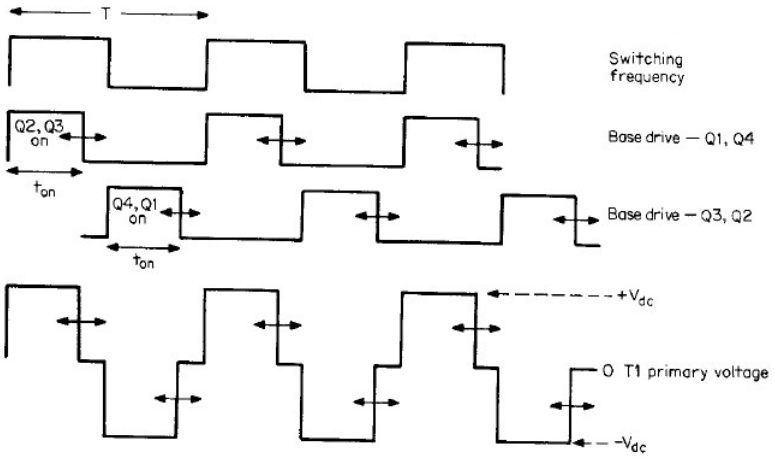
Full-Bridge Converter Circuit



Full Bridge Power Supply



Waveforms



Full-Bridge

- The transformer's flux is driven in both the positive and negative polarities.
- Its performance with respect to output power is significantly improved over that of the half-bridge converter.
- Two of the four power switches are turned on simultaneously.

Full-Bridge

- The maximum power-handling capability is doubled compared to half-bridge.
- The control circuitry remains unchanged.
- Core flux balancing is achieved by placing a small nonpolarized capacitor in series with the primary winding.

Full-Bridge

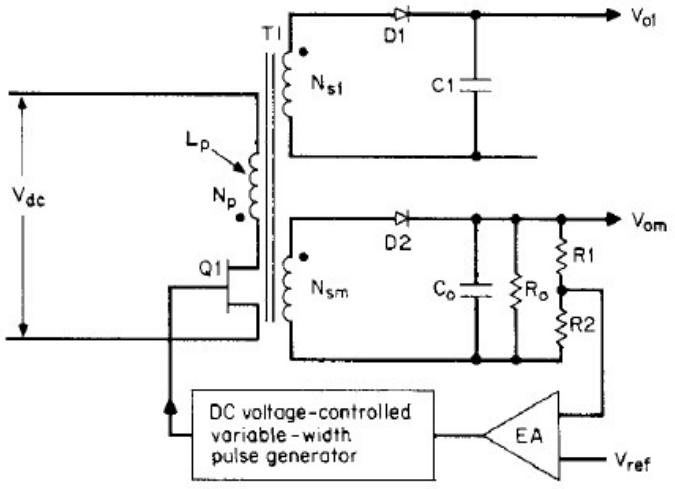
- The full-bridge regulator topology is used in applications requiring output powers of 300 W to many kilowatts.

Fly-back Converter

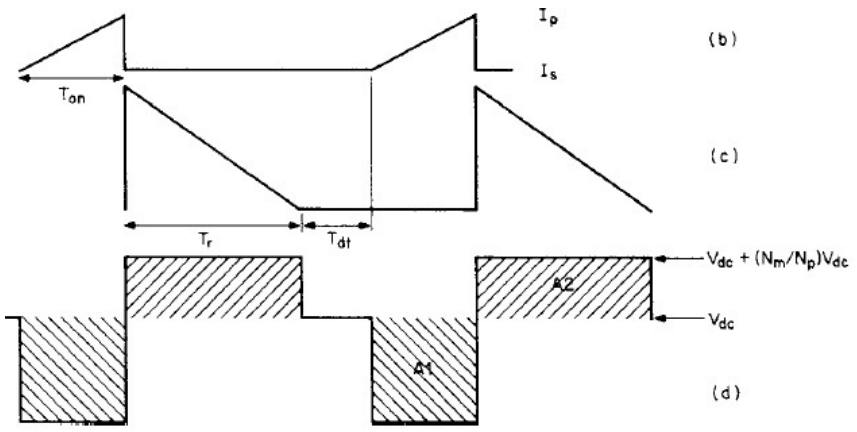
Switch Mode Power Supplies

Dr. Tahir Izhar

Converter Circuit



Waveforms



Operation

- When *Q*1 turns "on," all rectifier diodes become reverse-biased, and all output load currents are supplied from the output capacitors.
- T1 acts like a pure inductor and primary current builds up linearly in it to a peak value of *Ip*.

Ampere-Turn Balance

- There is no correlation between primary and secondary voltages as in case of conventional transformer.
- The primary to secondary ampere-turns ratios are conserved in contrast to the voltage ratios.
- If the primary has 100 turns and the current when *Q*1 turns "off" is 1 amp, the ampere-turns is 100 in the primary.

Operation

- When *Q*1 turns "off," all winding voltages reverse under flyback action, bringing the output diodes into conduction and the primary stored energy is delivered to the output to supply load current and replenish the charge on the output capacitors.
- The circuit is discontinuous if the secondary current has decayed to zero before the start of the next turn "on" period of *Q*1.

Ampere-Turn Balance

- This must be conserved in the secondary with, say, of 10 turns, the secondary current will be 10.
- In the same way, a single turn will develop 100 amps
- Or 1000 secondary turns will develop 0.1 amps.

Ampere-Turn Balance

- If we terminate the 10-turn 10-amp secondary winding with a 1-ohm load, we will get 10 volts.
- If we terminate it with 100 ohms, we will get 1000 volts!
- This is why the fly back topology is so useful for generating high voltages.
- Do not try to open circuit this winding because it will destroy the semiconductors.
- With several secondary windings conducting at the same time, then the sum of all the secondary ampere-turns must be conserved.

Fly-back Disadvantages

- Large Output Voltage Spikes
- Large Output Filter Capacitor and High Ripple Current Requirement

Fly-back SMPS Design

Fly-back SMPS Design

Assuming 80% efficiency

$$P_i = 1.25P_o \qquad (1)$$

Fly-back SMPS Design

Assuming 80% efficiency

$P_i = 1.25P_o$ (1)

$$P_o = \frac{{V_o}^2}{R_o} \qquad (2)$$

Fly-back SMPS Design

Assuming 80% efficiency

$$P_i = 1.25P_o \quad (1)$$

$$P_o = \frac{{V_o}^2}{R_o} \quad (2)$$

$$P_i = 1.25\frac{{V_o}^2}{R_o} \quad (3)$$

Fly-back SMPS Design

$$P_i = \frac{E}{t}$$

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Fly-back SMPS Design

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Putting (5) into (4)

Fly-back SMPS Design

$$P_i = \frac{E}{t}$$

$$P_i = \frac{\left({}^1/_2 L_p {I_p}^2\right)}{T} \qquad (4)$$

$$I_p = \frac{V_{DC}\, T_{on}}{L_p} \qquad (5)$$

Putting (5) into (4)

$$P_i = \frac{L_p}{2T}\left(\frac{V_{DC} T_{on}}{L_p}\right)^2$$

Fly-back SMPS Design

And from (3)

$$P_i = \frac{L_p}{2T}\left(\frac{V_{DC}T_{on}}{L_p}\right)^2 = 1.25\frac{{V_o}^2}{R_o}$$

Fly-back SMPS Design

And from (3)

$$P_i = \frac{L_p}{2T}\left(\frac{V_{DC}T_{on}}{L_p}\right)^2 = 1.25\frac{{V_o}^2}{R_o}$$

Therefore solving for $\boldsymbol{V_o}$

$$V_o = V_{DC}T_{on}\sqrt{\frac{R_o}{2.5TL_p}} \qquad (6)$$

Fly-back Design Procedure

Step-1

Calculate the transformer turn ratio

$$V_{ms} = V_{DC} + \left(\frac{N_p}{N_s}\right) V_o + 0.3V_{DC} \qquad (7)$$

In (7), $\boldsymbol{V_{ms}}$ is the maximum voltage stress across the power transistor, $\boldsymbol{V_{DC}}$ is the max input DC voltage, and $0.3\boldsymbol{V_{DC}}$ is 30 % voltage spike due to leakage inductance.

Fly-back Design Procedure

Step-2

Ensuring discontinuous operation and equating volt-second products (A1=A2), Calculate power transistor ON time.

$$V_{DC}T_{on} = V_o \left(\frac{N_p}{N_s}\right) T_r \qquad (8)$$

$$T_{on} + T_r = 0.8T \qquad (9)$$

From (8) and (9)

$$T_{on} = \left(\frac{0.8TV_o \left(\frac{N_p}{N_s}\right)}{V_{DC} + V_o \left(\frac{N_p}{N_s}\right)} \right) \qquad (10)$$

Fly-back Design Procedure

Step-3

Calculate primary Inductance from (6) of output voltage.

$$V_o = V_{DC} T_{on} \sqrt{\frac{R_o}{2.5 T L_p}} \qquad (6)$$

$$L_p = \frac{R_o}{2.5T} \left(\frac{V_{DC} T_{on}}{V_o} \right)^2$$

$$L_p = \frac{(V_{DC} T_{on})^2}{2.5 T P_o} \qquad (11)$$

Fly-back Design Procedure

Step-4

Calculate transistor peak current from (5)

$$I_p = \frac{V_{DC}\, T_{on}}{L_p} \qquad (5)$$

Fly-back Design Procedure

Step-5

Output Filter Capacitor

The output capacitor is designed on the basis of specified peak-to-peak output voltage ripple. The voltage on this capacitor droops by

$$\Delta V = \frac{I\left(T - T_{off}\right)}{C_o} \qquad (12)$$

Design Example

Design Data

- Transistor Peak Voltage =200V
- Output power =50W
- Input DC voltage = 40V to 60V
- Output Voltage = 10V
- Switching Frequency = 50K Hz
- Output Capacitor Voltage droop is 0.05V

Solution

Step-1

Calculate the transformer turn ratio

$$V_{ms} = V_{DC} + \left(\frac{N_p}{N_s}\right) V_o + 0.3V_{DC} \qquad (7)$$

$$200 = 60 + \left(\frac{N_p}{N_s}\right) 10 + 0.3X60$$

$$\left(\frac{N_p}{N_s}\right) = \frac{200 - 60 - 18}{10} = 12$$

Use maximum value for $\boldsymbol{V_{DC}}$ under worst case

Solution

Step-2

$$T_{on} = \left(\frac{0.8TV_o \left(\frac{N_p}{N_s}\right)}{V_{DC} + V_o \left(\frac{N_p}{N_s}\right)} \right) \qquad (10)$$

$$T_{on} = \frac{0.8X20X10X12}{40 + 10X12} = 12\mu S$$

Use minimum value for $\boldsymbol{V_{DC}}$ under worst case

Solution

Step-3

Calculate primary Inductance from (11) .

$$L_p = \frac{(V_{DC}T_{on})^2}{2.5TP_o} \qquad (11)$$

$$L_p = \frac{(40X12X10^{-6})^2}{2.5X20X10^{-6}X50}$$

$$L_p = 92.16\mu H$$

Solution

Step-4

Calculate transistor peak current from (5)

$$I_p = \frac{V_{DC}\,T_{on}}{L_p} \qquad (5)$$

$$I_p = \frac{40X12X10^{-6}}{92.16X10^{-6}}$$

$$I_p = 5A$$

Solution

Step-5

The output capacitor is designed on the basis of specified peak-to-peak output voltage ripple. The voltage on this capacitor droops by

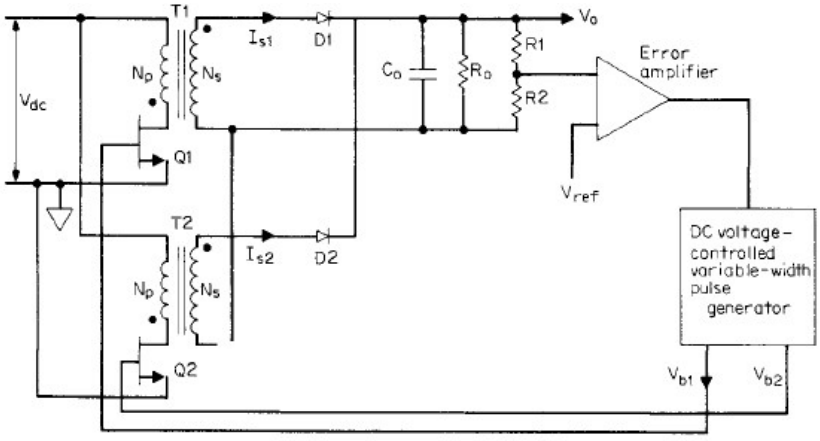
$$\Delta V = \frac{I(T - T_r)}{C_o} \qquad (12)$$

$$T_{on} + T_r = 0.8T \qquad (9)$$

$$T_r = 0.8\mathrm{T} - T_{on} = 0.8\mathrm{X}20 - 12 = 4$$

$$C_o = \frac{5(20 - 4)}{.05} = 1600\mu F$$

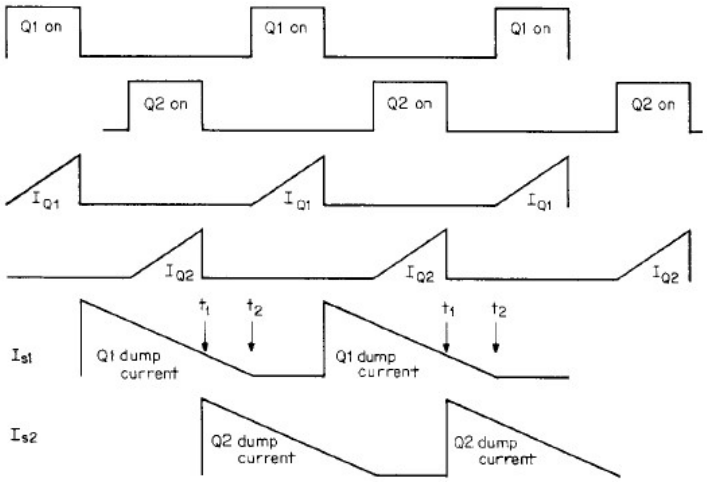
Interleaved Flyback



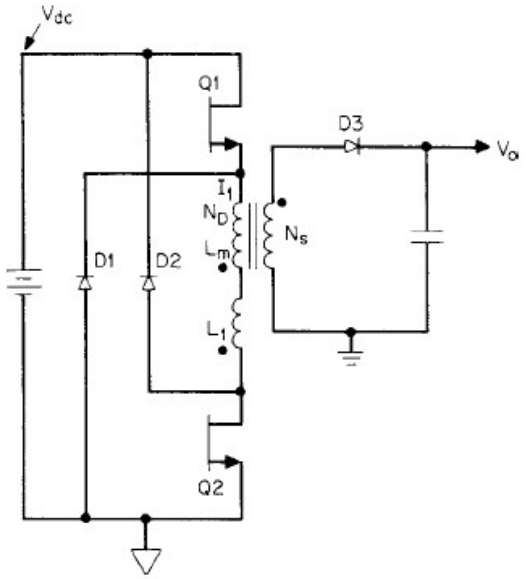
Operation

- Two discontinuous-mode fly-backs.
- Power Transistors are turned “on” at alternate half cycles.
- Secondary currents are added.
- Maximum power up to 300 W.
- A single fly-back at the 300-W is impractical due to very high peak primary and secondary currents.
- Up to 150W, a single forward converter is a better choice.

Waveforms



Double-Ended Fly-back



Basic Operation

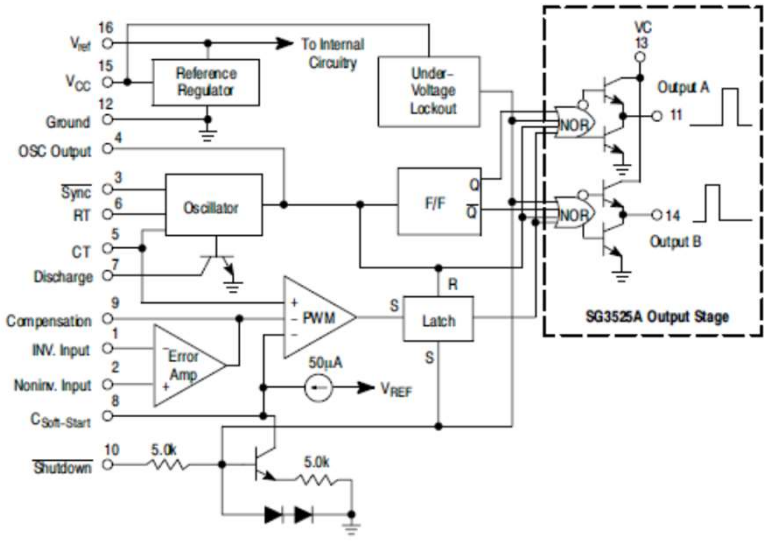
- Power transistors are turned “on” simultaneously.
- The dot end of the secondary is negative, *D*3 is reverse-biased, no secondary current.
- The primary behaves as an inductor, and current in it ramps up linearly.
- When *Q*1 and *Q*2 turn “off,” all primary and secondary voltages reverse polarity.
- *D*3 becomes forward-biased, and the stored energy is delivered to the load.

Basic Operation

- The “on” volt-second product must equal the “reset” volt-second product.
- The maximum voltage stress the transistor can never be more than V_{dc}.
- The disadvantage is two transistors and the two clamp diodes.

Control ICs

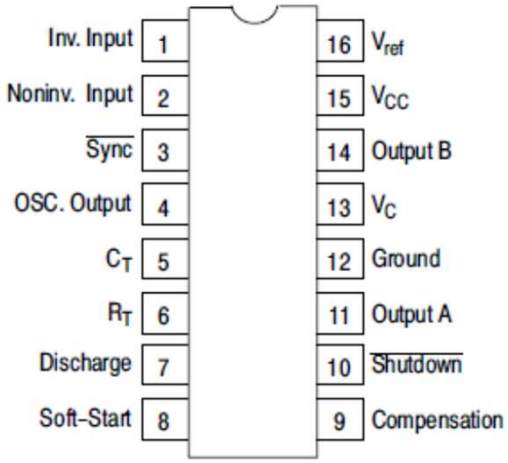
SG 3525 Block Diagram



SGS 3525 Features

- 8.0 V to 35 V Operation
- 5.1 V 1.0% Trimmed Reference
- 100 Hz to 400 kHz Oscillator Range
- Separate Oscillator Sync Pin
- Adjustable Deadtime Control
- Input Undervoltage Lockout
- Latching PWM to Prevent Multiple Pulses
- Pulse−by−Pulse Shutdown
- Dual Source/Sink Outputs: 400 mA Peak

PIN CONNECTIONS



(Top View)

Maximum Ratings

MAXIMUM RATINGS

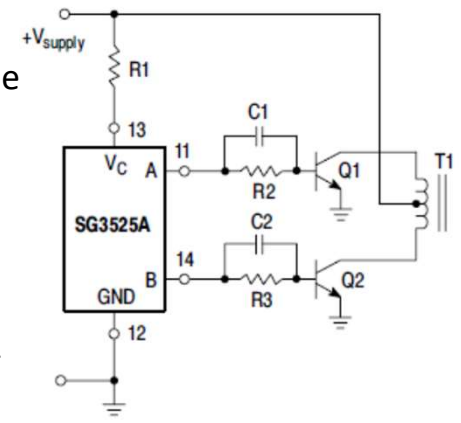
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	+40	Vdc
Collector Supply Voltage	V_C	+40	Vdc
Logic Inputs		−0.3 to +5.5	V
Analog Inputs		−0.3 to V_{CC}	V
Output Current, Source or Sink	I_O	±500	mA
Reference Output Current	I_{ref}	50	mA
Oscillator Charging Current		5.0	mA
Power Dissipation T_A = +25°C (Note 1) T_C = +25°C (Note 2)	P_D	 1000 2000	mW
Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	100	°C/W
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	60	°C/W
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Lead Temperature (Soldering, 10 seconds)	T_{Solder}	+300	°C

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	8.0	35	Vdc
Collector Supply Voltage	V_C	4.5	35	Vdc
Output Sink/Source Current (Steady State) (Peak)	I_O	 0 0	 ±100 ±400	mA
Reference Load Current	I_{ref}	0	20	mA
Oscillator Frequency Range	f_{osc}	0.1	400	kHz
Oscillator Timing Resistor	R_T	2.0	150	kΩ
Oscillator Timing Capacitor	C_T	0.001	0.2	µF
Deadtime Resistor Range	R_D	0	500	Ω
Operating Ambient Temperature Range	T_A	0	+70	°C

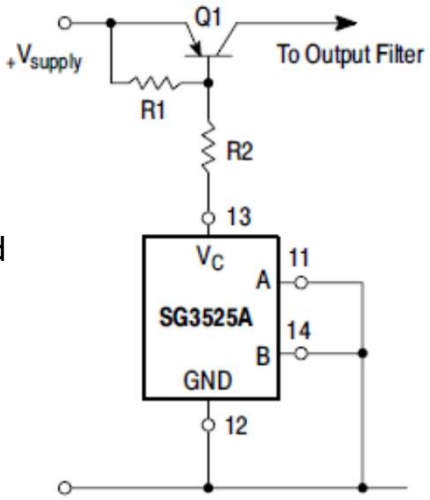
Connections for Push-Pull

- In conventional push-pull bipolar designs, forward base drive is controlled by R1-R3.
- Rapid turn-off times for the power devices are achieved with speed-up capacitors C1 and C2.

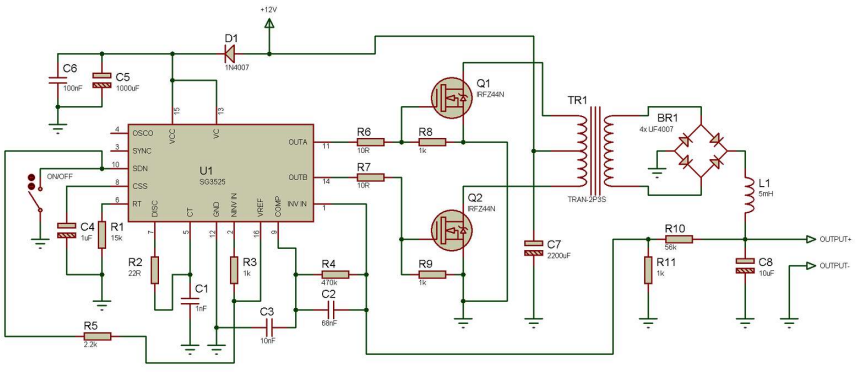


Connections for Single Ended

- For single-ended supplies, the driver outputs are grounded.
- The V_C terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.

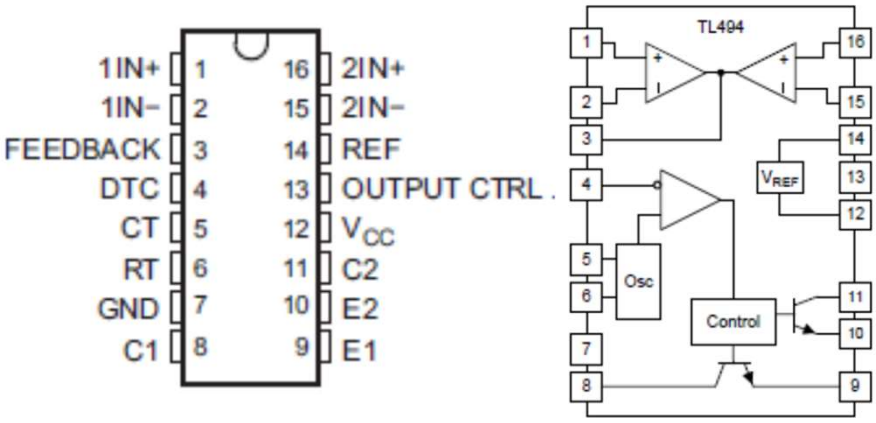


Push-Pull Application using SG3525



TL494 PWM Control Chip

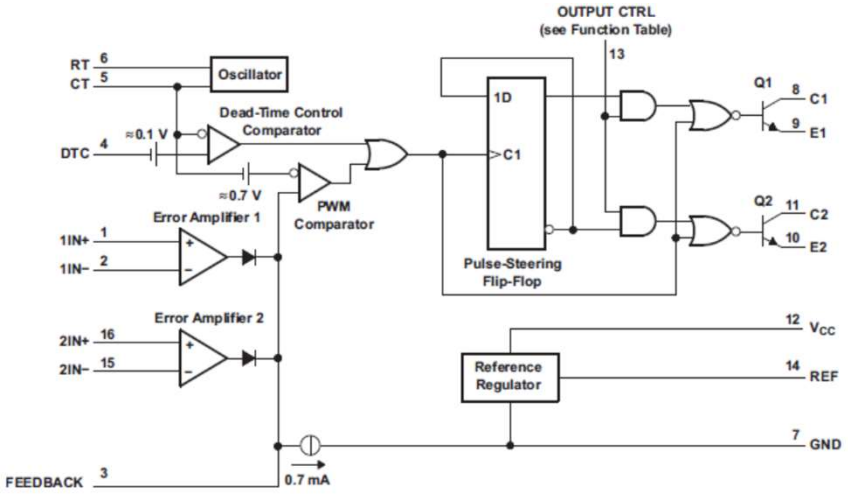
Pin Configuration and Simplified Block Diagram



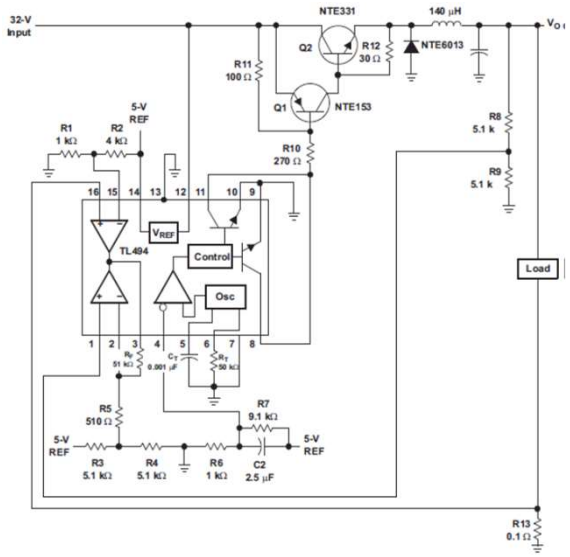
Features

- Complete PWM Power-Control Circuitry
- Uncommitted Outputs for 200-mA Sink or Source Current
- Output Control Selects Single-Ended or Push-Pull Operation
- Internal Circuitry Prohibits Double Pulse at Either Output
- Variable Dead Time Provides Control Over Total Range
- Internal Regulator Provides a Stable 5-V Reference Supply With 5% Tolerance
- Circuit Architecture Allows Easy Synchronization

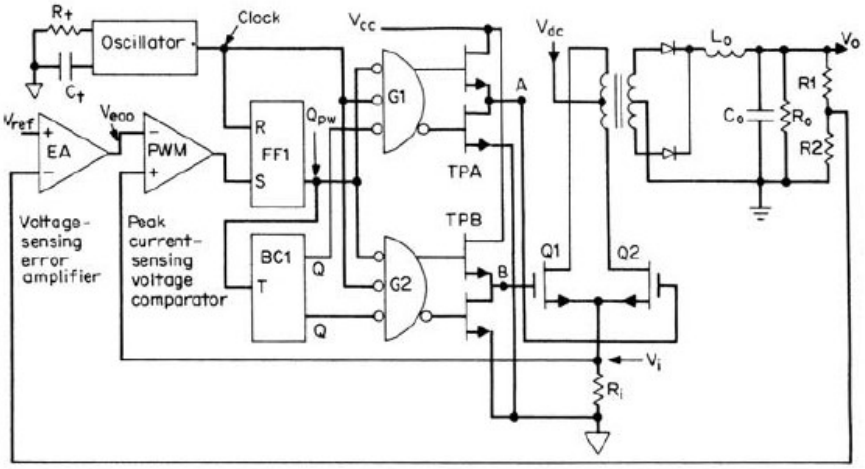
Functional Block Diagram



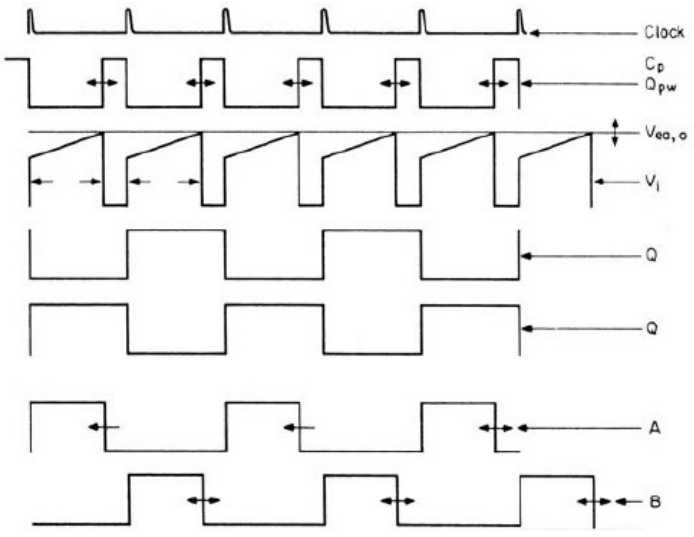
Typical Application 5-V/10-A



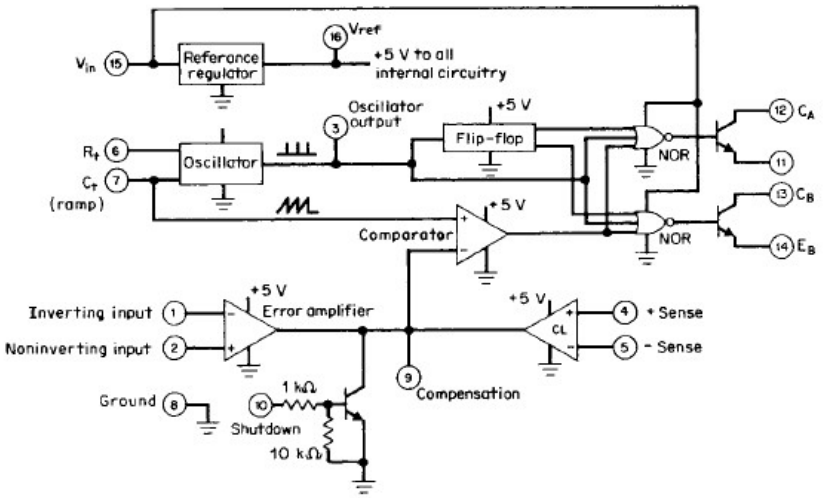
Current-Mode Control Circuitry



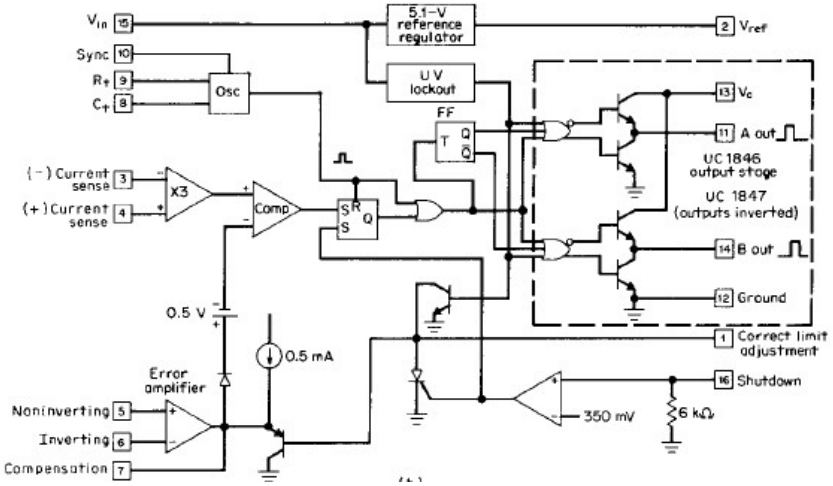
Waveforms



SG1524-PWM Control Chip



UC184-PWM Current-Mode Control



Transformers and Inductors

SMPS-19

Dr. Tahir Izhar

Introduction

- To design to Magnetic components, it is necessary to know the size, area of core, core window or bobbin winding area, peak flux density, operating frequency, and coil current density.
- The core size and frequency can be estimated.
- We can then calculate the approximate power available from the selected core, frequency, and the remaining parameters.

Introduction

- This initial estimate can then be easily corrected if the desired power is not available.
- Since all the parameters are interrelated, such interactive calculations may have to be done several dozen times before a satisfactory combination of the parameters is found.

Core Materials

- SMPS transformers are made with ferrite cores.
- Ferrites are ceramic ferromagnetic materials having a crystalline structure consisting of mixtures of iron oxide with either manganese or zinc oxide.
- Their eddy current losses are negligible, due to very high electrical resistivity.
- Core loss is mainly due to hysteresis which is low enough to permit use frequencies up to 1 MHz.

Ferrite Core Geometries

- Ferrite cores are manufactured in a relatively small number of geometric shapes and varying dimensions within the shapes.
- Cores are available from various manufacturers in standard shapes and dimensions.
- The core geometries are pot, RM, EE, PQ, UU and UI.
- The pot core is used at power levels up to 125W.

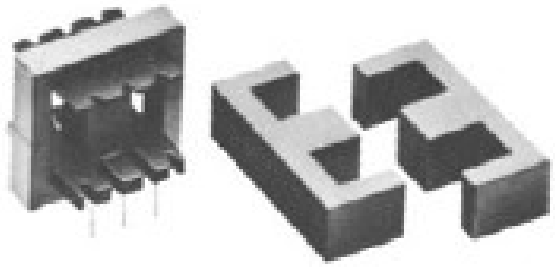
Pot Cores

- In Pot Core, the coil on the bobbin around the center post is almost entirely enclosed by ferrite material.
- This decreases its radiating magnetic field and hence is used when EMI or RFI problems must be minimized.
- The major disadvantage of the pot core is the narrow slot in the ferrite through which the coil leads exit. This makes it difficult to use at high input or output currents requiring large wire diameter, or in multi-output supplies with many wires exiting.

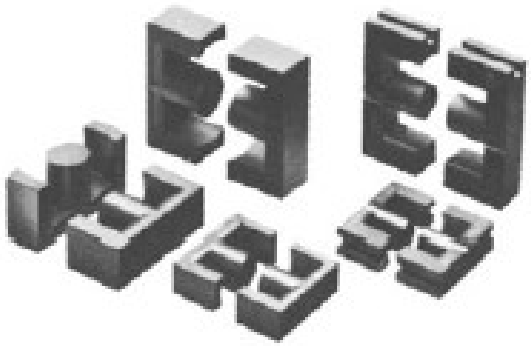
Pot Cores

- Many pot cores are available with gaps of various sizes in the center leg so that they may carry a DC bias current without saturating.
- Pot cores are used as output inductors in buck converters, forward converters and push-pull converters.

EE Core

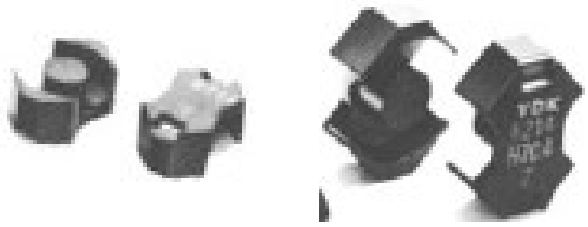


EC and ETD Cores



PQ Cores

RM Cores



Gapped Cores

- Most often, when a core is available with a gapped center leg, the manufacturer gives its value of inductance per 1000 turns and the cliff point in ampere turns at which it falls over its saturation cliff.
- If a gapped core is required, it is preferable to use a core with a gapped center leg rather than using un-gapped core halves separated with plastic shims.
- Shimming core halves will not yield reproducible values of inductance over time, temperature, and production spread. Also, gapping the outer leg will increase EMI.

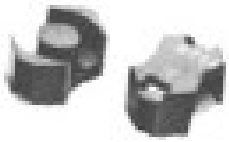
EE, EC and ETD Cores

- The most widely used are EE cores due to ample room for coil leads entering and leaving the bobbin.
- Since the coil is not fully surrounded by ferrite, it may produce a larger EMI-RFI field.
- However, airflow around the windings is unimpeded, which therefore run cooler.
- Cores are available with either a round center leg (EC, ETD).
- Round-center-leg cores have a small advantage in that the mean length of a turn is about 11% shorter than for a square-legged core of equal center-leg area. Coil resistance is 11% less, and copper loss and temperature rise are lower.

EE, EC and ETD Cores

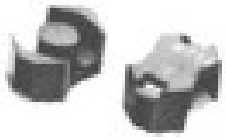
- There is a large range of EE core sizes, they can deliver output powers from under 5W up to 10kW.
- By using two square-center-leg EE cores side by side, the core area is doubled, requiring half the number of turns for the same voltages, peak flux density, and frequency.
- This doubles the power available from a single core, and may result in a smaller transformer than using a single core of the next larger size.

RM Cores



- RM core is a compromise between a pot and an EE core.
- It is effectively a pot core with a much wider notch cut out of the ferrite.
- It is thus easier to bring larger diameter or many wires in and out of the coil, so this core is usable for much higher output power levels and for multi-output transformers.
- The larger ferrite notch also provides easier access for convection air currents than in a pot core, which results in smaller temperature rise.

RM Cores



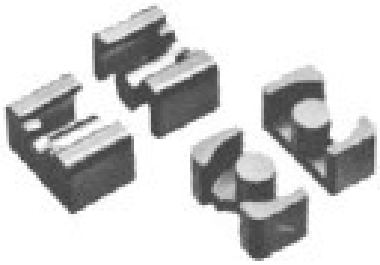
- The coil is not as fully surrounded by ferrite as in a pot core, it causes more EMI-RFI radiation.
- Compared to EE core, its EMI radiation is less for equal output power.
- RM cores are available with or without a center-leg hole. The center leg hole is used for mounting with a bolt.

PQ Cores

- The geometry of the PQ core is such that it provides an optimum ratio of volume to radiating surface and coil winding area.
- Since core losses are proportional to core volume, and heat radiation capability is proportional to radiating surface area, these cores have a minimized temperature rise for a given output power.
- Further, since the PQ core volume-to-coil-winding-area ratio is optimized, the volume is minimized for a given output power.

LP Cores

- Specifically designed for low-profile transformers.
- They have long center legs, which minimize leakage inductance.



UU and UI Cores

- UU or UI cores are used mainly for high-voltage or ultra-high-power applications.
- They are rarely used at power levels under 1 kW.
- Their large window area compared to an EE core of equal core area permits much larger wire sizes or many more turns.
- But their much larger magnetic path length does not yield as close primary-secondary coupling as in an EE core, and results in larger leakage reactances.

Peak Flux Density

- The number of transformer primary turns will be calculated from Faraday's law.

$$N = \frac{VT_{\text{on}}}{A_e \Delta B}$$

- Peak flux density B_{max} is selected.
- The larger the peak flux density, the fewer the primary turns so the larger the permissible wire size, the greater the available output power.

Peak Flux Density

- Two limitations to peak flux density in ferrite cores.
- More core losses resulting temperature rise.
- Core losses in most ferrite materials are proportional to the $B_{max}^{2.7}$.
- High peak flux densities cannot be permitted, especially at higher frequencies.
- Ferrites have such low losses below 25 kHz that core losses are not a limiting factor at those frequencies.

Peak Flux Density

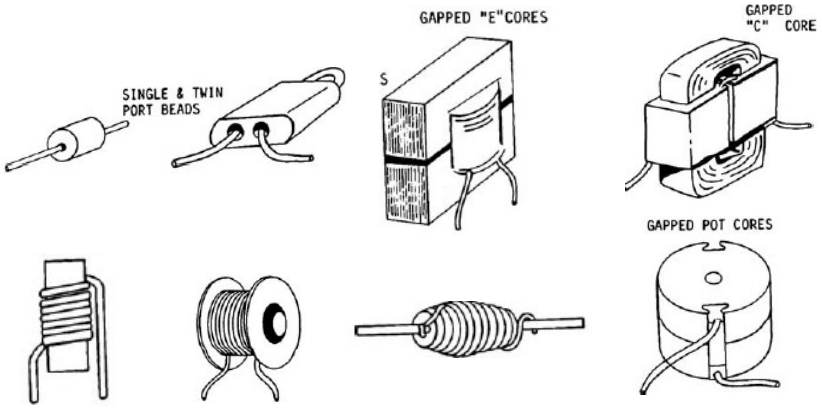
- At low frequencies, peak flux may extend into the curved area of the *BH* loop.
- However, the core should not move so far into saturation that the primary current increases to destroy the power transistor.
- Ferrite core losses also increase as the 1.7th power of the switching frequency.
- Thus at higher frequencies, for the more lossy materials, attempting a high peak flux density to minimize the number of turns results in very high losses.

Peak Flux Density

- Frequencies above 50 kHz, less lossy core material must be used, or peak flux density must be reduced.
- Reducing B_{max} requires more number of primary turns and hence requires smaller wire size for the same winding area resulting decreased power.

Inductors with Large DC Bias Current

Chokes are used extensively in SMPS.

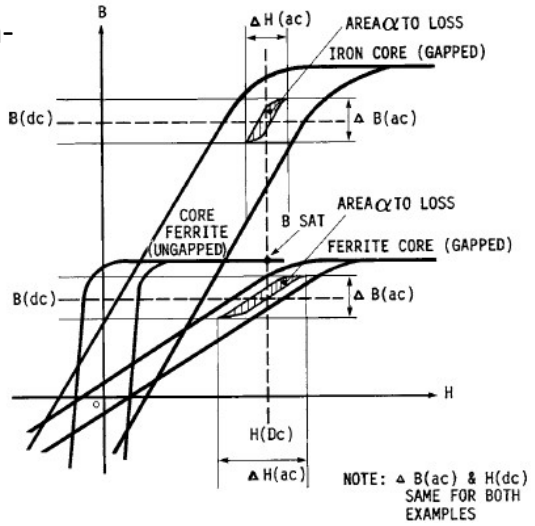


Inductor Design

- The design of inductors is quite straightforward, if there is no DC bias current.
- There are severe limitations on the design of chokes, when a large DC bias current is present.
- The B/H loop need to be examined with particular attention to the saturation properties of some typical core materials, and the effect of an air gap.

B/H Loop

First quadrant of a B/H loop for gapped and non-gapped ferrite cores

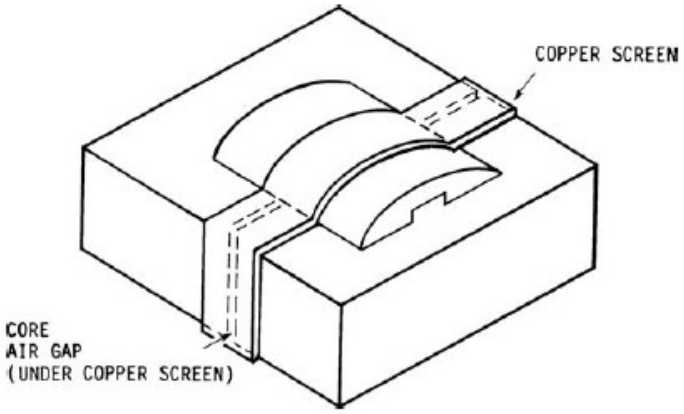


B/H Loop

- For an arbitrary value of DC bias current, resulting in a magnetization value H_{dc} shown by the vertical dotted line, that the ungapped ferrite core is completely saturated.
- The slope of the B/H loop for the ferrite at saturation is zero (horizontal).
- This means that the effective permeability of the ungapped ferrite core at this value of H is zero, so the choke will have near zero inductance.
- Clearly, an ungapped ferrite core is not much use as a choke with this value of DC bias current.

Copper Screening

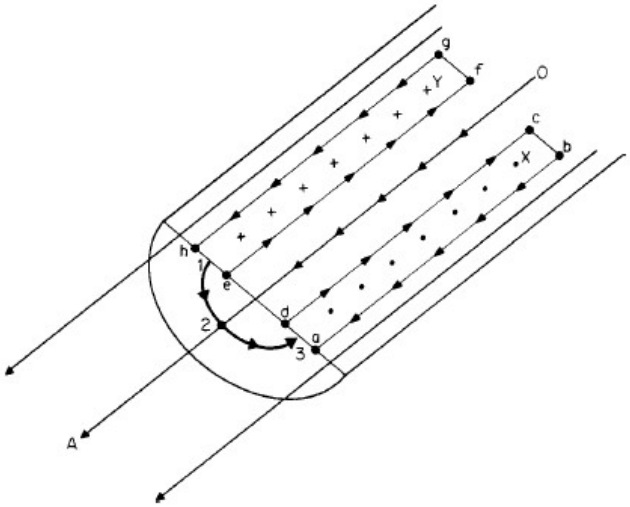
- A copper screen may be fitted around the outside of a gapped ferrite E core choke to reduce EMI radiation and fringing at the air gap.



Skin Effect

- Skin effect had been known since 1915.
- The main AC current in the wire induces eddy currents causing current to crowd into the thin outer skin of a conductor.
- The current-carrying area is less than the full wire area and the AC resistance is greater than the DC resistance by an amount determined by the skin thickness.

Skin Effect



Skin Depth

- Skin depth is defined as the distance below the surface where the current density has fallen to 1/*e*, or 37%, of its value at the surface.
- The relation between skin depth and frequency for copper wire at 70◦C is

$$S = \frac{2837}{\sqrt{f}}$$

where *S* is the skin depth in mils and *f* is frequency in hertz.

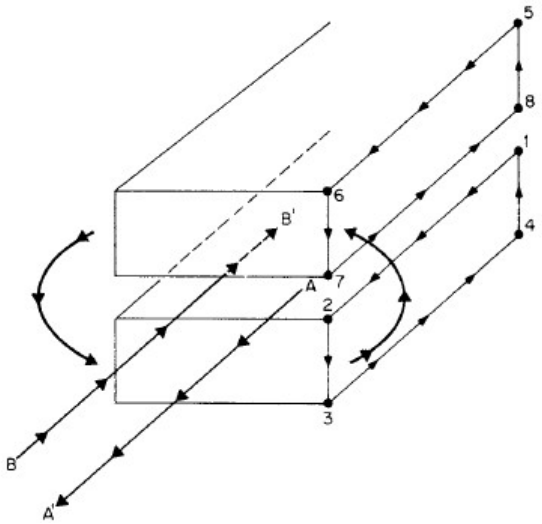
Skin Depth for copper wire at 70°C

Frequency, kHz	Skin depth, mils*
25	17.9
50	12.7
75	10.4
100	8.97
125	8.02
150	7.32
175	6.78
200	6.34
225	5.98
250	5.67
300	5.18
400	4.49
500	4.01

AC/DC Resistance Ratios Due to Skin Effect

AWG	25 kHz				50 kHz			100 kHz			200 kHz		
	Diameter d, mils	Skin depth S, mils	d/S	R_{ac}/R_{dc}	Skin depth S, mils	d/S	R_{ac}/R_{dc}	Skin depth S, mils	d/S	R_{ac}/R_{dc}	Skin depth S, mils	d/S	R_{ac}/R_{dc}
12	81.6	17.9	4.56	1.45	12.7	6.43	1.85	8.97	9.10	2.55	6.34	12.87	3.50
14	64.7	17.9	3.61	1.30	12.7	5.09	1.54	8.97	7.21	2.00	6.34	10.21	2.90
16	51.3	17.9	2.87	1.10	12.7	4.04	1.25	8.97	5.72	1.70	6.34	8.09	2.30
18	40.7	17.9	2.27	1.05	12.7	3.20	1.15	8.97	4.54	1.40	6.34	6.42	1.85
20	32.3	17.9	1.80	1.00	12.7	2.54	1.05	8.97	3.60	1.25	6.34	5.09	1.54
22	25.6	17.9	1.43	1.00	12.7	2.02	1.00	8.97	2.85	1.10	6.34	4.04	1.30
24	20.3	17.9	1.13	1.00	12.7	1.60	1.00	8.97	2.26	1.04	6.34	3.20	1.15
26	16.1	17.9	0.90	1.00	12.7	1.27	1.00	8.97	1.79	1.00	6.34	2.54	1.05
28	12.7	17.9	0.71	1.00	12.7	1.00	1.00	8.97	1.42	1.00	6.34	2.00	1.00
30	10.1	17.9	0.56	1.00	12.7	0.80	1.00	8.97	1.13	1.00	6.34	1.59	1.00
32	8.1	17.9	0.45	1.00	12.7	0.64	1.00	8.97	0.90	1.00	6.34	1.28	1.00
34	6.4	17.9	0.36	1.00	12.7	0.50	1.00	8.97	0.71	1.00	6.34	1.01	1.00

Proximity Effect



Housekeeping Topologies

Lecture 14

Dr Tahir Izhar

Introduction

- Low Output Power-(1 to 3 W, about 10- to 45-V).
- Specialized circuits for unique applications.
- Not always be regulated.
- Usual loads can tolerate a range of ± 15% max.
- Reliability is improved, if the supply is regulated (±2%).

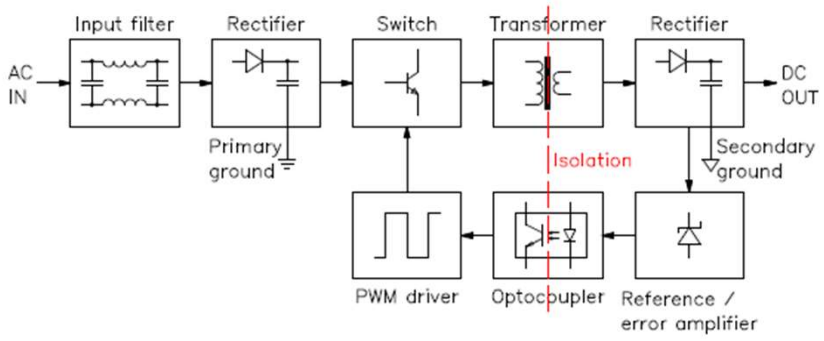
Design Objectives

The important objectives for these supplies.

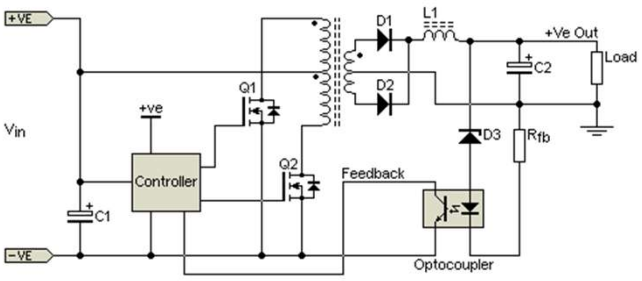
- Low in parts count.
- Low cost.
- Occupy a small space.

Design Decisions

Output or Input side common to PWM Chip.



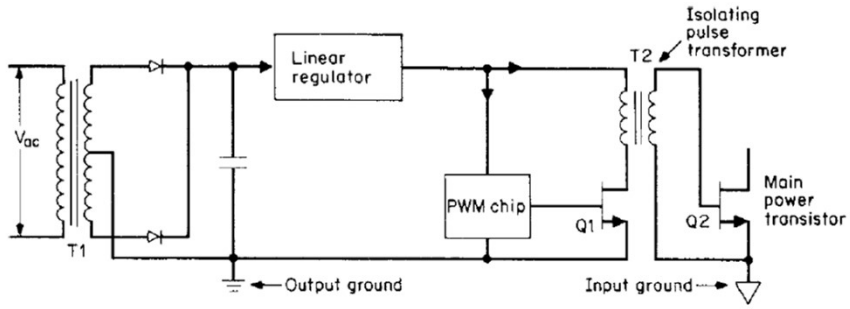
Input-side Common to PWM Chip



Specific Housekeeping Supply

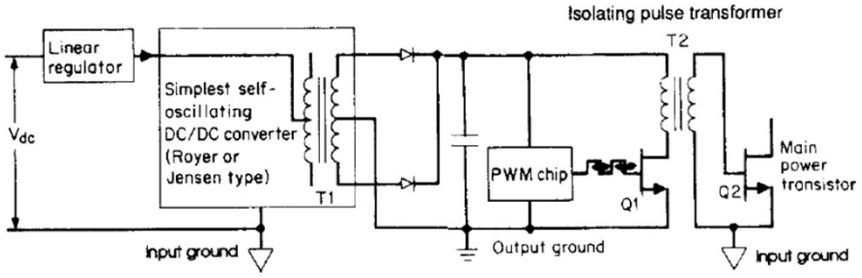
- Following Figures show the block diagrams of three reasonable approaches to a housekeeping supply where the error amplifier and pulse width modulator are in a PWM chip on output common.

Specific Housekeeping Supply Block Diagrams



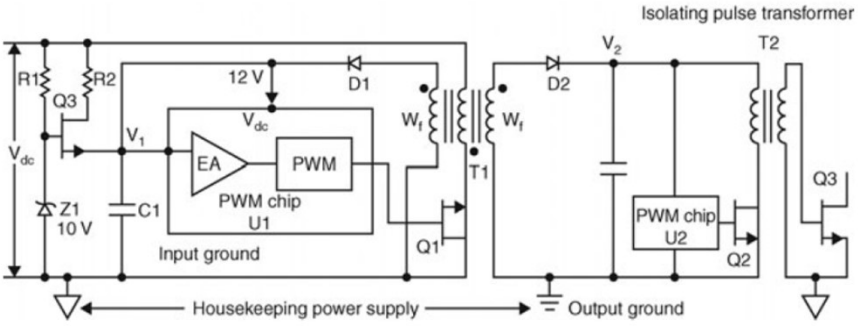
- The simplest off-line housekeeping supply.
- A small 50-Hz isolating transformer.
- Followed by an inexpensive linear regulator

Specific Housekeeping Supply Block Diagrams



- A housekeeping supply for DC input voltage.
- A regulator may be unnecessary if the main PWM chip can tolerate ±10% input voltage variation.

Specific Housekeeping Supply Block Diagrams

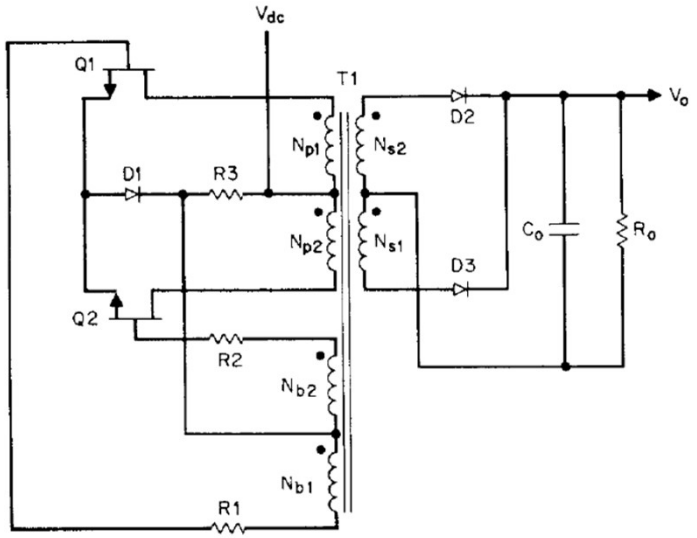


- A minimum-parts-count flyback as a housekeeping supply.
- It generates a regulated output V_2 without requiring any linear regulators.

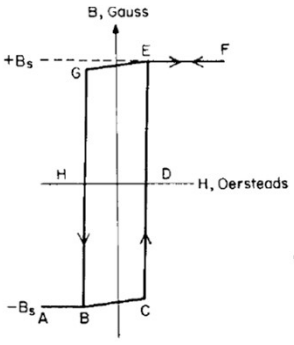
Royer Oscillator Housekeeping Supply

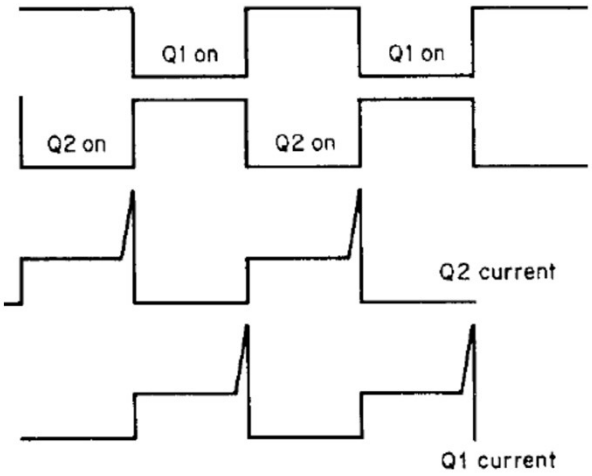
- Single or two-transistor transformer coupled, self-oscillating circuits.
- Saves the space and cost of a PWM chip.
- A transformer coupled feedback oscillator through separate winding on the transformer provides output power referenced to any desired DC voltage.

Royer Oscillator Housekeeping Supply



Waveforms





Royer Oscillator Operation

- One of the earliest applications of transistors to power electronics.
- It was conceived in 1955.
- It is a push-pull circuit with positive feedback from the collectors to the base windings to keep it oscillating.
- The positive feedback can be seen from the dots on the collector and base windings.

Royer Oscillator Operation

- Assume that Q1 is “on” and is in saturation. The no-dot end of the primary *Np*1 is positive, and hence the no-dot end of the base winding *Nb*1 is also positive. Voltage across *Np*1 is Vdc (assuming negligible *Vce* drop).
- *Np*1 delivers output current to the load via *Ns*1 and also enough current to the *Q*1 base via *Nb*1 and *R*1 to keep *Q*1 “on” and in saturation at the maximum current reflected into the primary by the minimum *Ro*.

Royer Oscillator Operation

- The transformer core is made of material with a square hysteresis loop.
- Assume that when *Q*1 turned "on" initially, the core was at point *C* on its hysteresis loop.
- With a voltage *V*dc across *Np*1, the rate of change of flux density in the core is given by Faraday's law as

$$\frac{dB}{dt} = \frac{Vdc \times 10^{+8}}{N_{p1} A_e}$$

Royer Oscillator Operation

- The core moves up the hysteresis loop from negative saturation to positive saturation.
- The time required for this is given as

$$T1 = \frac{T}{2} = \frac{dBN_{p1} A_e \times 10^{-8}}{V_{\text{dc}}}$$
$$= \frac{2B_s N_{p1} A_e \times 10^{-8}}{V_{\text{dc}}}$$

Royer Oscillator Operation

- When the core has reached point *E*, it is saturated, its permeability is close to unity, and coupling between the *Q*1 collector and base windings suddenly drops to zero. The *Q*1 base current quickly drops to zero and *Q*1 collector voltage starts rising.
- A small residual air coupling from the dot end of *Np*1 to the dot end of *Nb*2 starts turning *Q*2 "on."

Royer Oscillator Operation

- A positive feedback from the *Np*2 to the *Nb*2 winding speeds up the turn "on" process until *Q*2 is fully "on."
- When *Q*1 was "on," the no-dot end of *Np*1 was positive and the core moved up the hysteresis loop.
- With *Q*2 "on," the dot end of *Np*2 is positive and the core is driven back down the hysteresis loop along the path EGHBA.

Royer Oscillator Operation

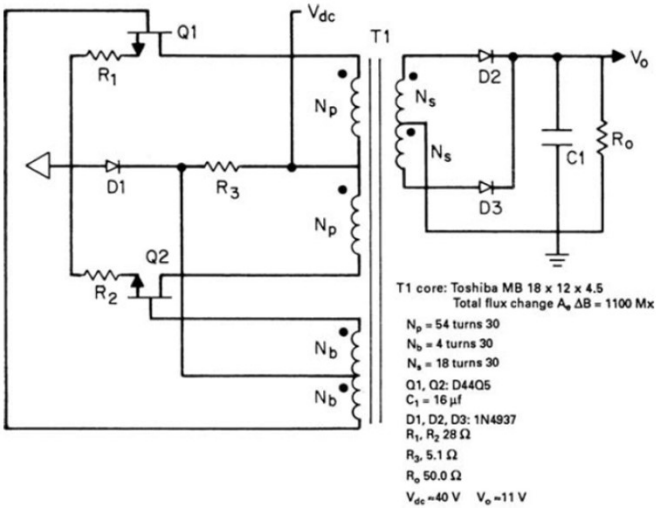
- The preceding cycles repeat and the circuit oscillates at a frequency given by

$$F = \frac{1}{T} = \frac{V_{dc} \times 10^{+8}}{4 B_s N_p A_e}$$

- The function of resistor *R*3 is to start the circuit oscillating.

- The transistor with the highest gain will be the one to turn “on” first.
- The base resistors serve to limit base current that may be excessive at high temperature and cause long transistor storage delay.
- Collector current may be limited with emitter resistors.

A typical Royer oscillator



A typical Royer oscillator

- A typical Royer oscillator DC/DC converter for 2.4-W output operating from 38 V DC—the minimum specified input for a telephone industry power supply.
- The Royer oscillator is clearly low in parts count.
- The low efficiency of only 50.6% is a consequence of the dissipation due to the current spikes at turn “on” and turn “off.”

Thanks