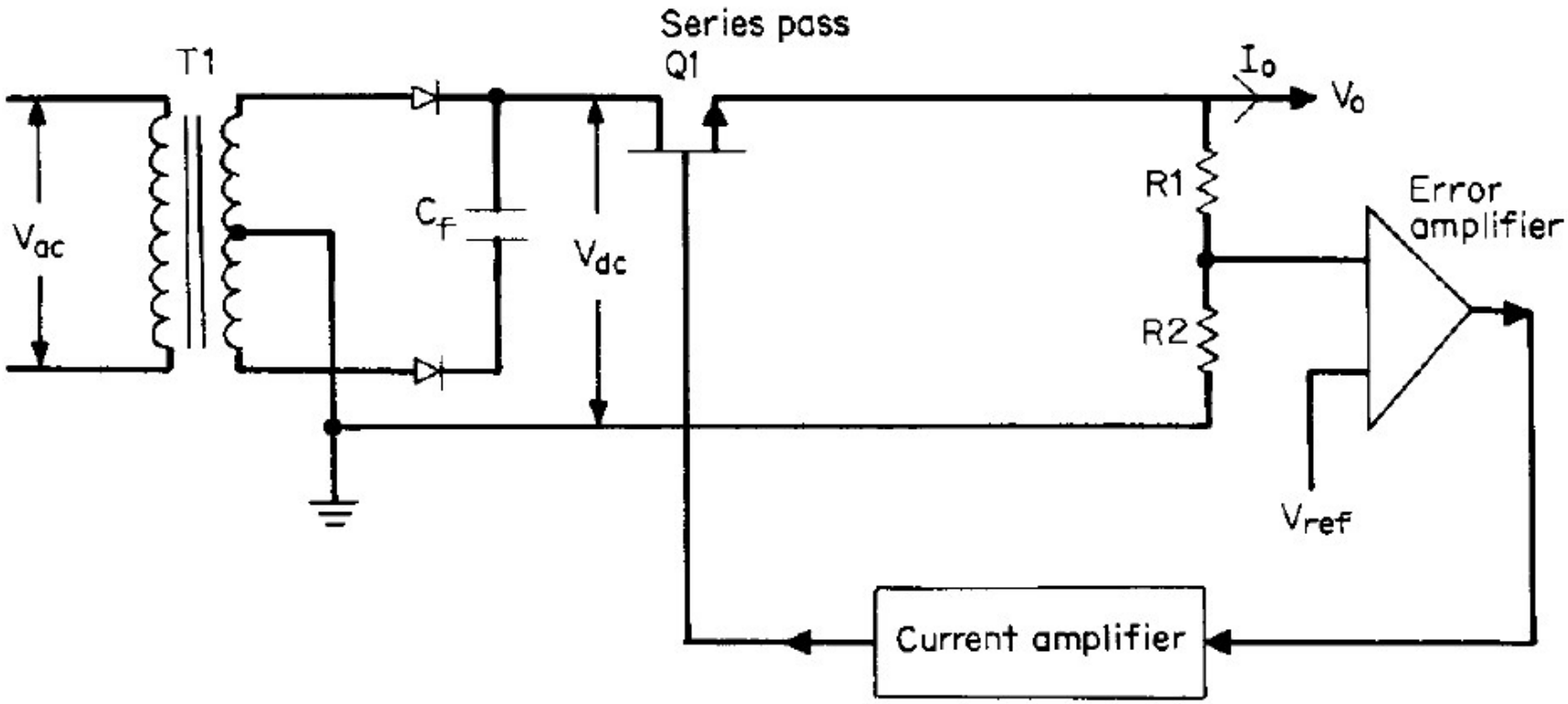
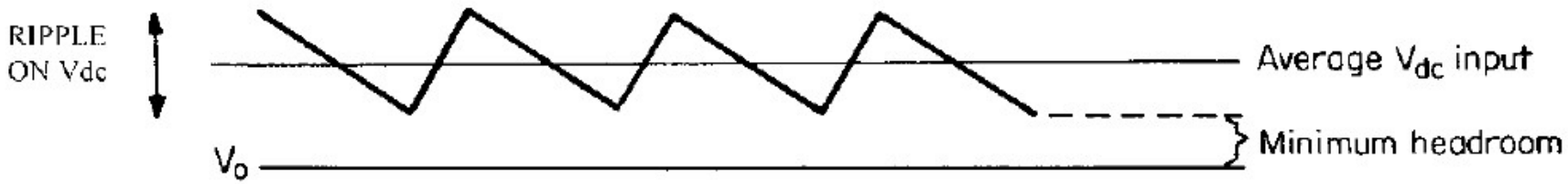
Linear Regulator

Dr. Tahir Izhar

The linear regulator Circuit



Input and Output Waveforms



The waveform shows the ripple normally present on the unregulated DC input (V_{dc}).

A minimum input-output voltage differential (headroom) of at least 2.5 V is required

Linear Regulator Limitations

- A lower regulated voltage from a higher input.
- No isolation between input and output.
- 50-Hz transformer high weight and volume.
- The efficiency is very low.
- Large heat sinks required.

Output voltage and Efficiency

V_o	I_o, A	$V_{dc(min)'}$ V	$V_{dc(max)'}$ V	Headroom, max, V	$P_{in(max)'}$ W	$P_{out_{(max)'}}$ W	Dissipation $Q1_{max}$	Efficiency, % $P_o/P_{in(max)}$
5.0	10	7.5	10.1	5.1	101	50	51	50
15.0	10	17.5	23.7	8.7	237	150	87	63
30.0	10	32.5	44.0	14	440	300	140	68

at lower DC output voltages the efficiency will be very low

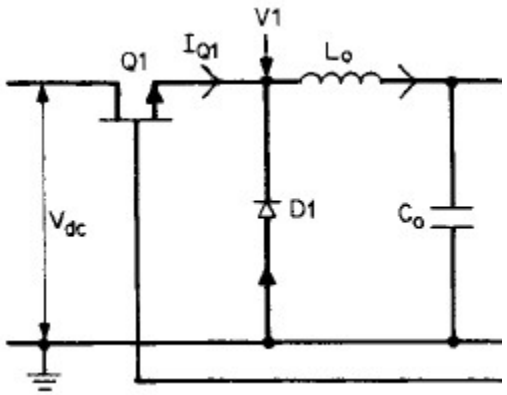
Buck Regulator Design

Lecture-4

Dr. Tahir Izhar

Inductor Design

- The output inductor and capacitor are considered as low pass filter.
- The Inductor tends to maintain the current constant during the switching action.
- The Buck converter is preferably operated in continuous mode.



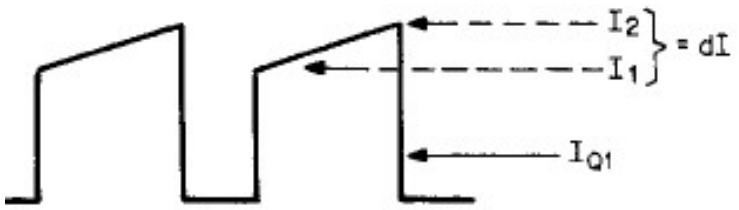
Inductor Design

- The mode depends on the size of the inductor and the load current.
- To ensure continuous mode of operation, the inductor is design for a minimum value of the load current.
- The minimum value of load current is usually taken as 10% of the rated load current

$$I_o(\min) = 0.1 I_{on}$$

The inductor current ramp is

$$dI = (I_2 - I_1).$$



Inductor Design

The onset of the discontinuous mode occurs at a DC current of half this amplitude, $dI = (I_2 - I_1)$.

$$I_o(\min) = 0.1 I_{\text{on}} = (I_2 - I_1)/2$$

Also

$$dI = V_L T_{\text{on}}/L = (V_1 - V_o) T_{\text{on}}/L$$

where V_1 is voltage at the output of Q_1 and is very close to input DC voltage, V_{dc},
then

$$L = \frac{(V_{\text{dc}} - V_o) T_{\text{on}}}{dI} = \frac{(V_{\text{dc}} - V_o) T_{\text{on}}}{0.2 I_{\text{on}}}$$

Inductor Design

Where

$$T_{on} = V_o T / V_{dc}$$

and

V_{dcn} and I_{on} are nominal values,

then

$$L = \frac{5(V_{dcn} - V_o)V_o T}{V_{dcn} I_{on}}$$

Thus, if L is selected from the above Eq., then

$$dI = (I_2 - I_1) = 0.2 I_{on}$$

Conclusions

- I_{on} is the center of the inductor current ramp at nominal DC output current.
- Since the inductor current will swing ±10% around its center value I_{on} , the inductor must be designed so that it does not significantly saturate at a current of at least 1.1 I_{on}.
- The optimum design of inductors will be discussed in latter sections.

Conclusions

- The current must not reach zero for the full range of load currents, as continuous mode is required
- Thus the inductor must support a DC current component and should be designed as a choke.
- Well-designed chokes have a low, but relatively constant, inductance under AC voltage stress and DC bias conditions.

Conclusions

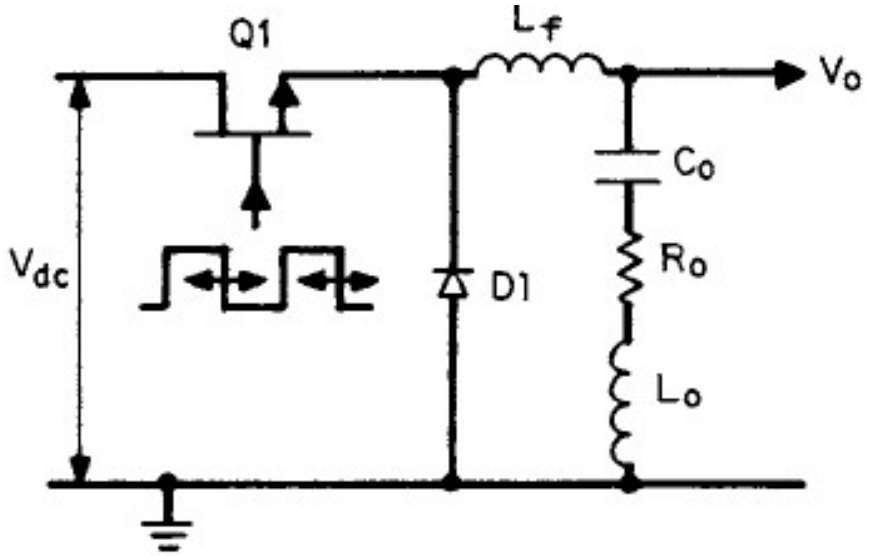
- Typically chokes use either gapped ferrite cores or composite cores of various powdered ferromagnetic alloys, including powdered iron or Permalloy, a magnetic alloy of nickel and iron.
- Powdered cores have a distributed air-gap because they are made from a suspension of powdered ferromagnetic particles, embedded in a nonmagnetic carrier to provide a uniformly distributed air-gap.

Conclusions

- The inductor value calculated above must be made so that it does not saturate at the specified peak current (110% of I_{on}).
- To remain in continuous conduction, the minimum current must not go below 10% of the rated I_{on}. Below this the load regulation will degrade slightly.

Output Capacitor Design

- C_o will not be an ideal capacitor.
- It will have a parasitic resistance R_o and inductance L_o in series with its ideal pure capacitance C_o.
- The ripple current flows into the capacitor C_o.



Output Capacitor Design

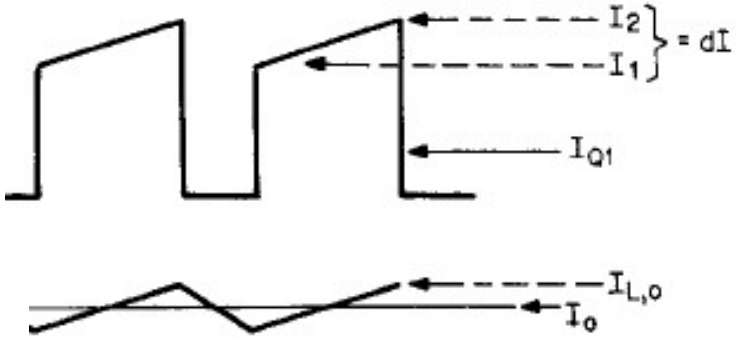
- Below about 500 kHz, L_o can normally be neglected and the output ripple is mainly determined by R_o and C_o.
- C_o is a relatively large electrolytic.
- The ripple voltage component contributed by C_o is small compared with that contributed by R_o.
- Ripple component generated by R_o is proportional to the peak-to-peak inductor ramp current and that due to C_o is proportional to the integral of that current so they are not in phase.
- However, for a worst-case comparison we can assume that they are in phase.

Ripple Due to Capacitance Part

- The ripple current is positive from the center of the "on" time to the center of the "off" time or for one-half of a period.
- This current produces a ripple voltage across the pure capacitance part C_o.
- The average value of this triangle of current is

$$(I_2 - I_1)/4$$

This current produces a ripple voltage across the capacitance C_o.



Ripple Due to Capacitance Part

The ripple produced by C_o can be given as

$$V_{cr} = \frac{It}{C_o}$$

The capacitor current is

$$I=(I_2 - I_1)/4$$

Assuming the minimum load is to be 10%

$$dI = (I_2 - I_1) = 0.2I_{on}$$

$$t=T/2$$

$$V_{cr}=0.2I_{on}T/8C_o$$

Ripple Due to ESR, R_o Part

The ripple produced by R_o can be given as

$$R_o = \frac{V_{or}}{I_2 - I_1} = \frac{V_{or}}{0.2I_{on}}$$

Design Example

Assume a design for a 25-kHz buck regulator with a step down from 20 V to 5 V with a load current I_{on} = 5A. The required ripple voltage to be below 50 millivolts with continuous conduction down to 10% load. The typical ESR/capacitance relationship is $R_o C_o = 50 \times 10^{-6}$.

Solution

Assuming the minimum load is to be 10%, then *Io*(min) = 0.1*I*on = 0.5 A.

$$L = \frac{5(V_{\text{dcn}} - V_o)V_o T}{V_{\text{dcn}} I_{\text{on}}}$$

$$= \frac{5(20-5)5 \times 40 \times 10^{-6}}{20 \times 5}$$

$$= 150\,\mu\text{H}$$

Solution

R_o can be calculated from

$$R_o = \frac{V_{or}}{I_2 - I_1} = \frac{V_{or}}{0.2 I_{on}}$$

R_o = 0.05/0.2x5

= 0.05 ohms

Solution

If we assume the majority of the output ripple voltage will be produced by the capacitor ESR (R_o), we can simply select a capacitor value such that the ESR will satisfy the ripple voltage as follows:

Using the typical ESR/capacitance relationship

$$R_o C_o = 50 \times 10^{-6}$$

Substituting the vale of R_o of 0.05 ohms in the above equation

$$C_o = 50 \times 10^{-6}/0.05 = 1000\text{uF}$$

Solution

The ripple voltage across the pure capacitance part C_o

$$V_{cr} = 0.2 I_{on} T/8C_o$$

$$I_{on} = 5A$$

$$T = 1/f$$

$$= 1/25000$$

$$= 40x10^{-6}$$

$$V_{cr} = 0.2x5x40x10^{-6}/8x1000x10^{-6}$$

$$= 0.005V$$

Comments

- The ripple component due to R_o is 50mV and due to C_o is only 5mV.
- The ripple due to the capacitance, in this particular case, is relatively small compared with that due to the ESR resistor R_o.

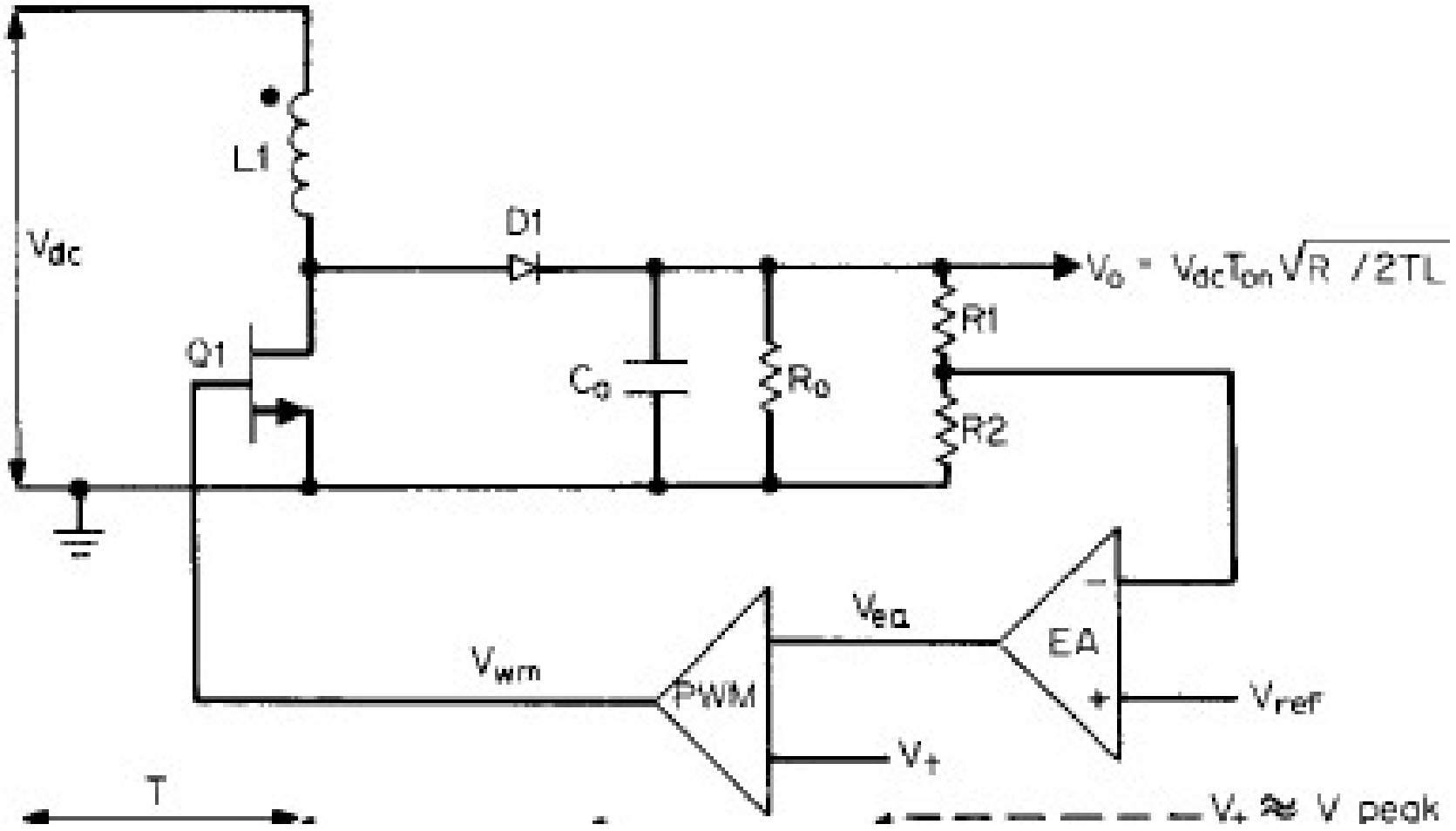
Boost Converter

Dr. Tahir Izhar

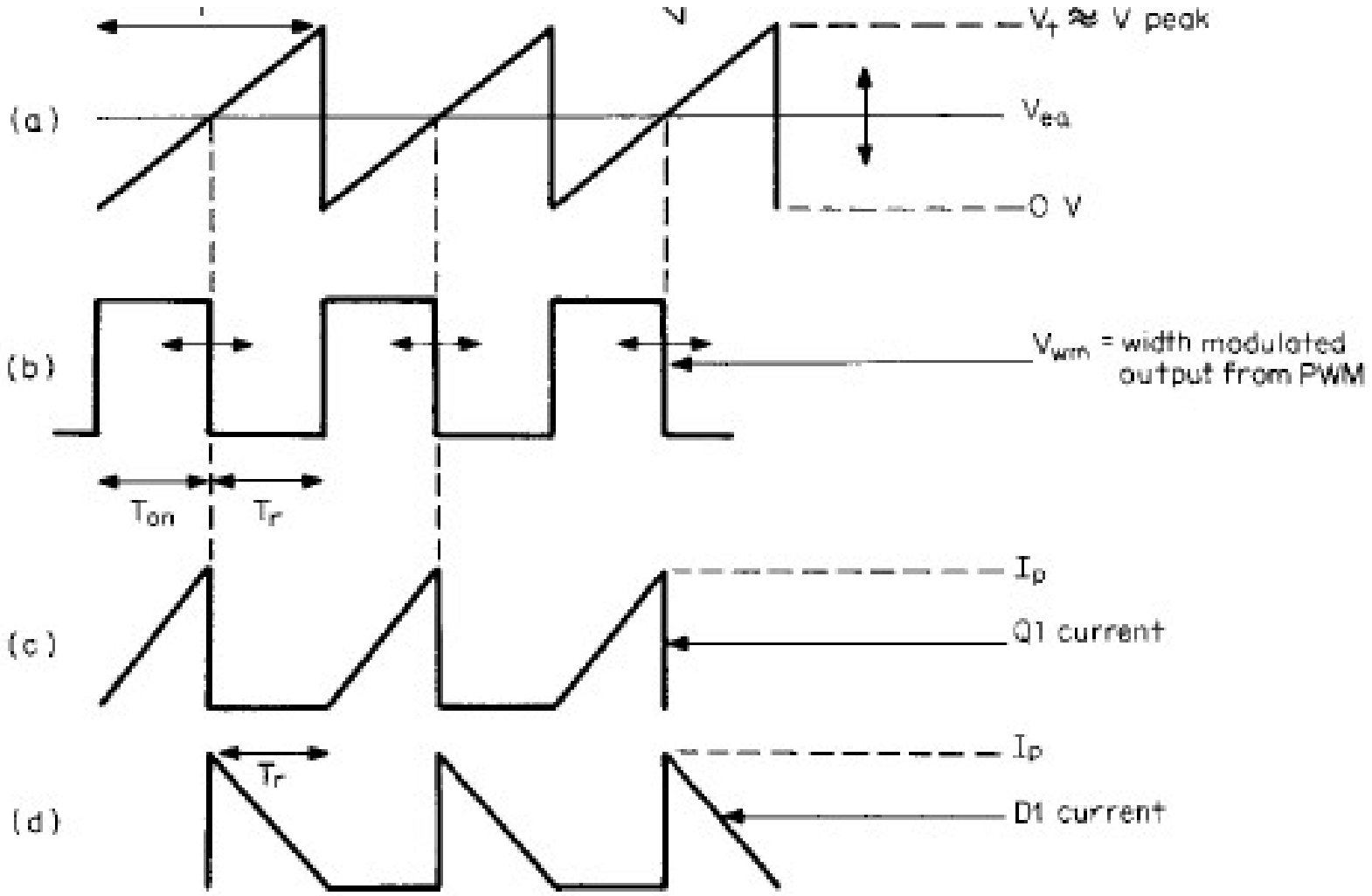
Boost Topology

- The buck regulator can only produce a lower voltage from a higher voltage.
- However, sometimes higher outputs are required.
- The boost regulator can produce a higher output voltage from a lower input voltage.
- To realized the boost converter, The Inductor, Transistor, Diode and Capacitor are rearranged.

Boost Power Supply Circuit



Waveforms


(a)
$V_t \approx V$ peak
V_{ea}
0 V
(b)
V_{wm} = width modulated output from PWM
T_{on}
T_r
(c)
I_p
Q1 current
(d)
T_r
I_p
D1 current

Operation 1/3

- When Q_1 turns “on”, V_{dc} is applied across L_1.
- D_1 is reverse biased.
- Input DC supply is disconnected from output.
- Current ramps up linearly in L_1.
- During “on” time, the output current is supplied entirely from C_o.

Operation 2/3

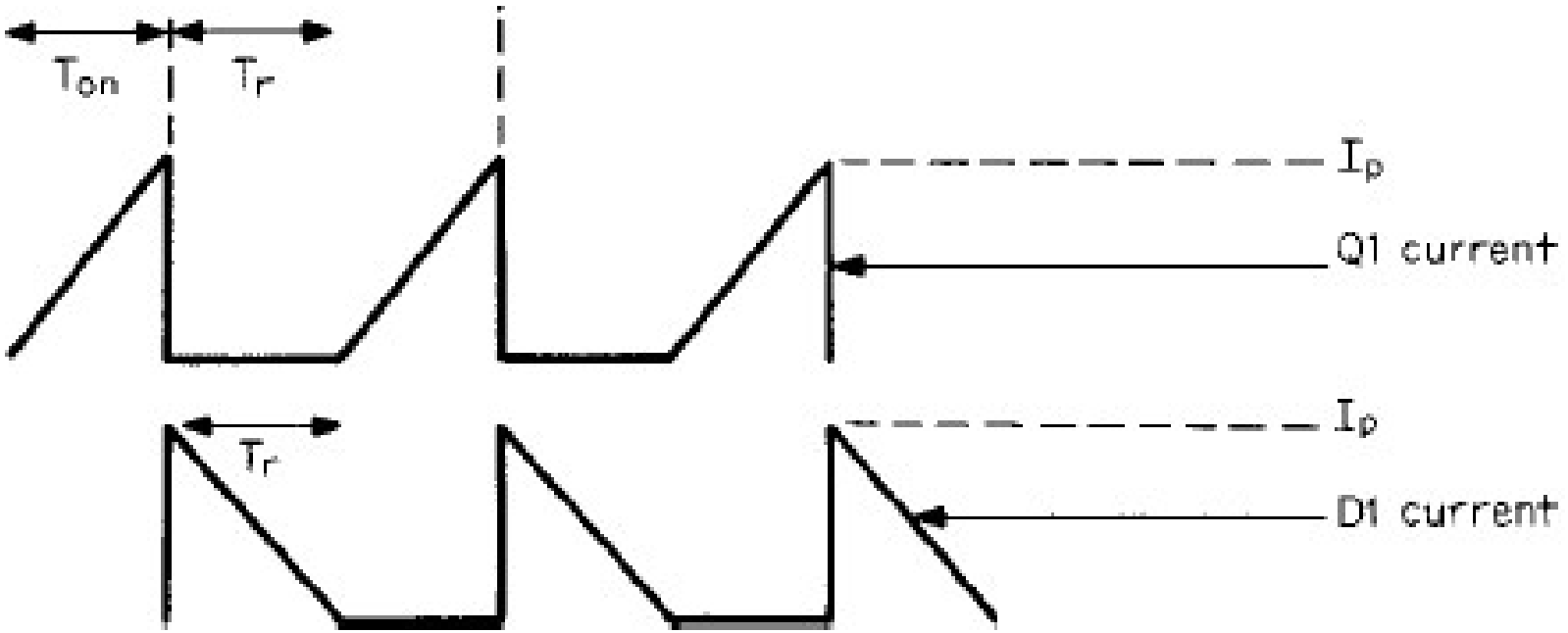
- When Q_1 turns "off," the voltage across L_1 reverses.
- V_o is "V_{dc}+V_L"
- L_1 delivers its stored energy to C_o via D_1.
- Hence C_o is *boosted* to a higher voltage than V_{dc}.
- The current is supplied to the load from V_{dc} via L_1 and D_1.

Operation 3/3

- V_o is regulated by controlling the Q_1 "on" time in a negative-feedback loop.
- If the load current increases, or the input voltage decreases, the "on" time of $Q1$ is automatically increased to deliver more energy to the load, or the converse.
- Hence, in normal operation the "on" period of $Q1$ is adjusted to maintain the output voltage constant.

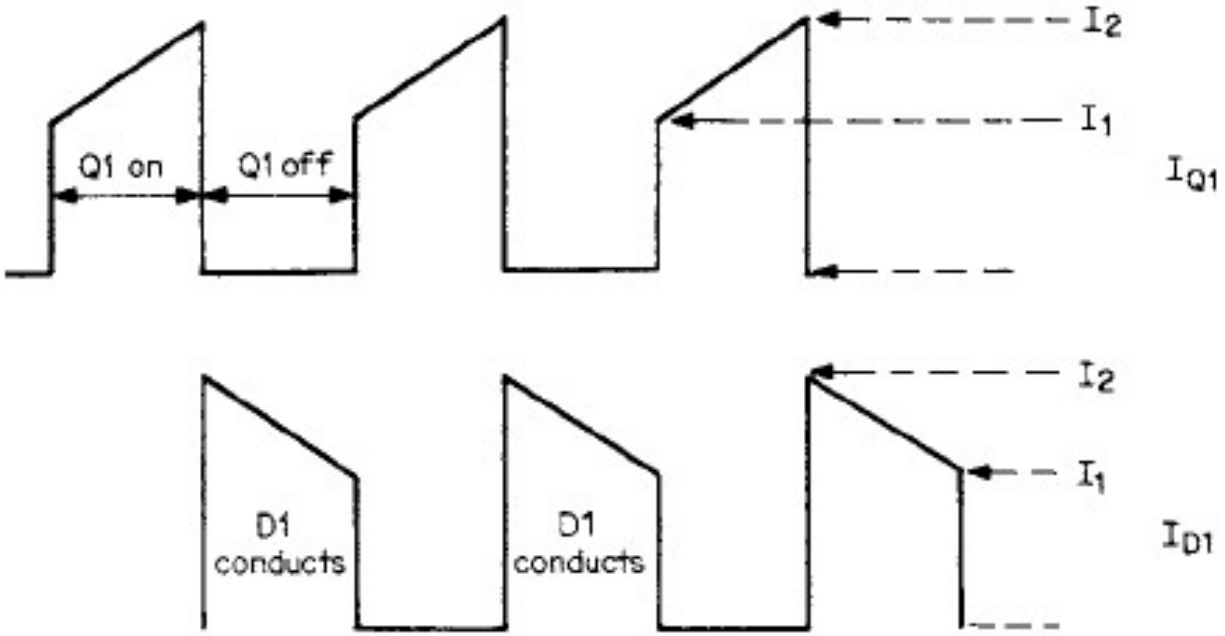
Discontinuous Mode

- ***Discontinuous mode***
  - the inductor current reaches zero at the end cycle.



Continuous Mode

- ***Continuous mode of operation***
  - current flowing in the inductor at the end cycle.



Important Points

- The boost regulator has a continuous input current but a discontinuous output current for all modes of operation.
- Hence the terms continuous and discontinuous mode refer to what is going on in the inductor.
- There is a dramatic difference in the transfer function between the two modes of operation that significantly changes the transient performance and stability which will be explained later.

Analysis[1/7]

When Q_1 turns "on," the current ramps up linearly in L_1 to a peak value I_p.

$$I_p = V_{dc} T_{on} / L1$$

Thus energy is stored in L_1, and at the end of the "on" period

$$E = 0.5 L_1 I_p^2$$

Analysis[2/7]

- If the current through L_1 has fallen to zero before the next Q_1 turn “on”, all the energy stored in L_1 during the previous Q_1 “on” period will have been delivered to the output load, and the circuit is said to be operating in the discontinuous mode.
- The energy *E* delivered to the load per cycle, divided by the period *T*, is the output power.

Analysis[3/7]

Output Power to the load from L_1 alone (assuming for the moment 100% efficiency) would be

$$P_L = \frac{{}^1\!/_2 L (I_p)^2}{T}$$

Analysis 4/7

During Q_1 "off", the current in L_1 is ramping down toward zero, and the same current is also flowing from the supply V_{dc} via L_1 and D_1 and is contributing to the load power P_{dc}. This is equal to the average current during T_r multiplied by its duty cycle and V_{dc} as follows:

$$P_{dc} = V_{dc} \frac{I_p}{2} \frac{T_r}{T}$$

Analysis[5/7]

The total power delivered to the load is then the sum of the two parts as follows:

$$P_t = P_L + P_{dc} = \frac{{}^1\!/_2 L_1 (I_p)^2}{T} + V_{dc}\frac{I_p}{2}\frac{T_r}{T}$$

Putting $I_p = V_{dc} T_{on}/L1$

$$P_t = \frac{({}^1\!/_2 L_1)(V_{dc} T_{on}/L_1)^2}{T} + V_{dc}\frac{V_{dc} T_{on}}{2L_1}\frac{T_r}{T}$$

$$= \frac{V_{dc}^2 T_{on}}{2T L_1}(T_{on} + T_r)$$

Analysis[6/7]

To ensure that the current in L_1 has ramped down to zero before the next Q_1 turn "on",

(T_{on} + T_r) is set to kT,

where k is a fraction less than 1.

Then

$$P_t = \frac{V_{dc}^2 T_{on}}{2TL_1}(kT)$$

Analysis[7/7]

But for an output voltage V_o and output load resistor R_o

$$P_i = \frac{V_{dc}^2 T_{on}}{2TL_1}(kT) = \frac{V_o^2}{R_o}$$

or

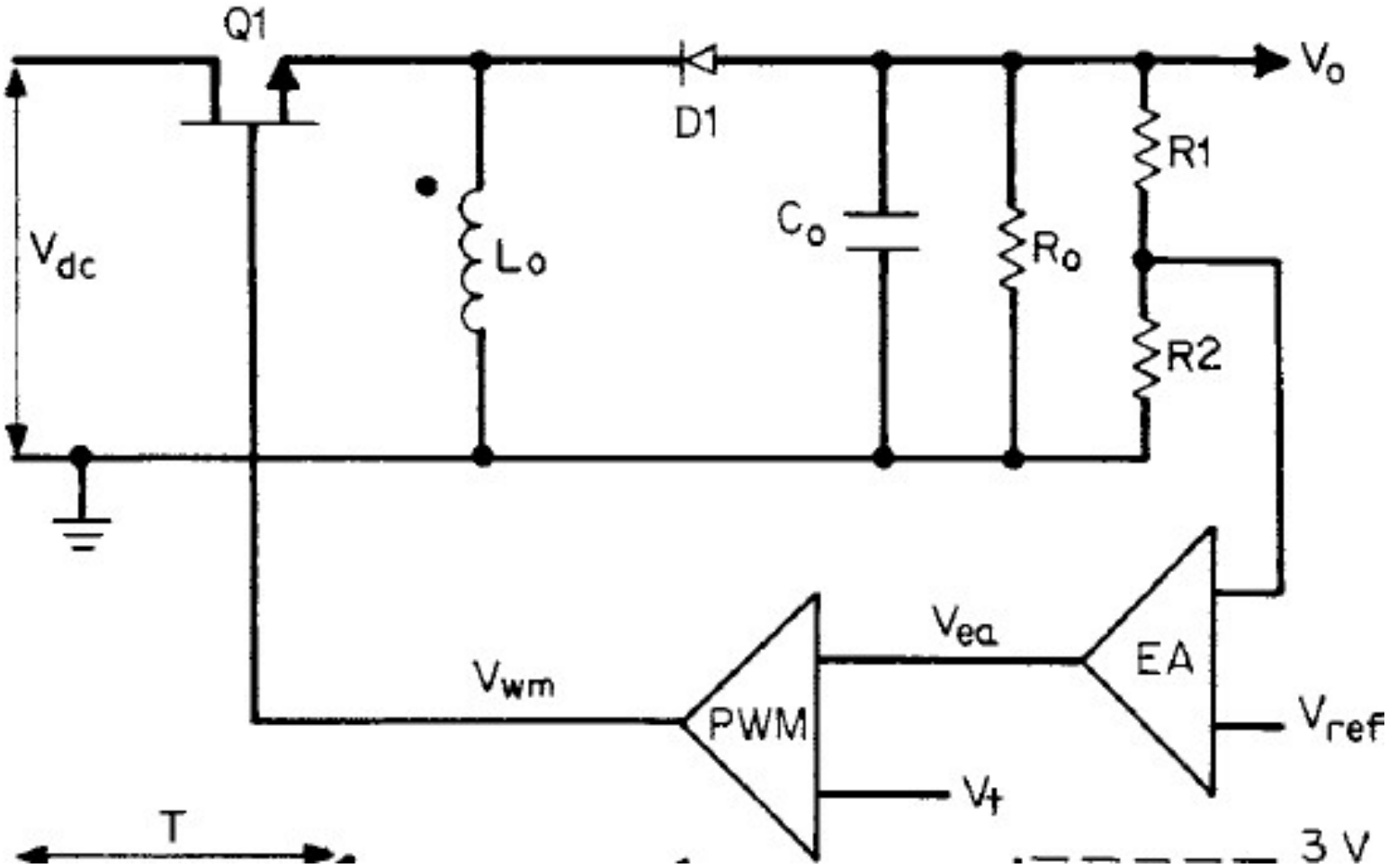
$$V_o = V_{dc}\sqrt{\frac{kR_o T_{on}}{2L1}}$$

As V_{dc} and R_o go down or up, the loop will increase or decrease *T*on so as to keep V_o constant.

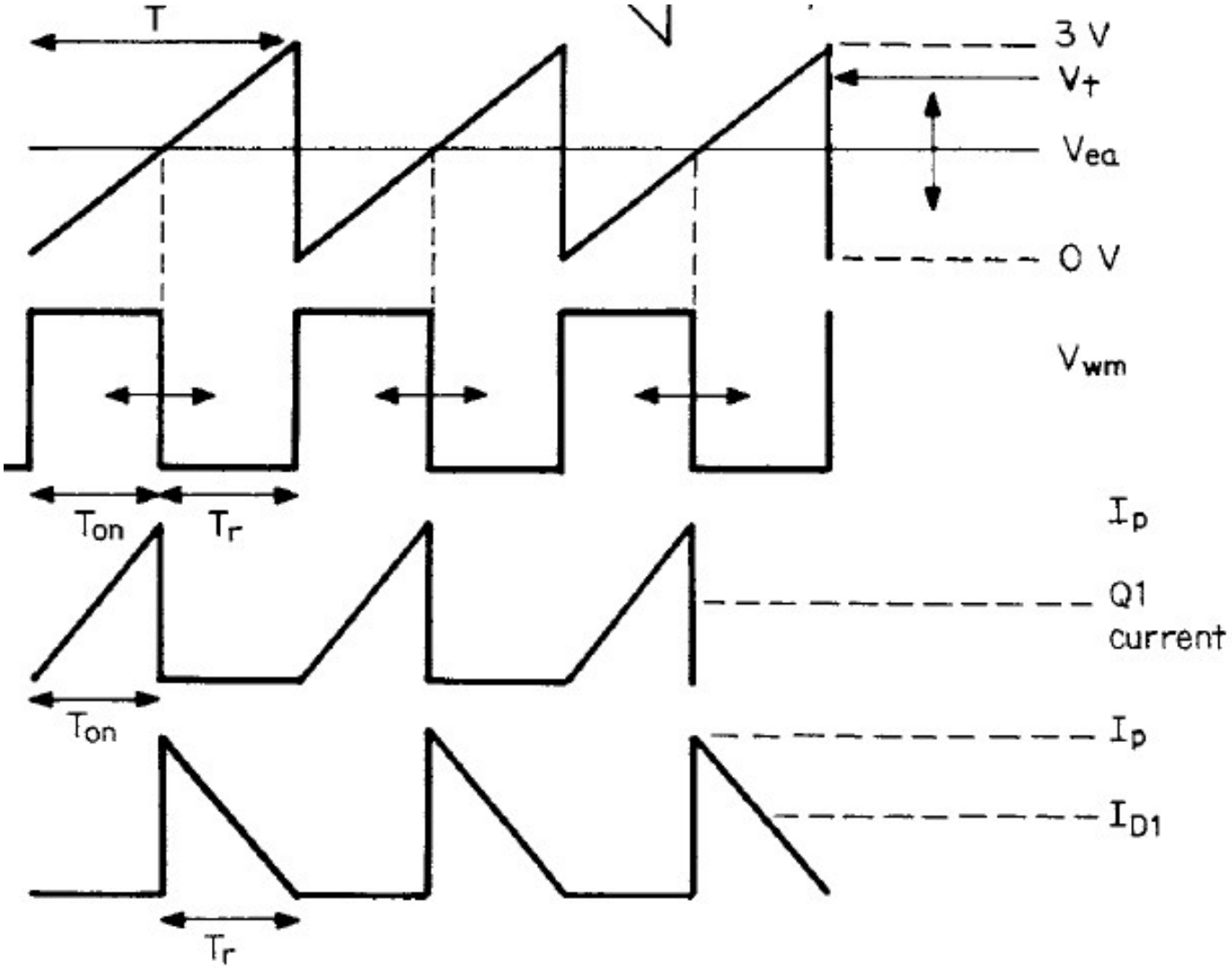
Polarity Inverting Converter

Dr. Tahir Izhar

Converter Circuit



Waveforms



Analysis

$$P_t = \frac{{}^1/_2 L_o I_p^2}{T}$$

$$P_o = \frac{V_o^2}{R_o} = \frac{{}^1/_2 L_o I_p^2}{T}$$

and for $I_p = V_{dc} T_{on} / L_o$,

$$V_o = V_{dc} T_{on} \sqrt{\frac{R_o}{2TL_o}}$$

Isolated Converter Topologies

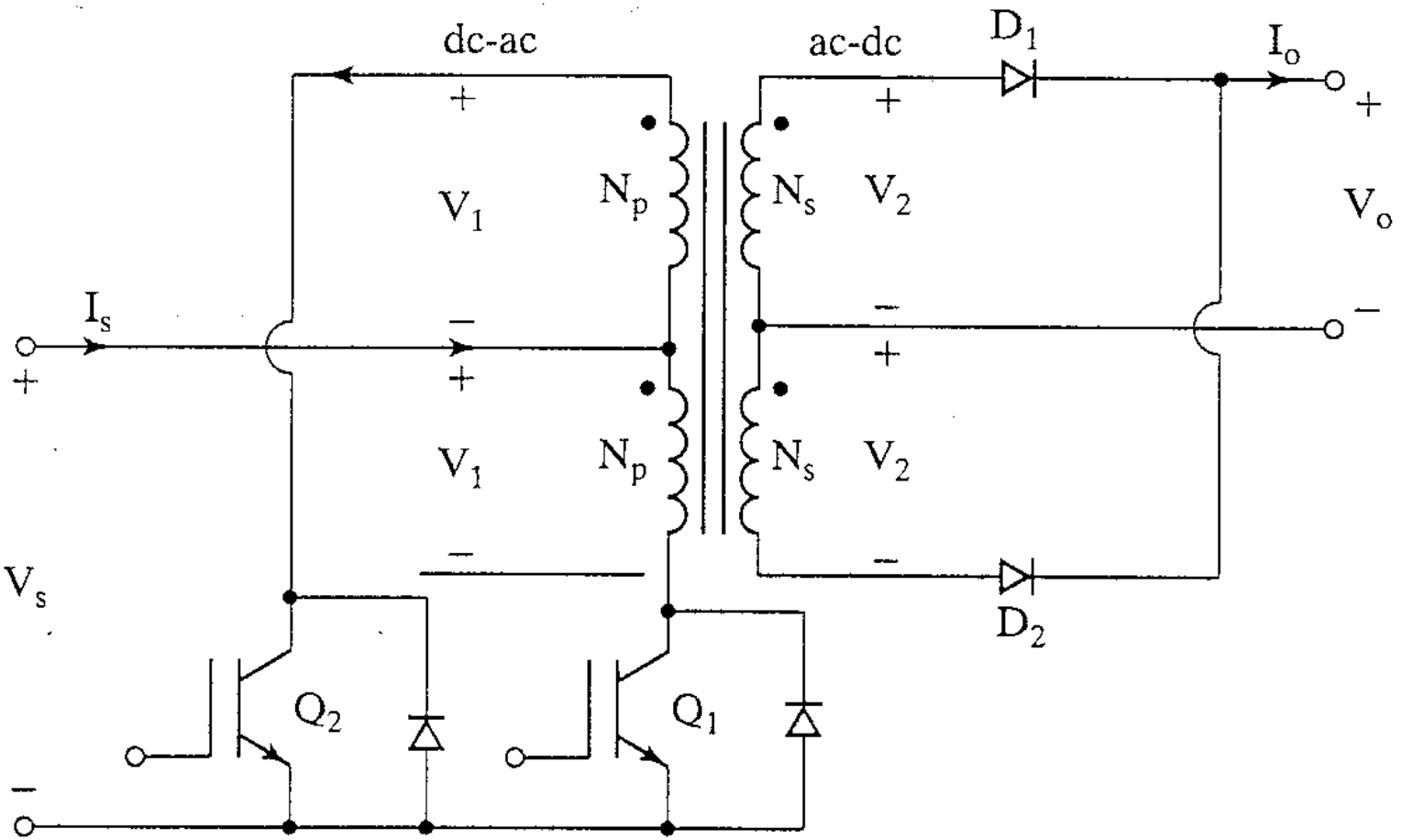
Push-Pull Topology

Dr. Tahir Izhar

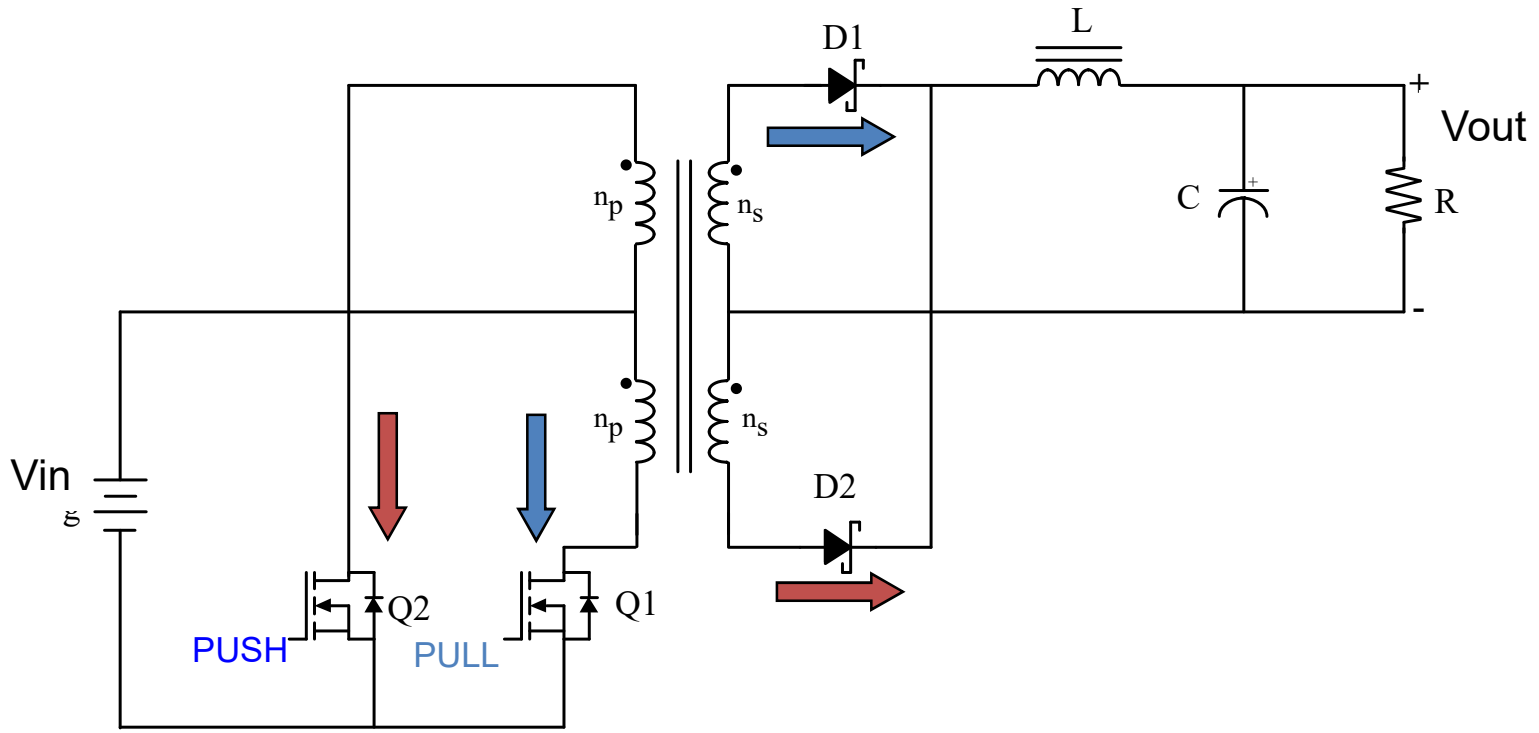
Isolated SMPS

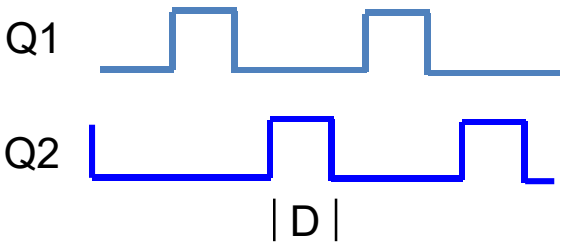
- Input terminals are isolated from output terminals.
- High frequency transformer is used for isolation.
- Control circuit is powered from input or from the output but the isolation is maintained through signal pulse transformer or opto-isolator.

Push-Pull Topology



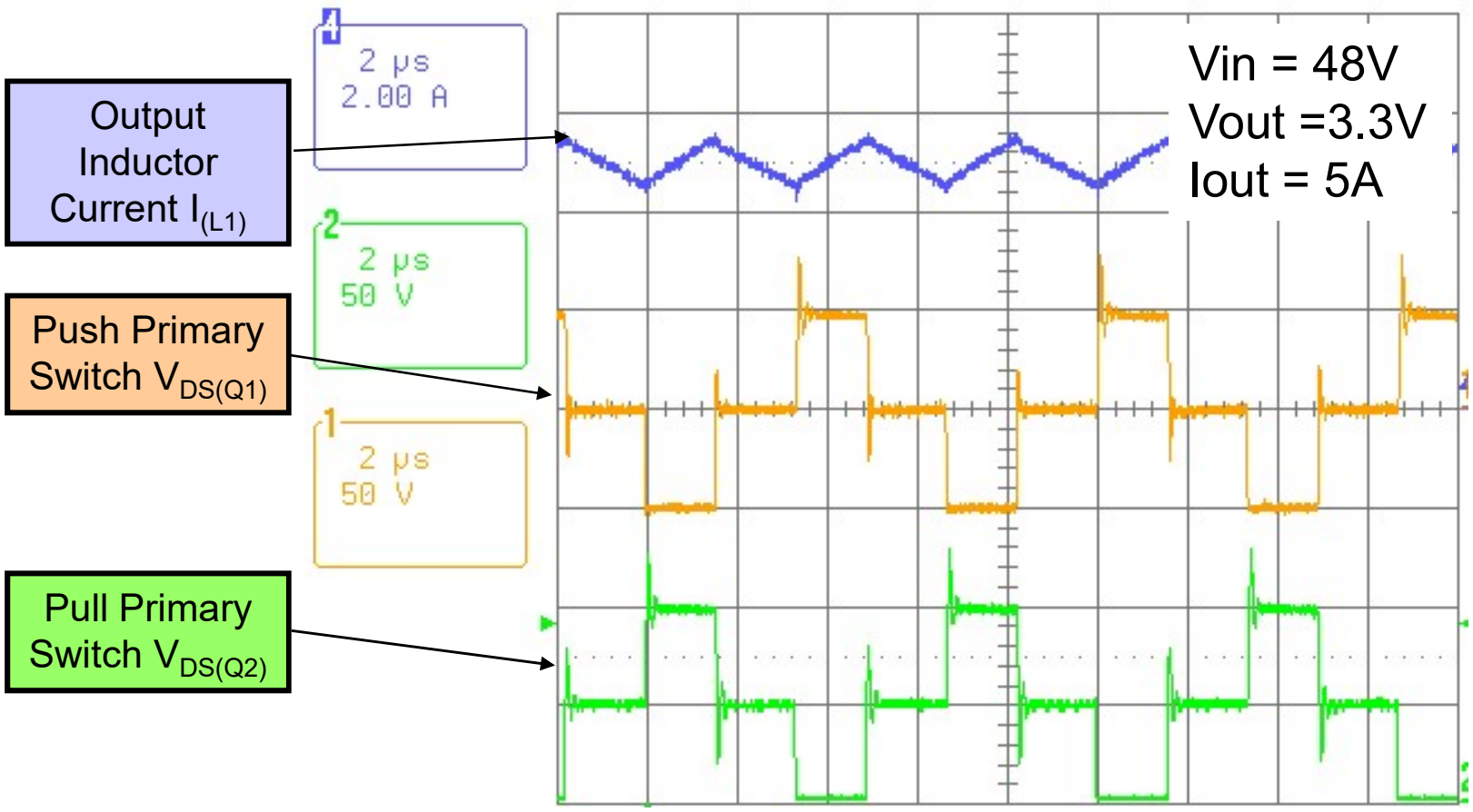
Push-Pull Topology





$$Vout = Vin \times D \times \frac{Ns \times 2}{Np}$$

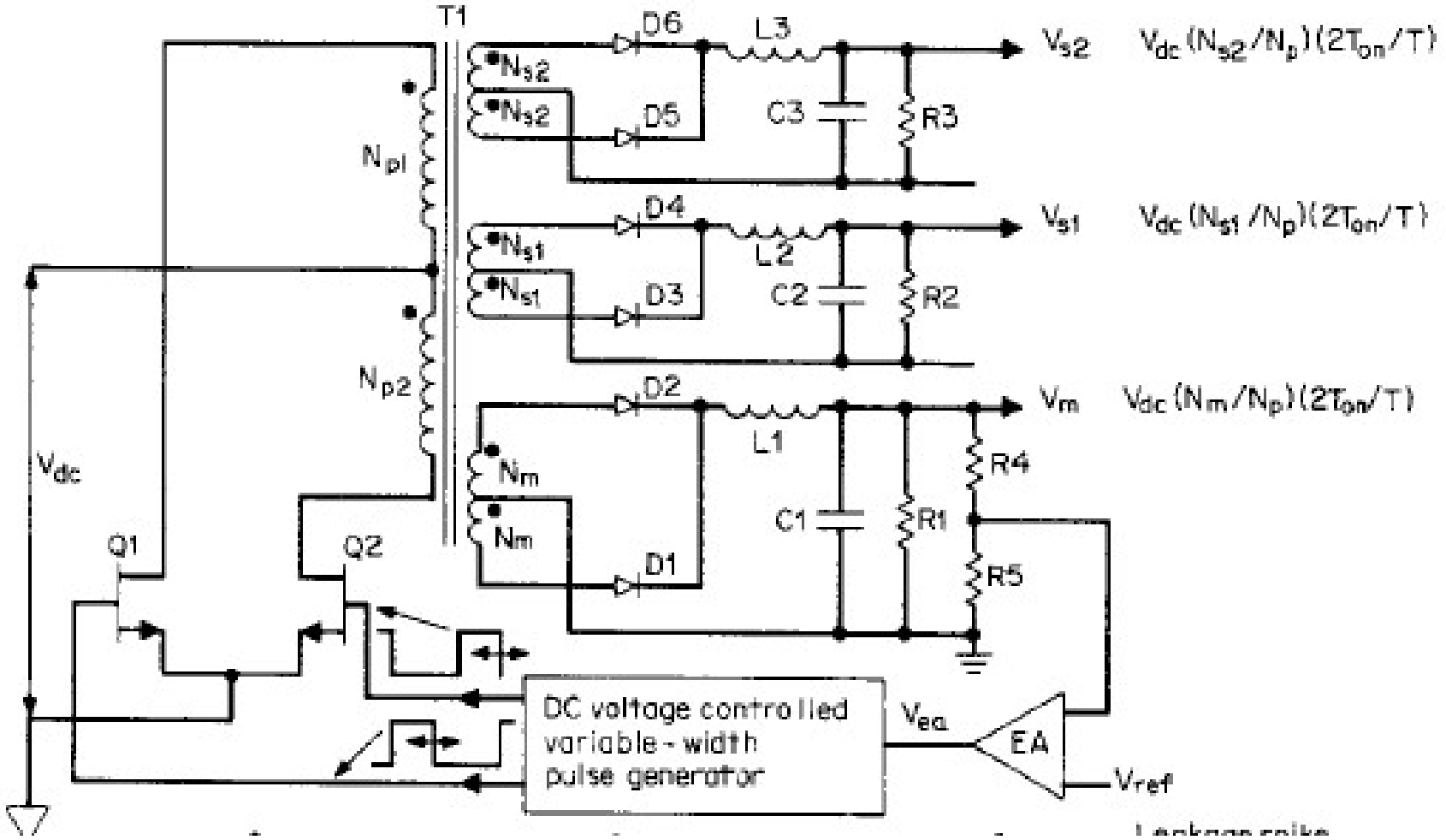
Push-Pull Switching Waveforms



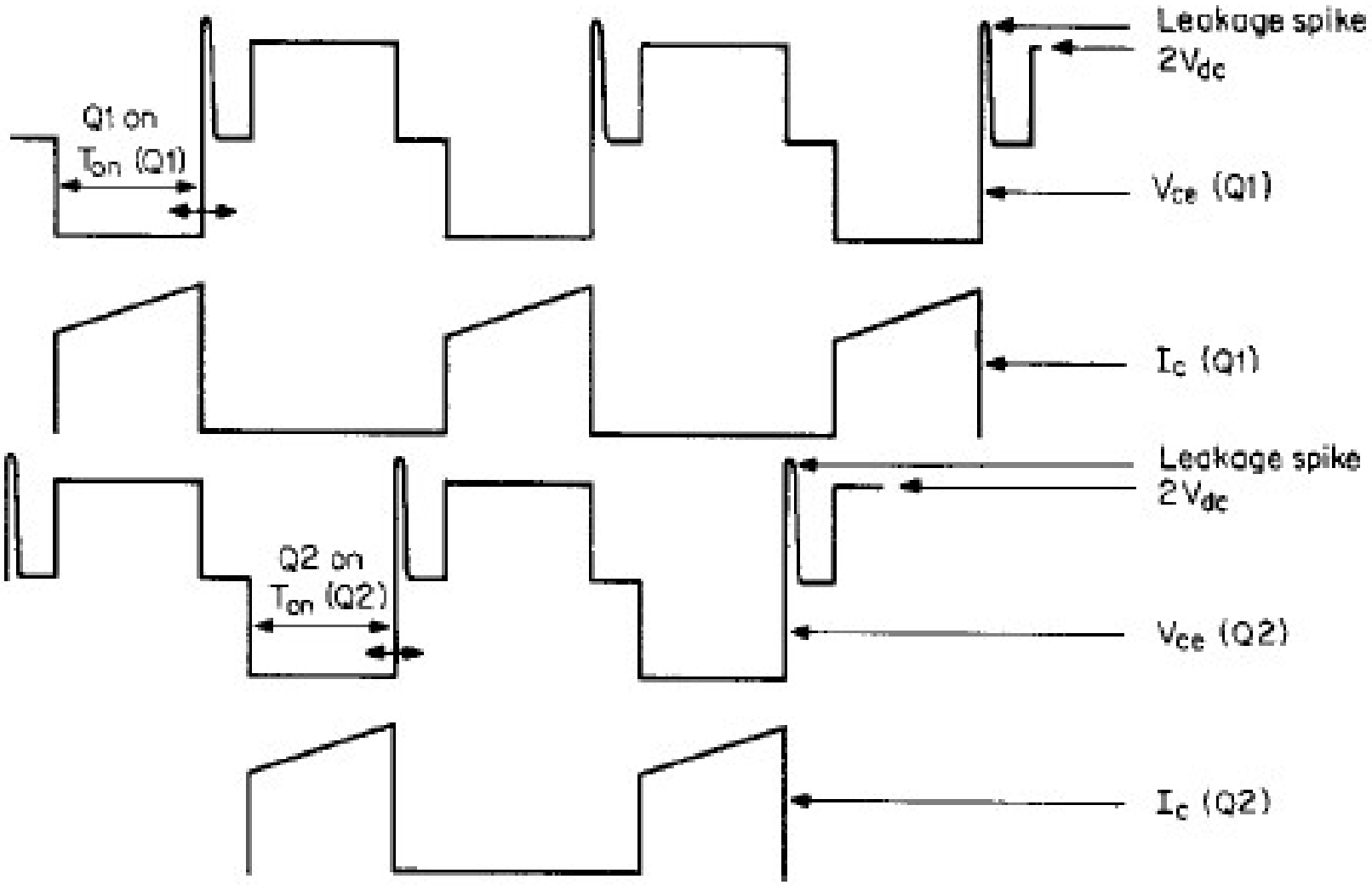
Push-Pull Characteristics

- A Push-Pull Converter is a Buck type converter with a dual drive winding isolation transformer
- Push-Pull transformers and filters are much smaller than standard Forward converter filters
- Voltage Stress of the Primary Switches is: Vin *2
- Voltage Step-down or Step-up
- Multiple Outputs Possible
- Low Output Ripple Current
- Lower Input Ripple Current
- Simple Gate Drive (dual)
- Large Achievable Duty Cycle Range

Multiple Outputs Push Pull Circuit



Waveforms


Leakage spike
$2V_{dc}$
Q1 on
T_{on} (Q1)
V_{ce} (Q1)
I_c (Q1)
Leakage spike
$2V_{dc}$
Q2 on
T_{on} (Q2)
V_{ce} (Q2)
I_c (Q2)

Multiple Outputs

- It consists of a transformer *T*1 with multiple secondaries.
- Each secondary delivers a pair of 180^{o} out-of-phase square-wave power pulses.
- The amplitude is fixed by the input voltage and the number of primary and secondary turns.

Multiple Outputs

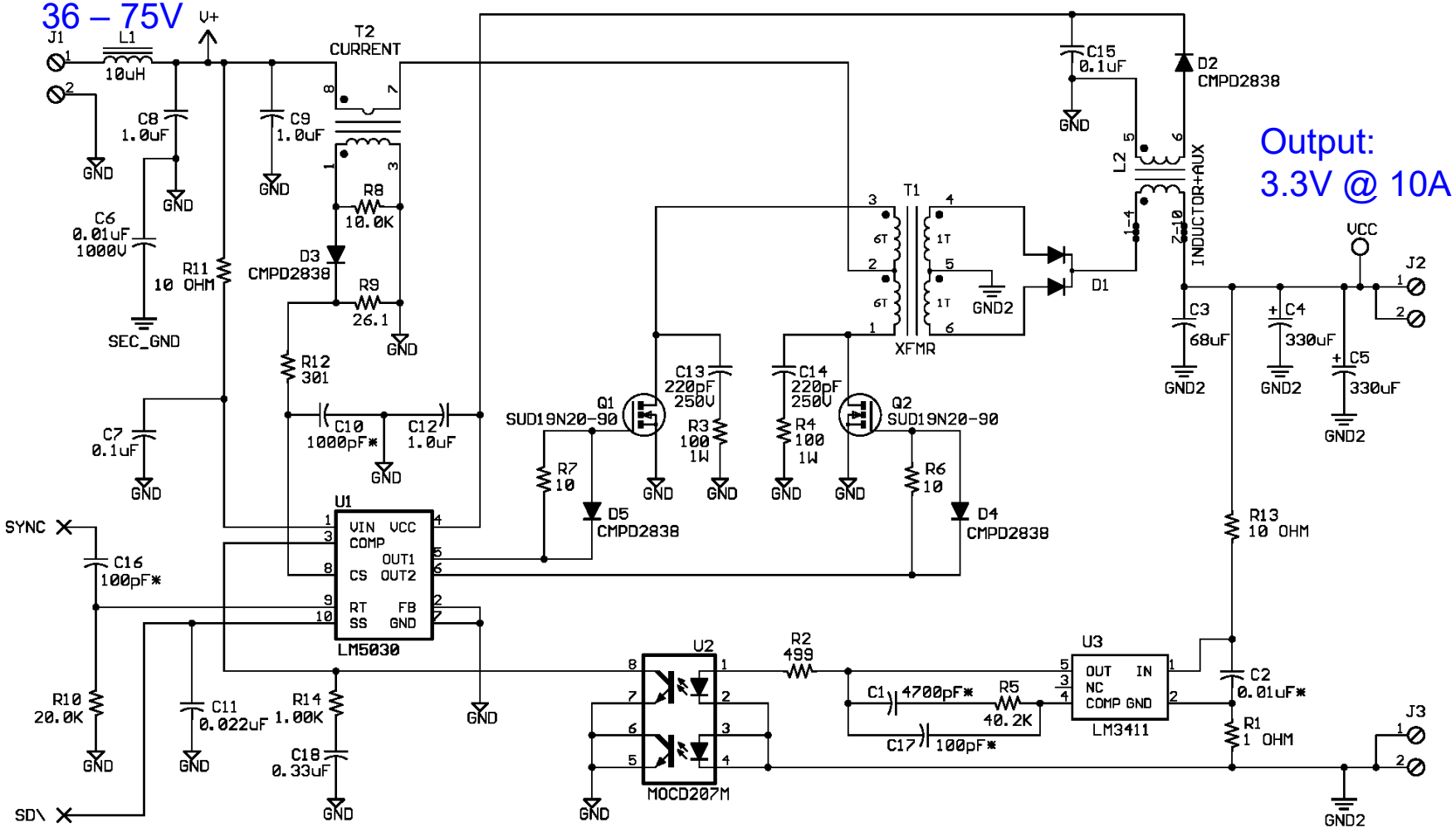
- The pulse widths for all secondaries are identical, as determined by the control circuit and the negative-feedback loop around the *master* output.
- The control circuit is similar to the buck and boost regulators except that two equal adjustable pulse-width, 180◦-out-of-phase pulses drive the bases of $Q1$, $Q2$.
- The additional secondaries $Ns1$, $Ns2$ are referred to as *slaves.*

LM5030 Push-Pull Demo Board

36V-75Vin to +3.3V @ 10A

Input:
36 – 75V

Output:
3.3V @ 10A



LM5030 Push-Pull Demo Board

Performance:
Input Range: 36 to 75V
Output Voltage: 3.3V
Output Current: 0 to 10A
Board Size: 2.3 x 2.3 x 0.45
Load Regulation: 1%
Line Regulation: 0.1%
Current Limit

Measured Efficiency: 84.5% @ 5A
82.5% @10A