Capacitance Model for Magnetic Devices

Thomas Duerbaum

Philips Research Laboratories
Weisshausstrasse 2
D-52066 Aachen
Germany

Abstract—Magnetic components are essential for switched-mode power supplies. The designer has to understand the parasitic behaviour of these non-standard devices. Besides the losses and leakage inductance a model should include the capacitive behaviour. The flat model describes the electrostatics of magnetics consisting of two layers. This paper demonstrates the extension towards an arbitrary number of layers. It will be shown how the resulting large number of capacitors in case of the layer based capacitance model can analytically be reduced to the minimum number needed for a correct description.

I. INTRODUCTION

A strong trend towards miniaturisation can be seen in all kind of power supplies. Smaller power supplies have to work at higher switching frequencies in order to reduce the size of passive components. The effects caused by parasitics are more pronounced at these higher switching frequencies. In case of hard-switched topologies, like the flyback converter, the turn-on losses associated with parasitic capacitances limit the maximum switching frequency.

Within the literature a lot of papers can be found dealing with the modelling of losses (e.g. [1] in case of core losses) and leakage inductance. Only a few papers exist that cover the capacitive characteristics of magnetic components. More often the capacitance behaviour is modelled by placing 2-3 capacitors more or less arbitrarily around the finished loss/leakage model.

J.-P. Keradec, et al. present a more rigorous approach in [2,3]. They consider the transformer as a system with three independent voltages. An equivalent circuit with six different capacitances describes such a system [2]. Fig. 1 depicts the resulting equivalent circuit. The complete equivalent circuit in [3] includes the magnetic coupling and loss mechanisms. An experimental method in [3] describes the determination of the equivalent circuit elements. Within the literature the so called 'flat model' is used to derive the values of the six capacitors in case of magnetic components consisting of two layers only. However, practical magnetic components normally exhibit more than two layers. The author describes a possibility to extend the flat model in order to predict the capacitances of these devices as well [4]. However, this extension requires a lot of capacitors to describe the behaviour. This paper demonstrates a way to reduce the number of capacitors to the minimum number of six by consequently applying the energy based approach.

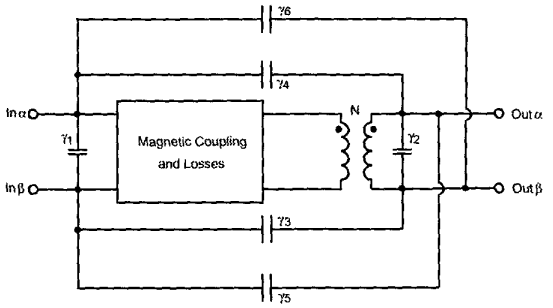

Fig. 1. The 'six capacitor equivalent circuit' according to [3].

The paper is outlined as follows. After this introduction the flat model and its extension towards the layer based capacitance model will be revised briefly. The next chapter demonstrates the feasibility of this approach by comparison with measurements. Chapter 4 explains and verifies the method to reduce the number of capacitances. The paper will end with a summary of the most important points.

II. FLAT MODEL

The 'flat model' derives an approximation of the six capacitor values. The calculation follows the ideas proposed in [2]. Electrostatically, a two winding transformer appears as a three input multipole (see Fig. 2).

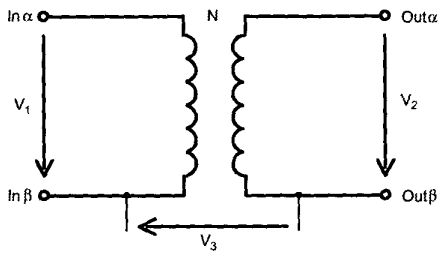

Fig. 2. The two winding transformer appears as a three input electrostatic multipole.

The electrostatic energy WE stored in the transformer is, at each time instant, a quadratic function of the three potentials V1, V2 and V3:

$$W_E = \tfrac{1}{2}\cdot C_{11}\cdot V_1^2 + \tfrac{1}{2}\cdot C_{22}\cdot V_2^2 + \tfrac{1}{2}\cdot C_{33}\cdot V_3^2 + C_{12}\cdot V_1\cdot V_2 + C_{13}\cdot V_1\cdot V_3 + C_{23}\cdot V_2\cdot V_3 \quad (1)$$

A comparison with the energy stored in the capacitors in Fig. 1 yields the following relationship between the coefficients Cij and γk:

$$\gamma_1 = C_{11}+C_{13},\ \gamma_2 = C_{22}-C_{23},\ \gamma_3 = C_{13}+C_{33}-C_{12}-C_{23},$$
$$\gamma_4 = -C_{12},\ \gamma_5 = C_{12}+C_{23},\ \gamma_6 = C_{12}-C_{13} \quad (2)$$

The flat model calculates the energy stored in a two winding transformer. Following the calculation in [2] the 'flat model' results in an estimation of the six capacitors of Fig. 1.

$$\gamma_1 = -\tfrac{1}{6}C_0,\ \gamma_2 = -\tfrac{1}{6}C_0,\ \gamma_3 = \tfrac{1}{3}C_0,\ \gamma_4 = \tfrac{1}{3}C_0,\ \gamma_5 = \tfrac{1}{6}C_0,\ \gamma_6 = \tfrac{1}{6}C_0 \quad (3)$$

C_0 in eq. (3) represent the so called 'static, volumetric capacitance' that can be measured as the capacitance between the short circuited primary and the short circuited secondary side.

The flat model corresponds to a two winding transformer that consists of only one layer per winding. In [4] the author has extended the flat model to an arbitrary number of layers.

This new approach will be called 'layer based capacitance model'. It is based on the idea that each pair of adjacent layers is connected by a six capacitor network as derived in the previous chapter. By means of this equivalent circuit the capacitive effects of transformers built by an arbitrary order and number of layers can be modelled. Fig. 3 depicts as an example a flyback transformer of three layers - two primary layers and one secondary layer. The secondary side is interleaved between the two primary layers.

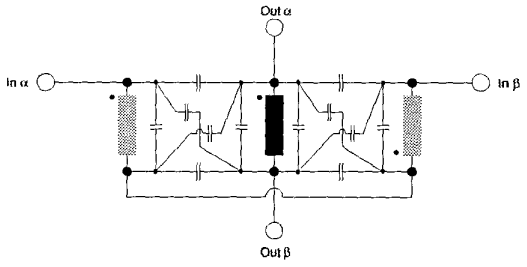

Fig. 3: Interleaved flyback transformer.

The benefits of the approach are obvious. The complete capacitive behaviour of the transformer can be described based on the values of the 'static, volumetric' capacitances between adjacent layers. Sometimes only one capacitance value has to be measured due to the fact that the others can be derived using geometrical ratios (distance between layers and area covered by the layers).

The influence of different winding configurations on the capacitive effects can be simulated and optimised before producing the magnetic component.

The behaviour of the transformer in different electrical circuits (e.g. secondary connected to a certain potential or floating) can be investigated.

The approach allows to investigate the capacitive effects in layer oriented wire wound components as well as in planar magnetic components, e.g. multi-layer based transformers.

In [4] some more remarks can be found regarding the flat model as well as the underlying assumptions and restriction of the layer based model.

III. EXPERIMENTAL RESULTS

The validity of the layer based capacitance model has been proven by an experimental verification. A planar transformer has been used for the measurements. Fig. 4 depicts the winding arrangement of the planar transformer comprising three windings built on 6 layers.

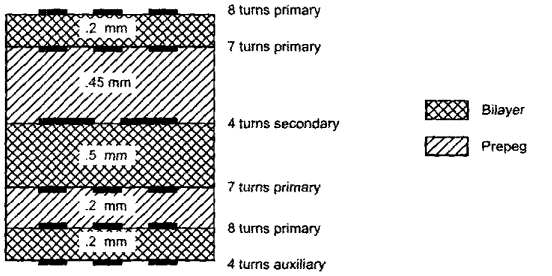

Fig. 4: Flyback transformer for comparison.

The first step necessary for modelling the transformer determines the 'static, volumetric' capacitance. To estimate this capacitance two layers containing multiple tracks will be replaced by two metallic plates from a parallel plate capacitor. The resulting area is:

$$A = 240mm^2$$

Using a relative dielectric constant ε_r=5, the capacitance of a parallel plate capacitor consisting of two plates 1 mm apart from each other can be calculated:

$$C_0(d=1mm) = \varepsilon_0\cdot\varepsilon_r\frac{A}{d} = 10.6\,pF$$

Remarks: The presented approximation of the layer to layer capacitance replaces the spiral turns by a homogenous metallic surface. Especially in case of the primary turns exhibiting only a fill factor of 0.5 this might be a rough approximation.

The relative dielectric constant εr is assumed to be 5 independent of material. Perhaps this value has to be

adapted even within one multilayer PCB because layers of base material and prepeg build the PCB.

Of course the estimation of the 'static, volumetric' capacitance can be verified by measurement of the existing transformer. The primary and secondary leads are short circuited. The capacitance between the two short circuited input terminals and the two short circuited output terminals has been measured using an impedance analyser. From this measurement the capacitance for 1mm can be derived that agrees very well with the estimated value:

$$C_{measured}(d=1mm)=10.9\,pF$$

A. Experimental results

The effective capacitance between the primary side input terminals has been measured by means of an impedance analyser. The value of the capacitance is determined using the built in 'Equivalent Circuit' parameter extraction capability of the measurement equipment. First two measurements are performed in order to extract the influence of the core on the effective capacitance. Because the capacitances towards the core as well as parasitic stray capacitances are not subject of this paper, their influence must be estimated in order to be able to compare the measured results with the simulated one. As described in [4] these capacitances are modelled by an effective capacitance of:

$$C_{eff\_core} = .7\ pF$$

After the influence of the core has been determined, measurements of the effective capacitances have been done under different conditions. This measurement set will be compared with corresponding simulations. Table I shows the measured and simulated results. The measurement conditions are according to the transformer depicted in Fig. 2.

B. Simulation results

The layer based model has been implemented in PSPICE, a circuit simulation program. Fig. 5 depicts the schematic used for the transformer within the PSPICE simulation.

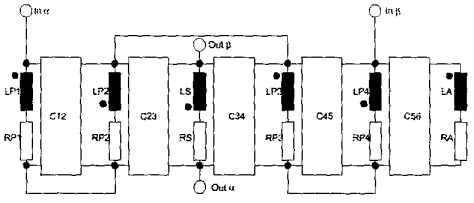

Fig. 5: Schematic of the transformer used within simulation.

The rectangular boxes represent sub-circuits containing the six capacitors describing the capacitive effects caused by two adjacent layers. Each of these boxes contains the capacitor network shown in Fig. 1. The values of the six capacitors are assigned by a single parameter C_0, that represents, of course, the 'static, volumetric' capacitance between the two layers under consideration.

The values of the elements within Fig. 5 are chosen as follows:

$$LP\,1=LP\,4=64\cdot AL\ ,\ LP\,2=LP\,3=49\cdot AL$$

$$LS=LA=16\cdot AL$$

$$C12=C45=C56=\frac{C_{0\_1mm}}{.2},\ C23=C34=\frac{C_{0\_1mm}}{.45}$$

Thus the complete winding construction can be described using two values C_{0_1mm} and AL. Within the simulation

$$C_{0\_1mm}=10.9\ pF$$

has been used as derived from the measured value. The AL value has been chosen to result in an overall primary side inductance of 154 µH.

$$AL=171nH \quad \Rightarrow \quad L_{prim}=30^2\cdot AL=154\,\mu H$$

The influence of the core on the capacitance effect is modelled by using an additional capacitance of

$$C_{eff\_core}=.7\ pF$$

The simulation has been done under the same conditions as the measurements. Table I depicts the obtained results together with the measured ones.

C. Comparison

Table I
Comparison of measurement with simulation.

Measurement condition	$C_{measured}$/pF	$C_{simulated}$/pF
secondary floating	9.1	11.1
Inα con. with Outα	18.3	20.3
Inα con. with Outβ	24.3	26.5
Inβ con. with Outα	23.3	26.5
Inβ con. with Outβ	17.5	20.3

Table I reveals that the simulation results are in good agreement with the measured ones. The simulation correctly reflects the influence of the short circuits. This means a floating secondary winding results in the lowest effective capacitance while connecting terminal Inα with Outβ or Inβ with Outα produces the largest effective capacitance. The comparison demonstrates the usefulness of the proposed model. In [4] a more detailed discussion of Table I is given.

IV. ANALYTICAL REDUCTION TO ONE CAPACITOR NETWORK

The proposed layer based capacitance model describes the capacitive effects of the transformer under different circuit conditions very well. Circuit simulation programs can make use of this new model directly. However, the model as described so far lacks of a good insight into the capacitance behaviour. Each capacitor network influences the overall effect. The extent of this influence is difficult to determine based on the complete transformer model. Therefore the next section derives a transformation that allows to separate the calculation for each capacitor network. A PSPICE simulation will verify the transformation for a practi-cal example of an interleaved flyback transformer.

A. Derivation of the transformation

The reason for the transformation is very simple. Despite the layer based origin of the capacitance effect the designer of switched mode power supplies wants a description of the transformer related to its external terminals - Inα, Inβ, Outα and Outβ. As already shown the six capacitor network depicted in Fig. 1 describes the capacitive behaviour of the transformer. Two transformation rules are necessary to reduce the large number of capacitor networks.

A1. Adjacent layer of the same winding

The first one deals with two adjacent layers of the same winding portion. In this case the well-known impedance transformation rule of a transformer can be applied as indicated in Fig. 6.

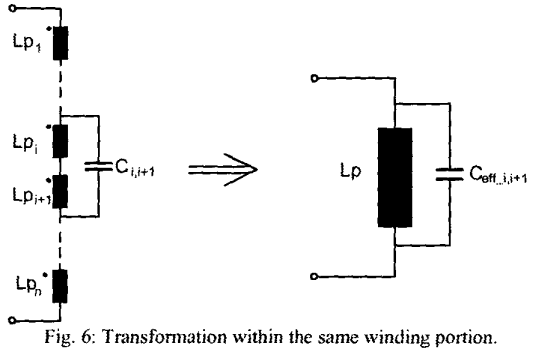

Fig. 6: Transformation within the same winding portion.

Fig. 6 assumes a winding portion consisting of n layers 1...n with number of turns $N_1...N_n$. Layer i and i+1 are adjacent layers. $C_{i,i+1}$ represents the capacitance between the beginning of layer i and the end of layer i+1. This capacitance can be calculated from the 'static, volumetric' capacitance. The left hand side of Fig. 6 represents an autotransformer loaded with a capacitance. Applying the transformation rule yields the corresponding effective capacitance:

$$C_{eff\_i,i+1} = \frac{\left(N_i + N_{i+1}\right)^2}{\left(\sum_{k=1}^{n} N_k\right)^2} \cdot C_{i,i+1} \tag{4}$$

If each layer consists of the same number of turns, eq. (4) simplifies:

$$C_{eff\_i,i+1} = \frac{4}{n^2} \cdot C_{i,i+1} \tag{5}$$

A2. Adjacent layer of the different windings

The second transformation deals with adjacent layers of different winding portions. Fig. 7 depicts the general case. The transformation uses the comparison of the electrostatic energy. Eq.'s (1-3) express the energy stored in the six capacitors γ1 through γ6 of Fig. 1 in dependence on the given voltages V1, V2 and V3. This section investigates the energy stored between the layers under consideration. This energy is determined in dependence on the same voltages V1, V2 and V3.

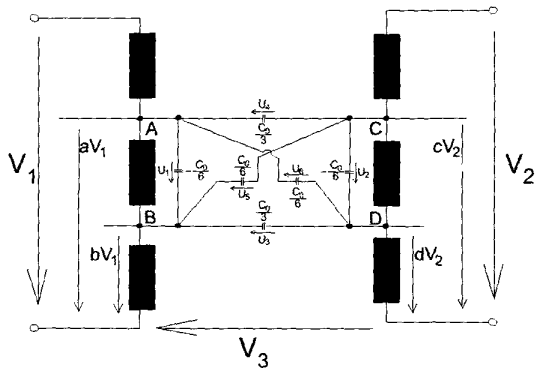

Fig. 7: General position of two adjacent layers - one of the primary winding and one of the secondary winding.

As in the 'flat model' the geometrical location of the winding is important. Thus for a given winding configuration the points A-C and B-D within Fig. 7 correspond to adjacent locations of the two layers within the practical design. aV1, bV1, cV2 and dV2 represent the voltages measured at these points expressed as fractions of the input and output voltages (V1 and V2).

Fig. 7 reveals the following relations for the six voltages U1 to U6 in dependence on V1, V2 and V3:

$$\begin{aligned} U_1 &= (a-b)\cdot V_1 & U_2 &= (c-d)\cdot V_2 \\ U_3 &= -b\cdot V_1 + d\cdot V_2 + V_3 & & \\ U_4 &= -a\cdot V_1 + c\cdot V_2 + V_3 & & \\ U_5 &= -b\cdot V_1 + c\cdot V_2 + V_3 & U_6 &= -a\cdot V_1 + d\cdot V_2 + V_3 \end{aligned} \tag{6}$$

The electrical energy WE stored in the system displayed in Fig. 7 can be calculated according to:

$$W_E = \frac{1}{2}\cdot\left(-\frac{C_0}{6}\right)\cdot U_1^2 - \frac{1}{2}\cdot\frac{C_0}{6}\cdot U_2^2 + \frac{1}{2}\cdot\frac{C_0}{3}\cdot U_3^2$$
$$\frac{1}{2}\cdot\frac{C_0}{3}\cdot U_4^2 + \frac{1}{2}\cdot\frac{C_0}{6}\cdot U_5^2 + \frac{1}{2}\cdot\frac{C_0}{6}\cdot U_6^2 \quad (7)$$

Using eq. (6) within eq. (7) and comparing the coefficients of the resulting equations with eq. (1) allows the determination of the corresponding values of C11 through C23:

$$C_{11}=\frac{C_0}{3}\left(a^2+b^2+a\cdot b\right)$$
$$C_{12}=-\frac{C_0}{6}\left(2\cdot a\cdot c+2\cdot b\cdot d+a\cdot d+b\cdot c\right)$$
$$C_{22}=\frac{C_0}{3}\left(c^2+d^2+c\cdot d\right) \qquad C_{13}=-\frac{C_0}{2}\left(a+b\right) \quad (8)$$
$$C_{33}=C_0 \qquad C_{23}=\frac{C_0}{2}\left(c+d\right)$$

Using eq. (8) together with eq. (3) the capacitances according to the equivalent circuit in Fig. 1 can be determined:

$$\gamma_1=\frac{C_0}{6}\left(2\cdot a^2+2\cdot b^2+2\cdot a\cdot b-3\cdot a-3\cdot b\right)$$
$$\gamma_2=\frac{C_0}{6}\left(2\cdot c^2+2\cdot d^2+2\cdot c\cdot d-3\cdot c-3\cdot d\right)$$
$$\gamma_3=\frac{C_0}{6}\left(6-3\cdot a-3\cdot b-3\cdot c-3\cdot d+2\cdot a\cdot c+2\cdot b\cdot d+a\cdot d+b\cdot c\right) \quad (9)$$
$$\gamma_4=\frac{C_0}{6}\left(2\cdot a\cdot c+2\cdot b\cdot d+a\cdot d+b\cdot c\right)$$
$$\gamma_5=\frac{C_0}{6}\left(3\cdot c+3\cdot d-2\cdot a\cdot c-2\cdot b\cdot d-a\cdot d-b\cdot c\right)$$
$$\gamma_6=\frac{C_0}{6}\left(3\cdot a+3\cdot b-2\cdot a\cdot c-2\cdot b\cdot d-a\cdot d-b\cdot c\right)$$

Eq. (9) represents the contribution of the capacitor network under consideration to each of the six capacitors of the generalised equivalent circuit of Fig. 1. The complete stored electrostatic energy is the sum of all energies stored in adjacent layers. Thus the contributions to the six capacitors have to be determined for all layer combinations. The next section applies the described transformation in case of an interleaved flyback transformer.

B. Verification

This section demonstrates the application of the above derived transformation in case of an interleaved flyback transformer. Fig. 8 depicts the winding structure. The transformer consists of two windings - one primary and one secondary winding. The primary winding consists of two layers with 10 turns. Five turns build the secondary winding. The secondary winding is often placed inside the splitted primary winding to reduce the leakage inductance. Thus we find two boundaries between primary and secondary windings. Two capacitor networks determine the capacitive behaviour of the interleaved flyback transformer in Fig. 8. According to Fig. 8 the 'static, volumetric' capacitances have values of Ca = 12pF and Cb = 24pF, respectively. (Remark: They are chosen differently to obtain the most general case.) Fig. 8 represents the implementation of the interleaved flyback transformer in PSPICE based on the layer based model. The results obtained for this transformer model form the basis for the verification of the model derived by the transformation.

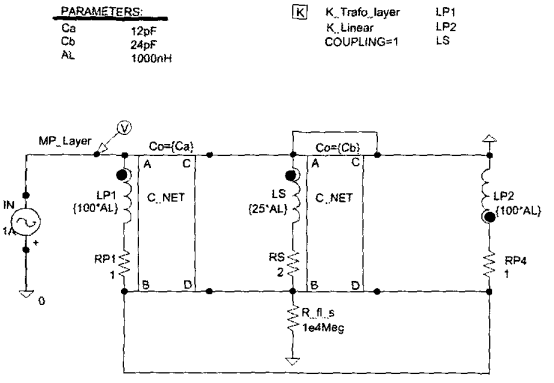

Fig. 8: Equivalent circuit of the interleaved flyback transformer as modelled within PSPICE.

The reduction of the layer based model to a model containing only one capacitor network comprises two steps. The first step determines the contribution of the capacitor network between LP1 and LS, while the second step deals with the network between LS and LP2.

B1 Contribution of the first capacitor network

The transformation of the capacitor network between LP1 and LS will be described as an example. Fig. 9 shows another representation of the schematic in Fig. 8. The schematic contains only the first capacitor network.

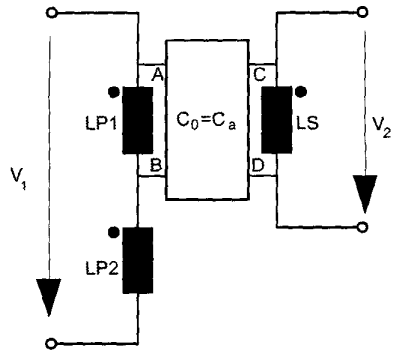

Fig. 9: Schematic used to derive the contribution of the first capacitor network.

Fig. 9 shows the relations for a_a, b_a, c_a and d_a:

$$a_a=1\ ,\quad b_a=0.5\ ,\quad c_a=1\ ,\quad d_a=0 \qquad (10)$$

Using the values of eq. (10) within eq. (9) yields in the contribution of the first network to the overall capacitive behaviour:

$$\gamma_{1a}=-\frac{1}{6}C_a=-2pF \qquad \gamma_{2a}=-\frac{1}{6}C_a=-2pF$$

$$\gamma_{3a}=\frac{1}{6}C_a=2pF \qquad \gamma_{4a}=\frac{5}{12}C_a=5pF \qquad (11)$$

$$\gamma_{5a}=\frac{1}{12}C_a=1pF \qquad \gamma_{6a}=\frac{1}{3}C_a=4pF$$

In the same manner the contribution of the capacitor network between LS and LP2 can be calculated. The overall capacitance values can then be obtained by the addition of both parts resulting in the capacitance values depicted in Fig. 10 that shows the PSPICE implementation of the general ESB.

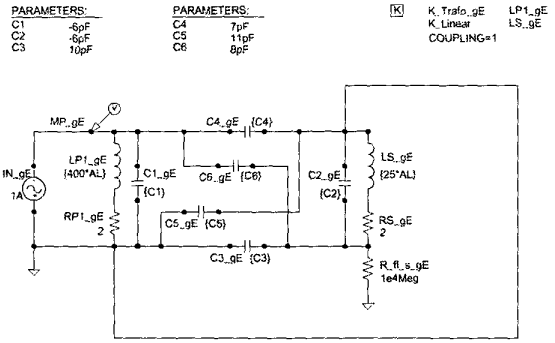

Fig. 10: PSPICE implementation of the derived model.

B2 Comparison

Simulations with the PSPICE implementations of Fig. 8 and Fig. 10 demonstrate that both circuits behave identically. Fig.'s 8 and 10 depict a certain environment - namely a short circuit between input terminal Inβ and output terminal Outα. Fig. 11 demonstrates the corresponding ac analysis. Fig. 11 simply shows two exact identical curves describing a resonant circuit. All simulations with different short circuits and floating secondary winding exhibit the same behaviour for both circuits thus verifying the validity of the transformation.

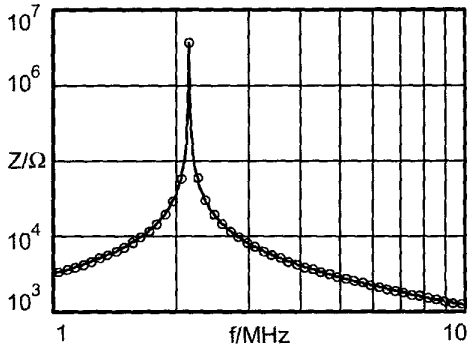

Fig. 11: The simulation results for both circuit implementations are exactly the same.

V. SUMMARY

This paper briefly describes the flat model and its extension towards arbitrary number and arrangement of layers. This extension, called layer based capacitance model, has been verified by measurements.

The only disadvantage of the new model is the high number of capacitances needed to model the behaviour. This disadvantage has been addressed. Two transformation rules allow to reduce the number of the capacitance down to the minimum of six. The transformation has been applied to an interleaved flyback transformer and the feasibility has been demonstrated by comparison of the full model with the reduced one.

VI. REFERENCES

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