Lahore University of Management Sciences

CS/EE-220 Digital Logic Circuits

Spring 2017

Course Catalog Description
This course focuses on the principles and practices of Digital Logic Circuit Design and is a first course in this area. Topics covered include: Boolean Algebra, Number Systems, Logic Gates, Logic Technologies, DRAM, SRAM, ROM, Inverters, Circuit Implementation of Logic Gates, Speed of Logic Gates and Operating Frequencies, Logic implementation of Boolean expressions, Karnaugh Maps, Analysis and Design of Combinational Logic Circuits, Analysis and Design of Sequential Logic Circuits, Circuits for Arithmetic Calculations, Circuits using memories and Flip-Flops, Registers and Register files, State-Machines, Memory Systems, Basic Processor and Control Unit Design.

Course Details	
Credit Hours	4 (3 for Theory +1 for Lab)
Core	BS EE / CS
Elective	For all LUMS students
Open for Student Category	
Closed for Student Category	

Course Prerequisite(s)/Co-Requisite(s)
Pre-requisites: None Co-requisites: None

Course Offering Details						
Lecture(s)	Nbr of Lec(s) Per Week	2	Duration	75 min	Timings and Venue	
Recitation (per week)	Nbr of Rec (s) Per Week	x	Duration			
Lab (if any) per week	Nbr of Session(s) Per Week	1	Duration	3 hrs		
Tutorial (per week)	Nbr of Tut(s) Per Week	X	Duration			

Instructor	Dr. Jahangir Ikram, Dr. Adeel Pasha, Dr. Wala Saadeh
Room No.	9-217A, 9-201A, 9-250
Office Hours	TBA
Email	jikram@lums.edu.pk , adeel.pasha@lums.edu.pk , wala.saadeh@lums.edu.pk
Telephone	8201, 8359, 8495
Secretary/TA	TBA
TA Office Hours	TBA
Course URL (if any)	LMS will be used

Course Learning Outcomes	
EE220+220L CLO1: CLO2: CLO3: CLO4: CLO5: CLO6:	The students should be able to: Develop Basic Knowledge in Number Systems, Boolean Algebra Analyze Combinational and Sequential Logic Circuits Design fairly complex logic circuits using Flip-Flops, Counter, ROM, RAM and basic logic gates Use modern tools such as Proteus to simulate logic circuits Commit to work in a team to design a technical project based on digital logic circuits Give presentations, make posters and demonstrate their technical projects to a diverse audience

Lahore University of Management Sciences

Relation to EE Program Outcomes				
EE/CS-220+220L CLOs	Related PLOs	Level of Learning	Teaching Methods	CLO Attainment checked in
CLO1	PLO1	Cog-3	Instruction, Assignments	Midterm, Final
CLO2	PLO2	Cog-4	Instruction, Assignments	Midterm, Final
CLO3	PLO3	Cog-5	Instruction, Assignments	Midterm, Final
CLO4	PLO5	Cog-4	Tutorials	Project
CLO5	PLO9	Aff-3	Instruction, Lab Manuals and Demos	Project
CLO6	PLO10	Psy-4	Tutorials	Project

Grading Breakup and Policy	
Lab Sessions (14):	13%
Quizzes (6-7):	15%
Assignments (2-3):	02%
Midterm Examination:	25%
Lab Project:	15%
Final Examination:	30%

Course Overview

Lecture	Topics	Recommended Readings	CLO Covered
1.	Course introduction and DLC basics	Chap-1 (MM[1])	CLO1
2.	Number Systems, Arithmetic Operations, Standard Codes	Chap-1 (MM[1])	
3.			
4.	Logic Gates, Boolean Algebra, Truth Tables and K-Maps	Hand-outs[4] Chap-2 (MM[1])	
5.			
6.			
7.			
8.			
9.			
10.	Combinational Circuits: Analysis and Design, Multiplexers, Decoders Rate Control	Chap-3 (MM[1]) Chap-4 (MM[1])	CLO2
11.			
12.			
13.			
14.			
Midterm Exam			
15.	Sequential Circuits: Introduction to Latches and Flip-Flops, Sequential Circuits Analysis and Design: State Diagrams and State Tables	Chap-5 (MM[1]) (5.1 – 5.7)	CLO2
16.			
17.			
18.			
19.	Registers and Counters: Shift Registers, Parallel Loading of Registers, Synchronous and Asynchronous Counters	Chap-7 (MM[1])	CLO3
20.			
21.			
22.	ROM, Combinational Logic Circuit Design through ROM	Chap-6 (MM[1])	
23.	Random Access Memory (RAM), Memory Decoding	Chap-8 (MM[1])	
24.			
25.	Register Transfer Operations, Buses	Chap-7 (MM[1])	
26.	Intro to Processor: Arithmetic Logic Unit (ALU) and Control Unit	Chap-9 (MM[1])	
27.			
28.	Intro to CMOS Technology: Transistor as a basic building block of Digital Circuits	Chap-6 (MM[1]) + Hand-outs[4]	CLO1
Final Exam			

Lahore University of Management Sciences

Lab + Project Overview			
Week	**Topics**	**Recommended Readings**	**CLO Covered**
1.	Introduction to the EE Lab, building your first circuit	Hands-outs[4]	CLO5
2.	Understanding the behavior of an Inverter		
3.	Digital Logic Gate Operations (AND, OR, NOT, NAND, NOR, XOR, Buffer)		
4.	Combinational circuits: Simplification & Implementation		
5.	Decoder and Comparator		
6.	Multiplexer and Logic Unit Design		
7.	Analog to Digital Converter, Temperature Sensor and Basic ON/OFF Control		
8.	Simulating a Digital Logic Circuit on Proteus Simulation Tool		
9.	Arithmetic Unit Design		
10.	ROM, RAM & ALU		
11.	NAND Latch & D Flip Flop		
12.	Up/Down Counter		
13.	Registers		
	Lab Project	Tutorials	CLO4, CLO6

Important Note: Students will be required to submit their Lab work and Lab handout at the end of the day's lab session.

Textbook(s)/Supplementary Readings
[1] Textbook: "Logic and Computer Design Fundamentals" by M.Morris Mano & Charles R. Kime, 4th Edition, 2008, (Prentice Hall Inc.) [2] Reference Book1: "Digital Fundamentals" by Thomas L. Floyd, 10th Edition (Pearson) [3] Reference Book2: "Digital Systems (Principles and Applications)" by Ronald J. Tocci, Neal S. Widmer & Gregory L. Moss, 10th Edition (Pearson) [4] Hand-outs provided for some lectures. Similarly, a lab manual will be provided to the students at the beginning of the each lab that carries the details of the experiments and related instructions to perform those experiments.

Examination Detail	
Midterm Exam	Yes/No: **Yes** Combine / Separate: **Combine** Duration: 3:00 hrs Preferred Date: TBA Exam Specifications: Closed Book, Closed Notes, Calculator Allowed
Final Exam	Yes/No: **Yes** Combine / Separate: **Combine** Duration: 3:00 hrs Exam Specifications: Closed Book, Closed Notes, Calculator Allowed

Prepared by:	**Dr. Adeel Pasha, Dr. Jahangir Ikram, Dr. Wala Saadeh**
Date:	**November 03, 2016**