Hvdc Light® Modeling for Dynamic Performance Analysis

Per-Erik Björklund, *Nonmember, IEEE*, Kailash Srivastava, *Senior Member, IEEE,*
and William Quaintance, *Senior Member, IEEE*

***Abstract*--The development of a detailed HVDC Light® model for dynamic simulation tools and implementation in PSS/E and Simpow are presented. The different requirements on such a model, the principles used for the model, and results from verification cases compared to EMTDC results are presented.**

***Index Terms*-- Dynamic response, HVDC transmission, Modeling, PSS/E, Simpow, Simulation**

I. Introduction

THIS paper presents the principles underlining the development of a detailed HVDC Light® model and its implementation in various dynamic simulation tools. Further_more the implementation of the detailed HVDC Light® model in PSS/E and Simpow are discussed. The paper also presents results showing the verification compared to PSCAD/EMTDC.

A. HVDC Light® in general

HVDC Light® [1]-[6] is a technology that utilizes Voltage Source Converters (VSC) rather than line commutated converters as used in conventional HVDC. Conventional HVDC transmission employs line commutated, current-source converters requiring a synchronous voltage source in order to operate. The conversion process demands reactive power from filters shunt banks, which are part of the converter station. Any surplus or deficit in reactive power must be accommodated by the ac system.

HVDC Light® avoids these demands and offers other advantages due to the possibility to independently control both active and reactive power. The theory of voltage source converters is well known, but only with the development of relatively cost effective semiconductors with current turn off capability have they become utilized in transmission systems. HVDC Light® employs Insulated Gate Bipolar transistors (IGBTs), plus other important technological developments:

1. High voltage valves with series-connected IGBTs
2. Compact, dry, high-voltage dc capacitors
3. High capacity control system
4. Solid dielectric DC cable

Per-Erik Björklund is with ABB Power Systems/HVDC, Ludvika, Sweden
Kailash Srivastava is with ABB Corporate Research, Västerås, Sweden
William Quaintance is with ABB Inc., Raleigh, NC, USA

In the HVDC Light® transmission schemes, the switching of the IGBT valves follows a pulse width modulation (PWM) pattern with a frequency in the kHz range. This switching control allows simultaneous adjustment of the amplitude and phase angle of the converter AC output voltage with constant dc voltage.

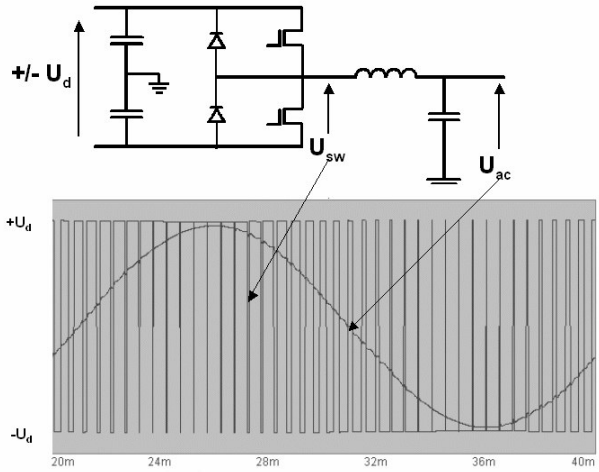

Fig. 1. Principles of using a PWM pattern to generate a sinusoidal voltage

With these two independent control variables, separate active and reactive power control loops can be used for regulation.

Two recent HVDC Light® projects are the Cross Sound Cable Interconnector, Connecticut - Long Island, USA and the Murraylink Interconnection, Victoria – South Australia. Both employ IGBT voltage source converter technology at ± 150 kV, coupled with solid dielectric cables, but have different characteristics according to the location and differing environments. The Cross Sound Cable Interconnector is an undersea cable, 40 km, connecting continental US to Long Island, with a power rating of 330 MW, making it the largest VSC converter project to date. The Murraylink Interconnection, 220 MW, has a 176 km land cable, believed to be the world's longest underground transmission system.

B. HVDC Light® simulation model

The first HVDC Light® transmission in a commercial ac system was set into operation for more than ten years ago. Simple models have been available during the time, but the rapid development of the HVDC Light® control system, with its new features, requires a proper representation in simulation tools. The detailed model developed allows for new control features, such as:

1. Optimized firing control, which can be used to reduce losses; the necessary algorithms for this feature must be properly represented
2. Passive ac system operation mode, used for offshore platform power supply and black start after system collapse
3. Robust model platform for introducing additional features necessary for new applications

II. Model requirements

Simulation models can be grouped in two different categories;

1. Electro-Magnetic Transient Program, like PSCAD/EMTDC and EMTP, based on instantaneous values
2. Electro-Mechanical Transient Program, like PSS/E, Simpow, PSLF, Digsilent, BPA, PSASP etc, based on fundamental frequency vector representation quantities

A. Electro-Magnetic Transient Program

In the category of Electro-Magnetic Transient Programs, we use PSCAD/EMTDC for control system design and dynamic performance verification. For these simulations we use a very detailed representation of the converter main circuit and a replica of the real control system. This type of model will not be further discussed in this paper.

B. Electro-Mechanical Transient Program

Simulations with Electro-Mechanical Transient Programs are used on a very wide range of applications, from initial planning studies by utilities to detailed project studies by manufacturers. Also, a wide range of simulation tools are used by different utilities.

Many of the simulation tools in this group use numerical solution methods with a fixed time step. To minimize the total simulation time, users often want to use a time step in the range 5-10 ms. For HVDC models in general, including HVDC Light®, such a large time step is a challenge in combination with the time constants in HVDC control.

III. Decisions in design

1) Definition of model

A model for simulation programs can cover different aspects. At least four different aspects have been defined:

1. Load flow representation
2. Loss representation (for optimized load flow)
3. Dynamic representation
4. Short circuit currents

The development of the simulation model was focused on the dynamic representation. The load flow representation was only used to get a starting point for the dynamic simulation. The loss representation was not implemented in detail, since for most cases this does not affect the dynamics. The short circuit current behavior was only included as a user instruction to disconnect the HVDC Light® converter at short circuit current calculations to cope with the current limitation from a HVDC Light® converter (maximum 1 pu current).

2) Common model to be used in all tools

The second design decision was to create a common logical model, with the intention that the same logical model can be implemented in all tools. The benefits are that it is known what can be expected from the different implementations of HVDC Light®, and the different implementations can be verified in a common way.

3) Transparency to the real control system

The third design decision was to follow the same structure as the real control system. The reason for that was to establish a robust platform that can be used also for future extensions of the control system in new applications.

4) Robust in applications

Since the HVDC Light® is a component that can serve different type of applications in a system, and the experience in utilities is not yet so large, it was assumed that the model should be robust in different type of applications.

5) Easy to use

An obvious design decision is that the models shall be easy to use for an experienced user of the tool. The amount of information to be given by the user shall be minimized. The concept of HVDC Light® with defined standard levels of rated power provides a well defined matrix with nine different setup alternatives. Input data for these nine alternatives are provided with the model. The HVDC Light® control system design is based on a robust approach, which has verified that the same control system and parameter settings can cope with a large range of ac systems and applications. This makes the use of the HVDC Light® simulation model much easier, since virtually all control parameters can use default values.

6) Numerically robust

In simulation tools using a fixed time step, there is a latent conflict in the size of time step the user wants to use and the internal time constants of an HVDC Light® converter. The design decision was that the simulation model shall be numerically robust, and at the same time allow for an open choice of time step to use. Only minor degrading of the simulation results shall be acceptable at the maximum expected time step 10 ms (50 Hz system), and this degrading shall be well defined by verification cases.

7) Core of the HVDC Light control

The core of the HVDC Light control is a robust design that the user do not need to change settings or control algorithms. The core control is distributed as a pre compiled code, this makes the model easier to use, and the user is not tempted to include changes that are not possible to realize in a real system. Users can affect the model behavior with auxiliary inputs from higher level controls.

8) Input from higher level control

The design decision is that the HVDC Light® model shall be provided with three auxiliary inputs. These inputs give an opportunity for the user to design higher level controls for different kinds of modulation. The following auxiliary inputs are provided:

1. ΔP_{ref}, to be used for active power modulation to achieve frequency control or damping control (end point damping)

2. ΔQ_{ref}, to be used for reactive power modulation to achieve damping control (mid point damping)
3. ΔU_{acref}, to be used for ac voltage modulation, the usage is not yet defined in detail

IV. Implementation and Verification

A. HVDC Light control

The principal control of HVDC Light® is shown in Fig. 2. In the figure the references P_{ref}, Q_{ref} and U_{acref} are shown. These are normally picked from the load flow as the initial condition; the user can modify these to represent power order changes or other step changes. The auxiliary inputs ΔP_{ref}, ΔQ_{ref} and ΔU_{acref} can be used for modulation as discussed in the previous section. Each converter can be in reactive power control mode (Q_{ref}) or ac voltage control mode (U_{acref}), independent of each other. Furthermore one of the converters is in active power control mode (P_{ref}) and the other in dc voltage control mode (fixed reference U_{dcref}). The user can select between these modes.

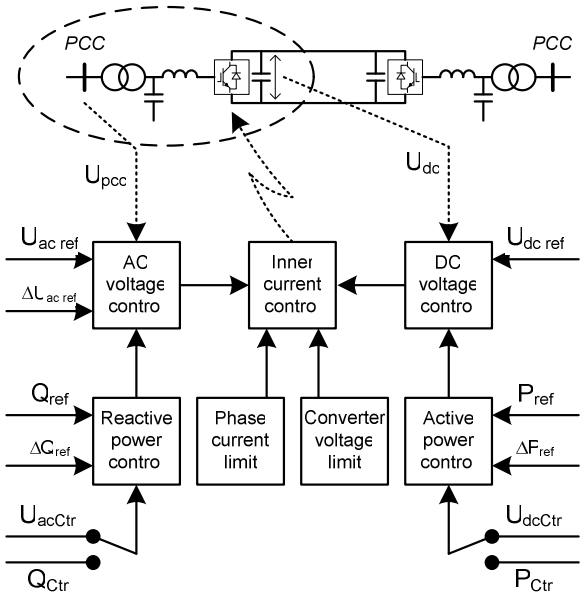

Fig. 2. Principal control of HVDC Light®, each converter is provided with an identical control, independent of rectifier or inverter operation. PCC is the Point of Common Connection, i.e. the point of converter connection to the ac system, and the reference point for ac voltage, active power P, and reactive power Q. This figure indicates the modes ac-voltage control and dc-voltage control.

B. Characteristics of HVDC Light® and challenge in implementation

The characteristics of an HVDC Light® transmission and the challenge to implement can be summarized with the following items:

1. DC system representation and its time constants
2. Time constants that are short, in the control system
3. Inner current control

The dc system of an HVDC Light® transmission is dominated by the dc capacitors of the converters. These capacitors dominate the dc system capacitance even for relatively long dc cables. Typically the dc system time constant is in the range of 8-10 ms. The fastest controls in an HVDC Light® control have time constants in the range of 5-10 ms.

Very often a time step in the range of 5-10 ms is used (tools with fixed time step), or at least this is what the user wants. The time step in combination with the system time constants is close to the limit of what can be performed and must be handled with care. One can then ask why it is necessary to represent the dc side dynamics and controls related to that at all. Experience from previous models of HVDC Light® have shown that the integrating behavior of the dc side capacitance is the best solution to take care of the active power control, and related mode shifts between the converter. Furthermore, it is actually a representation of the reality.

The inner current control is the heart of the HVDC Light® control. The current control is fast, and the intention with the current control is to get an ideal behavior as close as possible, at least for the phenomenon studied with Electro-Mechanical Transient Programs. In the HVDC Light® model it is assumed as a simplification or generalization that the inner current control is ideal. In verification cases it is found that this approach only makes the HVDC Light® model to act a few milliseconds faster than the real control. The decision at implementation has therefore been to omit the inner current control, to limit the efforts in implementation. Furthermore, verification tests have shown that the deviation is only a few milliseconds at large transients.

C. Verification cases

A number of Benchmark cases have been used to verify the implemented simulation models as shown in Fig. 3. The identical cases have been simulated in PSCAD/EMTDC with a replica of the complete HVDC Light® control system included. The PSCAD/EMTDC simulations are performed with a time step of 1 μs.

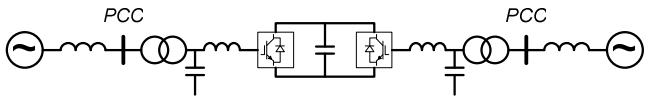

Fig. 3. Benchmark system used for verification. PCC is the Point of Common Connection, i.e. the point of converter connection to the ac system. This system is used in the Simpow verification, for the final PSS/E verification a slightly more detailed ac system is used.

D. PSS/E

1) Implementation

The program PSS/E uses a fixed time step as a fundamental solution principle. The implementation of the HVDC Light® model in PSS/E must cope with the fixed time step and the items related to that discussed above. At large time steps (normally above 5 ms) the time constants in the dc system and HVDC Light® control are virtually increased to at least the same as the used time step. These increased time constants introduce performance degradation, and the user must evaluate what is gained in using a time step above 5 ms, compared to the performance degradation.

A large number of verification cases have been simulated,

and the model implementation is found to be robust and stable. It is however assumed that some systems in combination with large time steps may introduce numerical oscillations. The primary recommendation in such a case is to lower the time step used, but in some situations this may not be possible. Therefore, a user defined parameter has been implemented, with which the user can lower the threshold for degradation to maintain numerical stability.

In general the implementation in PSS/E went very well and the verification cases show surprisingly good results up to 5 ms time step. There is not much in return, to use time steps shorter than 5 ms, even if the user is recommended to repeat some sample case with a shorter time step. Even the performance degradation using 10 ms was much less than expected, even if it is noticeable.

2) Verification

In the following plots from test cases are shown. The legend shown in Table I is valid:

TABLE I
LEGEND OF PSS/E VERIFICATION CASES

Curve	**Simulated with**
Solid, marked with □	PSCAD/EMTDC 1 μs time step
Dashed, marked with Δ	PSS/E with 0.5 ms time step
Dashed, marked with ◊	PSS/E with 1 ms time step
Dashed, marked with +	PSS/E with 5 ms time step
Dashed, marked with X	PSS/E with 10 ms time step

Plots from the verification cases for the PSS/E implementation of HVDC Light® are shown in Fig. 4 to Fig. 13.

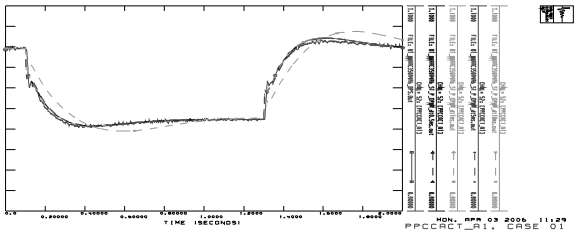

Fig. 4, Step in active power reference, steady state mode, 0.1 pu down and up. Only the PSS/E 10 ms time step case differs slightly. The total simulated time is 2 s.

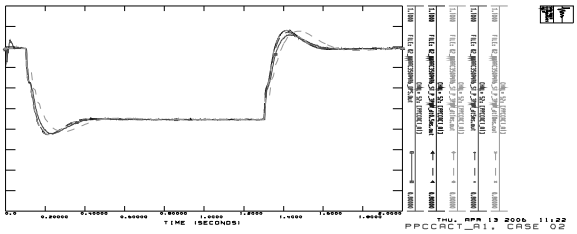

Fig. 5 Step in active power reference, transient mode, 0.1 pu down and up. Only the PSS/E 10 ms time step case differs slightly. The total simulated time is 2 s

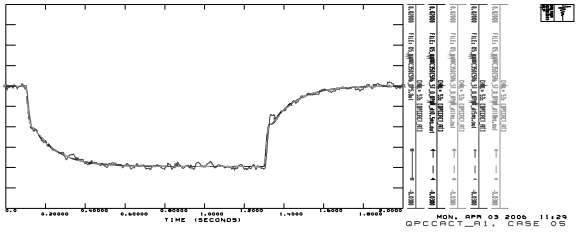

Fig. 6, Step in reactive power reference, steady state mode, 0.2 pu down and up, all cases match perfectly. The total simulated time is 2 s.

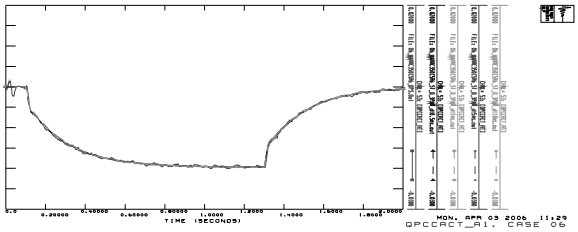

Fig. 7, Step in reactive power reference, transient mode, 0.2 pu down and up, all cases match perfectly. The total simulated time is 2 s.

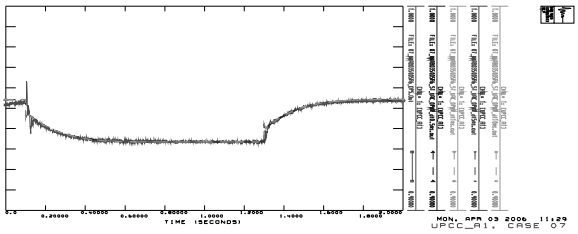

Fig. 8, Step in ac voltage reference, steady state mode, 0.02 pu down and up, all cases match perfectly. The total simulated time is 2 s.

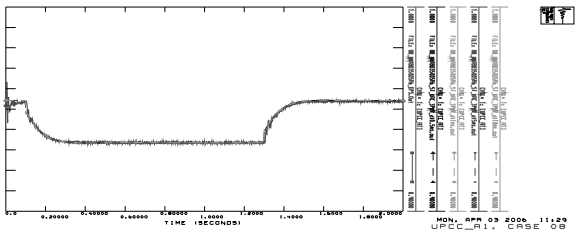

Fig. 9, Step in ac voltage reference, transient mode, 0.02 pu down and up, all cases match perfectly. The total simulated time is 2 s.

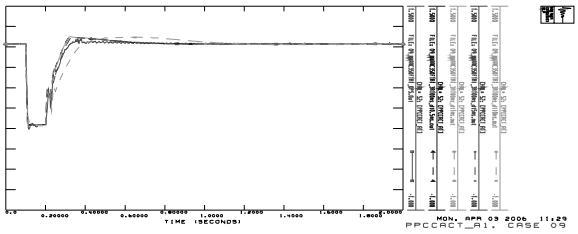

Fig. 10, The active power in the rectifier at a ground fault in the rectifier, 10% remaining voltage. The PSS/E cases with 0.5-5 ms time step are slightly faster, and the PSS/E cases with 10 ms time step case is slightly slower. The total simulated time is 2 s.

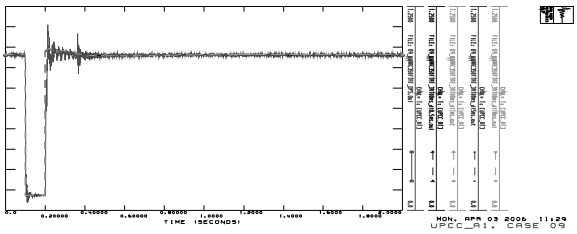

Fig. 11, The ac voltage in the rectifier at a ground fault in the rectifier, 10% remaining voltage. Only the PSS/E 10 ms time step case shows a small deviation. The total simulated time is 2 s.

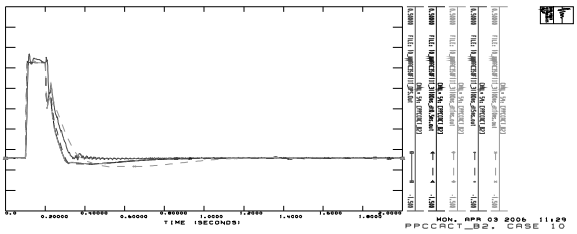

Fig. 12, The active power in the inverter at a ground fault in the inverter, 10% remaining voltage. The PSS/E cases with 0.5-5 ms time step are slightly faster, and the PSS/E cases with 10 ms time step case is slightly slower. The total simulated time is 2 s.

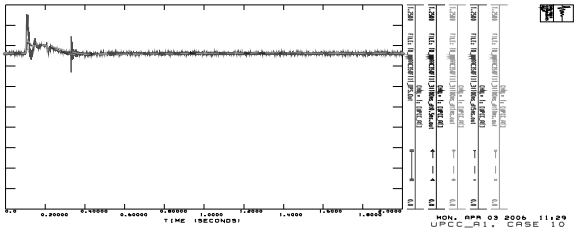

Fig. 13, The ac voltage in the rectifier at a ground fault in the inverter, 10% remaining voltage, all cases match perfectly. The total simulated time is 2 s. The rectifier voltage is shown as comparison, because the rectifier is weaker and shows a larger disturbance.

E. Simpow

Unlike PSS/E, Simpow utilises variable time step algorithm for numerical integration thereby permitting the time step to automatically increase once the transients have died out. It separates stiff variables from non-stiff variables and uses backward differentiation for the former and trapezoidal method for the later to take advantage of both the methods. This hastens the simulation process while maintaining the same accuracy.

Simpow also has dc node, dc line and dc shunt elements as standard component available in its library. These features of Simpow enable accurate representation of dc system outside the user written model.

The converter and control system was implemented using Dynamic Simulation Language (DSL) [7] for loadflow and dynamic simulation. During loadflow, a user needs to specify the power order at one of the converters and the dc voltage at the other converter. The ac voltage or reactive power order at both the converters must also be specified.

The losses are assumed to be known a priori and represented by equivalent shunt resistances at dc node. Loadflow solution is used to start the dynamic simulation. The model is suitable for simulating steady state and transient operating modes of the converter. The control system includes an automatic logic to detect the transient condition and change the operating mode accordingly during dynamic simulation.

The performance of model was evaluated for the different networks having short circuit capacity 3 to 34 times that of the converter rating at the point of common connection. Some of the disturbances considered were step change in active/reactive or voltage order, trip of converter and three phase fault at converter bus. The model has demonstrated good agreement with PSCAD simulation results. Fig. 14 illustrates the performance of model for a step change in active power.

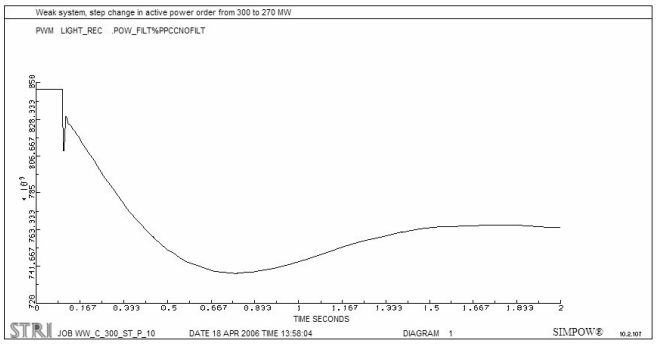

Fig. 14. Step change in active power reference, 0.1 pu down at t = 0.1 s. The total simulated time is 2 s. The short circuit capacity at converter bus is 3 times that of converter capacity.

V. Applications for the Simulation Model

The simulation models can be used in the following applications:

1. Reactive power control, each converter independent of each other, the reactive power order could be selected to best suit the ac system, or could be modulated with an auxiliary input from some external control
2. Ac voltage control, each converter independent of each other, the ac voltage order is normally constant, but may also be modulated with an auxiliary input from some external control
3. System recovery after three phase ac faults close to the converter, or distant faults
4. Active power modulation capability, to be used in damping control, frequency control etc.
5. Passive net operation, to be used feeding a passive system or at black start, this mode is under development in the PSS/E model.

VI. Common Component

The development of the HVDC Light® concept continues with new applications and further improved control system. It would have been helpful if the different simulation tools would have the possibility to call an external program component that includes the HVDC Light® representation. Instead of implementing the HVDC Light® in each simulation tool, one common component could be developed, and that component

could be called from each simulation tool. This scenario would improve the implementation, maintenance and quality of the HVDC Light® representation in different simulation tools. Different simulation tools use different numerical solution principles, which make development of such a common component a challenge. However, we have started a feasibility study to find out if it is possible to develop such an interface, and common component, for the simulation programs that today allow for external code.

VII. References

[1] Gunnar Asplund, Kjell Eriksson and Kjell Svensson, "DC transmission based on Voltage Source Converters", Paper presented at Cigré colloquium on HVDC and FACTS in South Africa, 1997 [Online]. Available: http://www.abb.com/hvdc

[2] Stefan G Johansson, Gunnar Asplund, Erik Jansson and Roberto Rudervall, "Power System Stability Benefits with VSC DC-Transmission Systems", Presented at CIGRE Session, Paris, France, 2004 [Online]. Available: http://www.abb.com/hvdc

[3] B. D. Railing, J. J. Miller, P. Steckley, G. Moreau, P. Bard, L. Ronström and J. Lindberg, "Cross Sound Cable Project - Second generation VSC Technology for HVDC", Presented at CIGRE Session, Paris, France, 2004 [Online]. Available: http://www.abb.com/hvdc

[4] U. Axelsson, A. Holm, C. Liljegren, M. Åberg, K. Eriksson, O. Tollerz, The Gotland HVDC Light project - experiences from trial and commercial operation. Presented at CIRED 2001, Amsterdam, Netherlands, June 2001 [Online]. Available: http://www.abb.com/hvdc

[5] J. Hanson, T. Hunger. "Network Studies for Offshore Wind Farm Grid Connections – Technical Need and Commercial Optimization." Presented at EWEC 2004 - European Wind Energy Conference & Exhibition, London, U.K, November 2004. [Online]. Available http://www.2004ewec.info/files/23_1400_juttahanson_01.pdf

[6] Dag Ravemark, Bo Normark, "Light and invisible: Underground transmission with HVDC Light", Article in ABB Review 4/2005. [Online]. Available: http://www.abb.com/hvdc

[7] Simpow [Online]. Available: http://www.stri.se/simpow

VIII. Biographies

Per-Erik Björklund was born in Bjursås, Sweden on October 1, 1958. He graduated from the Royal Institute of Technology, Stockholm, in 1984. Since then he has been employed at ABB Power Systems, HVDC, in Ludvika, Sweden, in two periods, in total 17 years.

Kailash Srivastava was born at Fatehpur (UP) in India on October 3, 1962. He graduated in Electrical Engineering from MMM Engineering College Gorakhpur (India) in 1983 He did his MTech and PhD in Power Systems from IIT Kanpur (India) in 1986 and 1995 respectively. He worked in India and Italy for different companies before joining ABB Corporate Research Sweden where he has been working for past 9 years.

William Quaintance was born in Raleigh, NC, USA in 1965. He graduated with a Bachelor of Science degree from North Carolina State University, Raleigh NC, in 1989, and with a Master of Science degree from Clemson University, Clemson SC USA, in 1991. After graduation, he worked in the Transmission Planning Department of Duke Power Company for 7 years. He has since been working at ABB, Raleigh NC, in the Research and Consulting departments.