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HVDC Light: Modeling, Application and Control Design

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Abstract **– Voltage Source Converter (VSC) based HVDC transmission technology has been selected as the basis for several recent projects due to its controllability, compact modular design, ease of system interface, and low environmental impact. This paper investigates the dynamic performance of a 200MW, ±100kV VSC-HVDC transmission system under some faulted conditions using MATLAB/Simulink. Simulation results confirm the satisfactory performance of the proposed system under active and reactive power variations and fault conditions.**

Keywords: HVDC, Voltage source converter (VSC), IGBT, SPWM, Control design

I. NOMENCLATURE

U_L = the sinusoidal AC voltage in the AC network
U_f = AC voltage in the AC network at the filter-bus
$U_{V(1)}$ = the fundamental line to line voltage (valve side)
X_L = the leakage reactance of the transformer
u = phase shift between U_L and $U_{V(1)}$
I_V = source current
L, R = phase reactor inductance and resistance
C = DC side capacitance
S = source voltage angular frequency
m = modulation index
P, Q = AC active, reactive power inputs
U_d, I_d, P_d = DC side voltage, current, power
α, β = stationary α -β axis
d, q = synchronous d -q axis
p, n = positive, negative components
$*$ = reference value for controller

II. INTRODUCTION

With the development of power electronic technology and the relatively high switching frequency of Pulse Width Modulation (PWM), HVDC transmission system based on Voltage Source Converters (VSCs) has taken on some excellent advantages. The new VSC-HVDC system known as "HVDC Light" or "HVDC Plus" [1,2] by leading vendors, has been applied in several special occasions such as the connection of off-shore wind farms or oil drilling platforms into the mainland electrical network and for underground transmission or distribution systems within congested cities. The differences in structure between the two types of converters (Conventional HVDC and VSC-HVDC) contribute to the differences in their performance. Generally, the new transmission technology has the following advantages compared with conventional, thyristor based HVDC [3,4,5]:

- Possibility to control the reactive power (consumed or generated by the converter) independently of the active power (to or from the converter).
- No risk of commutation failures in the converter.
- Ability to connect to weak AC networks, or even dead networks.
- Faster response due to increased switching frequency (PWM).
- Minimal environmental impact.

However, VSC transmission does have some disadvantages, which include potentially high power losses and high capital costs when compared with conventional HVDC, but the technology continues to evolve.

This paper presents the elements of VSC-HVDC which uses six pulse three level converter topology and its control design. The paper wills first give a brief description about the VSC based HVDC transmission system and its terminal control functions. Following that typical operating contingency scenarios are simulated in order to evaluate transient performance. The simulation results confirm that the control strategy has fast response and strong stability.

III. FUNDAMENTALS OF VSC TRANSMISSION

The fundamentals of VSC transmission operation may be explained by considering each terminal as a voltage source connected to the AC transmission network via a three-phase reactor. The two terminals are interconnected by a DC link, as schematically shown in Fig. 1.
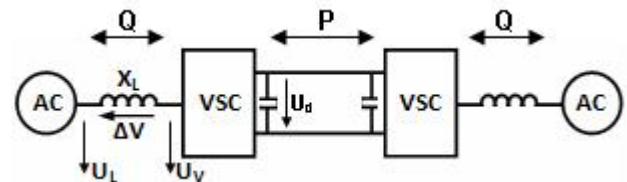

Fig 1: Basic VSC transmission

Fig. 2 shows a phasor diagram for the VSC converter connected to an AC network via a transformer inductance. The fundamental voltage on the valve side of the converter transformer, i.e. $U_{V(1)}$, is proportional to the DC voltage as been expressed in equation (1):

$$U_{V(1)} = k_u \cdot U_d \qquad (1)$$

The quantity k_u can be controlled by applying additional number of commutation per cycle, i.e. applying pulse with modulation (PWM). Using the definition of the apparent power and neglecting the resistance of the transformer results in the following equations for the active and reactive power:

$$P = U_d \cdot I_d = \frac{U_L \cdot U_{V(1)}}{X_L} \sin u \qquad (2)$$

$$Q = \frac{U_L \cdot (U_L - U_{V(1)} \cdot \cos u)}{X_L} \qquad (3)$$

The active and reactive power will in the following be defined as positive if the powers flow from the AC network to the converter. The phase displacement angle u will then be positive if the converter output voltage lags behind the AC voltage in phase.
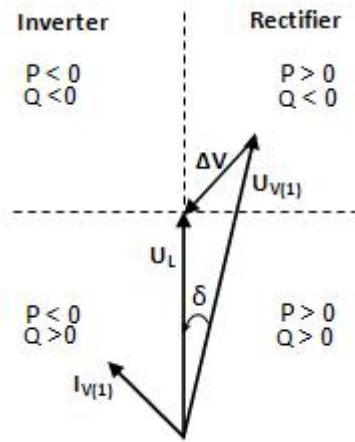

Fig 2: Phasor diagram of VSC and direction of power flows

Equation (2) gives that the active power is proportional to the DC current and the DC voltage. Furthermore it is mainly determined by the phase-displacement angle . A positive phase-shift results in that the active power flows from the AC network to the converter. However the reactive power is mainly determined by the difference between the magnitudes of the AC bus voltage and the converter output voltage according to the equation (3). The reactive power is fed from the voltage with higher magnitude towards the voltage with the lower magnitude. Theses features permit the independent control of the reactive and active power which is a major advantage for the VSC. P-Q diagram is a circle according to equation (4) with the center not located at origin as it does for the line commutated converters as shown in fig 3.
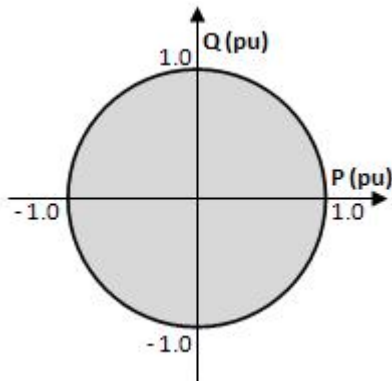

Fig 3: P-Q characteristics of a VSC-HVDC system

$$P^2 + \left(Q - \frac{U_L^2}{X_L}\right)^2 = \left(\frac{U_L \cdot U_{V(1)}}{X_L}\right)^2 \qquad (4)$$

If the output voltage of the converter $U_{V(1)}$ is reduced, e.i by using PWM, supply of any active and reactive power within the circle is possible.

IV. SYSTEM DESCRIPTION

A 200 MW (± 100 kV DC) forced-commutated voltage-sourced converter (VSC) interconnection is used to transmit power from a 230 kV, 2000 MVA, 50 Hz system to another identical AC system. The AC systems (1 and 2) are modeled by damped L-R equivalents with an angle of 80 degrees at fundamental frequency and at the third harmonic. The rectifier and the inverter are three-level Neutral Point Clamped (NPC) VSC converters using close IGBT/Diodes. The rectifier and the inverter are interconnected through a 100 km cable (i.e. 2 pi sections) and two 8 mH smoothing reactors. The sinusoidal pulse width modulation (SPWM) switching uses a single-phase triangular carrier wave with a frequency of 27 time's fundamental frequency (1350 Hz). A converter transformer (Wye grounded /Delta) is used to permit the optimal voltage transformation. The present winding arrangement blocks tripplen harmonics produced by the converter. The 0.15 pu phase reactor with the 0.15 pu transformer leakage reactance permits the VSC output voltage to shift in phase and amplitude with respect to the AC system Point of Common Coupling (PCC) and allows control of converter active and reactive power output. The tap position is rather at a fixed position determined by a multiplication factor applied to the primary nominal voltage of the converter transformers. The multiplication factors are chosen to have a modulation index around 0.85 (transformer ratios of 0.915 on the rectifier side and 1.015 on the inverter side). To meet AC system harmonic specifications, AC filters form an essential part of the scheme. They can be connected as shunt elements on the AC system side or the converter side of the converter transformer. Since there are only high frequency harmonics, shunt filtering is therefore relatively small compared to the converter rating. The 40 Mvar shunt AC filters are 27th and 54th high-pass tuned around the two dominating harmonics.

V. VSC-HVDC CONTROL STRATEGY

Fig. 4 shows an overview diagram of the VSC control system and its interface with the main circuit [6]. The converter 1 and converter 2 controller designs are identical. The two controllers are independent with no communication between them. Each converter has two degrees of freedom. In our case, these are used to control:

- P and Q in station 1 (rectifier)
- U_d and Q in station 2 (inverter).

A. Phase locked loop

The phase locked loop (PLL) shown in fig.4 is used to synchronise the converter control with the line voltage and also to compute the transformation angle used in the *d-q* transformation. The PLL block measures the system

frequency and provides the phase synchronous angle Θ for the d-q transformations block. In steady state, $\sin(\Theta)$ is in phase with the fundamental (positive sequence) of the α component and phase A of the point of common coupling voltage (U_{abc}).
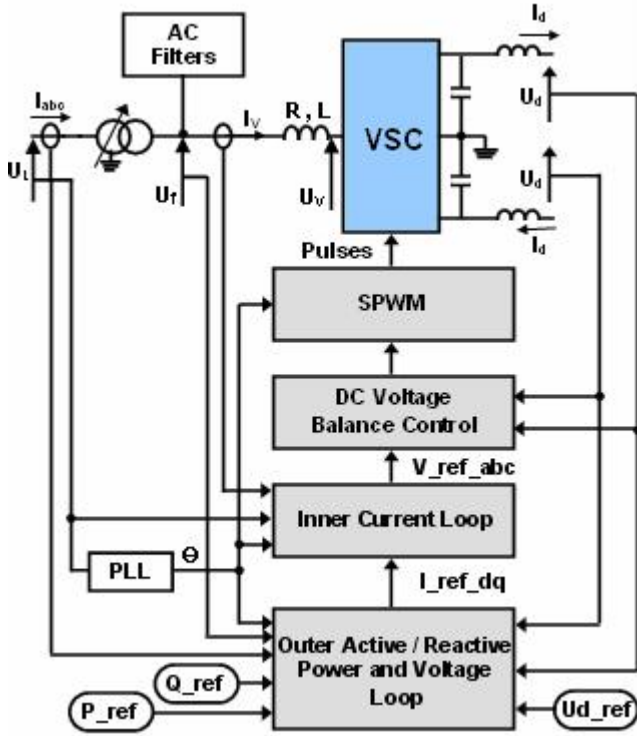

Fig 4: Overview diagram of the VSC control system

B. Outer active and reactive power and voltage loop

The active power or the DC voltage is controlled by the control of   and the reactive power is controlled by the control of the modulation index (m). The instantaneous real and imaginary power of the inverter on the valve side can be expressed in terms of the dq component of the current and the voltage on the valve side as follows:

$$p = \frac{3}{2} \cdot \mathrm{Re}(\overline{u}_f^{dq} \cdot \overline{i}_v^{*dq}) = \frac{3}{2} \cdot (u_{fd} \cdot i_{vd} + u_{fq} \cdot i_{vq}) \tag{5}$$

$$q = \frac{3}{2} \cdot \mathrm{Im}(\overline{u}_f^{dq} \cdot \overline{i}_v^{*dq}) = \frac{3}{2} \cdot (-u_{fd} \cdot i_{vq} + u_{fq} \cdot i_{vd}) \tag{6}$$

If the reference of the dq-frame is selected such that the quadrature component of the voltage is being very small and negligible ($u_{Lq} \approx 0$) then the equations (5) and (6) indicate that the active and the reactive power are proportional to the d and q component of the current respectively. Accordingly, it is possible to control the active power (or the DC voltage or the DC current) and the reactive power (or the AC bus voltage) by control of the current components i_{vd} and i_{vq} respectively. The active and reactive power and voltage loop contains the outer loop regulators that calculate the reference value of the converter current vector (I^*_{dq}) which is the input to the inner current loop.

C. Inner current loop

For each of the phases we can write:

$$u_f - u_v = L\frac{di_v}{dt} + R \cdot i_v \tag{7}$$

During unbalanced operation [7], the expression for the voltage drop over the reactor ($R + j\check{S}L$) holds for positive as well as for negative-sequence voltages and currents. The voltages drops are described by the differential equation:

$$\frac{d}{dt}\begin{bmatrix} i_{vaX} \\ i_{vbX} \\ i_{vcX} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & 0 & 0 \\ 0 & -\frac{R}{L} & 0 \\ 0 & 0 & -\frac{R}{L} \end{bmatrix} \begin{bmatrix} i_{vaX} \\ i_{vbX} \\ i_{vcX} \end{bmatrix}$$
$$- \begin{bmatrix} \frac{1}{L} & 0 & 0 \\ 0 & \frac{1}{L} & 0 \\ 0 & 0 & \frac{1}{L} \end{bmatrix} \begin{bmatrix} u_{vaX} \\ u_{vbX} \\ u_{vcX} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 & 0 \\ 0 & \frac{1}{L} & 0 \\ 0 & 0 & \frac{1}{L} \end{bmatrix} \begin{bmatrix} u_{faX} \\ u_{fbX} \\ u_{fcX} \end{bmatrix} \tag{8}$$

Where $X = (p)$ for positive sequence and (n) for negative sequence. Equation (8) can be transformed to the α β-frame. This gives for the voltages and currents:

$$\frac{d}{dt}\begin{bmatrix} i_{vrX} \\ i_{vsX} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & 0 \\ 0 & -\frac{R}{L} \end{bmatrix} \begin{bmatrix} i_{vrX} \\ i_{vsX} \end{bmatrix} - \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \end{bmatrix} \begin{bmatrix} u_{vrX} \\ u_{vsX} \end{bmatrix}$$
$$+ \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \end{bmatrix} \begin{bmatrix} u_{frX} \\ u_{fsX} \end{bmatrix} \tag{9}$$

Equation (9) can be further transferred into the rotating dq-frame:

$$\frac{d}{dt}\begin{bmatrix} i_{vdp} \\ i_{vqp} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & \check{S} \\ -\check{S} & -\frac{R}{L} \end{bmatrix} \begin{bmatrix} i_{vdp} \\ i_{vqp} \end{bmatrix} - \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \end{bmatrix} \begin{bmatrix} u_{vdp} \\ u_{vqp} \end{bmatrix}$$
$$+ \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \end{bmatrix} \begin{bmatrix} u_{fdp} \\ u_{fqp} \end{bmatrix} \tag{10}$$

and

$$\frac{d}{dt}\begin{bmatrix} i_{vdn} \\ i_{vqn} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & -\check{S} \\ \check{S} & -\frac{R}{L} \end{bmatrix} \begin{bmatrix} i_{vdn} \\ i_{vqn} \end{bmatrix} - \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \end{bmatrix} \begin{bmatrix} u_{vdn} \\ u_{vqn} \end{bmatrix}$$
$$+ \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \end{bmatrix} \begin{bmatrix} u_{fdn} \\ u_{fqn} \end{bmatrix} \tag{11}$$

The positive and negative sequence voltages of the VSC side are obtained from (10) and (11):

$$u_{vdp} = u_{fdp} - R \cdot i_{vdp} + \check{S}L \cdot i_{vqp} - L\frac{d}{dt}i_{vdp} \tag{12}$$

$$u_{vqp} = u_{fqp} - R \cdot i_{vqp} - \check{S}L \cdot i_{vdp} - L\frac{d}{dt}i_{vqp} \tag{13}$$

and

$$u_{vdn} = u_{fdn} - R \cdot i_{vdn} - \check{S}L \cdot i_{vqn} - L\frac{d}{dt}i_{vdn} \tag{14}$$

$$u_{vqn} = u_{fqn} - R \cdot i_{vqn} + \check{S}L \cdot i_{vdn} - L\frac{d}{dt}i_{vqn} \tag{15}$$

The mean voltages over the sample period k to $k+1$ are derived by integrating (12), (13), (14) and (15) from kT_s to $(k+1)T_s$ and dividing by T_s (where T_s is the sampling time).

$$\bar{u}_{vdp} = \bar{u}_{fdp} - R \cdot \bar{i}_{vdp} + \check{S}L \cdot \bar{i}_{vqp} - \frac{L}{T_s}\{i_{vdp}(k+1) - i_{vdp}(k)\} \tag{16}$$

$$\bar{u}_{vqp} = \bar{u}_{fqp} - R \cdot \bar{i}_{vqp} - \check{S}L \cdot \bar{i}_{vdp} - \frac{L}{T_s}\{i_{vqp}(k+1) - i_{vqp}(k)\} \tag{17}$$

and

$$\bar{u}_{vdn} = \bar{u}_{fdn} - R \cdot \bar{i}_{vdn} - \check{S}L \cdot \bar{i}_{vqn} - \frac{L}{T_s}\{i_{vdn}(k+1) - i_{vdn}(k)\} \tag{18}$$

$$\bar{u}_{vqn} = \bar{u}_{fqn} - R \cdot \bar{i}_{vqn} + \check{S}L \cdot \bar{i}_{vdn} - \frac{L}{T_s}\{i_{vqn}(k+1) - i_{vqn}(k)\} \tag{19}$$

By assuming linear current and constant network voltage (the network voltage varies very little during a switching time period) during one sample period T_s we obtain from (16) through (19):

$$u_{vdp}(k+1) = u_{fdp}(k) - \frac{R}{2}\{i_{vdp}(k+1) + i_{vdp}(k)\}$$
$$+ \frac{\check{S}L}{2}\{i_{vqp}(k+1) + i_{vqp}(k)\} - \frac{L}{T_s}\{i_{vdp}(k+1) - i_{vdp}(k)\} \tag{20}$$

$$u_{vqp}(k+1) = u_{fqp}(k) - \frac{R}{2}\{i_{vqp}(k+1) + i_{vqp}(k)\}$$
$$- \frac{\check{S}L}{2}\{i_{vdp}(k+1) + i_{vdp}(k)\} - \frac{L}{T_s}\{i_{vqp}(k+1) - i_{vqp}(k)\} \tag{21}$$

$$u_{vdn}(k+1) = u_{fdn}(k) - \frac{R}{2}\{i_{vdn}(k+1) + i_{vdn}(k)\}$$
$$- \frac{\check{S}L}{2}\{i_{vqn}(k+1) + i_{vqn}(k)\} - \frac{L}{T_s}\{i_{vdn}(k+1) - i_{vdn}(k)\} \tag{22}$$

$$u_{vqn}(k+1) = u_{fqn}(k) - \frac{R}{2}\{i_{vqn}(k+1) + i_{vqn}(k)\}$$
$$- \frac{\check{S}L}{2}\{i_{vdn}(k+1) + i_{vdn}(k)\} - \frac{L}{T_s}\{i_{vqn}(k+1) - i_{vqn}(k)\} \tag{23}$$

The control is based on (20), (21), (22) and (23), where the voltages and currents at time $(k+1)$ are thus equal to the reference values at time step (k).

D. DC voltage balance control

The difference between the DC side voltages (positive and negative) are controlled to keep the DC side of the three level bridge balanced (i.e., equal pole voltages) in steady-state. Small deviations between the pole voltages may occur at changes of active/reactive converter current or due to nonlinearity on lack of precision in the execution of the pulse width modulated bridge voltage. Furthermore, deviations

between the pole voltages may be due to inherent unbalance in the circuit components impedance.

VI. SIMULATIONS RESULTS

The dynamic performance of the transmission system is verified by simulating the:

1. Steps on the regulators references,
2. Recovery from severe perturbations in the AC system.

A. Step responses

In order to test the dynamic responses of the VSC-HVDC regulators, four test cases have been studied. The simulation includes power reversion from – 0.5pu to + 0.5pu, of station 1 at t = 1.3s, then active power step changes from 0.5pu to 1.0pu at t = 2.5s (Case 1 and 2). At t = 2.0s, the reactive power step change from 0 pu to – 0.3pu of station 1, then set to +0.3 pu at t = 2.7s (Case 3). At station 2, the DC voltage step change from 1 pu to 0.095 pu at t = 3 s (case 4, with the constant reactive power of – 0,1pu). The results are shown in fig.5. After steady state has been reached, the converter 1 active power reference value is changed from from – 0.5 pu to + 0.5 pu and then set to 1.0 pu at t = 2.5s. As can be seen, the active power can track the reference of the active power. The transferred active powers at both sides change the direction which causes transients on the DC voltage then returns to the reference value due to the DC voltage controller. The AC voltages at the filter bus (U_{f1} and U_{f2}), can be kept constant except for some transients that occur when both the step changes are applied. The active power flow is adjusted to the new setting within 30 ms. At t = 2.0s the reactive power step change is applied, then another step at t = 2.7s. Theses two steps change cause transients on the DC voltage, but, as expected, the step change of the active power causes a much higher transient than that with the change in reactive power. At t = 2.5s the active power change to 1pu, and later another step is also applied on the reference DC voltage of the station 2 at t =3.0s. The reactive power and the DC voltage can track the references of the reactive power and the DC voltage. The active and reactive power responses are decoupled by the control design.

B. AC side perturbations.

A single phase to ground fault was first applied at t = 1.3s during 0.10s (5 cycles) at station 1 in order to investigate the behaviour of VSC-HVDC during unbalanced faults. A second perturbation follows. A three-phase to ground fault is applied at station 2 at t = 2.0s and is cleared at 5 cycles after the fault, i.e., at t = 2.1s. Fig.6 presents the simulations results. From the simulation, it can be noted that before a single phase to ground fault at station 1, the active power flow is 1.0 pu, transmitted from converter 1 to converter 2, and is kept constant during the fault. The DC voltage drops and it contains an oscillation during the fault. Consequently the transferred DC power contains also the oscillation. During the station 1 side fault the transmitted power can be kept constant except a small oscillation during the fault. All oscillations in voltages and currents at both

systems, means that the phase voltages and currents at both systems are unbalanced.
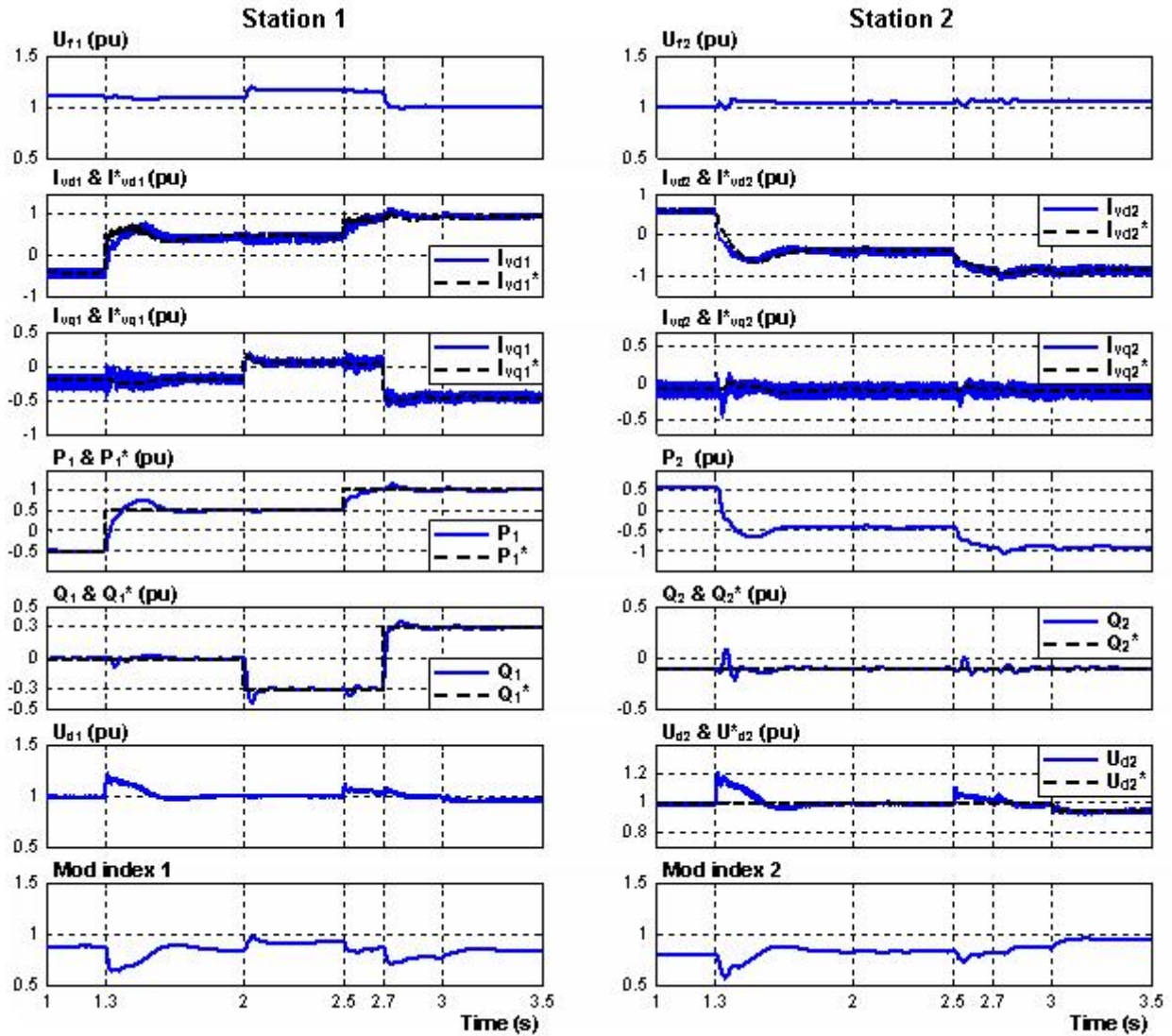

Fig 5: Steps on the regulators references

During the severe three-phase fault at station 2 at t = 2.0 s, the AC voltage at station 2 side is decreased to 0.1 pu during the fault and recovers fast and successfully to 1.0 pu voltage after clearing the fault. The transmitted power flow is reduced to very low value during the fault and recovers to 1.0 pu after the fault. The DC voltage, which can be controlled to 1.0 pu during the fault, has some oscillations at the beginning of the fault and at clearing the fault, and its maximum transient value is about 1.2 pu. On the other hand, the phase currents at station 1 side decrease to low values to reduce the power flow.

VI. CONCLUSION

In this paper, we have presented the steady-state and dynamic performances of VSC based HVDC transmission system during step changes of the active and reactive powers, balanced and unbalanced faults. In all cases the proposed control strategy has been shown to provide fast and satisfactory dynamic responses of the proposed system. From the simulation, it can be obtained that the VSC-HVDC can fulfil fast and bi-directional power transfers. It can be obtained also that during a single-phase fault the transmitted power can be kept constant except a small oscillation during the fault. However, during a three-phase fault; the decreased voltage at the converter terminals strongly reduces the power flow by the DC link. When the fault is cleared, normal operation is recovered fast.

APPENDIX

Station 1(Rectifier side)	230kV(80°), 2000 MVA, $SCR = 10$, $L_1 = 31.02$ mH, $R = 13.79\,\Omega$, $L_2 = 62.23$ mH.
Station 2 (Inverter side)	230kV(80°), 1000 MVA, $SCR = 5$, $L_1 = 62.04$ mH , $R = 27.58\,\Omega$, $L_2 = 124.46$ mH
Transformer	Yg/ , 230kV/100kV, 200 MVA, 15%
Main DC capacitor	70 µF
DC Cables	100km×2 (R=0.0139 Ω /km, $L = 0.159$ mH/km, $C = 23.1$ µF/km

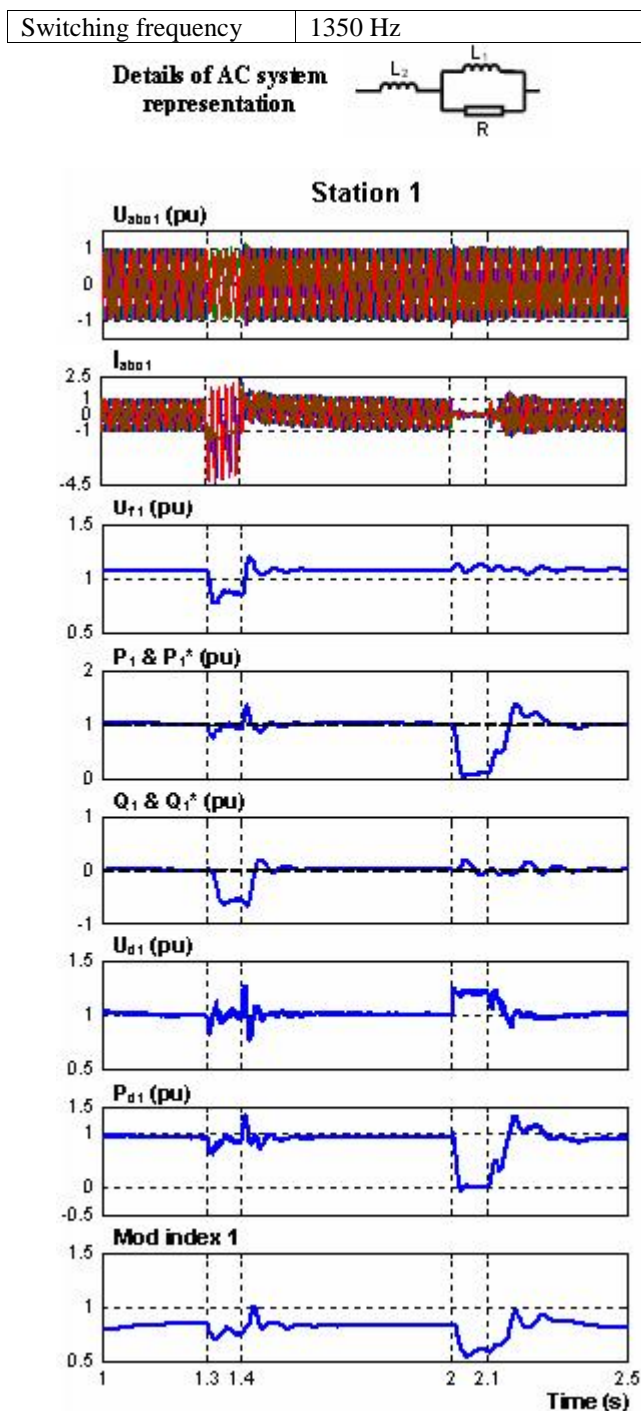| Switching frequency	1350 Hz

Details of AC system representation

Fig 6: AC side perturbations

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