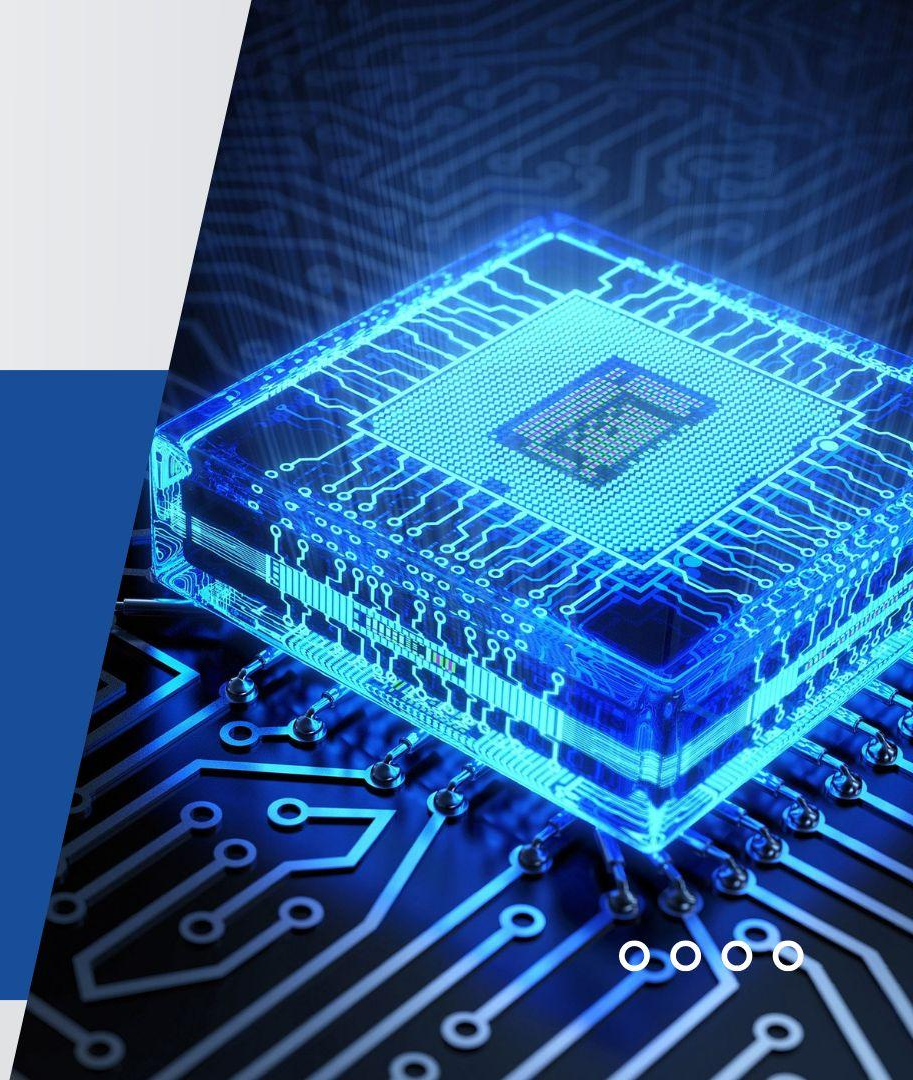
MERL

Accelerating Engineering Innovation

RISC-V Pipeline Core

MERL DSU

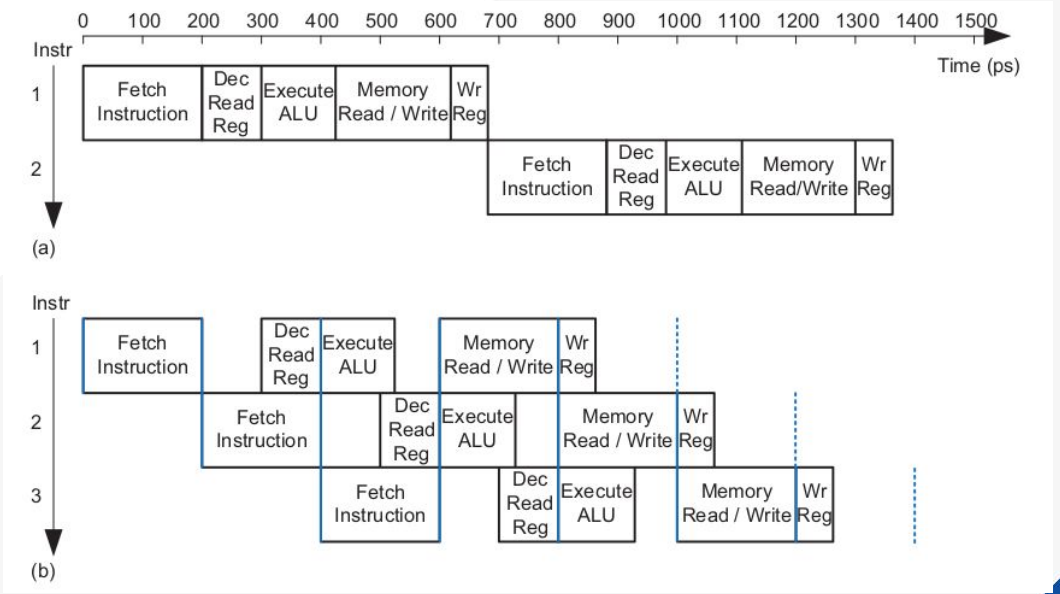
TABLE OF CONTENTS



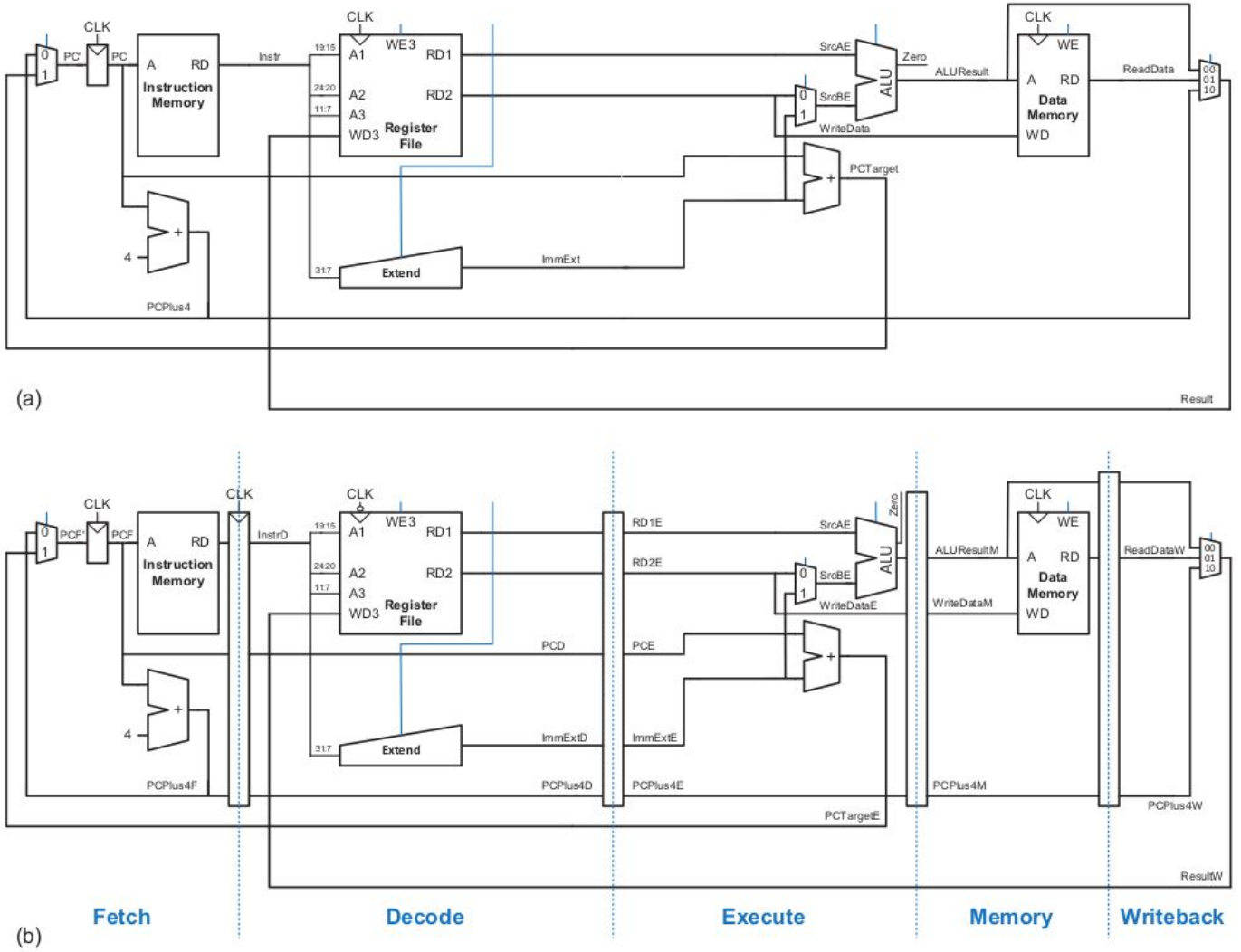
Overview

Pipelining

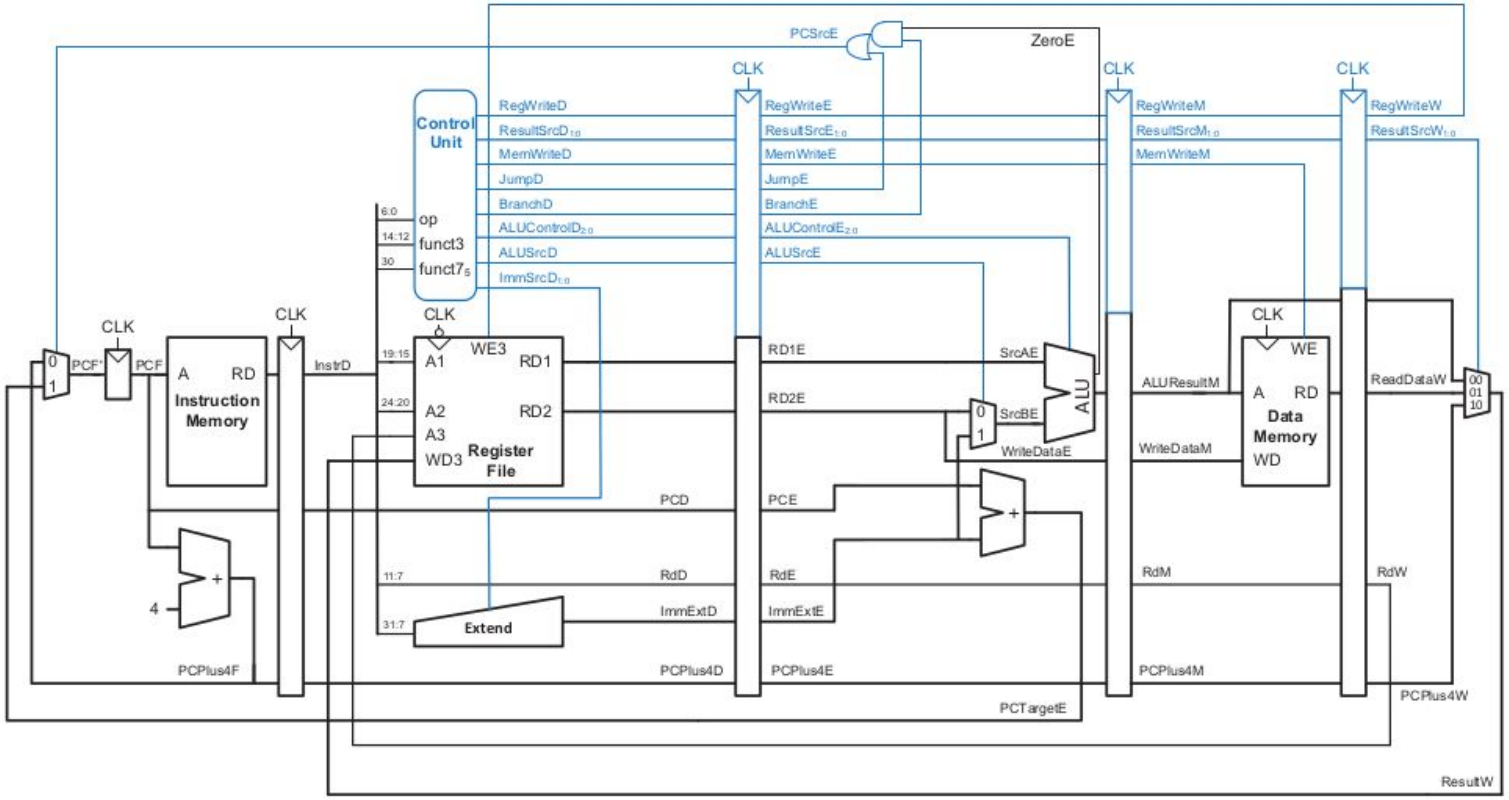
We design a pipelined processor by subdividing the single-cycle processor into five pipeline stages. Thus, five instructions can execute simultaneously, one in each stage. Because each stage has only one-fifth of the entire logic, the clock frequency is approximately five times faster.



Pipelining


CLK
PC
PC
A
RD
Instruction Memory
Instr
19:15
24:20
11:7
A1
A2
A3
WD3
WE3
RD1
RD2
Register File
SrcAE
Zero
ALU
ALUResult
SrcBE
WriteData
CLK
WE
A
RD
Data Memory
WD
ReadData
00
01
10
PCTarget
4
ImmExt
31:7
Extend
PCPlus4
Result
(a)
CLK
PCF'
PCF
A
RD
Instruction Memory
InstrD
19:15
24:20
11:7
A1
A2
A3
WD3
WE3
RD1
RD2
Register File
RD1E
RD2E
SrcAE
Zero
ALU
ALUResultM
SrcBE
WriteDataE
WriteDataM
CLK
WE
A
RD
Data Memory
WD
ReadDataW
00
01
10
PCD
PCE
4
ImmExtD
ImmExtE
31:7
Extend
PCPlus4F
PCPlus4D
PCPlus4E
PCPlus4M
PCPlus4W
PCTargetE
ResultW
Fetch
Decode
Execute
Memory
Writeback
(b)

Pipeline Datapath



MERL

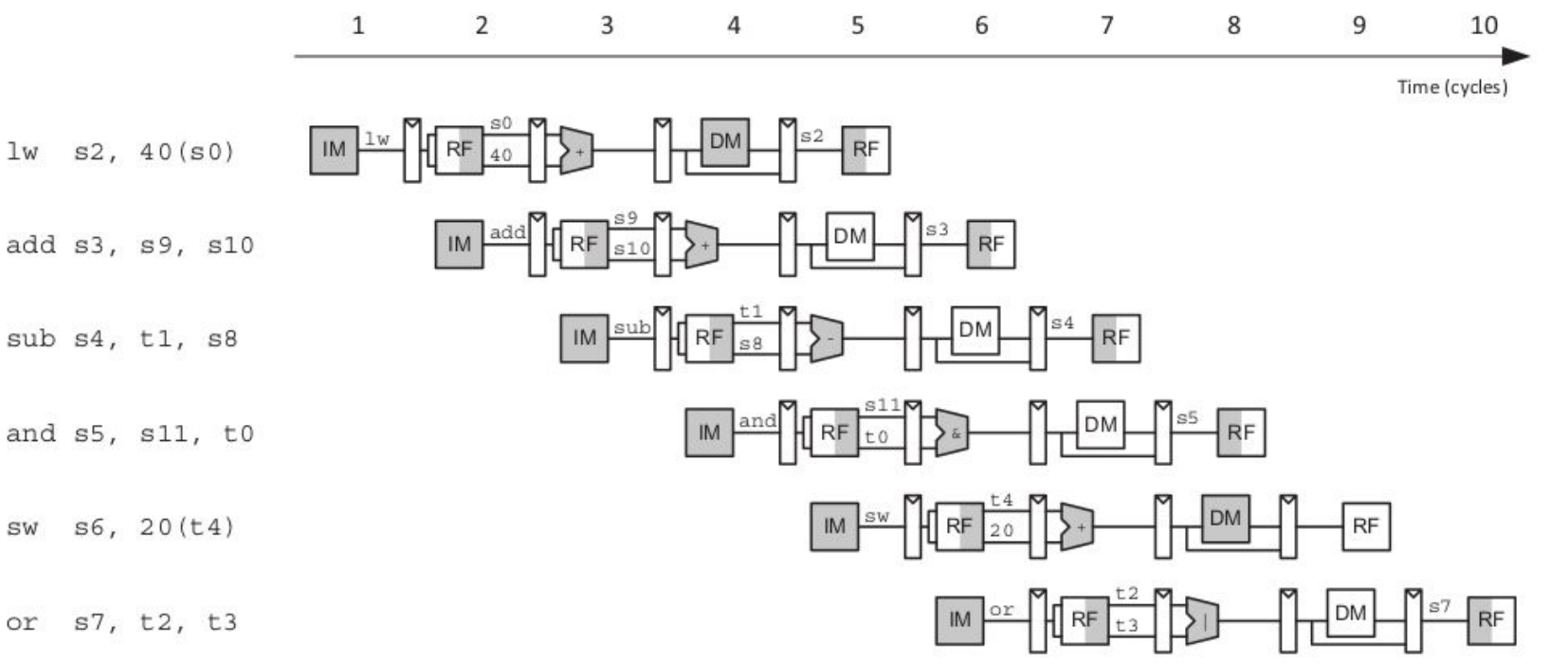
Accelerating Engineering Innovation

RISC-V Pipeline Core

MERL DSU

Implementation of Fetch Cycle

Abstract View of Pipelining



Fetch Cycle Datapath

Modules to be Integrated:

1) PC Mux
2) Program Counter
3) Adder
4) Instruction Memory