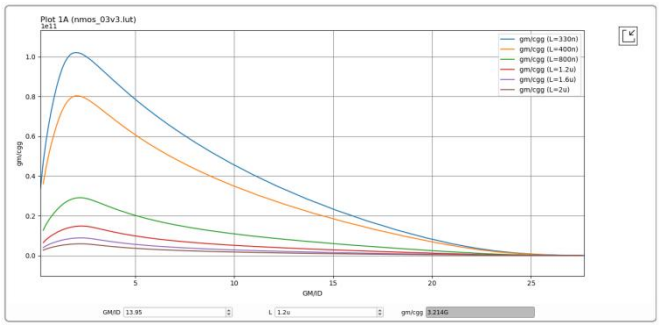
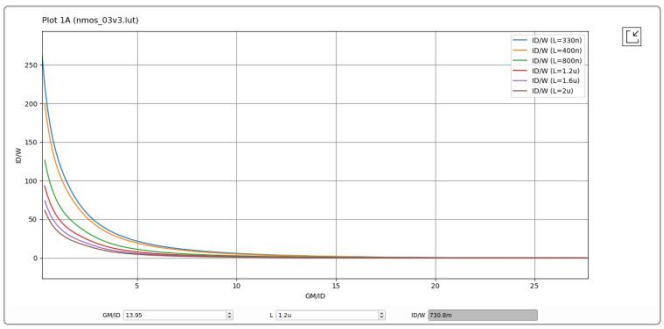
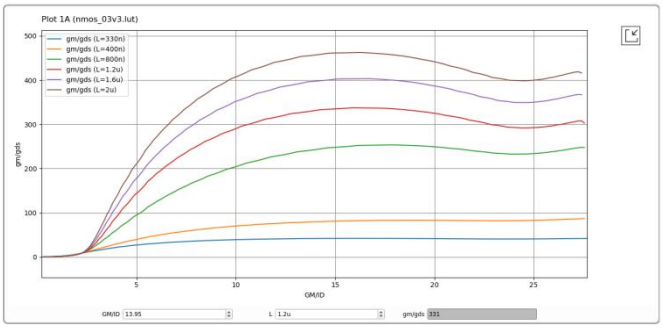
Lab 7: OTA DESIGN

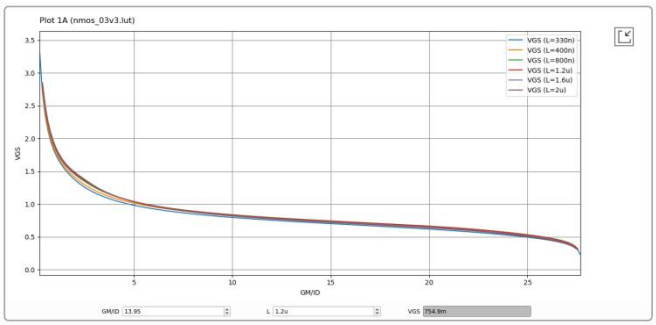
Part 1: g_m / I_D design charts:

For NMOS, design charts:

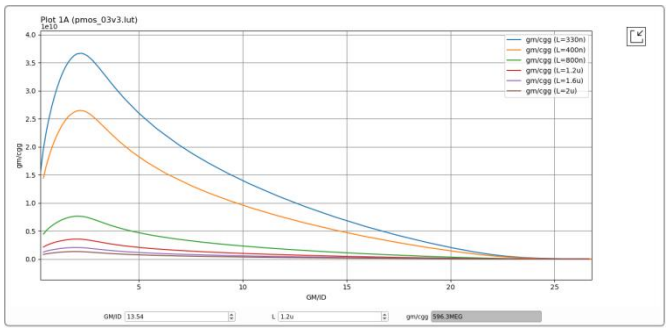


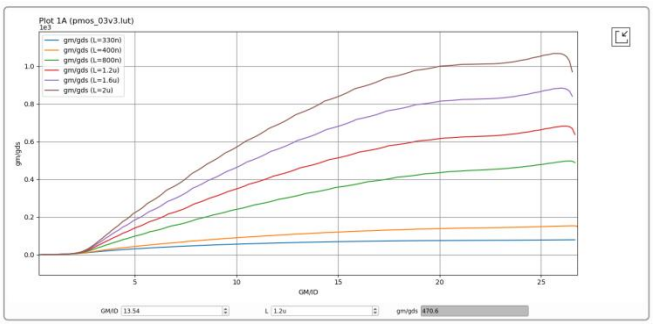


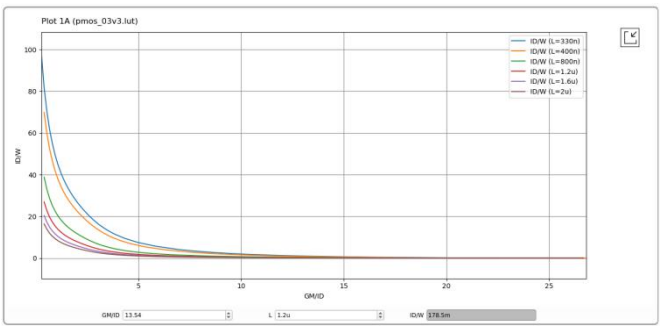


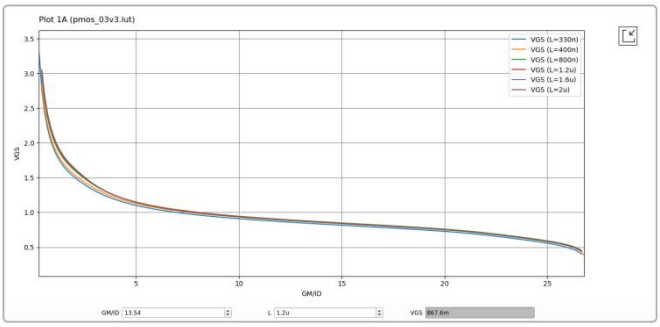


For PMOS, design charts:



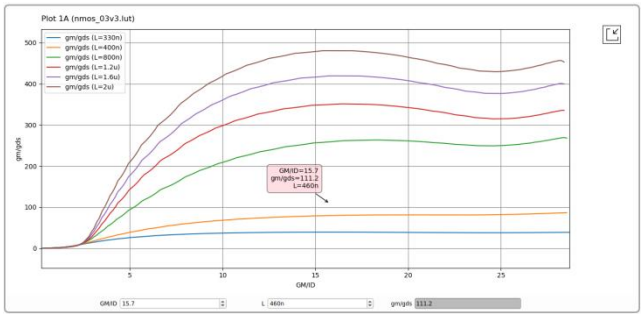






We used NMOS input stage, as we can see that the range of the VINCM is close to VDD and away from ground.

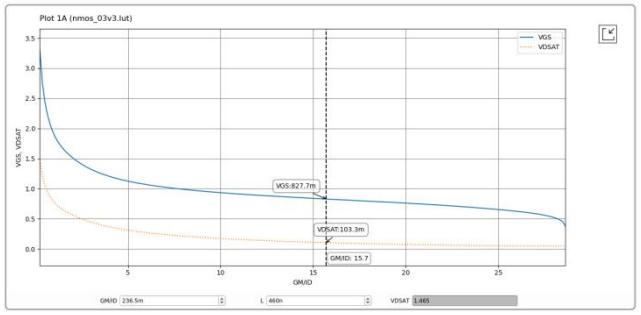
Detailed design procedure and hand analysis:



Input pair:

$A_o = \frac{g_{m0,1}\, r_o}{2} = 34\ \text{dB}, \therefore g_{m0,1}\, r_o = 100.2$

Sweeping the DC gain over g_m over I_D then we got the value of L, L = 460nm

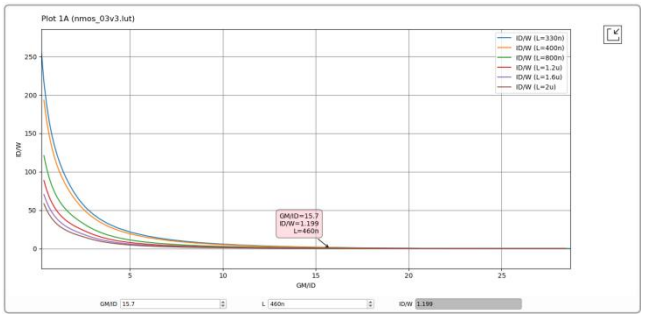


$GBW = \frac{g_{m0,1}}{2\pi C_L} = 10\ \text{MHz} \therefore g_{m0,1} = 100\pi\ \mu\text{S}$

Assume $g_m/I_D = 5\pi = 15.7\ V^{-1}$

Then $I_D / W = 1\ \mu A/\mu m$ Then $W = 16.6\ \mu m$

But after design we found that $W = 20\ \mu m$ is the most suitable value for the input pair

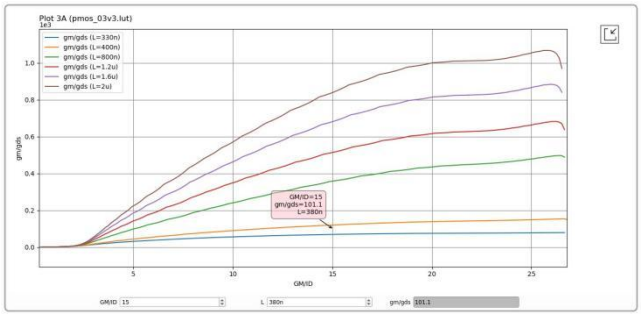


We got the value of:
$V_{GS} = 827\ \text{mV}$ $V_{DSAT} = 105\text{mV}$

Cascoded PMOS devices:

Assume $g_m/I_D = 15\ V^{-1}$, $g_m = 300\ \mu S$, and we have the value of r_o from the previous design, then $g_{m2,3}\, r_o = 95.68$

Now we got the value of L, L = 380 nm.



Using the spec: $V_{IN,MAX} \geq 1.5$:

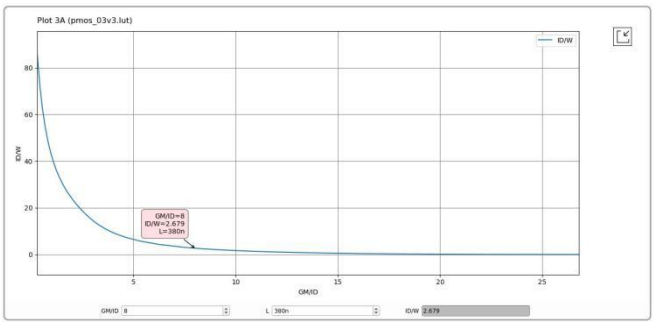
$V_{IN,MAX} = V_{DD} - V_{SG} + V_{GS} - V_{DSAT} \geq 1.5$

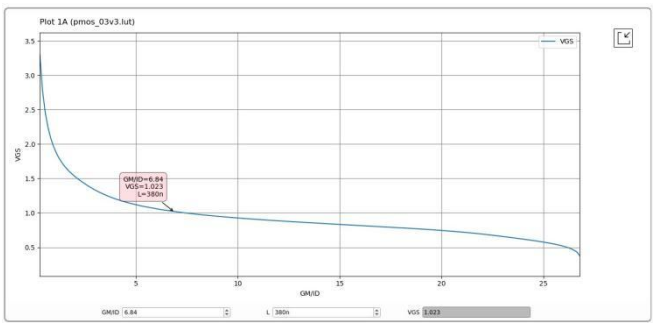
$1.8 - 1.5 + 0.827 - 0.103 \geq V_{SG}$

Then $1.023 \geq V_{SG}$

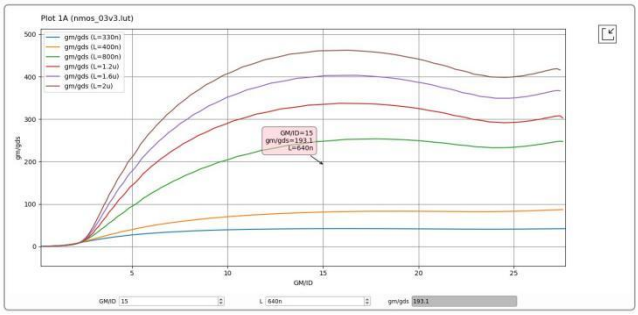
we got the right value of g_m / I_D, $g_m / I_D = 8$.

Then $I_D / W = 2.679\ \mu A/\mu m$ Then $W = 8\ \mu m$





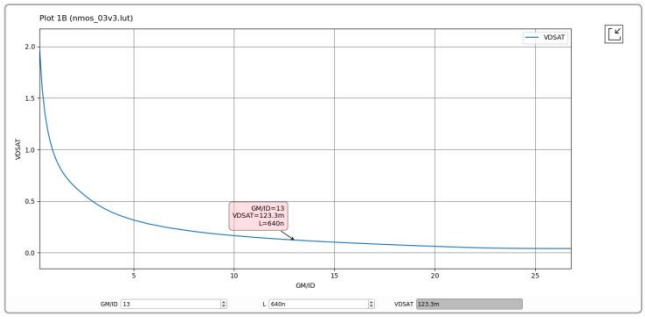
Current mirror sizing:



$$\text{CMRR} = \frac{g_{m0,1}\, r_o}{2} 2g_{m2,3}r_{o5},\ \therefore r_{o5} = 312562\ \text{ohm}$$

Assume $g_m/I_D = 15\ V^{-1}$, $g_{m5} = 600\ \mu S$

$\therefore g_{m5}\, r_{o5} = 187$ $\quad$ $L = 640$ nm

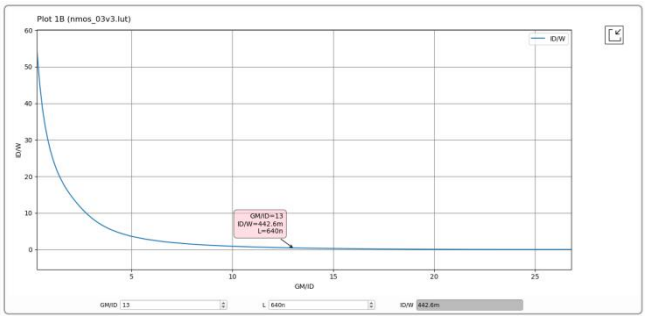


Using the spec: $V_{IN,MAX} \leq 1$:

$V_{IN,MIN} = V_{GS} + V_{DSAT,5} \leq 1$

Then $0.173 \geq V_{DSAT}$

we got the right value of g_m / I_D, $g_m / I_D = 13$.



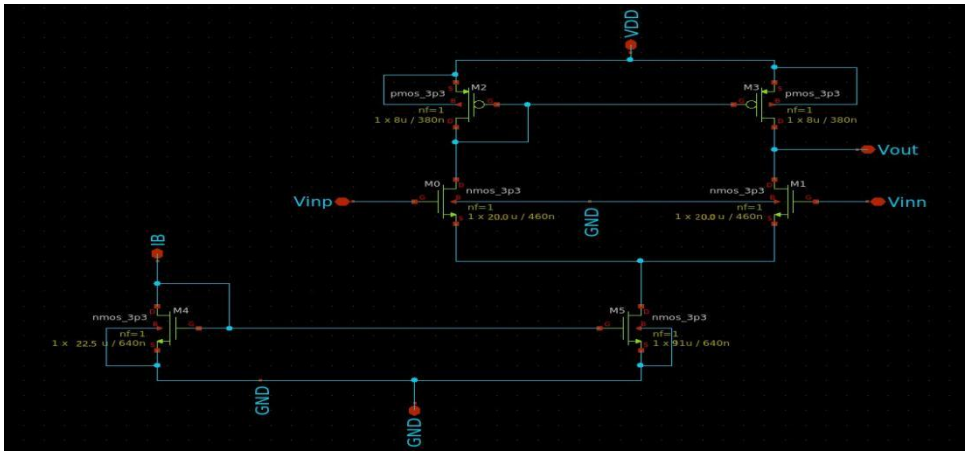
Then $I_D / W = 0.442\ \mu A/\mu m$ $\quad$ Then $W = 90\ \mu m$

Now we can deduce the size of the reference device M4:

$L = 640$ nm $\quad$ $W = 90 / 4 = 23\ \mu m$

	M0	M1	M2	M3	M4	M5
W	20 um	20 um	8 um	8 um	23 um	90 um
L	460 nm	460 nm	380 nm	380 nm	640 nm	640 nm
g_m	100π µS	100π µS	300 µS	300 µS	520 µS	520 µS
I_D	20 µA	20 µA	20 µA	20 µA	10 µA	40 µA
g_m / I_D	5π V^{-1}	5π V^{-1}	8 V^{-1}	8 V^{-1}	13 V^{-1}	13 V^{-1}
V_{DSAT}	103 mV	103 mV	219 mV	219 mV	123 mV	123 mV
V_{OV}	29 mV	29 mV	296 mV	296 mV	97 mV	97 mV
V^*	127 mV	127 mV	250mV	250mV	153 mV	153 mV

Part 3: OTA OPEN LOOP SIMULATION:



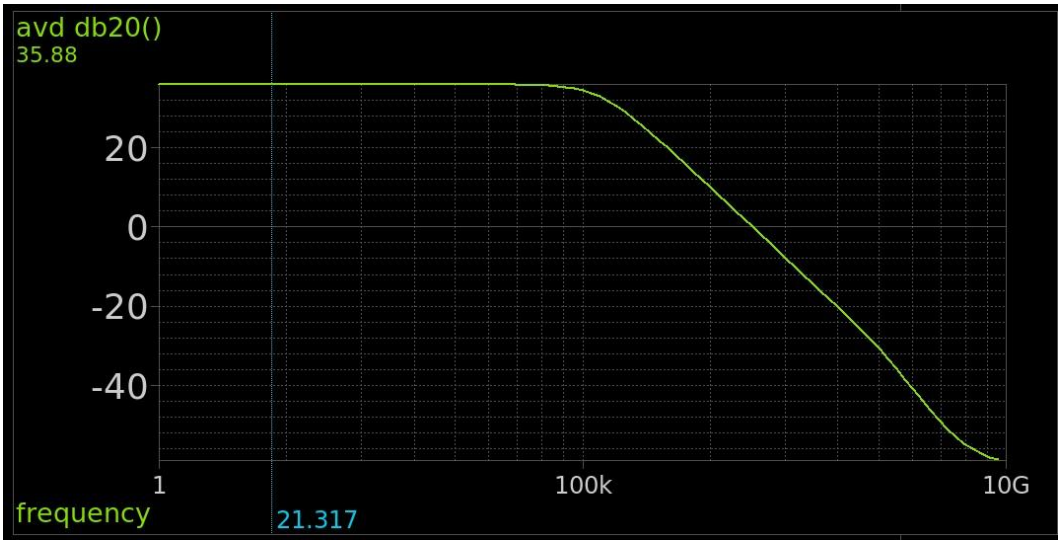
```
f2                =  1.567980e+05
peak = 6.399306e+01
f2 = 1.567980e+05
gbw = 1.003398e+07
 BSIM4v5: Berkeley Short Channel IGFET Model-4
     device           m.x1.xm4.m0          m.x1.xm5.m0          m.x1.xm3.m0
      model           nmos_3p3.13          nmos_3p3.13           pmos_3p3.8
         gm          0.000183113          0.000725042          0.000156271
       gmbs          6.74608e-05          0.000267011          6.34088e-05
        gds          8.37325e-07          4.13585e-06          1.71904e-06
        vds             0.694392             0.402934             0.985093
      vdsat            0.0810139             0.080989             0.220791
        vgs             0.694393             0.694393             0.985097
        vth             0.702963              0.70302             0.774523
         id                1e-05          3.94006e-05          1.97003e-05

 BSIM4v5: Berkeley Short Channel IGFET Model-4
     device           m.x1.xm2.m0          m.x1.xm1.m0          m.x1.xm0.m0
      model           pmos_3p3.8           nmos_3p3.12          nmos_3p3.12
         gm          0.000156271          0.000321908          0.000321908
       gmbs          6.34088e-05          8.93451e-05          8.93451e-05
        gds          1.71904e-06          3.28371e-06          3.28371e-06
        vds             0.985093             0.411962             0.411962
      vdsat             0.220791            0.0974711            0.0974711
        vgs             0.985097             0.847064             0.847064
        vth             0.774523             0.830341             0.830341
         id          1.97003e-05          1.97003e-05          1.97003e-05

binary raw file "OTA_TB.raw"
ngspice 1 ->
```

from these results, we can see that I_D and g_m of the input pairs are exactly equal, and the reason for that is that is if we assumed the current is high in a branch, then it is should be low in the other branch, but this assumption always wrong, so they are equal.

- the DC voltage at $V_{out} = V_{DS,0} + V_{DS,5} = 0.813$ V

Diff small signal:

Diff gain VS freq:




```
f2                =  1.607189e+05
peak = 6.225101e+01
f2 = 1.607189e+05
gbw = 1.000491e+07
```

Hand analysis calculation:

$$A_{vd} = g_{m0,1}\,(r_{o3}//r_{o1}) = 321\times10^{-6}\times(304878\,//\,584795) = 64.32 = 36\ \text{dB}$$

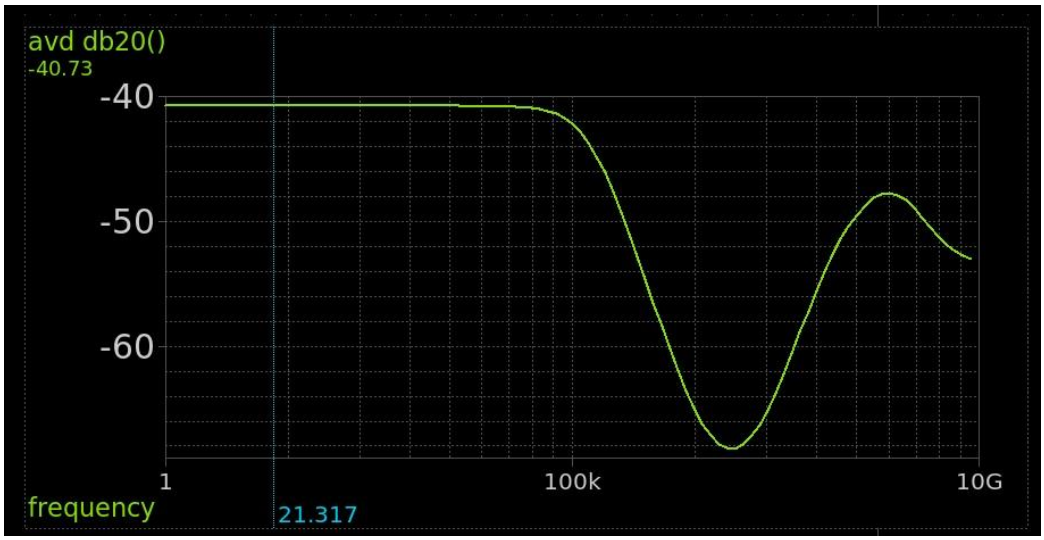
$$BW \approx \frac{1}{2\pi C_L(r_{o3}//r_{o1})} \approx \frac{1}{2\pi\times5\times10^{-12}\times(304878\,//\,584795)} \approx 158.83\ \text{kHz}$$

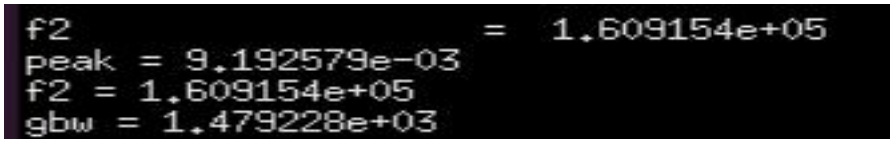
$$GBW = A_{vd}\times BW = \frac{g_{m0,1}}{2\pi C_L} = \frac{1}{2\pi\times5\times10^{-12}} = 10.21\ \text{MHz}$$

	Analytical soltution	Simulation
DC gain	64.32 | 36 dB	62.25 | 35.88 dB
Band width	158.83 kHz	160.7 kHz
GBW	10.21 MHz	10.04 MHz

CM small signal:

CM gain VS freq:





Hand analysis calculation:

$$A_{vcm} \approx \frac{-1}{2g_{m2,3}r_{o5}} \approx \frac{-1}{2\times156\times10^{-6}\times241837} = -12.8\times10^{-3} = -37.8\ \text{dB}$$

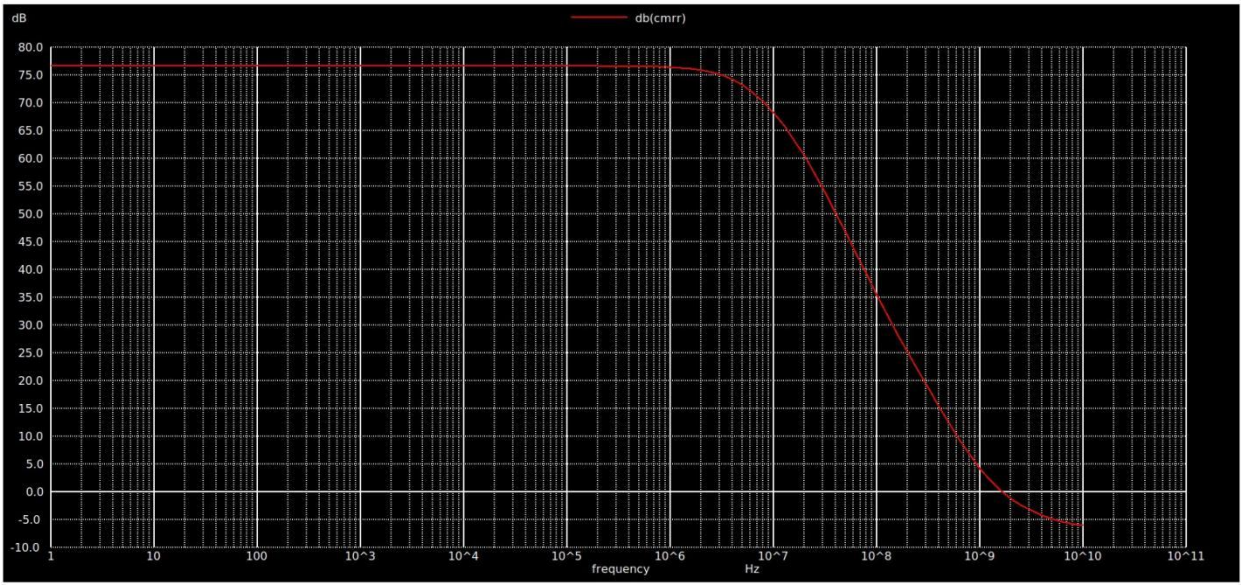
$$BW = \frac{1}{2\pi C_L(r_{o3}//r_{o1})} \approx \frac{1}{2\pi\times5\times10^{-12}\times(304878\,//\,584795)} \approx 158.83\ \text{kHz}$$

$$GBW = |A_{vcm}|\times BW = 12.8\times10^{-3}\times158.83 = 2025\ \text{Hz}$$

	Analytical soltution	Simulation
DC gain	0.0128 | -37.8 dB	0.00919 | -40.73 dB
Band width	158.83 kHz	160.9 kHz
GBW	2.02 kHz	1.47 kHz

CMRR simulation:

CMRR vs frequency:

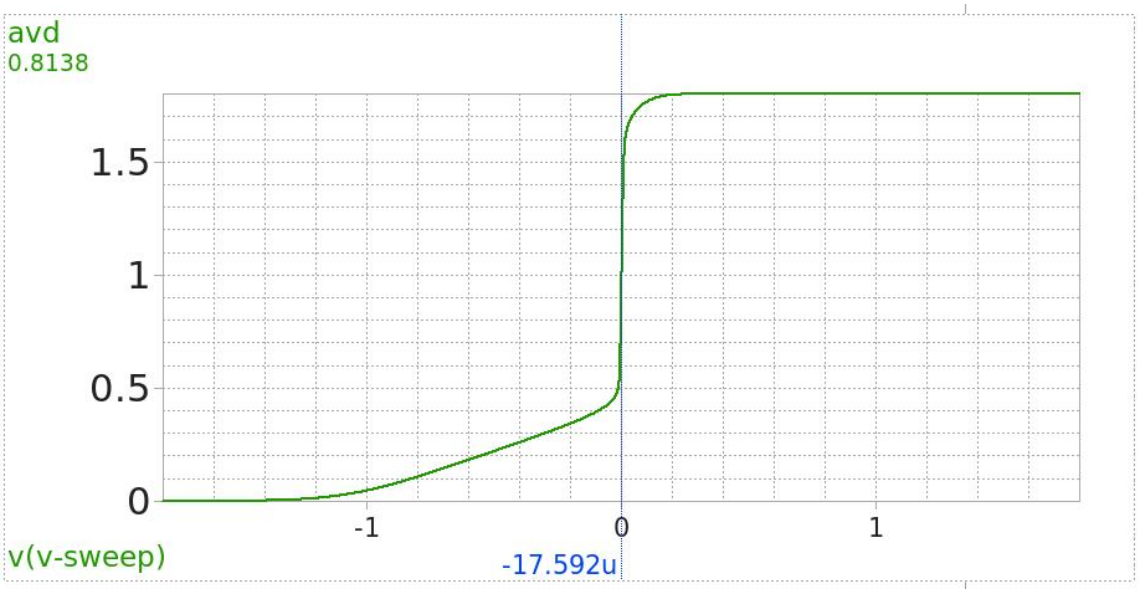


$$\text{CMRR} = \frac{A_{vd}}{A_{vcm}} = g_{m0,1}\,(r_{o3}//r_{o1}).\,2g_{m2,3}r_{o5} = 5016 = 74\ \text{dB}$$

	Analytical soltution	Simulation
CMRR	5016 | 74 dB	6760 | 76.6 dB

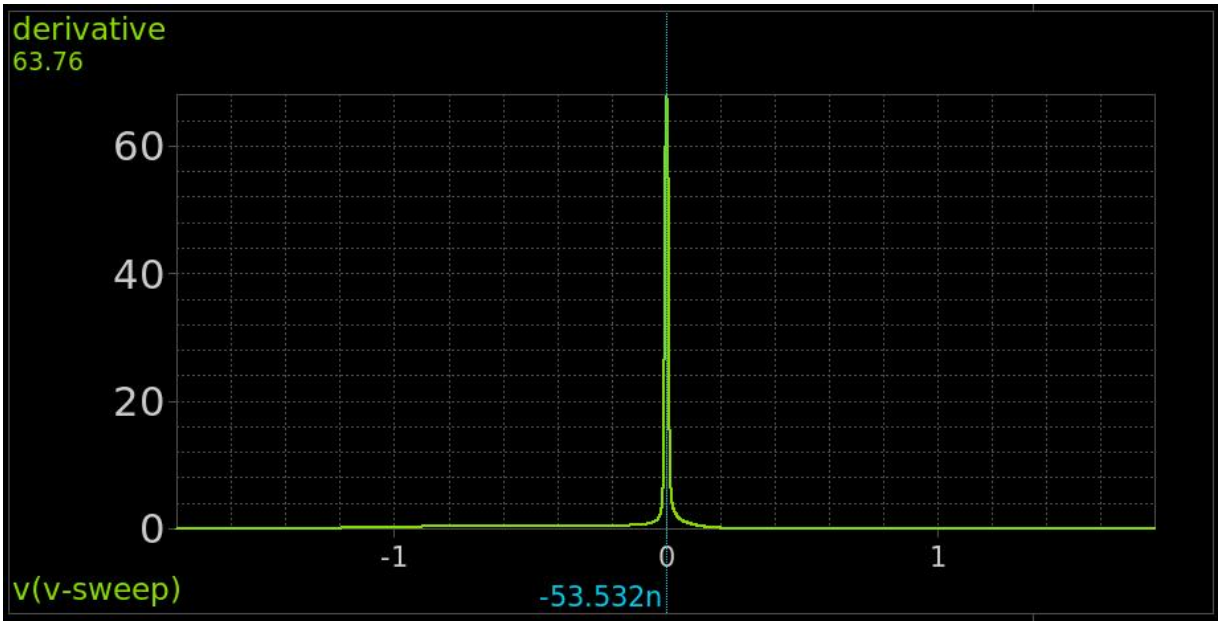
DIff large signal analysis:

V_{OD} vs V_{ID} :



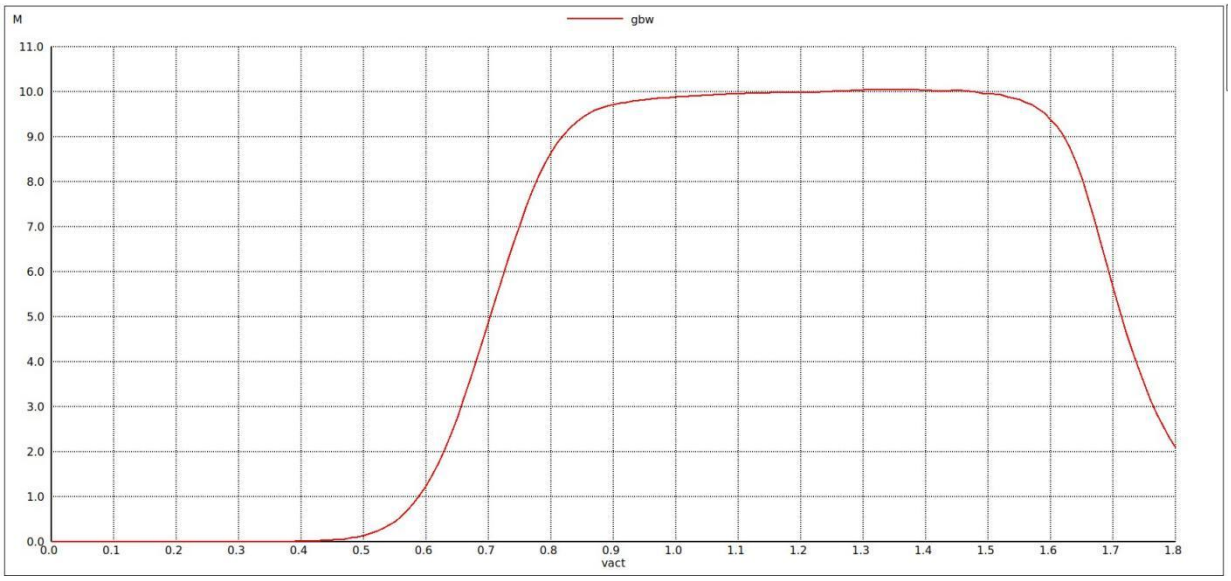
At $V_{ID} = 0$, $V_{OD} = 0.813$ V

Derivative of V_{OD} VS V_{ID}:



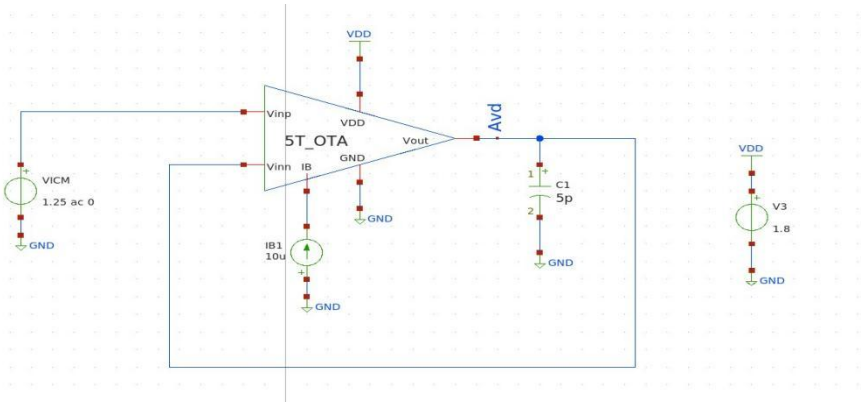
CM large signal:

GBW vs VINCM:




```
No. of Data Rows : 111
diffgain          =  3.815597e-01 at=  1.000000e+00
f3db              =  6.080836e+06
Warning from checkvalid: vector vicm is not available or has zero length.
Error: RHS "vact + vicm" invalid
binary raw file "OTA.raw"
vicmmax = 1.620000e+00
vicmmin = 8.100000e-01
ngspice 1 -> 
```

Part 4: closed_loop OTA simulation:



device	m.x1.xm4.m0	m.x1.xm5.m0	m.x1.xm3.m0
model	nmos_3p3.13	nmos_3p3.13	pmos_3p3.8
gm	0.000169102	0.000664931	0.000155517
gmbs	6.22864e-05	0.000244836	6.32366e-05
gds	7.61485e-07	3.66347e-06	2.57079e-06
vds	0.716397	0.444546	0.507385
vdsat	0.0913748	0.0913479	0.214834
vgs	0.716398	0.716398	0.979592
vth	0.702959	0.703012	0.776451
id	1e-05	3.91443e-05	1.90823e-05

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x1.xm2.m0	m.x1.xm1.m0	m.x1.xm0.m0
model	pmos_3p3.8	nmos_3p3.12	nmos_3p3.12
gm	0.000162764	0.000316257	0.000327548
gmbs	6.60272e-05	8.50252e-05	8.81051e-05
gds	1.7678e-06	2.59167e-06	3.70461e-06
vds	0.979588	0.848059	0.375855
vdsat	0.216179	0.0945382	0.0976603
vgs	0.979592	0.84806	0.855452
vth	0.774755	0.837224	0.838497
id	2.0062e-05	1.90823e-05	2.0062e-05

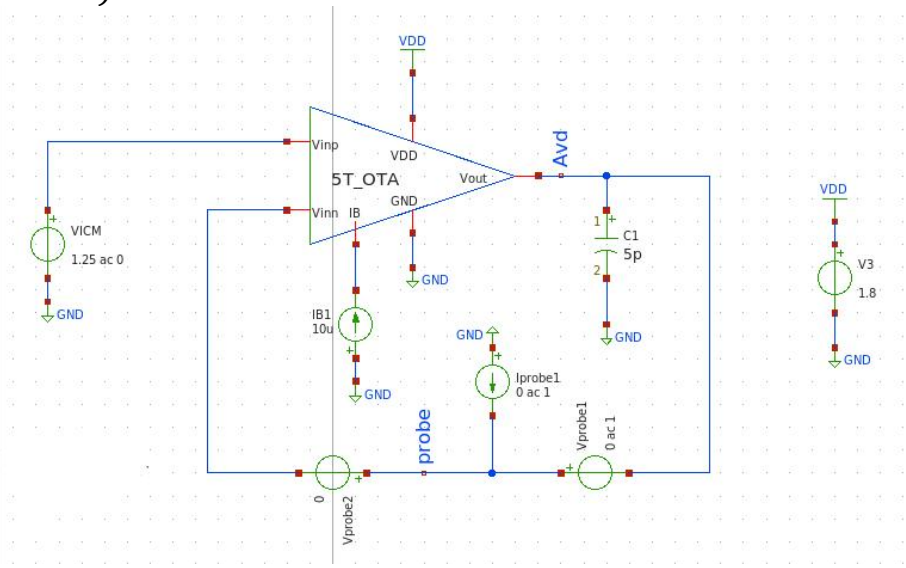
gm_mismatch = 1.129160e-05
id_mismatch = 9.797114e-07

From these results, it is clear that I_D and g_m for input pairs are not equal, and the reason for that is node of output no longer follow the drain node of the other input pair, then the current will be different because of CLM that make the current has some dependence on V_{DS}, then gm will be different, too. That case is opposite to OTA open loop case, as output node was following the drain node of the i/p pair.

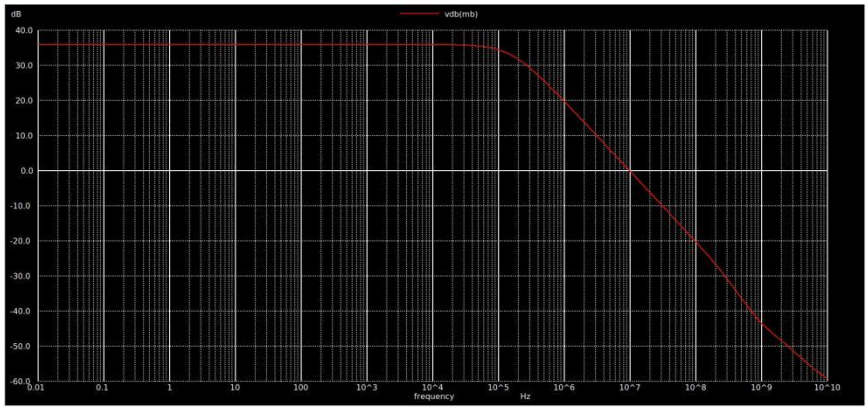
Mismatch in $g_m = \frac{327 - 321}{321} * 100 = 1.869\%$ Mismatch in $I_D = \frac{1.97 - 2.0062}{1.97} * 100 = 1.83\%$

Where $g_m = 321$ uS is the nominal value, and $I_D = 1.97$ uA is the nominal value.

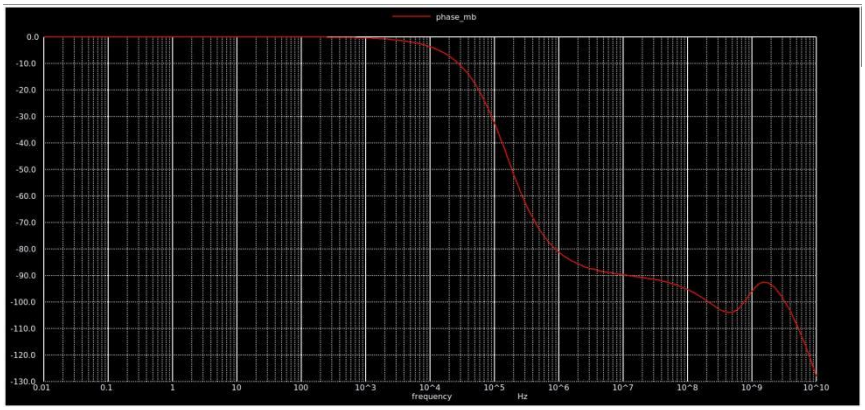
Loop gain (PM and GM):



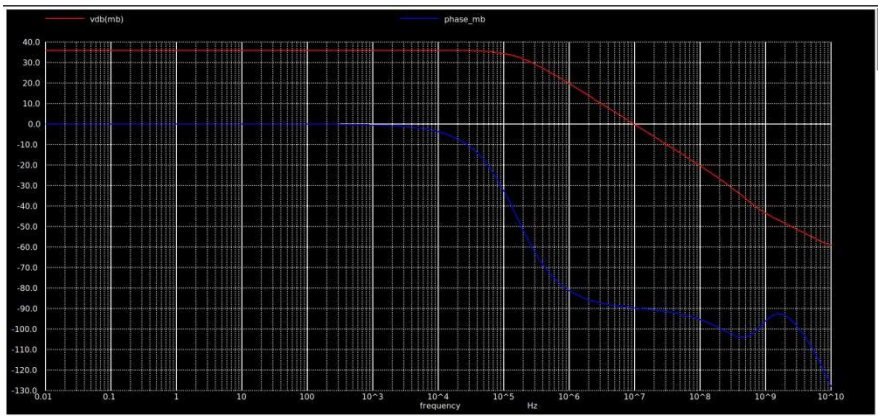
Loop gain vs frequency:



Phase vs frequency:



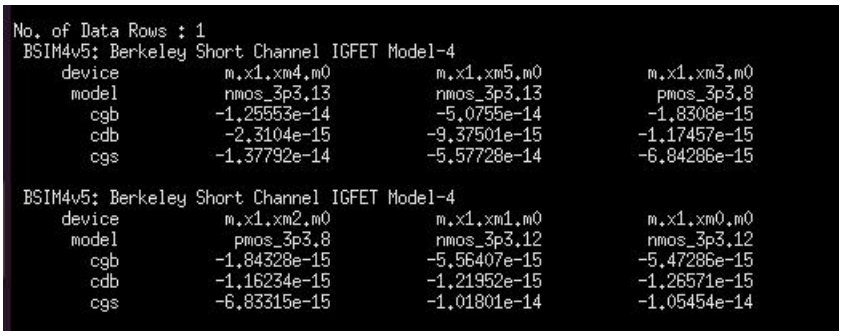
Phase and mag (overlaid) vs frequency:



Results and OP Point:

```
peak                =  6.277052e+01 at=  2.238721e+00

Error: measure  f1  when(WHEN) ; out of interval
 meas ac f1 when vmag(mb)=4.438546e+01 rise=1 failed!

bw                  =  1.562775e+05
pm_deg              =  -8.963814e+01
dominant_pole_f     =  9.812251e+06
loop_gain           =  3.595511e+01
gbw = 9.809620e+06
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000


No. of Data Rows : 1
 BSIM4v5: Berkeley Short Channel IGFET Model-4
     device          m.x1.xm4.m0          m.x1.xm5.m0          m.x1.xm3.m0
      model          nmos_3p3.13          nmos_3p3.13           pmos_3p3.8
         gm          0.000169102          0.000662842          0.000155954
       gmbs          6.22864e-05          0.000244055          6.33959e-05
        gds          7.61485e-07          3.85137e-06          2.39666e-06
        vds             0.716397             0.405886              0.55647
      vdsat            0.0913748             0.091344             0.214312
        vgs             0.716398             0.716398             0.978758
        vth             0.702959             0.703019             0.776274
         id                1e-05          3.89992e-05          1.90741e-05

 BSIM4v5: Berkeley Short Channel IGFET Model-4
     device          m.x1.xm2.m0          m.x1.xm1.m0          m.x1.xm0.m0
      model           pmos_3p3.8          nmos_3p3.12          nmos_3p3.12
         gm          0.00016219          0.000316191          0.000326149
       gmbs          6.57913e-05            8.648e-05          8.92431e-05
        gds          1.75842e-06          2.59567e-06          3.46715e-06
        vds             0.978754             0.837633             0.415349
      vdsat             0.215514            0.0943304            0.0970518
        vgs             0.978758             0.837635             0.844111
        vth             0.774758             0.826951             0.828073
         id          1.9925e-05          1.90741e-05          1.99255e-05
```

	Closed loop	Open loop
DC gain	62.7 | 35.95 dB	64.6 | 36.1 dB
GBW	9.81 MHz	10.04 MHz



```
No. of Data Rows : 1
 BSIM4v5: Berkeley Short Channel IGFET Model-4
    device          m.x1.xm4.m0          m.x1.xm5.m0          m.x1.xm3.m0
     model          nmos_3p3.13          nmos_3p3.13          pmos_3p3.8
       cgb        -1.25553e-14          -5.0755e-14         -1.8308e-15
       cdb         -2.3104e-15         -9.37501e-15        -1.17457e-15
       cgs        -1.37792e-14         -5.57728e-14        -6.84286e-15

 BSIM4v5: Berkeley Short Channel IGFET Model-4
    device          m.x1.xm2.m0          m.x1.xm1.m0          m.x1.xm0.m0
     model           pmos_3p3.8          nmos_3p3.12          nmos_3p3.12
       cgb        -1.84328e-15         -5.56407e-15        -5.47286e-15
       cdb        -1.16234e-15         -1.21952e-15        -1.26571e-15
       cgs        -6.83315e-15         -1.01801e-14        -1.05454e-14
```

Hand analysis calculations:
As we connected the gate of M1 with the output node, then parasetic capacitance will increase, which means that BW will decrease, then GBW will decrease.

$$A_{v-\text{loop gain}} = \beta A_{vd} = 321 \times 10^{-6} \times (418410 // 386100) = 63.45 = 36\ \text{dB}$$

The equivalent output capacitance, $C_{out} = C_L + 2C_{gs,1} + C_{db,1} + C_{db,3} + C_{gb,1}$
We can see that there are additional parasetic caps.

$$\text{BW} \approx \frac{1}{2\pi C_{out}(r_{o3} // r_{o1})} \approx \frac{1}{2\pi \times 5.0315 \times 10^{-12} \times (304878 // 584795)} \approx 157.5\ \text{kHz}$$

$$\text{GBW} = A_{vd} \times \text{BW} = \frac{g_{m0,1}}{2\pi C_{out}} = \frac{1}{2\pi \times 5.0315 \times 10^{-12}} = 9.995\ \text{MHz}$$

	Hand analysis	simulation
DC gain	63.45 | 36 dB	62.7 |35.95 dB
GBW	9.995 MHz	9.84 MHz