Self-Biased Sub-1V Bandgap Reference Circuit

Under supervision of:

Dr. Hesham Omran
TA. Moatasem bayoumy
TA. Ahmed Muhammed

Specs required for the band gap reference circuit:

Technology	**65nm**
Supply voltage	**2**
Corners	**Temp: -40 to 125** **Process: SS, SF, FS, FF**
Output voltage	**0.8**
Bias current	**< 10uA**
Phase margin	**> 60°**

BGR core circuit:

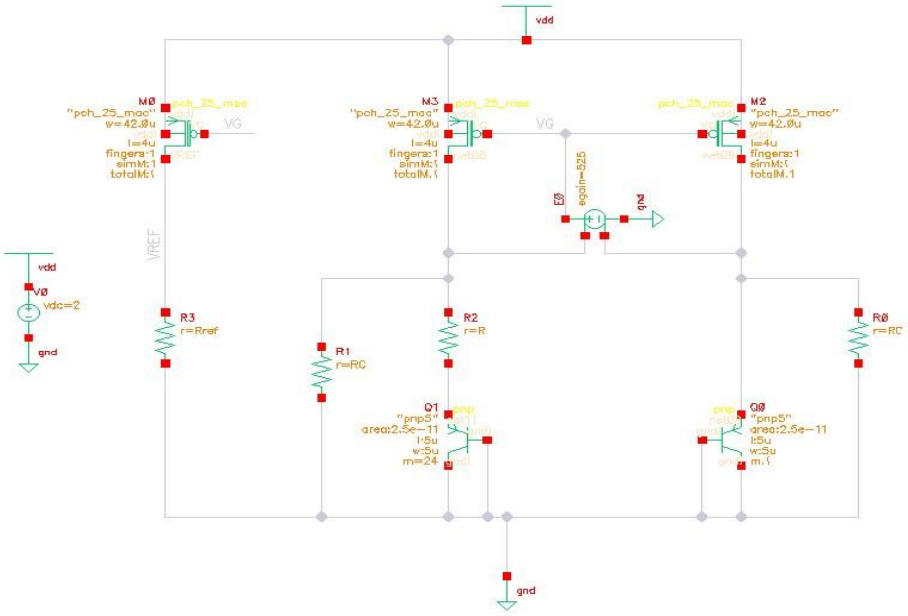

Figure 1 Schematics with device sizing

Hand analysis of the core circuit:

- After getting the characteristics of the BJT:
- Assume current in each branch = 1 µA

$$V_{BE,Q0} = 660.2\ mV$$

$$V_{BE,Q1} = 577.3\ mV$$

$$\Delta V_{BE} = 82.7\ mV$$

$$\therefore \mathrm{R_2} = \frac{\Delta V_{BE}}{\mathrm{I}/2} = 165.4\ \mathrm{kohm}$$

$$R_{1,3} = \frac{V_{BE,Q0}}{\mathrm{I}/2} = 1.3204\ Mohm$$

$$R_{REF} = \frac{V_{REF}}{I} = 800\ kohm$$

Design of the PMOS devices:

The considerations I took in my design are:

- The inversion level of the devices is week.
- large length, to avoid mismatch.

DC OP of the core circuit:

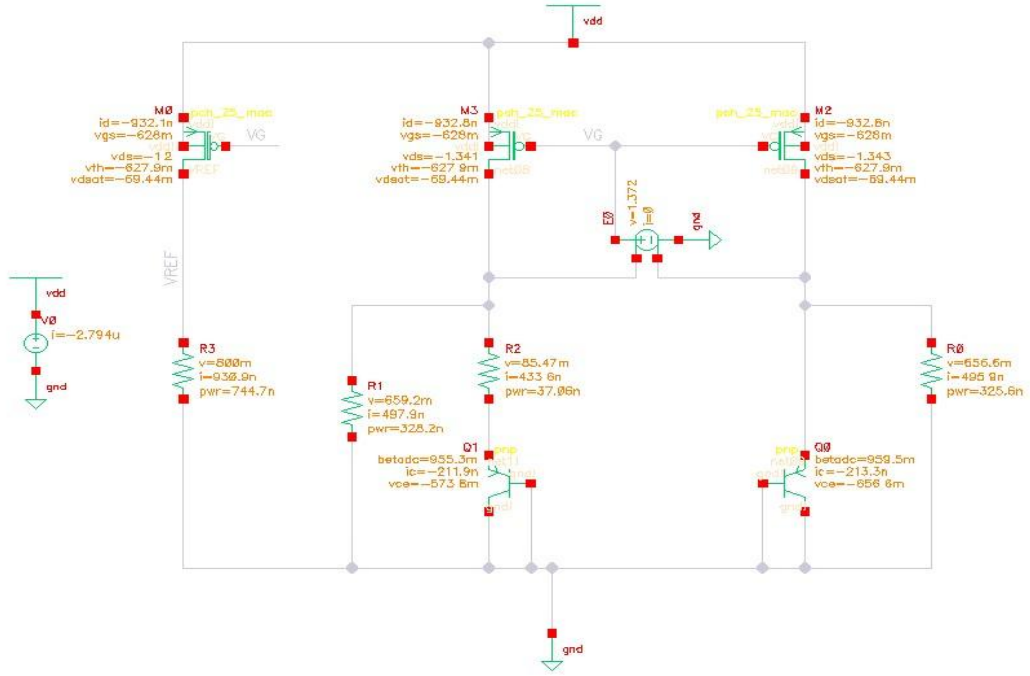

Figure 2 Schematics with DC OP and node voltages annotated

V_{REF} VS temp across nominal corners:

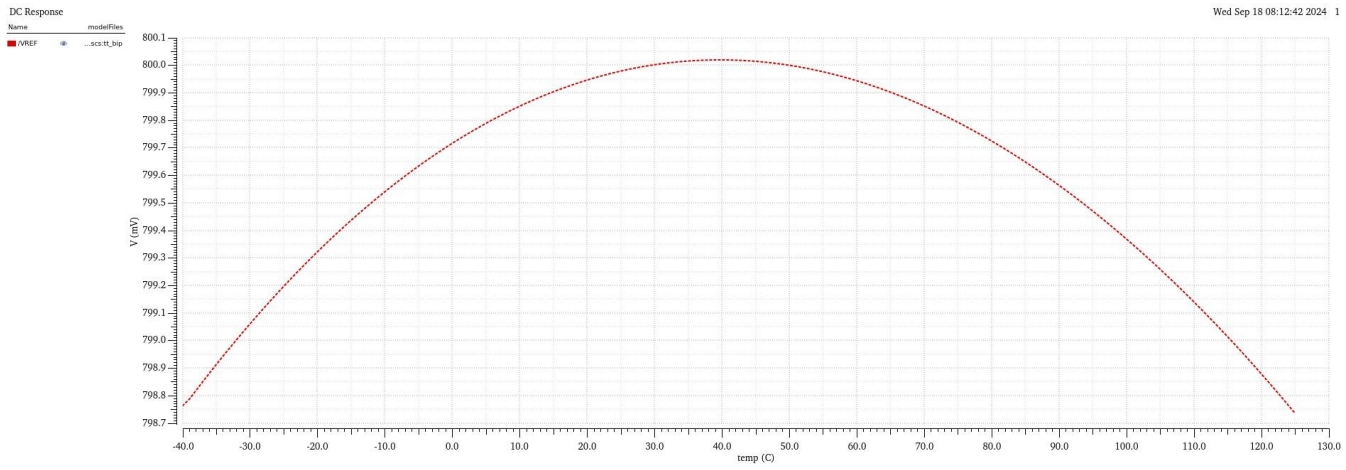

Figure 3 Change of reference voltage at nominal corners with temp

V_{ref} vs temperature (-40 to 125) at TT, SS, FF, SF, FS:

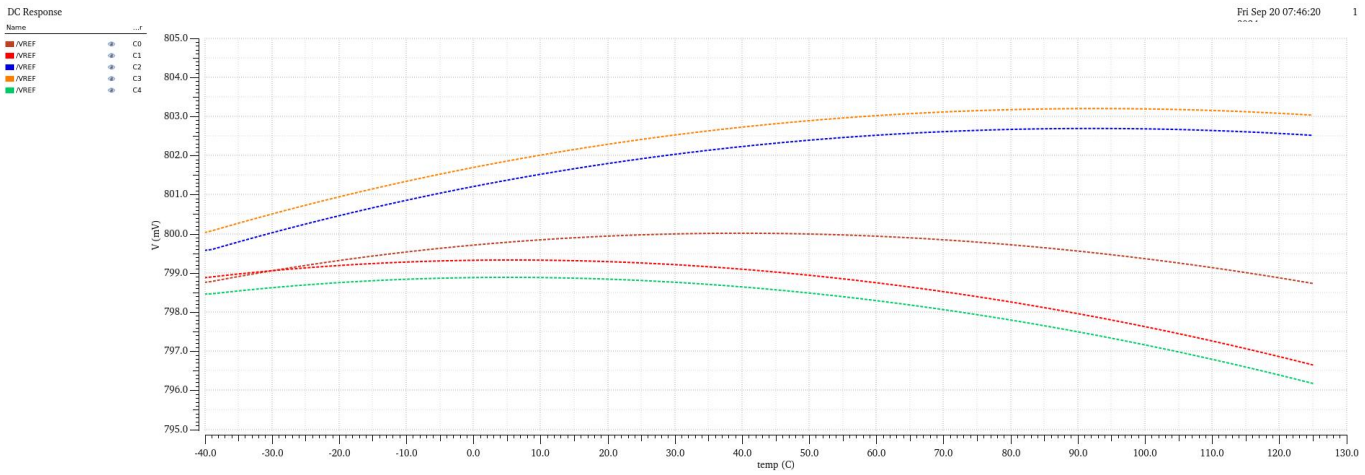

Figure 4 Change of reference voltage across corners with temp

Band gap reference circuit with actual error amplifier:

The consideration I took in designing the error amplifier:

- We need a high gain around 500.
- Current consumption in the OTA does not exceed 1 µA
- We designed the OTA so that its input pair has low V_{GS}, which means the device will be in the deep subthreshold region, so that the tail current source has a V_{dsat} margin and kept in saturation.

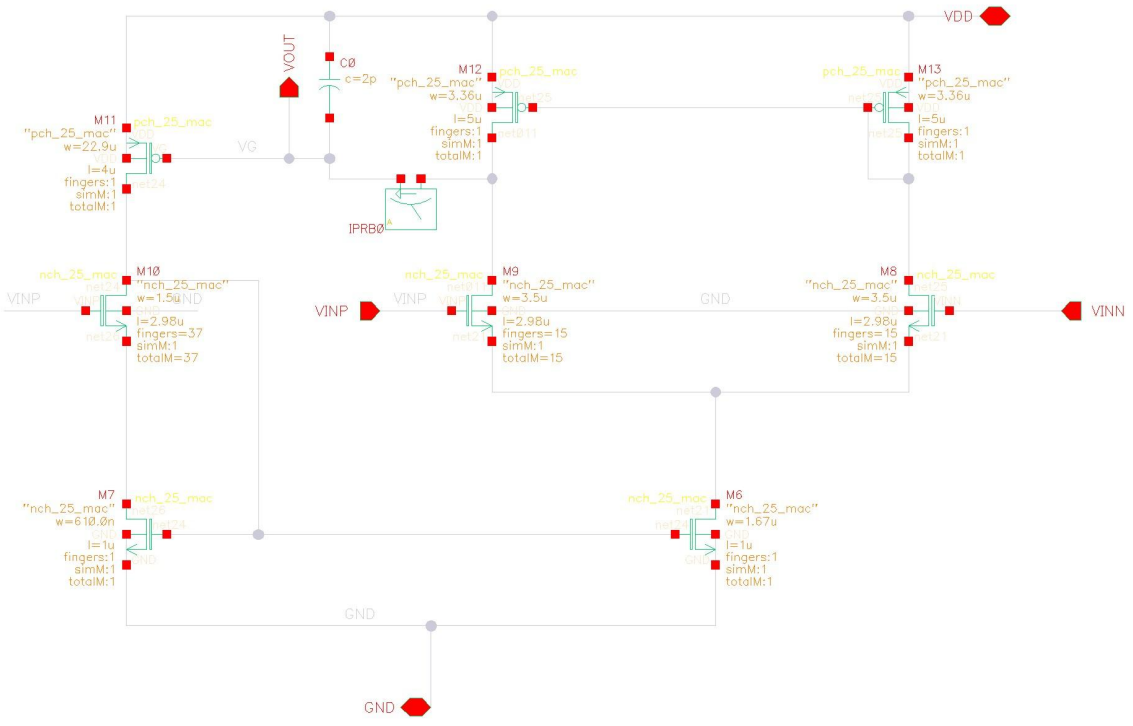

Figure 5 Schematics of the error amplifier with device sizing

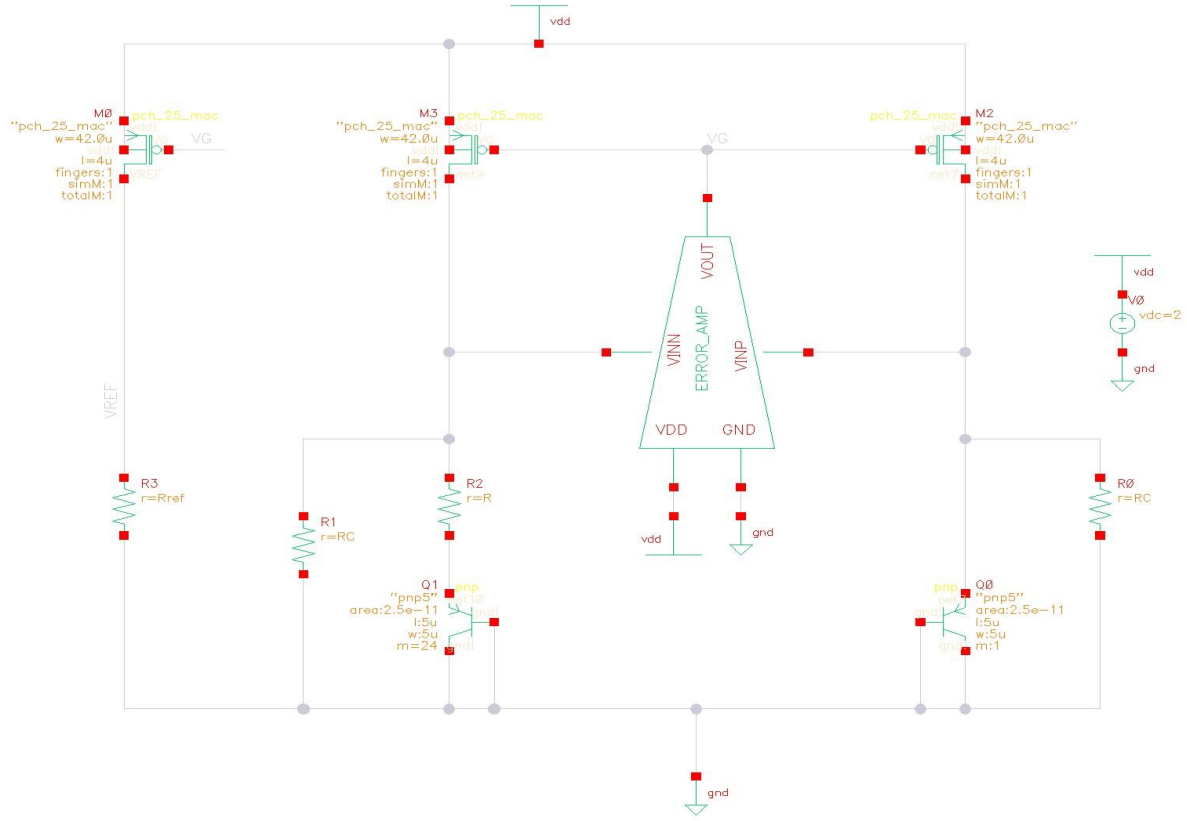

Figure 6 Schematics of whole circuit with device sizing

DC OP of core circuit and error amplifier:

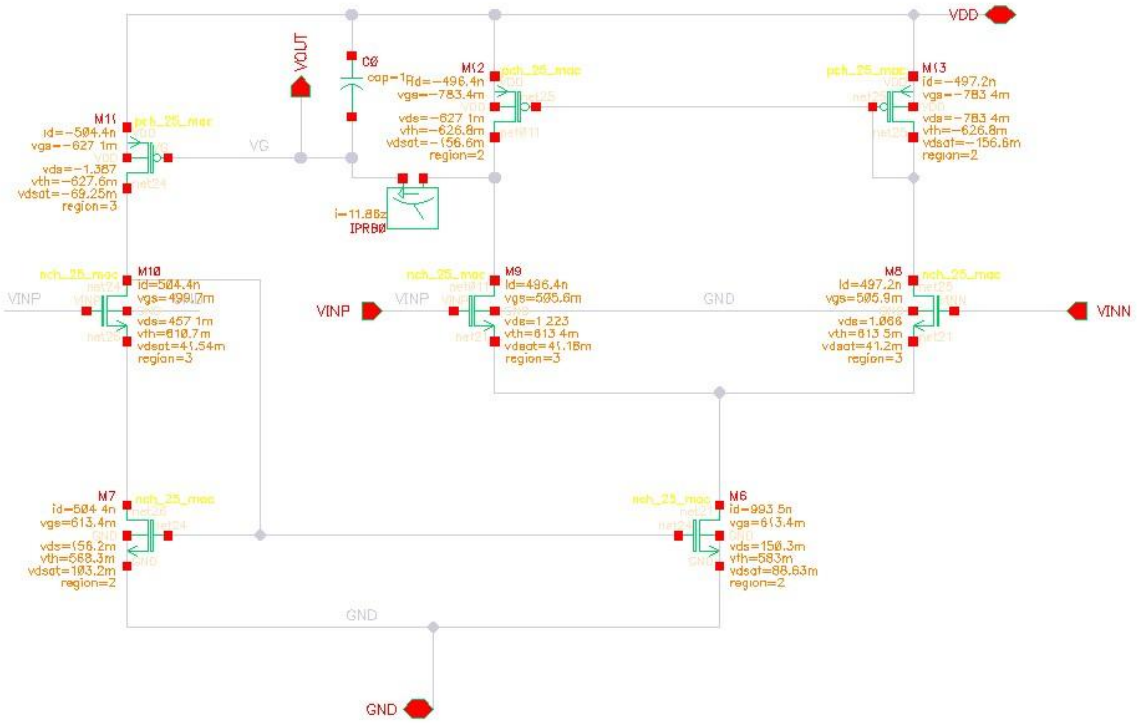

Figure 7 DC OP of the error amplifier

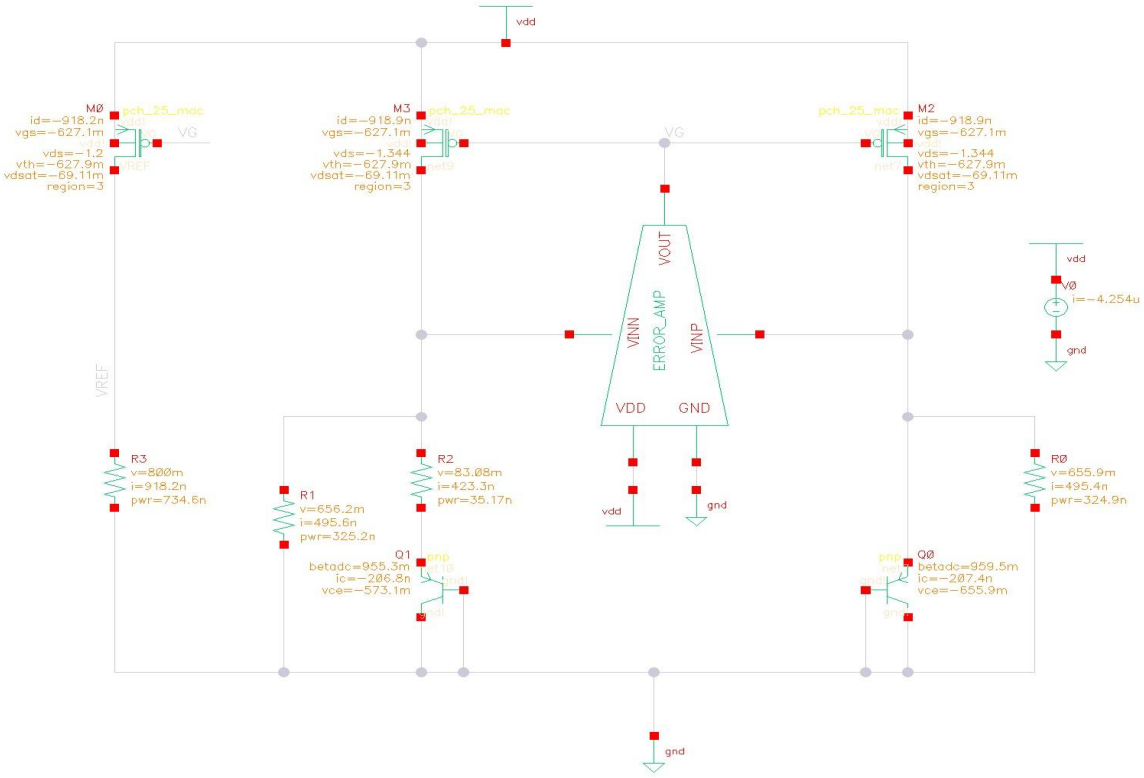

Figure 8 DC OP of the core circuit with actual error amplifier

V_{REF} VS temp across nominal corners:

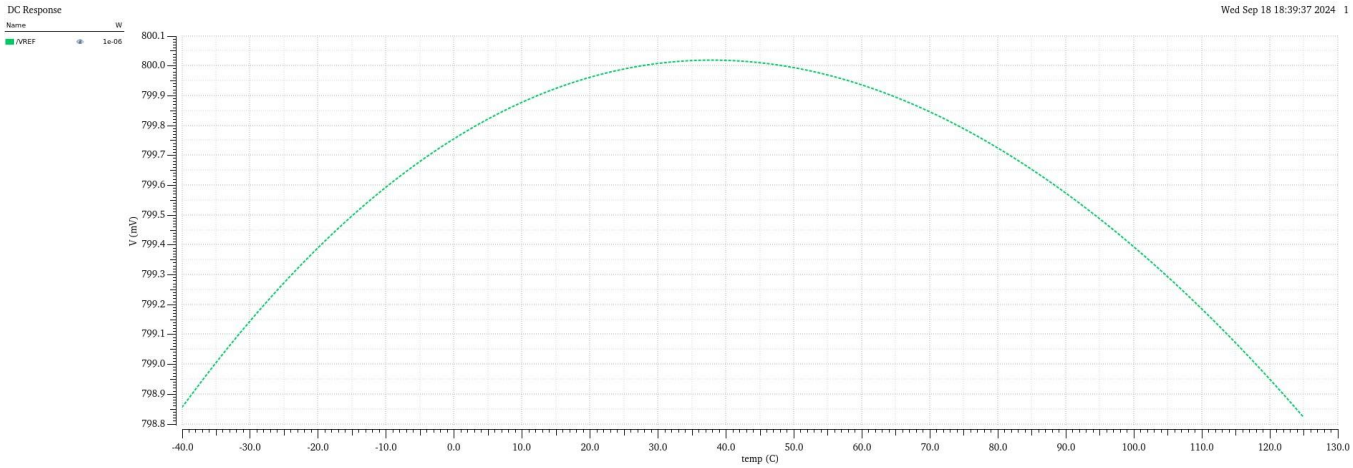

Figure 9 Change of reference voltage at nominal corners with temp

V_{ref} vs temperature (-40 to 125) at TT, SS, FF, SF, FS:

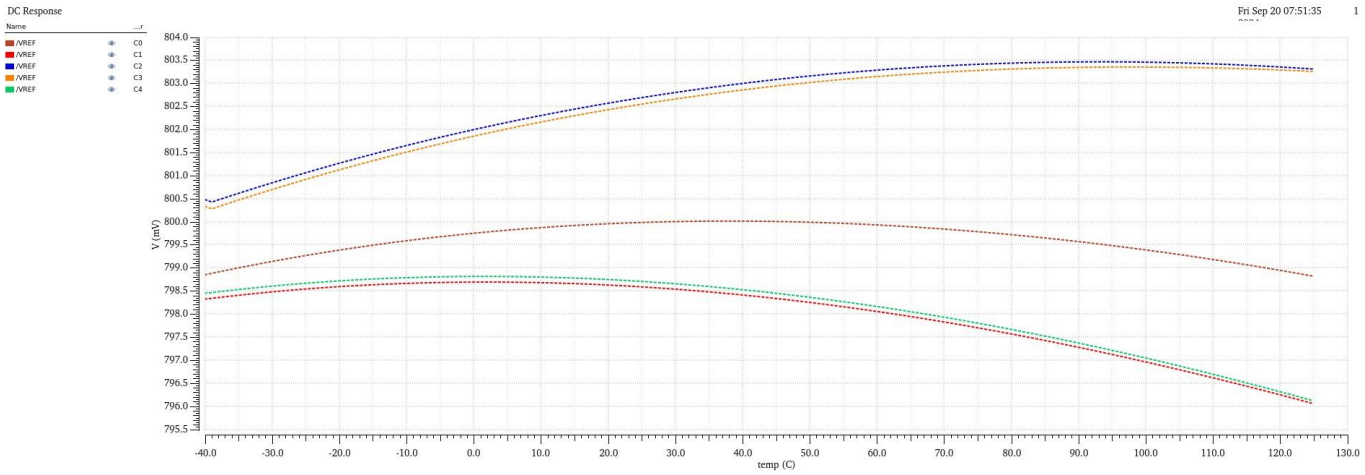

Figure 10 Change of reference voltage across corners with temp

STB analysis results:

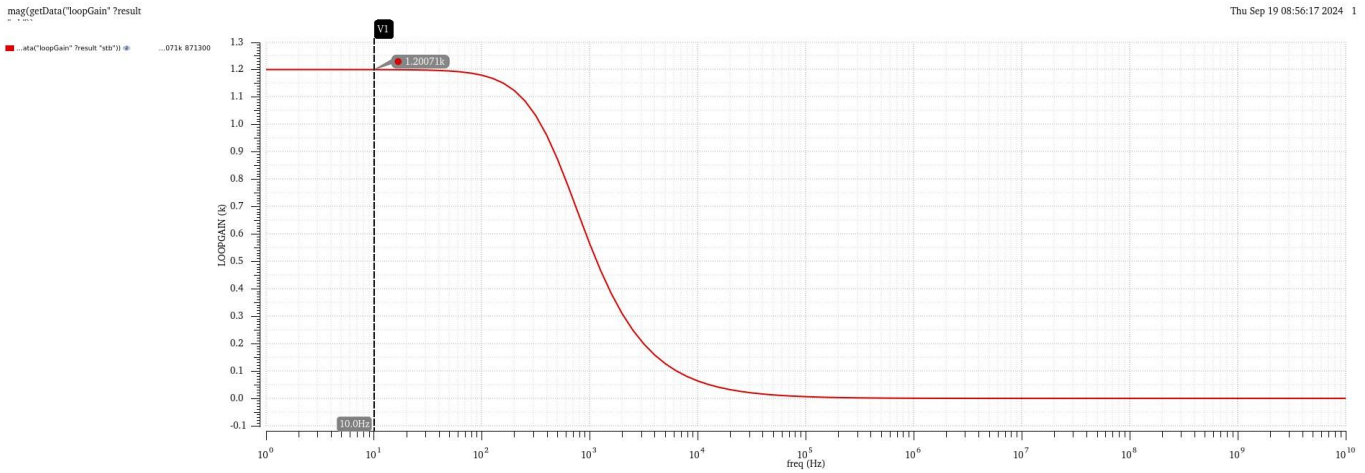

Figure 11 DC loop gain of the error amplifier

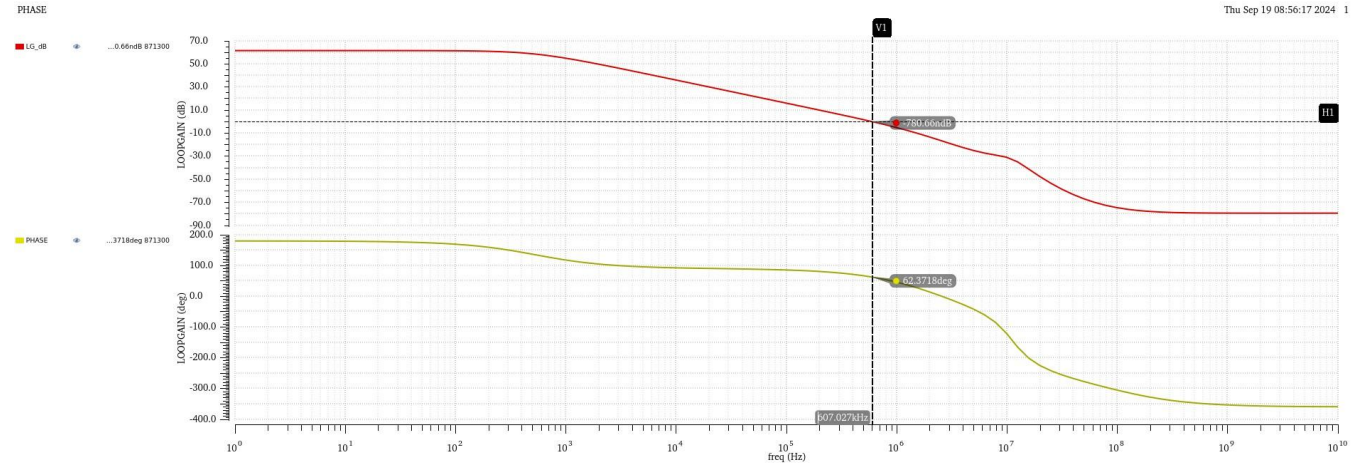

Figure 12 phase margin and unity gain frequency

	Parameter						C0	C1	C2	C3	C4
	crn65gplus_2...						tt_bip	ff_bip	ss_bip	ss_bip	ff_bip
	crn65gplus_2...						tt_25	ff_25	ss_25	fs_25	fs_25

Test	Output	Spec	Weight	Pass/Fail	Min	Max	C0	C1	C2	C3	C4
Design_challenge:Part_2:1	UGF				590.3k	625.1k	608.6k	595.3k	625.1k	592.7k	590.3k
Design_challenge:Part_2:1	phase margin	> 60		pass	61.16	63.45	62.26	62.91	61.16	63.04	63.45

Figure 13 change of UGF and phase margin across corners

Design of the start up circuit:

Consideration I took in designing the start up circuit:

- The PMOS transistor which will be off during the right operation of the circuit, must have large V_{GS}, about 1.2 V, to ensure that all V_{DD} dropped on it, so that the V_{GS} of the NMOS transistor that contributes in starting the circuit will be off.

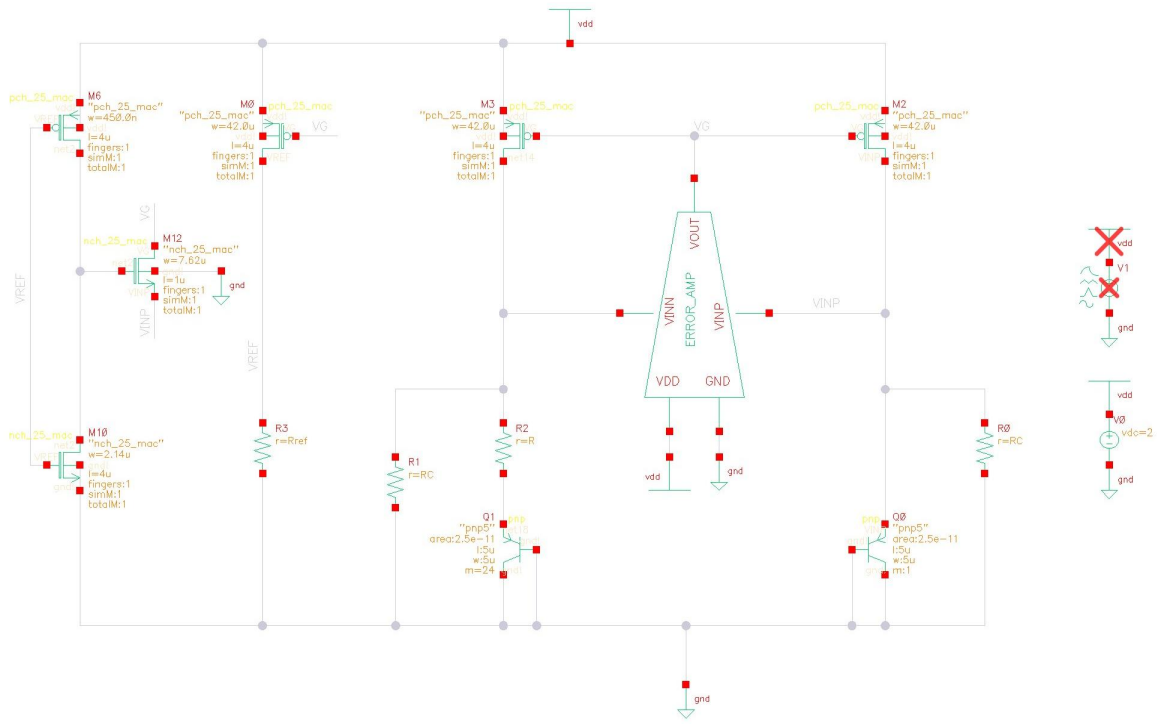

Figure 14 Schematics of whole circuit with device sizing

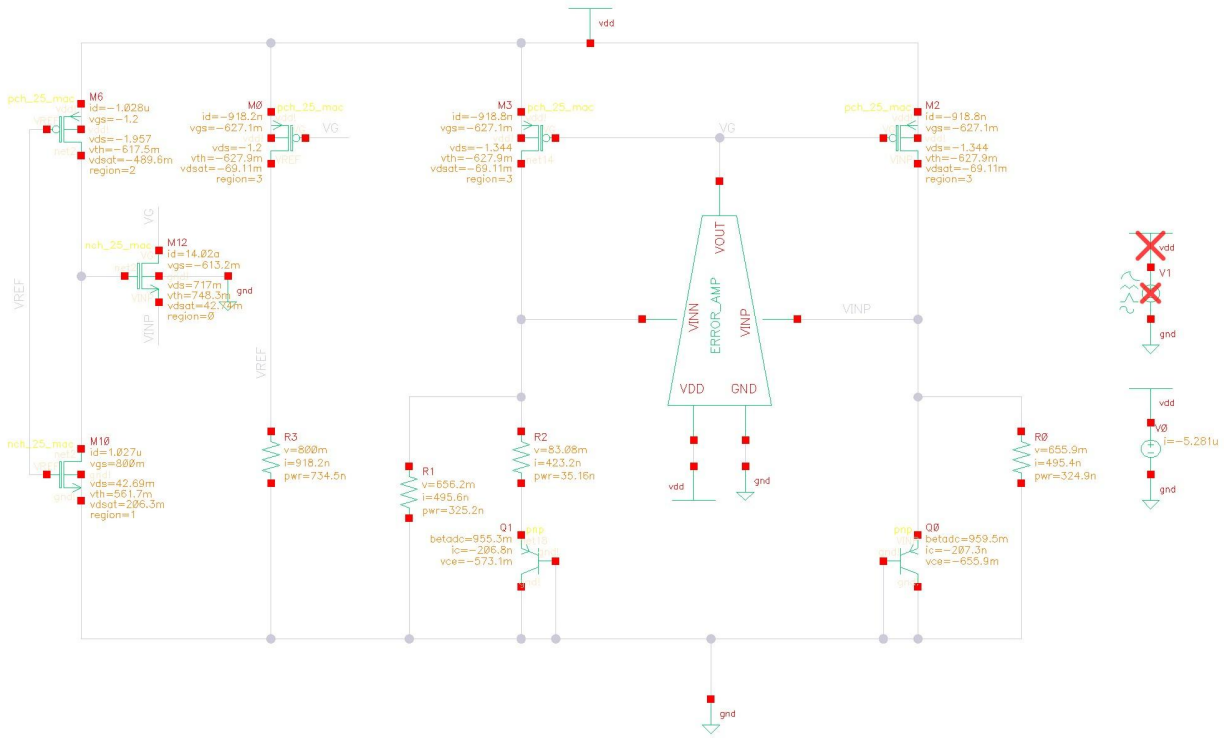

Figure 15 DC OP of the circuit with the start up circuit

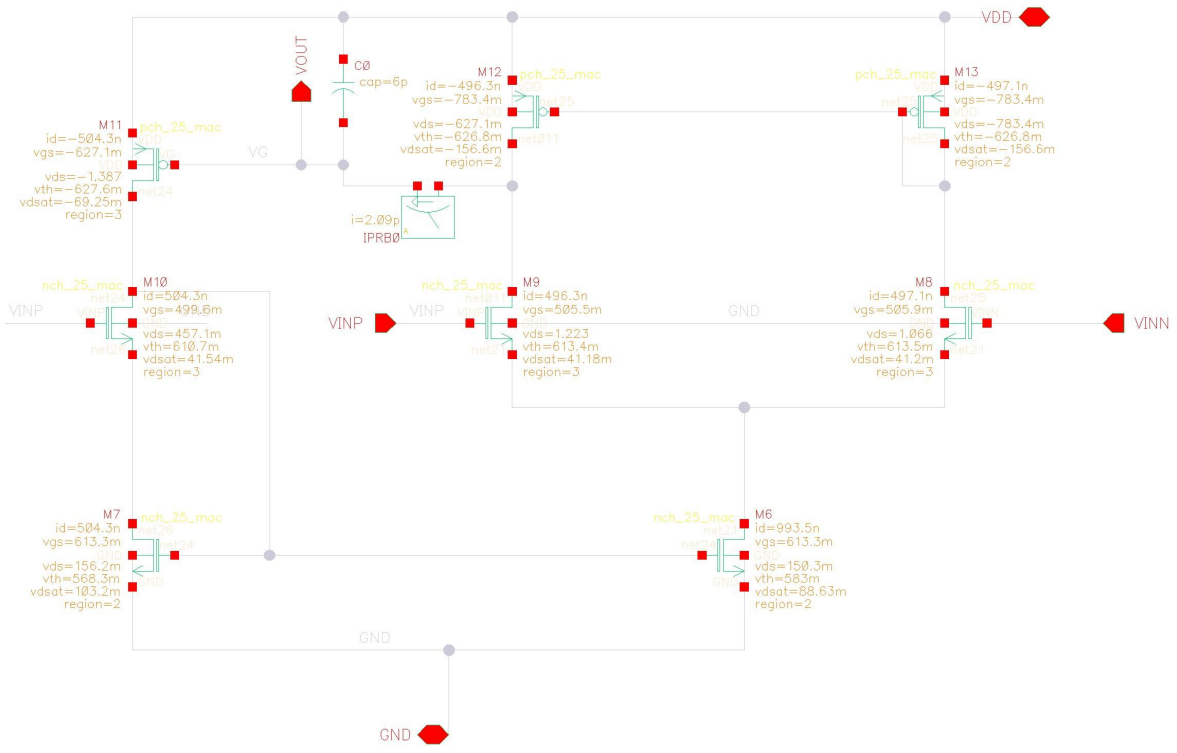

Figure 16 DC OP of the error amplifier

Transient simulation of V_{REF} as a ramp from (0,0) to (1ms,2V):

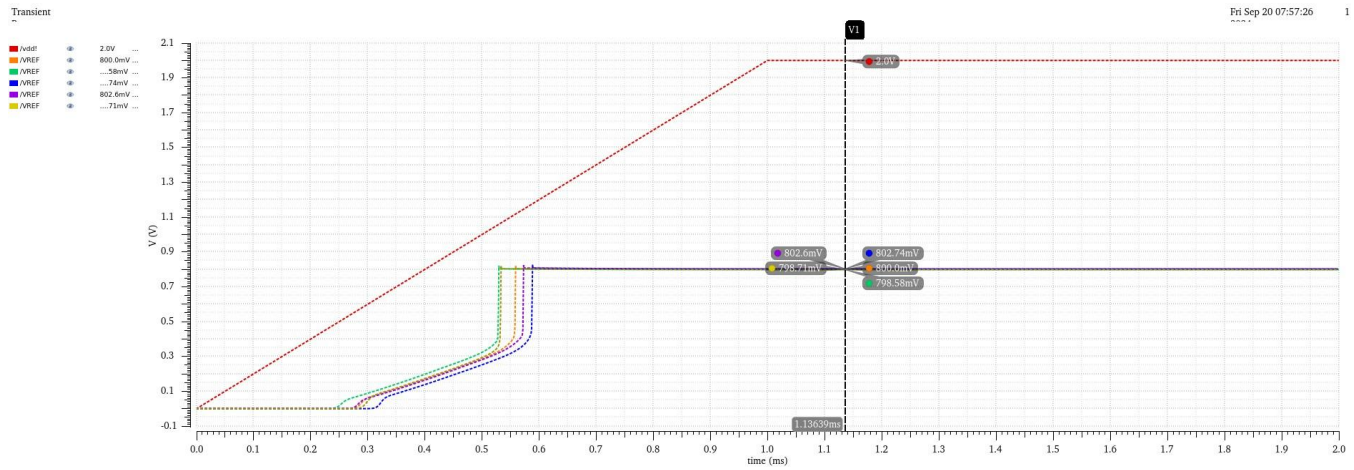

Figure 17 V_{DD} as a ramp and V_{REF} across corners

From these results, all specs are achieved:

- Spec of phase margin has been achieved: 62 deg
- Spec of power consumption has been ahieved: 5.28 µA
- Spec of V_{REF} has been achieved: 800 mV