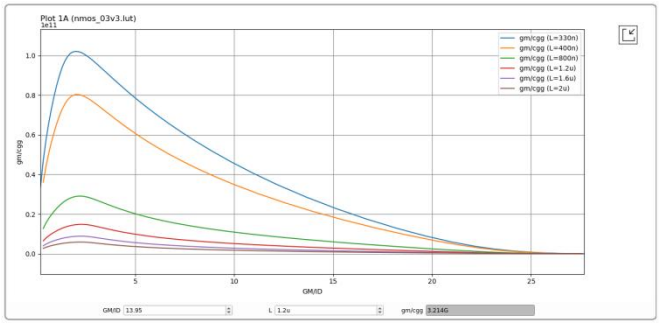
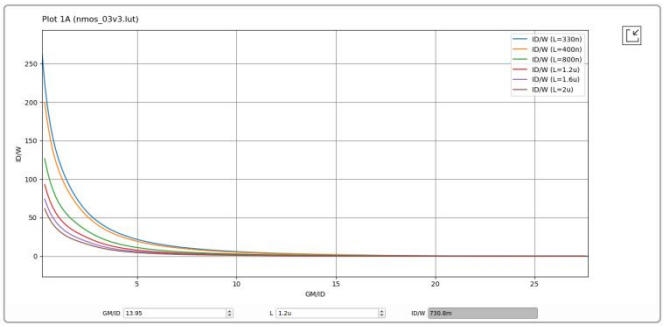
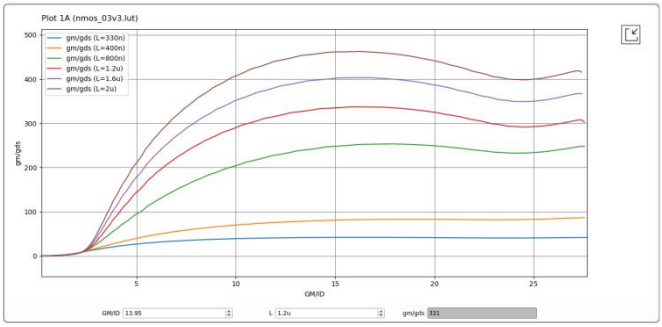
FD Folded cascode OTA

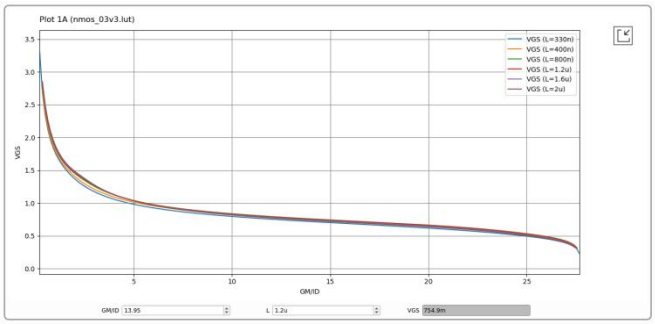
Part 1: g_m / I_D design charts:

For NMOS, design charts:

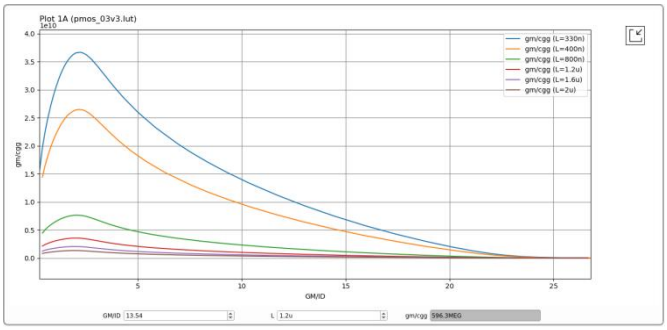


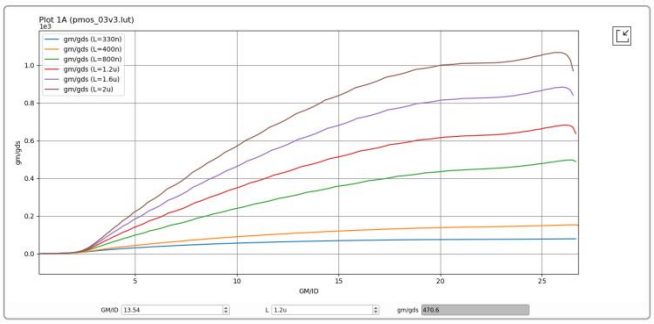


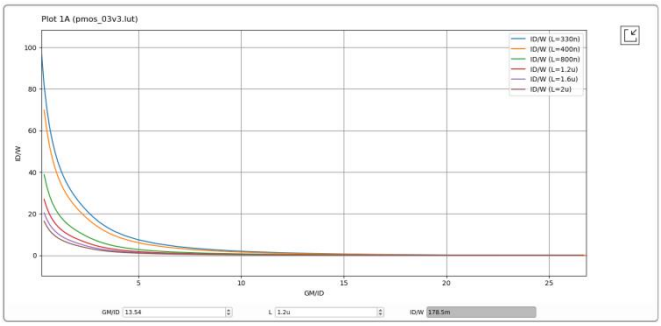


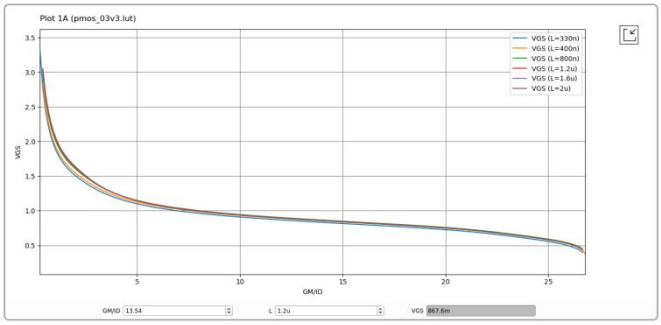


For PMOS, design charts:









We used PMOS input stage, as we can see that the range of the VINCM is close to GND and away from supply.

Specs required:

Technology	GF180MCU
Supply voltage	2.5
Closed loop gain	2
CMRR @ DC	>= 74dB
Phase margin	>= 70
CMIR – high	>= 1V
CMIR – low	<= 0 V
Differential output swing	0.2 – 1.6V
Load	500 fF
DC Loop gain	60 dB
CL settling time for 1% error	100 ns

Detailed design procedure and hand analysis:

First of all, We need the loop gain = 1000, then we need the open loop gain greater that 3000:
Our feedback configuration is voltage - current feedback.
The feedback network is the 1pF feedback capacitor,

$$Y_{21} = \beta_g = -SC_F$$

$$\text{LG} = \beta_g A_{OL,R} = \beta A_{OL}$$

$$\beta = \frac{C_F}{C_F + C_S + C_{IN}} \approx \frac{1}{4}$$

$$\therefore A_{OL} = \frac{1000}{1/4} = 4000$$

We will take some margin to make sure that we meet specs, then $A_{OL} > 4500$, $BW_{OL} = 10$ kHz

Input pair:

From the settling time spec:

$$\text{Settling time for 1\% error} = 4.6\tau$$

$$\text{BW}_{\text{CL}} = \frac{1}{\tau} = \frac{4.6}{100\text{n}} = 7.32\ \text{MHz}$$

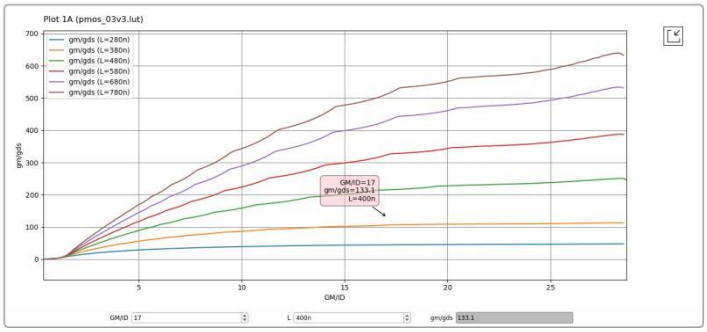
$$\text{GBW} = \text{BW}_{\text{CL}}.\text{A}_{\text{CL}} = 14.6\ \text{MHz}$$

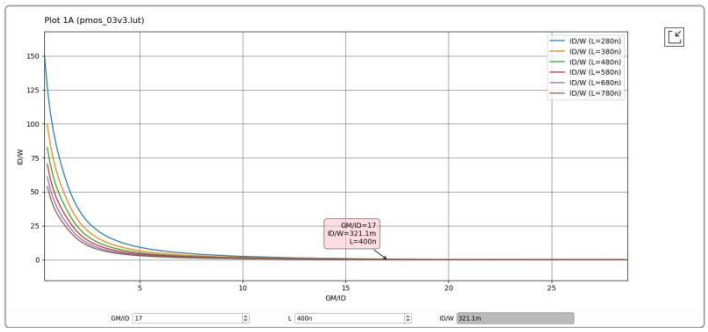
$$BW_{OL} = \frac{\text{BW}_{\text{CL}}}{1 + LG} = 10\ kHz$$

$$\text{GBW}_{\text{OTA}} = BW_{OL}A_{OL} = 30\ MHz$$

$$\text{GBW} = \frac{\text{g}_{\text{m1,2}}}{2\pi \text{C}_{\text{L}}}, \text{g}_{\text{m1,2}} = 142\ \mu\text{S}$$

We assumed $\frac{gm}{id}$ =17, then we need current in input pair equal to 10 µA





Then we from charts:

L = 400 nm, W = 31.1 µm

Cascoded devices:

From the open loop spec:

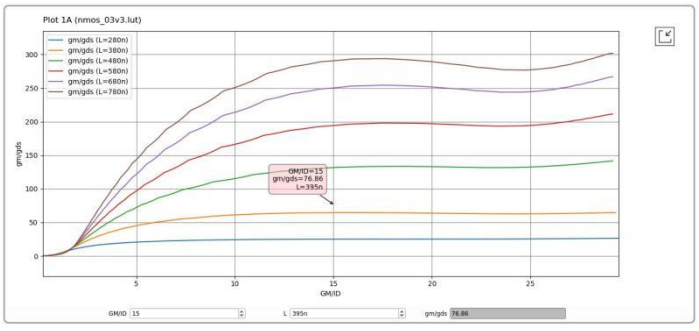
$$A_{OL} = g_{m1,2}((g_{m4}.r_{o4}.r_{o5})//(g_{m3}.r_{o3}.(r_{o2}//r_{o1}))) \approx \frac{(g_m.r_o)^2}{3} = 4000$$

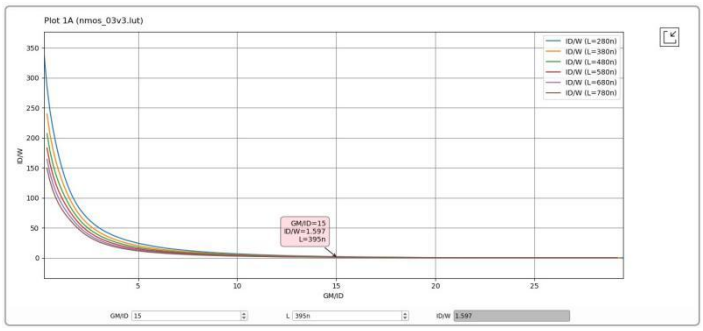
Assume $\frac{gm}{id}$ =15, and the current in CG device will be 1/3 from the input pair current, and if we assumed that all cascoded devices and their current sources have the same g_{ds} and we know r_{o1},then we know the value of g_{ds}, using some mathematics:

$$\frac{r_o^2.r_{o1}}{r_o + 2r_{o1}} = \frac{4000}{g_{m1,2}.g_{m3,4}}$$

$$r_o = 752146\ ohm$$
$$\therefore g_m.r_o = 75$$

For NMOS cascod device:

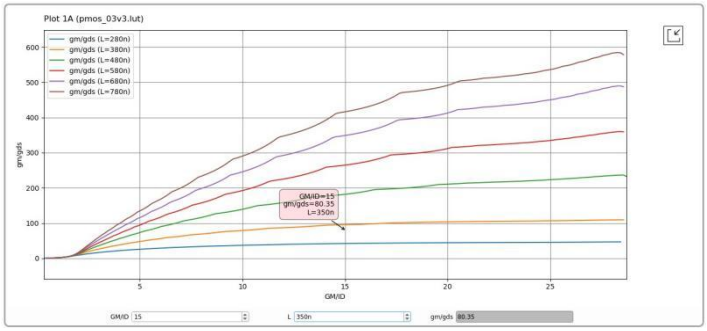


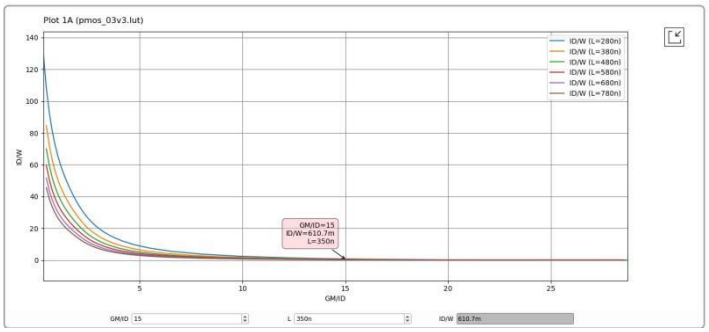


L = 395 nm, W = 3.75 µm

as gain will be high because of the body transconductance, then we will tune the length of NMOS cascoded device to meet specs, L will be 375 nm.

For PMOS cascod device:

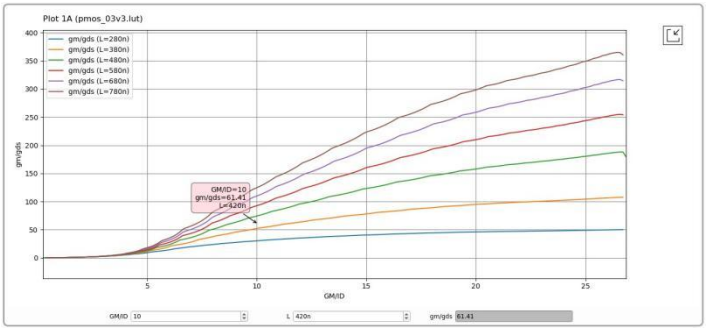


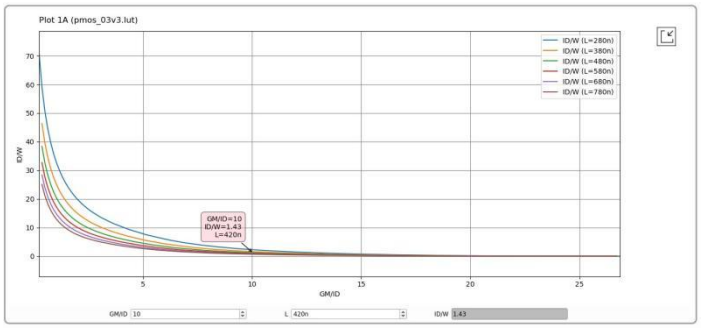


L = 350 nm, W = 9.83 µm, we tuned L to get a reasonable gain, so L will be 320 nm.

PMOS current source:

Assume $\frac{gm}{id}$ =10, I_D = 6 µA, using the r_o we used above, then $g_m.r_o = 60$

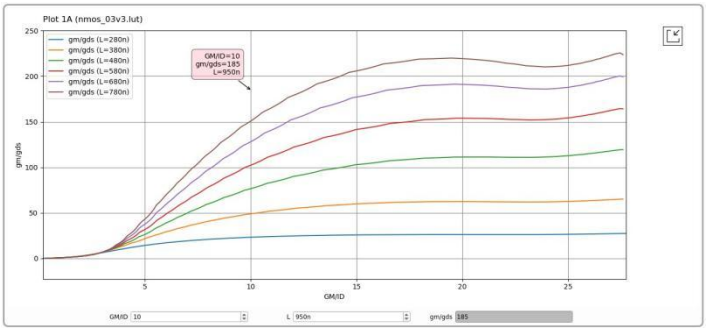


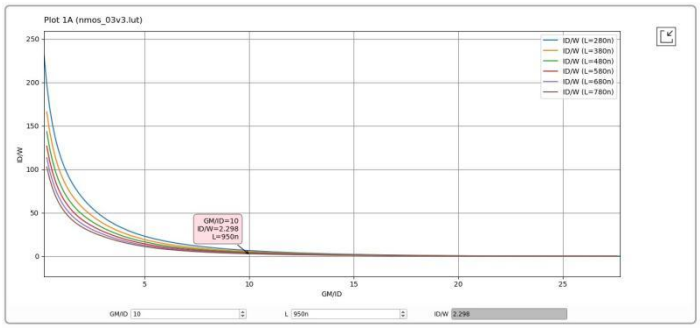


L = 420 nm, W = 4.4 µm.

NMOS current source:

Assuming $\frac{gm}{id}$ = 10, I_D = 16 µA, $g_m.r_o = 180$, as g_m is higher than that in the PMOS one, because the current is higher.





L = 950 nm, W = 6.64 µm.

The remained device have known L, but W will be calculated by mirroring ratio.

Design of the biasing circuit:

We had design it, so that it will generate the same bias voltage needed from an ideal voltage source.

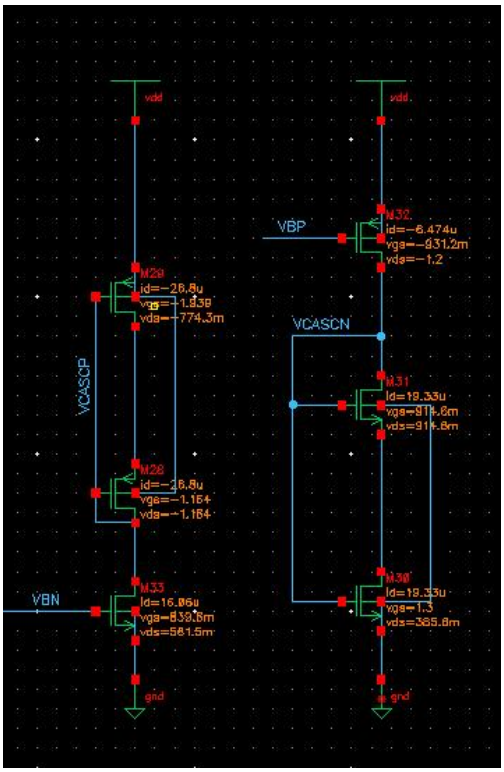
V_{CASCN} = 1.3 V V_{CASCP} = 1.2 V

We put 3 transistors, one of them will mirror the current form the OTA itself.

Sizing of M33, M28, M32 and M31 are known from the OTA devices, but for M29 and M30, we choose a suitable W and L to get the required voltage.

M29: L = 1.5 µm, W = 2.42 µm

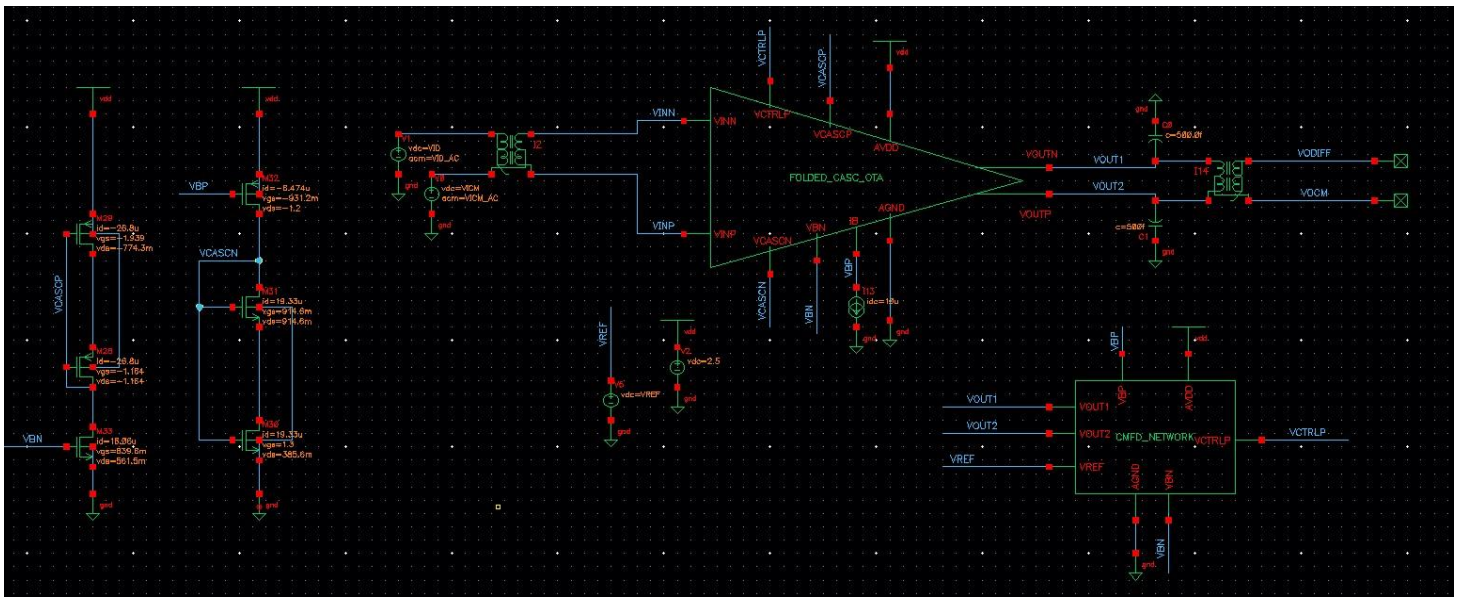
M30: L = 3 µm, W = 2.54 µm



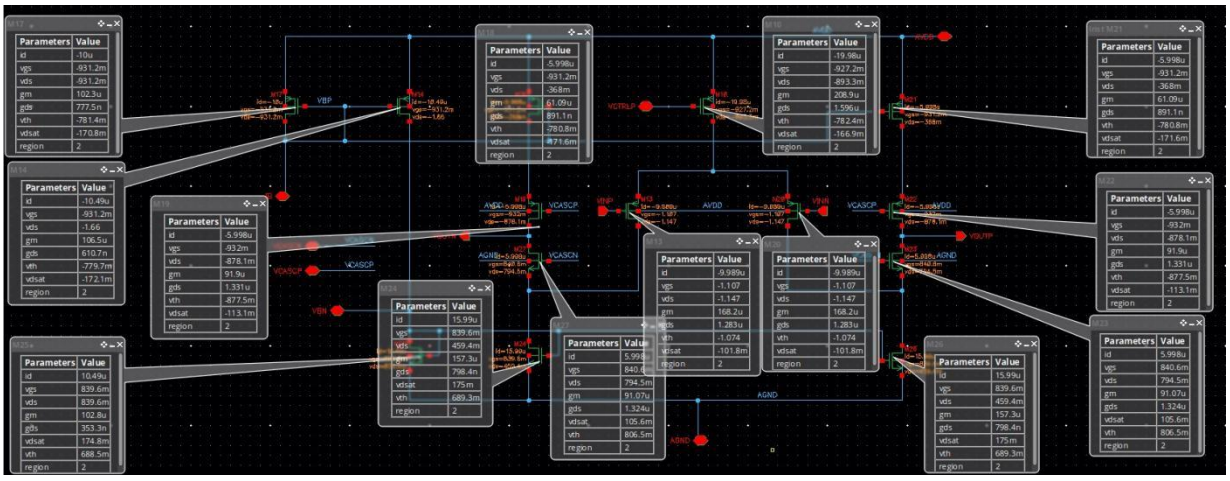
All sizes and parameters of transistors are in the following table:

	M0 (ref)	M1	M2	M3	M4	M5	M6
W	7 µm	31.1 µm	6.64 µm	3.75 µm	9.83 µm	4.4 µm	14.7 µm
L	420 nm	400 nm	950 nm	375 nm	320 nm	420 nm	420 nm
g_m	102 µS	168 µS	157 µS	91 µS	92 µS	61 µS	208 µS
I_D	10 µA	10 µA	16 µA	6 µA	6 µA	6 µA	20 µA
g_m/I_D	10 V^{-1}	16.8 V^{-1}	9.8 V^{-1}	15.1 V^{-1}	15.1 V^{-1}	10.1 V^{-1}	10.4 V^{-1}
V_{DSAT}	171 mV	102 mV	175 mV	105 mV	113 mV	172 mV	166 mV
V_{OV}	150 mV	33 mV	150 mV	27 mV	55 mV	151 mV	150 mV
V^*	200 mV	119 mV	204 mV	129 mV	130 mV	198 mV	196 mV

Open-Loop OTA Simulation (Behavioral CMFB):



Schematic of the OTA with DC OP annotating:



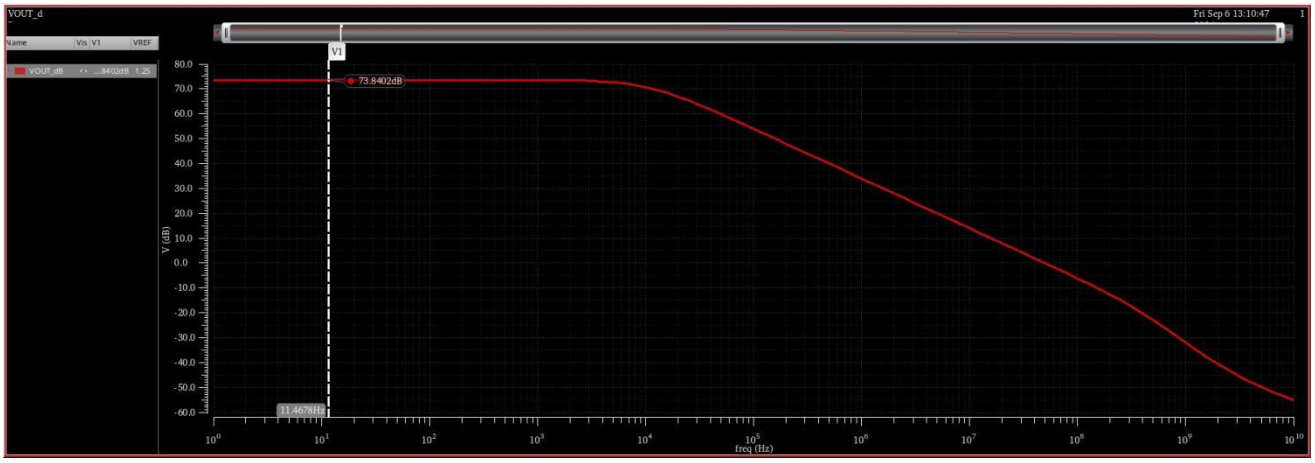
DC voltage of output node, V_{OUT} = 1.254 V.

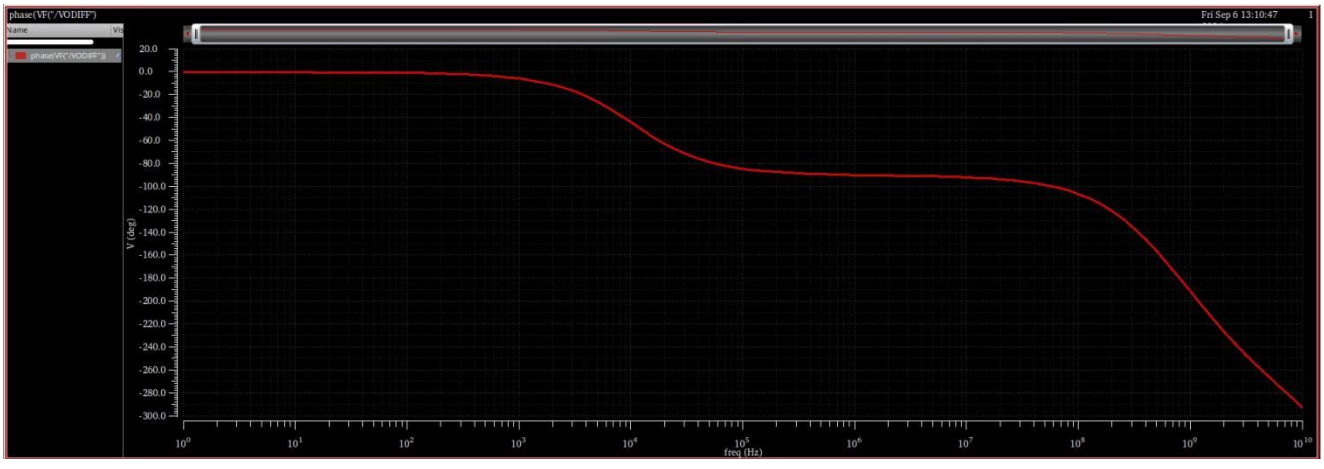
Differential input of the error amplifier = V_{CM} - V_{REF} = 4 mV

Differential output of the error amplifier = V_{BP} - V_{CTRLP} = 1.573 - 1.569 = 4 mV

The relation between them is the error amplifier gain.

Diff small signal:





folded_cascode:test_bench:1	Ao	4.921k			
folded_cascode:test_bench:1	Ao_dB	73.84			
folded_cascode:test_bench:1	BW	10.41k			
folded_cascode:test_bench:1	GBW	51.22M			
folded_cascode:test_bench:1	UGF	51.15M			
folded_cascode:test_bench:1	phaseMargin(VF("/VODIFF"))	81.76			

Hand analysis:

$$A_{OL} = g_{m1,2}((g_{m4} + g_{mbs4}).r_{o4}.r_{o5})//((g_{m3} + g_{mbs3}).r_{o3}.(r_{o2}//r_{o1}))) = 4860 = 73.7\ dB$$

$$\mathrm{BW} = \frac{1}{2\pi \mathrm{C_L R_{OUT}}} = \frac{1}{2\pi \mathrm{C_L}((g_{m4} + g_{mbs4}).r_{o4}.r_{o5})//((g_{m3} + g_{mbs3}).r_{o3}.(r_{o2}//r_{o1})))} = 10.7\ \mathrm{kHz}$$

$$\mathrm{GBW} = A_{OL}.BW = 52\ MHz$$

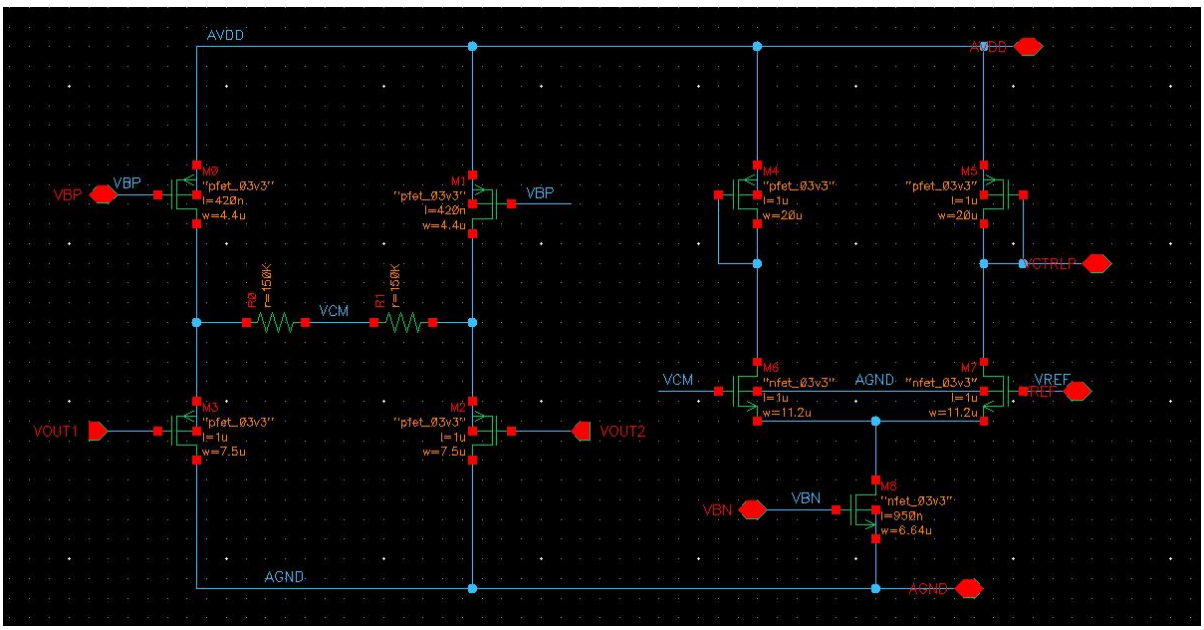
$$\mathrm{A_{OL}(S)} = \frac{\mathrm{A_{OL}}}{\sqrt{1 + (\frac{S}{\omega_{p1}})^2}} = 1,\ \mathrm{S\ (UGF)} = \omega_{p1}\sqrt{(\mathrm{A_{OL}}^2 - 1)} = 51.9\ \mathrm{MHz}$$

$$\mathrm{PM} = 180 - \tan^{-1}(\frac{\omega}{\omega_{p1}}) - \tan^{-1}(\frac{\omega}{\omega_{p2}}) = 76.1\ \mathrm{deg}$$

	Hand analysis	simulation
A_{OL}	4860 | 73.7 dB	4921 | 73.8 dB
BW	10.7 kHz	10.4 kHz
GBW	52 MHz	51.22 MHz
UGF	51.9 MHz	51.15 MHz
PM	76.1 deg	81.76 deg

Open-Loop OTA Simulation (Actual CMFB):

Design of the CMFD circuit:



We have three transistors that we already know their size, M0, M1, M8.

For tail CD devices:

Assume $g_m/I_D = 15$, and L = 1 µm, so from charts, W = 7.5 µm.

The current mirror load in the OTA:

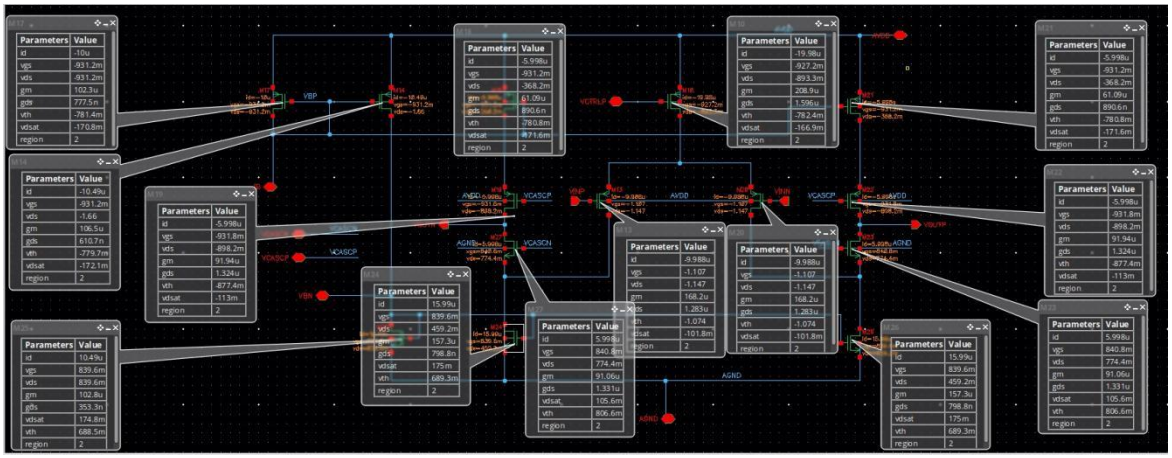
Assume $g_m/I_D = 15$, and L = 1 µm, so from charts, W = 20 µm.

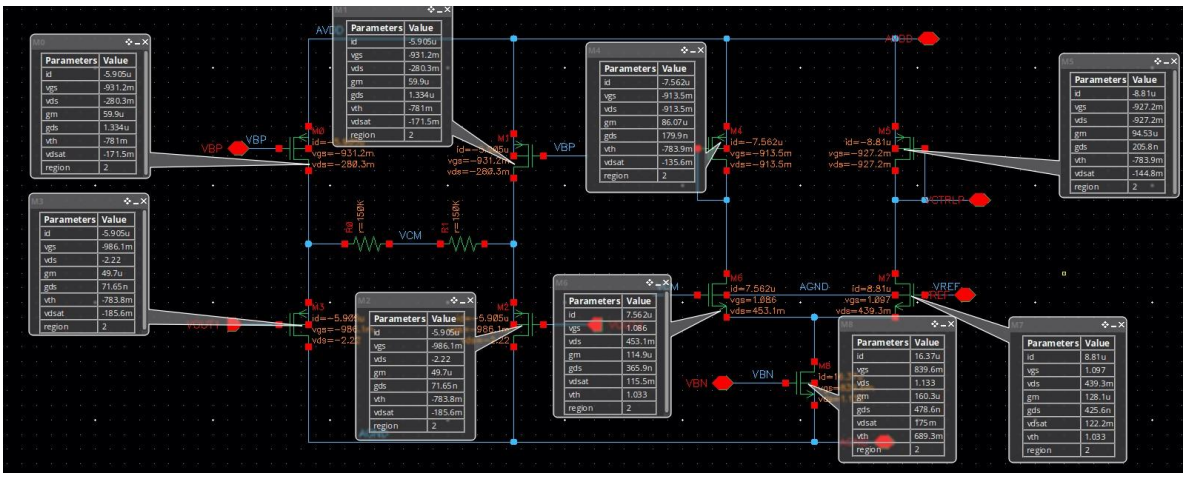
Calculating a suitable value of resistors to prevent starving of tail CD devices:

Assume the current in that branch is equal to 6 µA, so the maximum differential output is the peak to peak value, and it we take some margin:

$$6\mu = \frac{1.8}{2R}, \mathrm{R} = 150\ \mathrm{kohm}$$

Size of M8 is like M2 in the folded OTA, M0, M1 are like M5.





The common level at the OTA output = 1.237 V, when we choose $V_{REF} = V_{REF,OLD} + V_{SG}$, then the value of $V_{CM} = V_{OCM} + V_{SG}$, which is close the $V_{REF,NEW}$, then the error is multiplied by the gain of the error amp, which will be V_{CTRLP}, that value control the current in input pair current source, so that the voltage level at the output is about 1.2 V

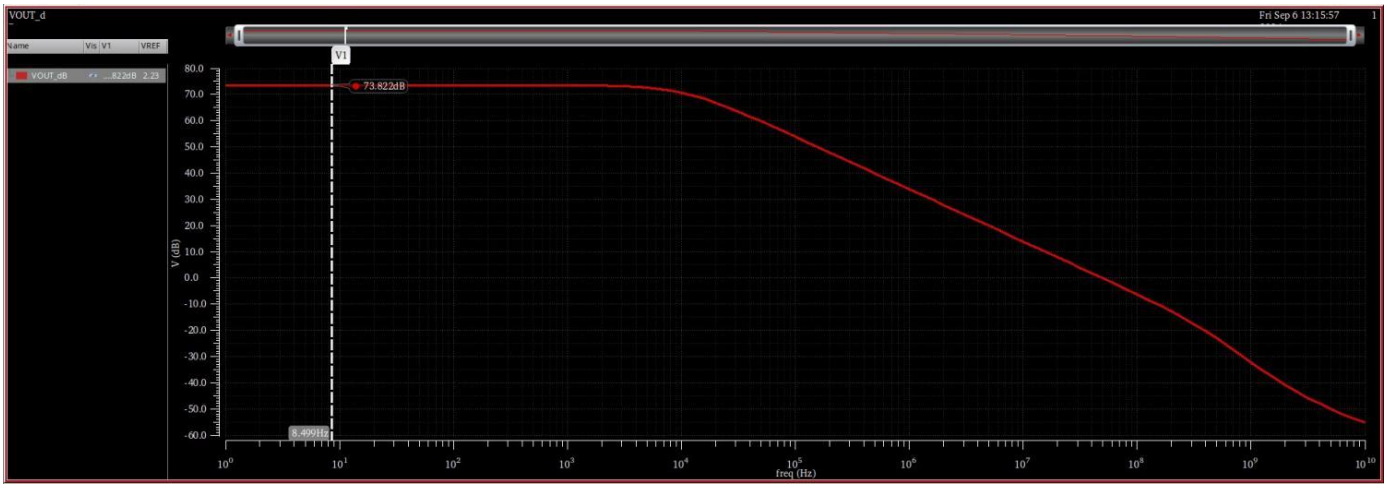
Differential input of the error amplifier = V_{CM} - V_{REF} = 11 mV

Differential output of the error amplifier = V_{BP} - V_{CTRLP} = 1.573 - 1.569 = 4 mV

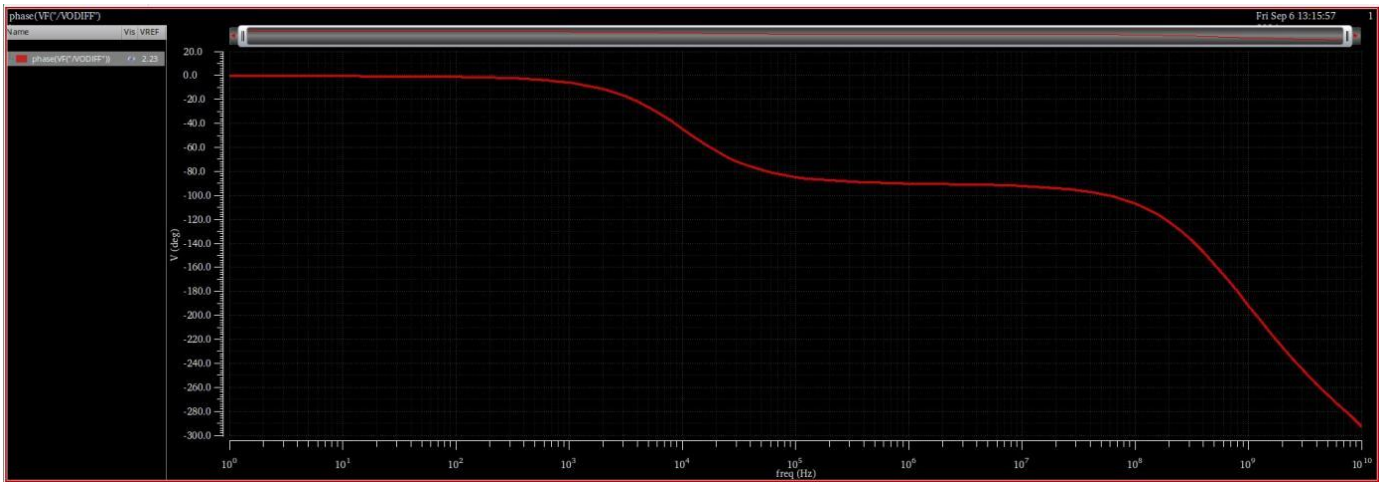
The relation between them is the error amplifier gain.

Diff small signal:

V_{ODIFF} in dB VS frequency:



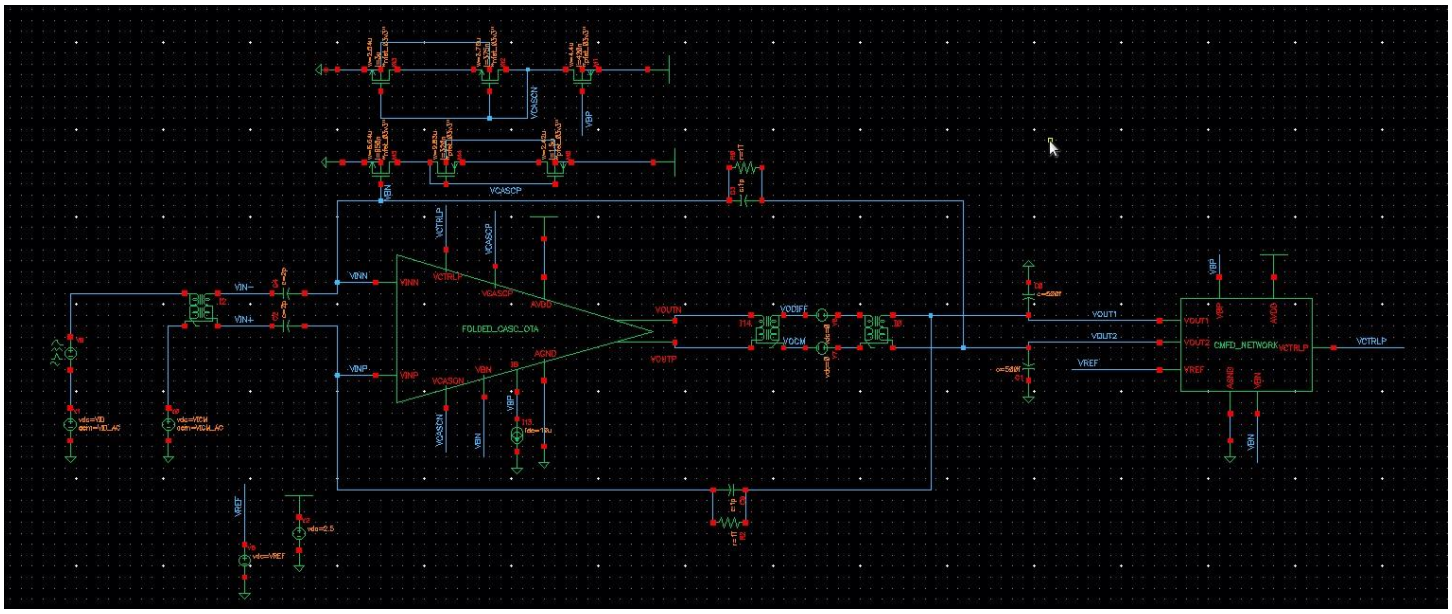
Phase of V_{ODIFF} VS frequency:

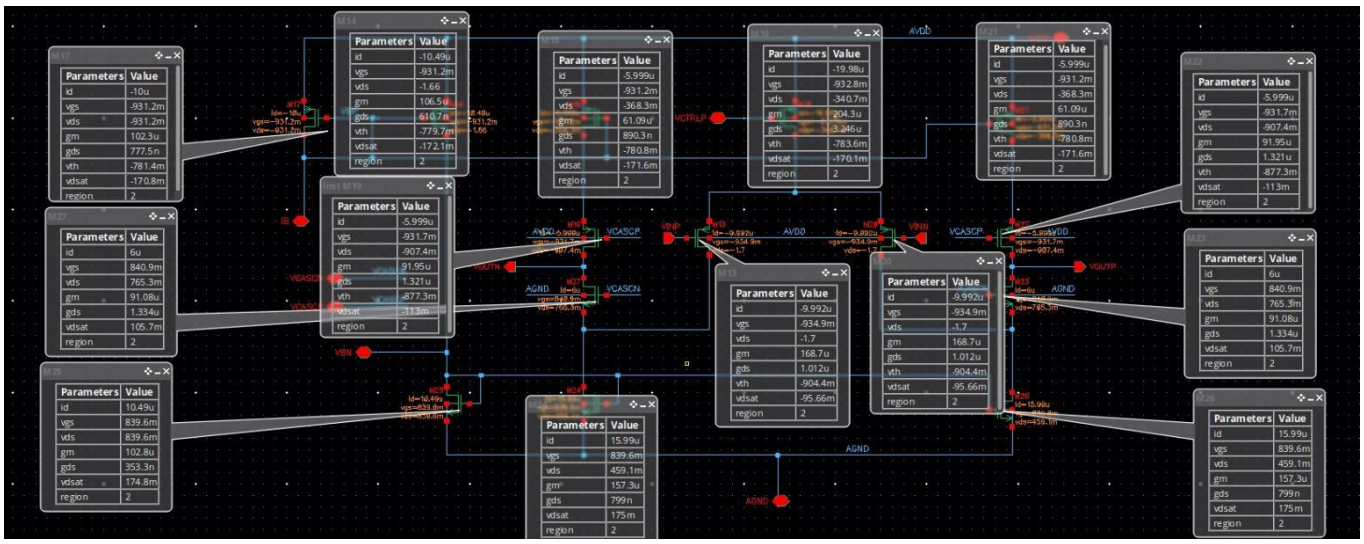


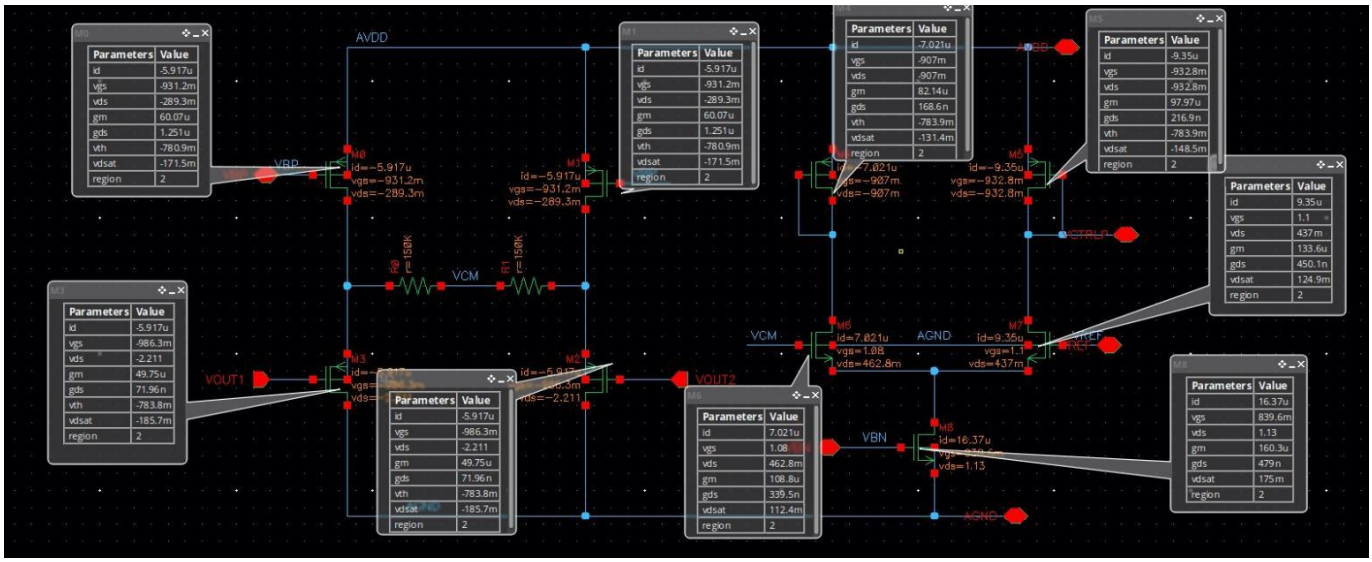
Circuit parameters:

folded_cascode:test_bench:1	Ao	4.91k			
folded_cascode:test_bench:1	Ao_dB	73.82			
folded_cascode:test_bench:1	BW	10.34k			
folded_cascode:test_bench:1	GBW	50.75M			
folded_cascode:test_bench:1	UGF	50.59M			
folded_cascode:test_bench:1	phaseMargin(VF("/VODIFF"))	81.74			

Closed Loop Simulation (AC and STB Analysis):







CM level at the OTA output = 1.224 V

when we choose $V_{REF} = V_{REF,OLD} + V_{SG}$, then the value of $V_{CM} = V_{OCM} + V_{SG}$, which is close the $V_{REF,NEW}$, then the error is multiplied by the gain of the error amp, which will be V_{CTRLP}, that

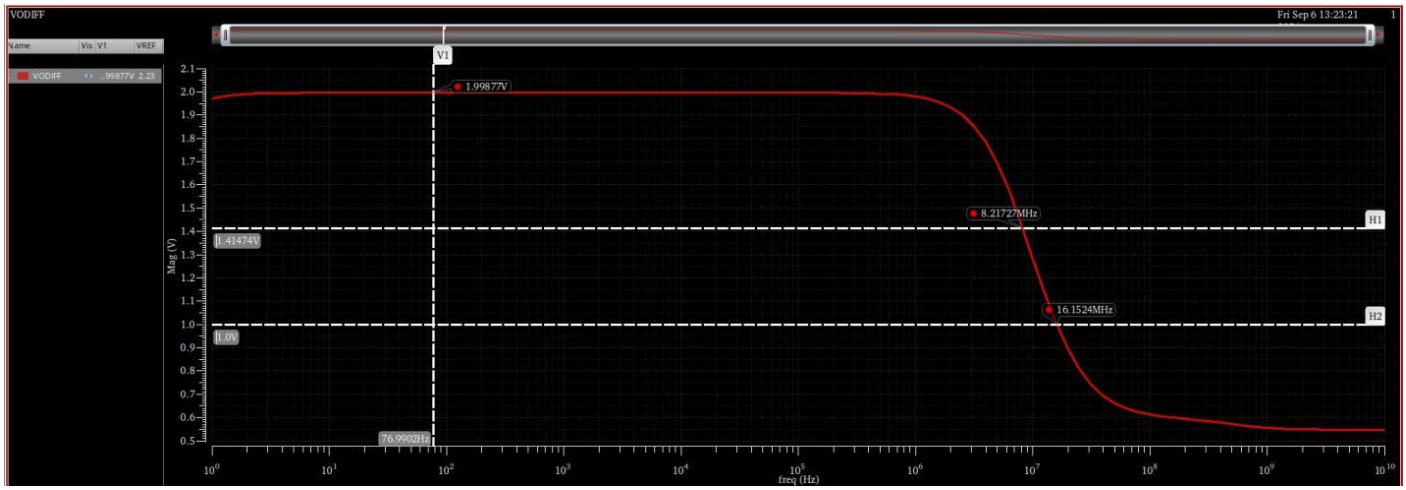
value control the current in input pair current source, so that the voltage level at the output is kept by the CMFD circuit on 1.22 V

CM level at the OTA input = 1.224 V

that's because the 1T ohm resistor makes current in that branch equal to zero, and as there is no DC path except that then the input voltage will be equal to the output voltage.

Differential closed-loop response:

V_{ODIFF} VS frequency:



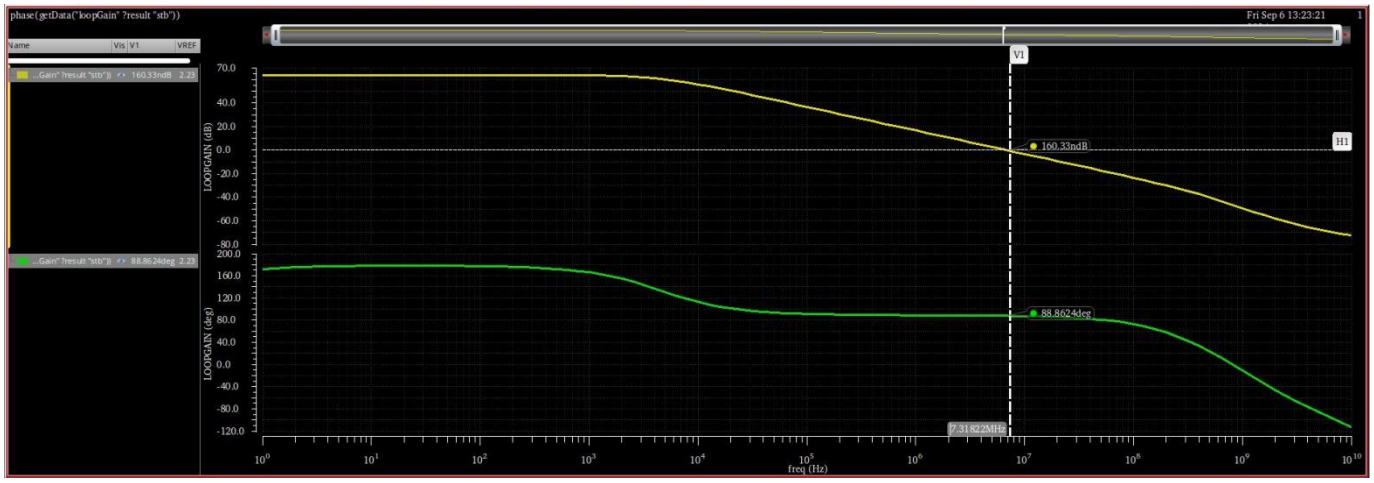
folded_cascode:closed_loop_testbench:1	A_OL_dB	6.015			
folded_cascode:closed_loop_testbench:1	A_OL	1.999			
folded_cascode:closed_loop_testbench:1	BW	8.457M			
folded_cascode:closed_loop_testbench:1	GBW	16.9M			
folded_cascode:closed_loop_testbench:1	UGF	16.15M			

Using cursors on the plot:

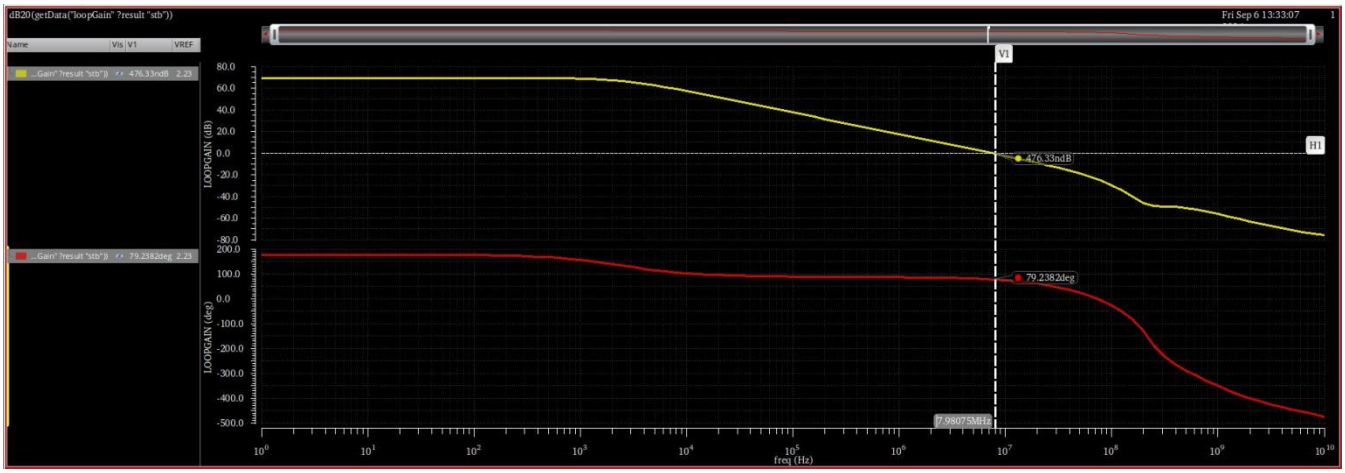
DC gain = 1.998 V BW = 8.217 MHz UGF = 13.152 MHz GBW = 16.417 MHz

Differential and CMFB loops stability (STB analysis):

Loop gain and phase VS frequency (DIFF PATH):



Loop gain and phase VS frequency (CM PATH):



DIFF loop results:

bandwidth(getData("loopGain" ?result "stb") 3 "low")	4.357k		
(ymax(mag(getData("loopGain" ?result "stb"))) * bandwidth(getData("loopGain" ?result "stb") 3 "low"))	7.195M		
dB20(getData("loopGain" ?result "stb"))			
ymax(mag(getData("loopGain" ?result "stb")))	1.651k		
unityGainFreq(getData("loopGain" ?result "stb"))	7.362M		

CM loop results:

folded_cascode:closed_loop_testbench:1	bandwidth(getData("loopGain" ...	2.557k		
folded_cascode:closed_loop_testbench:1	(ymax(mag(getData("loopGain" ...	8.024M		
folded_cascode:closed_loop_testbench:1	dB20(getData("loopGain" ?resul...			
folded_cascode:closed_loop_testbench:1	ymax(mag(getData("loopGain" ?...	3.139k		
folded_cascode:closed_loop_testbench:1	unityGainFreq(getData("loopGai...	7.985M		

	DIFF PATH	CM PATH
PM	88.8 deg	79.2 deg
GBW	7.195 MHz	8.024 MHz

PM of the DIFF path is higher that the CM path, and the reason for that is the ratio between the non-dominant pole and the unity gain frequency of the diff path is higher than the CM path, GBW of the CM path is higher, since the gain of the CM path is higher.

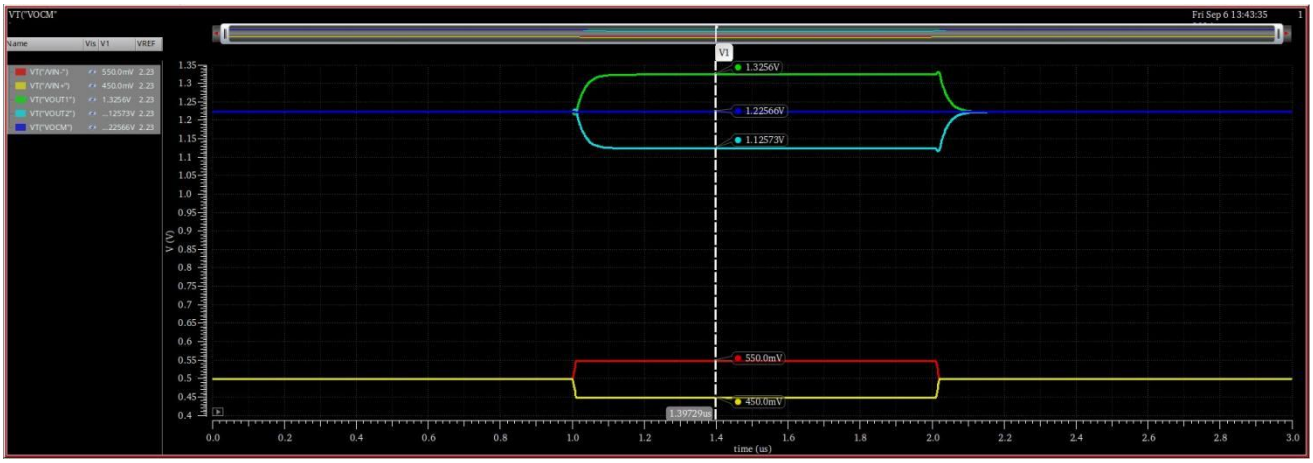
	Diff loop	Open loop
DC LG	1651	4921
GBW	7.195 MHz	50.75 MHz

Open loop gain and BW are higher than the DIFF loop, as the feedback factor beta reduces the loop gain and GBW, also the feedback cap reduces the bandwidth, so the decrease in GBW is more than the decrease in DC LG.

Closed Loop Simulation (Transient Analysis):

Differential and CMFB loops stability (transient analysis) + CL settling time: Differential input pulse

Input and output signals VS time:



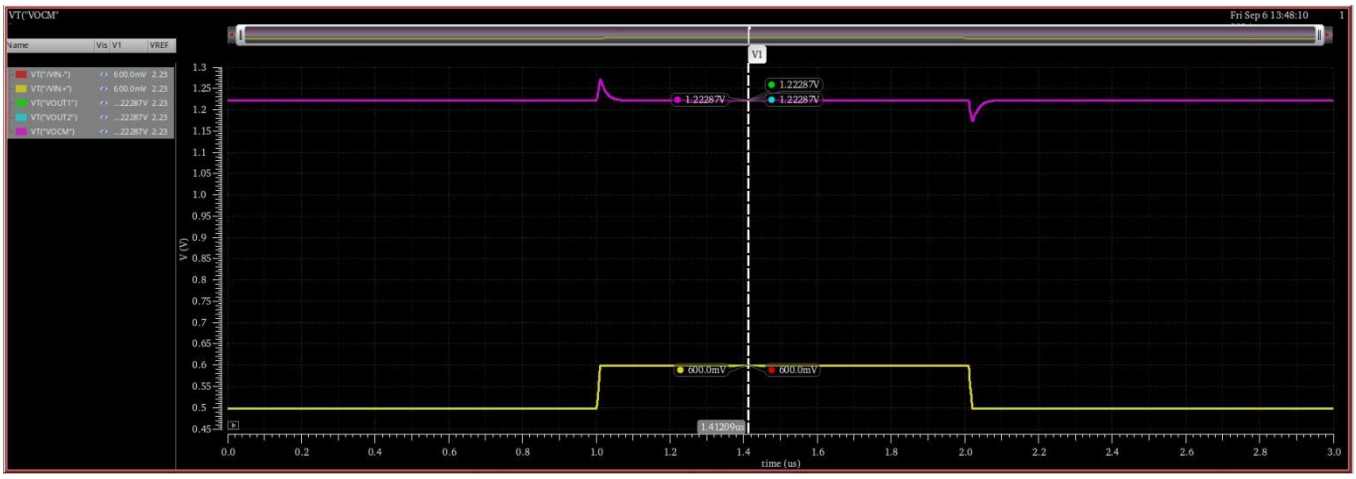
There are no DIFF or CM ringing in output, there is a little spark or spike in the output due to the caps.
The two loops are stable with adequate phase margin, both of them have phase margin more than 76 deg, then they are stable, and don't suffer from any ringing.

The 1% settling time:

folded_cascode:closed_loop_testbench:1	VT("VOCM")				
folded_cascode:closed_loop_testbench:1	riseTime(VT("VODIFF") 0.0 nil 0....	99.67 n			

The spec was 100ns, so that result meet the spec.
Differential and CMFB loops stability (transient analysis): CM input pulse

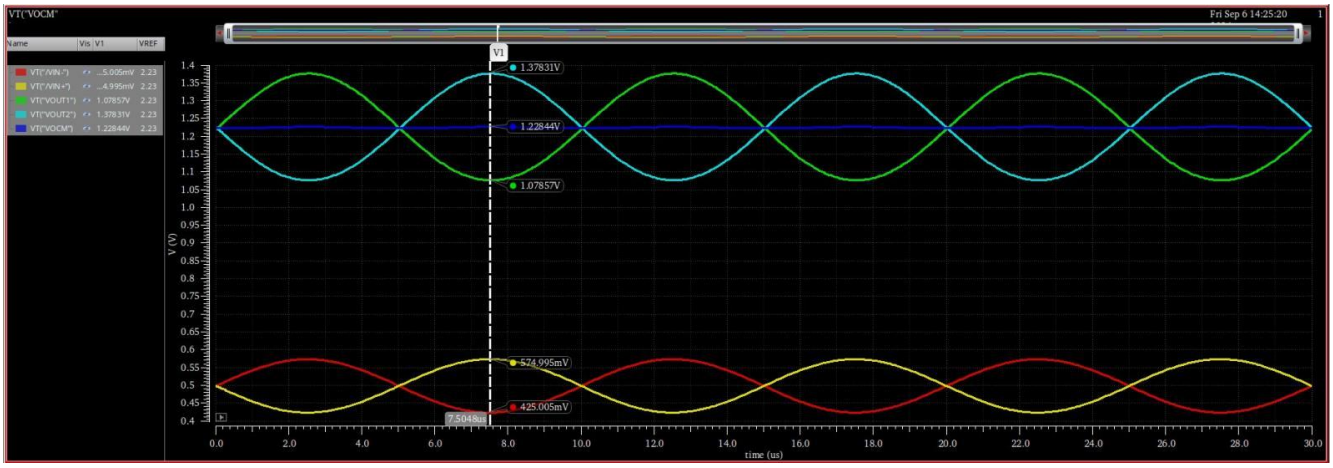
Input and output signals VS time:



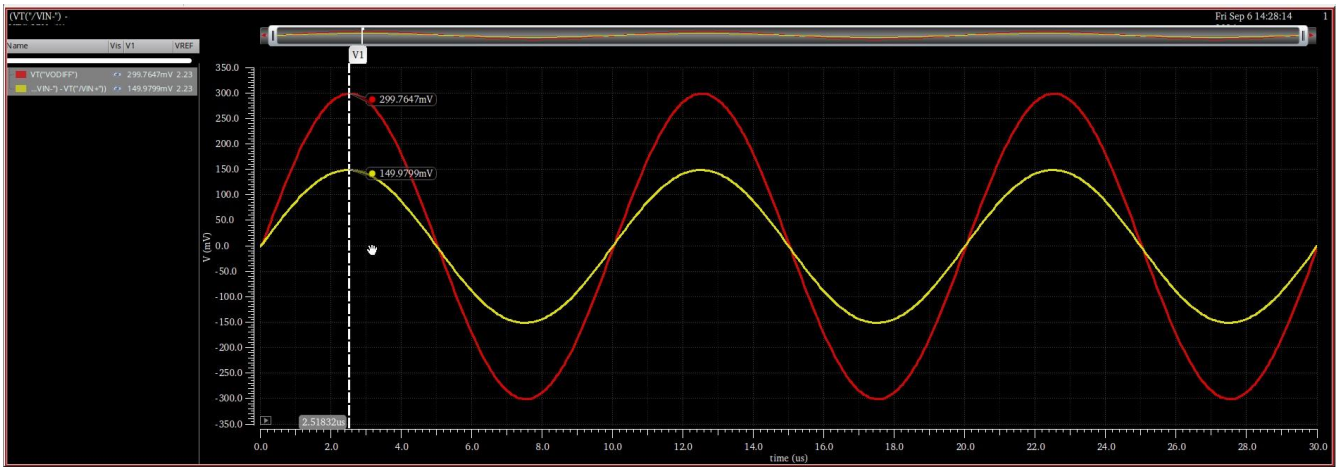
There are no DIFF or CM ringing in output, there is a little spark or spike in the output due to the caps.

The two loops are stable with adequate phase margin, both of them have phase margin more than 76 deg, then they are stable, and don't suffer from any ringing.

Output swing:
Input and output signals VS time:



V_{ODIFF} and V_{OCM} on the same plot VS time:



Peak to Peak for input and output and DC gain:

folded_cascode:closed_loop_testbench:1	peakToPeak((VT("/VIN-") - VT("/V...	300m
folded_cascode:closed_loop_testbench:1	peakToPeak(VT("/VODIFF"))	599.5m
folded_cascode:closed_loop_testbench:1	(peakToPeak(VT("/VODIFF")) / pe...	1.999

Peak to peak for the input = 300 mV

Peak to peak for the ouput = 599.5 mV

The DC gain = 599.5 / 300 = 1.999