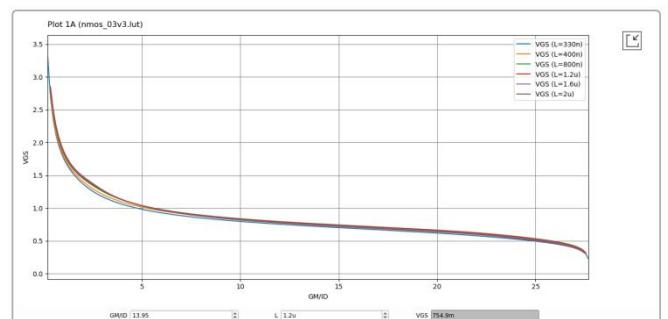
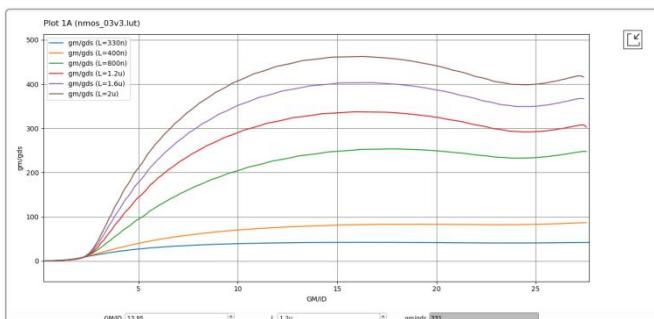
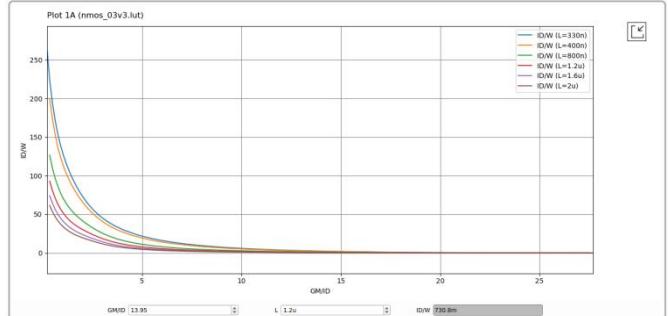
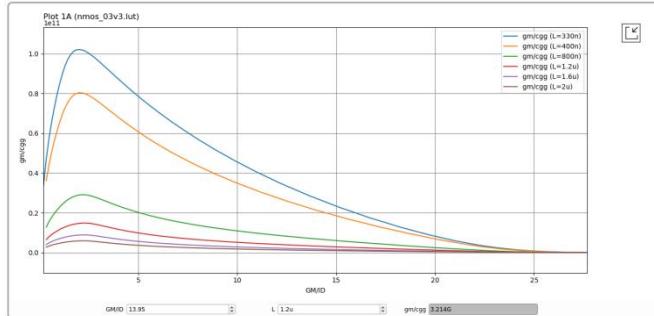


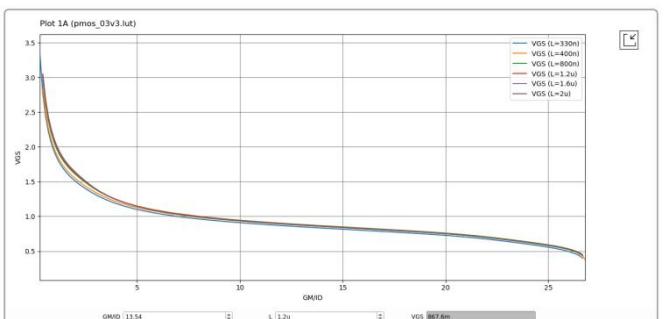
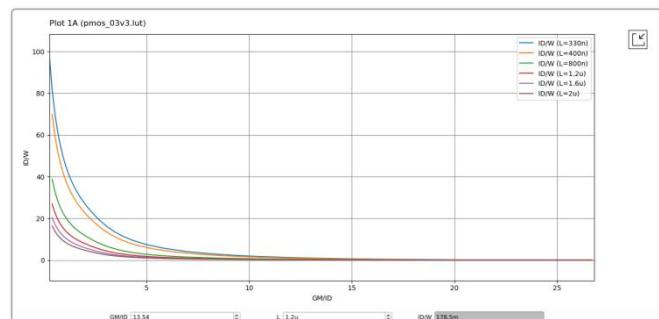
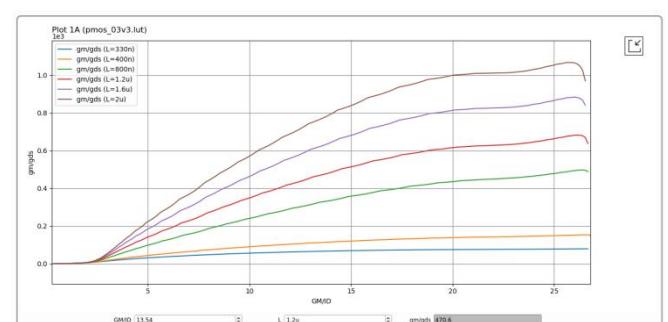
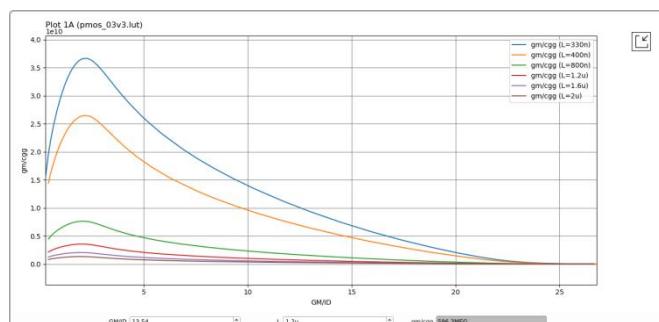
Two stage miller OTA DESIGN

Part 1: g_m / I_D design charts:

For NMOS, design charts:



For PMOS, design charts:



We used PMOS input stage, as we can see that the range of the VINCM is close to GND and away from supply.

Specs required:

Technology	0.18um
Supply voltage	1.8V
Static gain error	<= 0.05%
CMRR @ DC	>= 74dB
Phase margin	>= 70
OTA current consumption	<= 60uA
CMIR – high	>= 1V
CMIR – low	<= 0.2V
Output swing	0.2 – 1.6V
Load	5pF
Buffer closed loop rise time (10% to 90%)	<= 70ns
Slew rate (SR)	5V/ μS

Detailed design procedure and hand analysis:

Input pair:

- from the rise time requirement:

$$UGF = \frac{2.2}{2\pi t_{rise}} = \frac{2.2}{2\pi \times 70n} = 5\text{MHz}$$

- this was the closed loop rise time, which mean that for a buffer, the UGF is equal to the closed loop bandwidth.
- from the SR requirement, the maximum value of the current, C_c is equal to half of C_L .

$$I_{max} = 5 \times C_c = 12.5\mu\text{A}$$

$$UGF = \frac{g_m}{2\pi C_c} = 5\text{MHz}, g_m = 2\pi C_c \times 5\text{M} = 25\pi \mu\text{S}$$

$$I_D \text{ at each branch} = 6.25\mu\text{A}$$

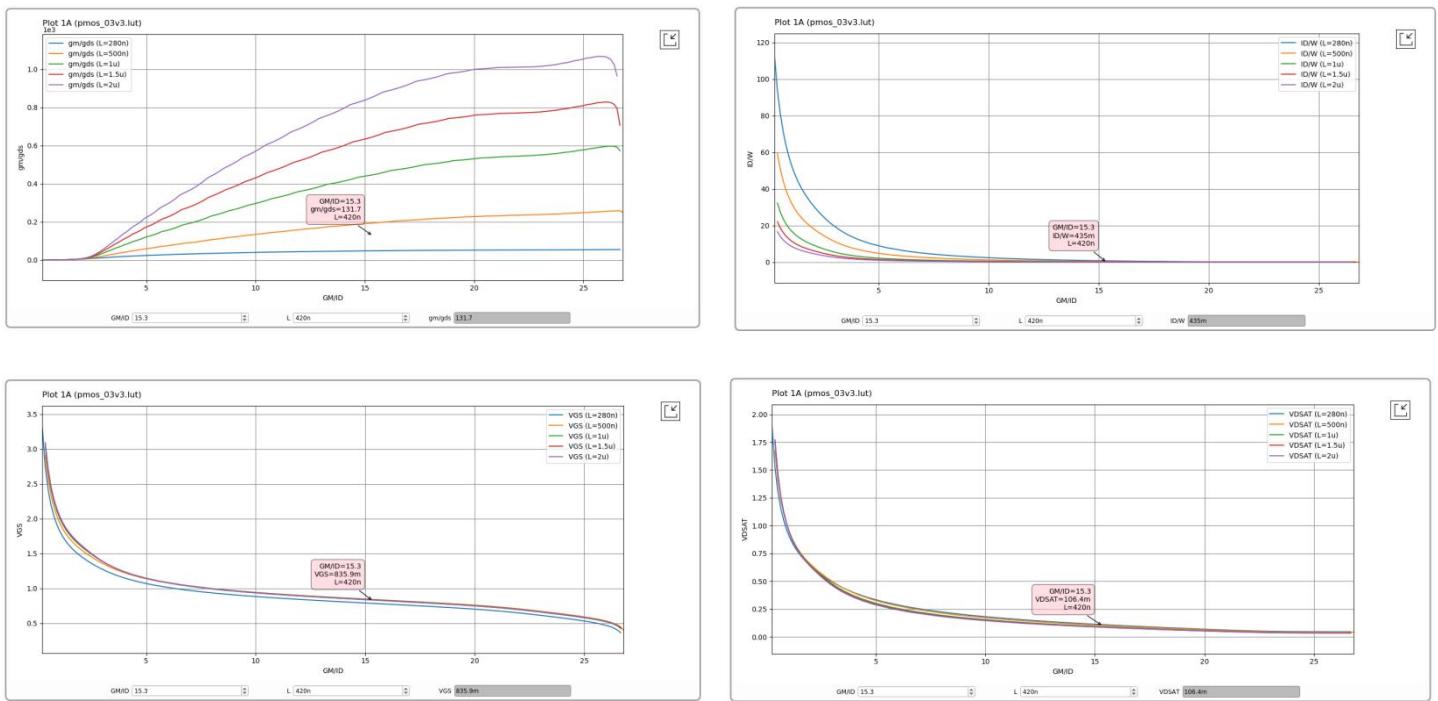
- then $\frac{g_m}{I_D}$ for the input pair = 4π , we will increase it to 15.3.
- from the static gain error, $A_{OL} = \frac{100}{0.05} = 2000$, then we need open loop gain greater than it.
- if we assign larger gain for the first stage, like the double of the second stage, then

$$A_{OL} = A_{v1} \times A_{v2} = A_{v1} \times 0.5A_{v1}, \text{ then } A_{v1} = 63.2$$

- Then the intrinsic gain of the first stage = 126.4
- we did that for some reasons:

- high gain at the first stage will push the dominant pole inwards, which will improve stability
- High gain at the second stage may be limited by the output swing
- High gain at the second stage may cause a low frequency pole which affect stability.

- Now we can choose values of L, W of the input pair:

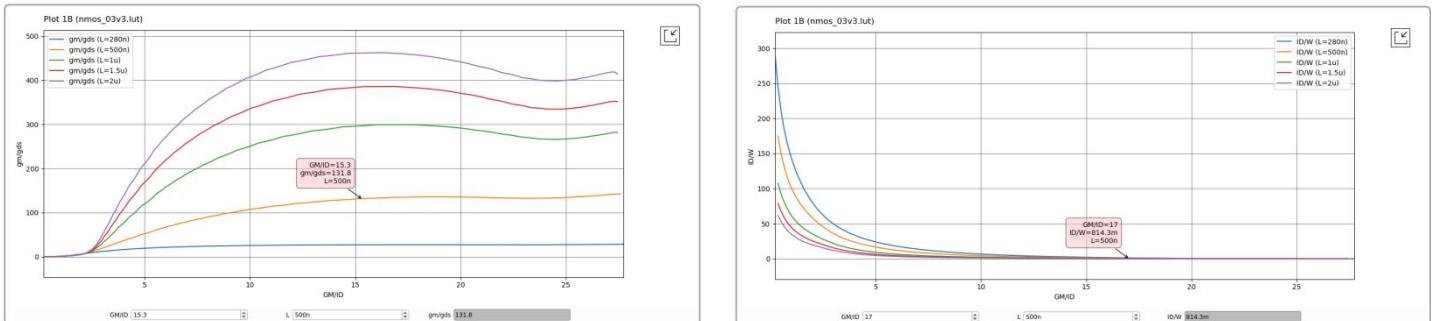


From the graphs, $L = 420 \text{ nm}$, $V_{GS} = 835 \text{ mV}$, $V_{DSAT} = 106 \text{ mV}$

$$W = \frac{I_D}{435 \text{ m}} \approx 14 \mu\text{m}$$

Current mirror load design:

Assume it has the same g_{ds} as input pair, then it has the same intrinsic gain at the same $\frac{g_m}{I_D}$



After that, from the spec of VICM-low, we found that V_{GS} of the current mirror load should not exceed some value:

$$V_{IN,MIN} = -V_{SG1,2} + V_{DSAT,1,2} + V_{GS3,4} \leq 0.2$$

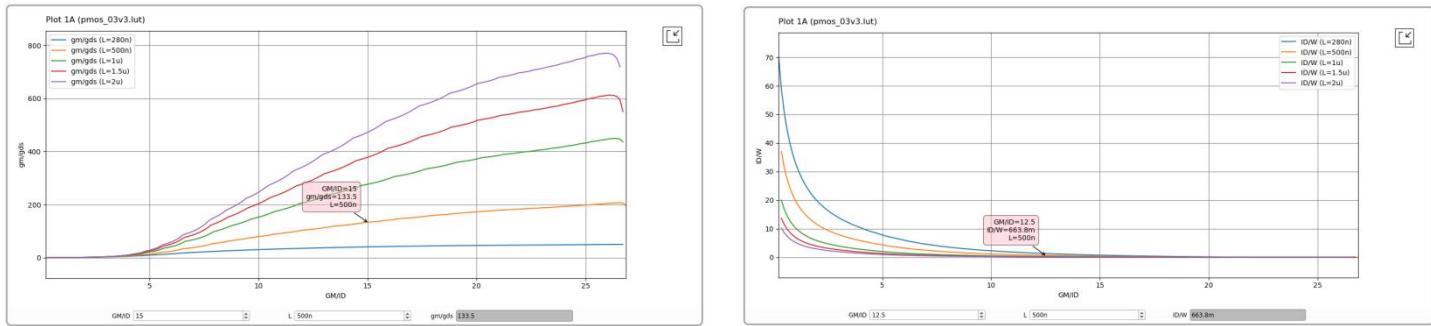
$$V_{GS3,4} \leq 0.2 + V_{SG1,2} - V_{DSAT,1,2}$$

$$V_{GS3,4} \leq 930 \text{ mV}$$

Then we choose a reasonable value of $\frac{g_m}{I_D}$ after tuning and it was suitable for the output devices, $\frac{g_m}{I_D} = 17$.

Then $L = 500 \text{ nm}$, and $W = 8.1 \mu\text{m}$

Tail current source design:



Assume $\frac{g_m}{I_D} = 15$, from the CMRR spec:

$$CMRR = g_{m1,2} \cdot r_{o1,2} \cdot g_{m3,4} \cdot r_{o5}$$

$$r_{o5} = \frac{5012}{g_{m1,2} \cdot r_{o1,2} \cdot g_{m3,4}} = 727.27 \text{ k ohm}$$

$$g_{m5} \cdot r_{o5} = 15 \times 12.5\mu \times 727.27\text{k} = 136$$

Then from the VINCM-high spec, we can get the maximum V_{dsat5} :

$$V_{IN,MAX} = V_{DD} - V_{SG1,2} - V_{DSAT5} \geq 0.8$$

$$V_{DSAT5} \leq V_{DD} - V_{SG1,2} - 0.8$$

$$V_{DSAT5} \leq 165 \text{ mV}$$

We used $V_{IN,MAX} = 0.8$, as that spec will be impossible to achieve with that technology.

If we choose that V^* is equal to V_{DSAT5} , then we made sure that the device has some margin, then we can choose $\frac{g_m}{I_D} = 12.5$

Then sizing of the tail current source:

W after some tuning = 19.8 μm , $L = 500 \text{ nm}$.

Design of the output load:

- the output load has the same length as M5 as they are current mirrors from the same device, and the same $\frac{g_m}{I_D}$, then the only different parameter is the width:

$$W_7 = 19.8 \times 0.8 \times 4.75 = 75\mu\text{m}$$

And after tuning the width to get the right current, $W_8 = 72 \mu\text{m}$

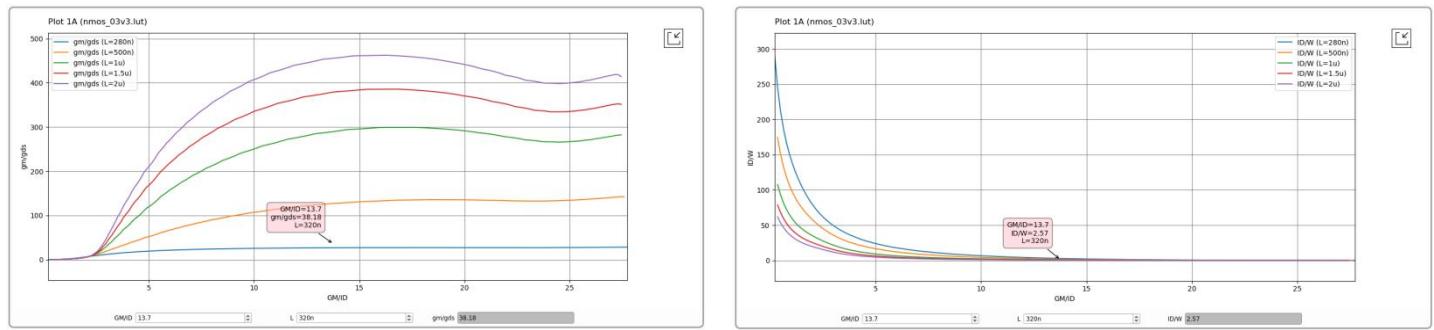
Design of the reference device:

It is the same like the tail current source but different W .

$$W_0 = 19.8 \times 0.8 = 15.8\mu\text{m}$$

And after some tuning $W_0 = 15.2 \mu\text{m}$

Design of the second stage input device:



From PM spec, we can assume that $\omega_{p2} = 4\omega_u$:

$$\frac{g_{m7}}{C_L} = \frac{4 \cdot g_{m1,2}}{C_C}, g_{m7} = \frac{4 \times 25\pi\mu \times 5p}{2.5p} = 200\pi\mu S$$

Then $\frac{g_{m6}}{I_{D6}} = 13.2$, we will tune it to 13.7

Gain of the second stage is half of the first one, $g_{m7}(r_{o7}/r_{o6}) = 31.6$

Then from ADT we can the value of r_{o8} then get the value of r_{o6} , $r_{o6} = 63.85$ k ohm

Then the intrinsic gain of M6, $g_{m6} \cdot r_{o6} = 38$

The sizing of the device: $L = 320$ nm, $W = 18.5$ μm , after tuning, $W = 17.7$ μm

Parameter of all devices:

	M0	M1	M2	M3	M4	M5	M6	M7
W	15.2 μm	13.3 μm	13.3 μm	8.1 μm	8.1 μm	19.8 μm	17.7 μm	72 μm
L	500 nm	420 nm	420 nm	500 nm	500 nm	500 nm	320 nm	500 nm
g_m	127 μS	95.1 μS	95.1 μS	106 μS	106 μS	158 μS	649 μS	613 μS
I_D	10 μA	6.25 μA	6.25 μA	6.25 μA	6.25 μA	12.5 μA	47.5 μA	47.5 μA
g_m/I_D	12.7 V^{-1}	12.5 V^{-1}	15.2 V^{-1}	17 V^{-1}	17 V^{-1}	12.7 V^{-1}	13.7 V^{-1}	12.9 V^{-1}
V_{DSAT}	132 mV	106 mV	106 mV	89 mV	89 mV	123 mV	116 mV	132 mV
V_{OV}	101 mV	56 mV	56 mV	4 mV	4 mV	101 mV	56 mV	101 mV
V^*	157 mV	131 mV	131 mV	117 mV	117 mV	157 mV	145 mV	157 mV

PART 3: Open-Loop OTA Simulation:

DC OP analysis:

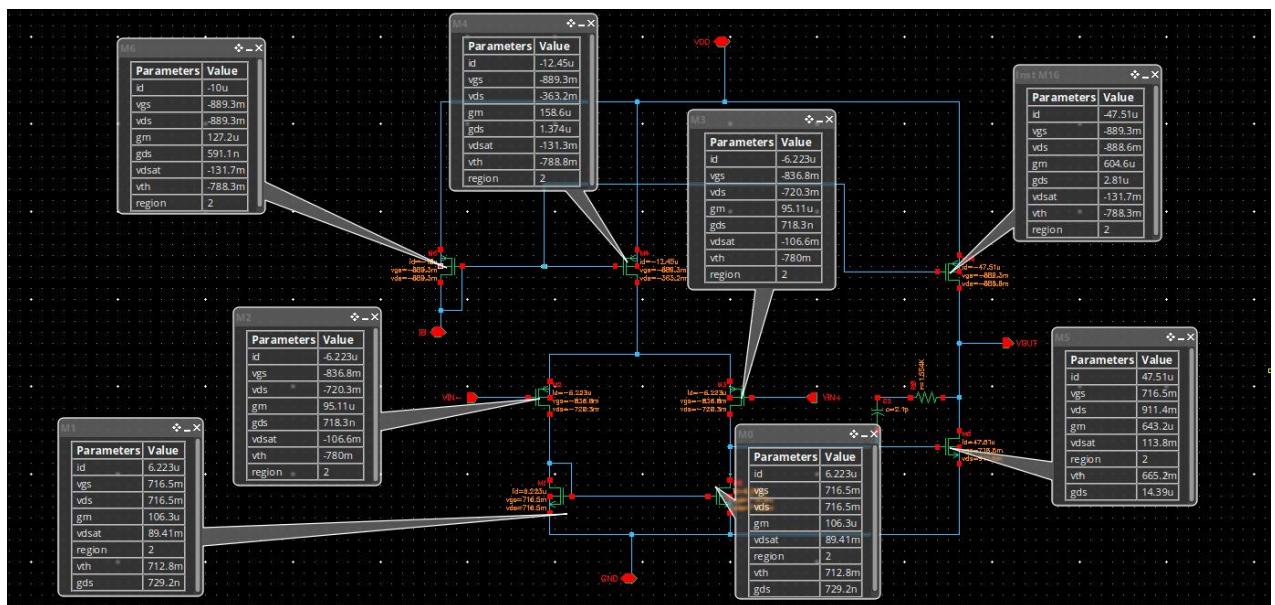
From the results, we can see that g_m and I_D of the input pairs are equal.

$$V_{out2} = 911.4 \text{ mV} \quad V_{out1} = 716.5 \text{ mV}$$

V_{out1} is forced by the current in the output branch, it determines V_{GS} of the input device of the second stage, and V_{GS6} is equal to the output of the first stage, and $V_{GS6} = 716.8 \text{ mV}$.

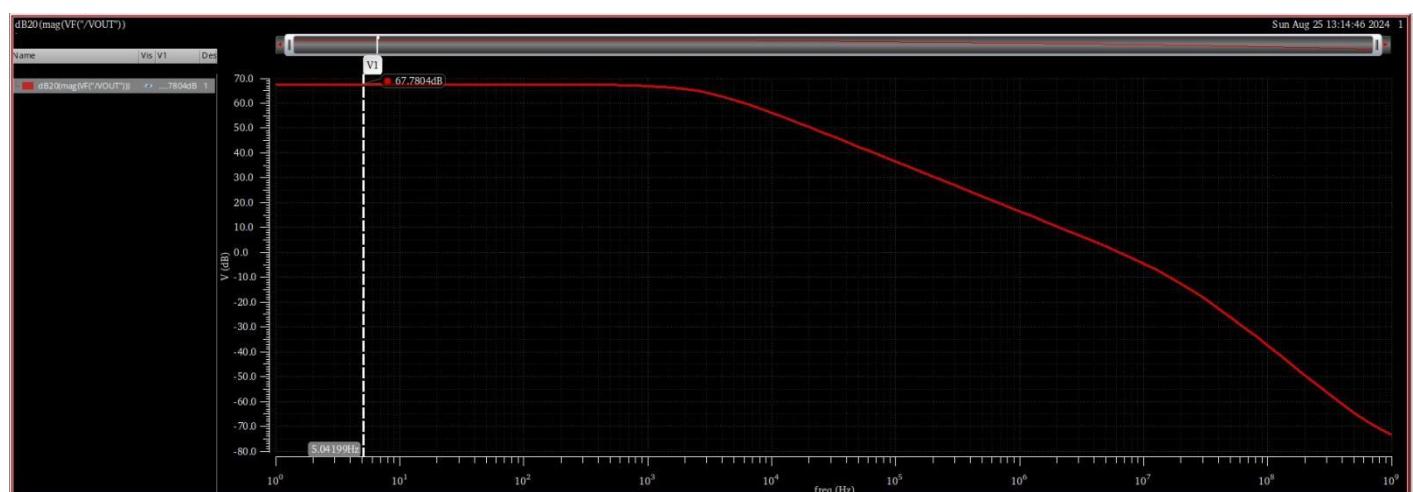
V_{out2} we had design the width of the current mirror load so that the DC output voltage is equal to 900 mV at DC analysis.

DC OP annotated on all devices:



Diff small signal:

Diff gain in dB VS frequency:



Results from the simulation:

Test	Output	Nominal	Spec	Weight	Pass/Fail
two_stage_OTA:test_bench_final:1	VF("/VOUT")				
two_stage_OTA:test_bench_final:1	Ao	2.449k			
two_stage_OTA:test_bench_final:1	BW	2.82k			
two_stage_OTA:test_bench_final:1	Ao_dB	67.78			
two_stage_OTA:test_bench_final:1	GBW	6.908M			
two_stage_OTA:test_bench_final:1	UGF	6.614M			

Hand analysis:

$$A_{OL} = A_{v1} \times A_{v2} = (g_{m1,2}(r_{o1,2}/r_{o3,4})).(g_{m6}(r_{o6}/r_{o7}))$$

$$A_{OL} = (95.11\mu \times (\frac{1}{718n}/\frac{1}{729n})).(643\mu \times (\frac{1}{2.81\mu}/\frac{1}{14.39\mu})) = 2457 = 67.8 \text{ dB}$$

$$BW = \frac{1}{2\pi R_{OUT1} R_{OUT2} G_{m2} C_C} = \frac{1}{2\pi \times 58139 \times 691085 \times 643\mu \times 2.1p} = 2.93 \text{ kHz}$$

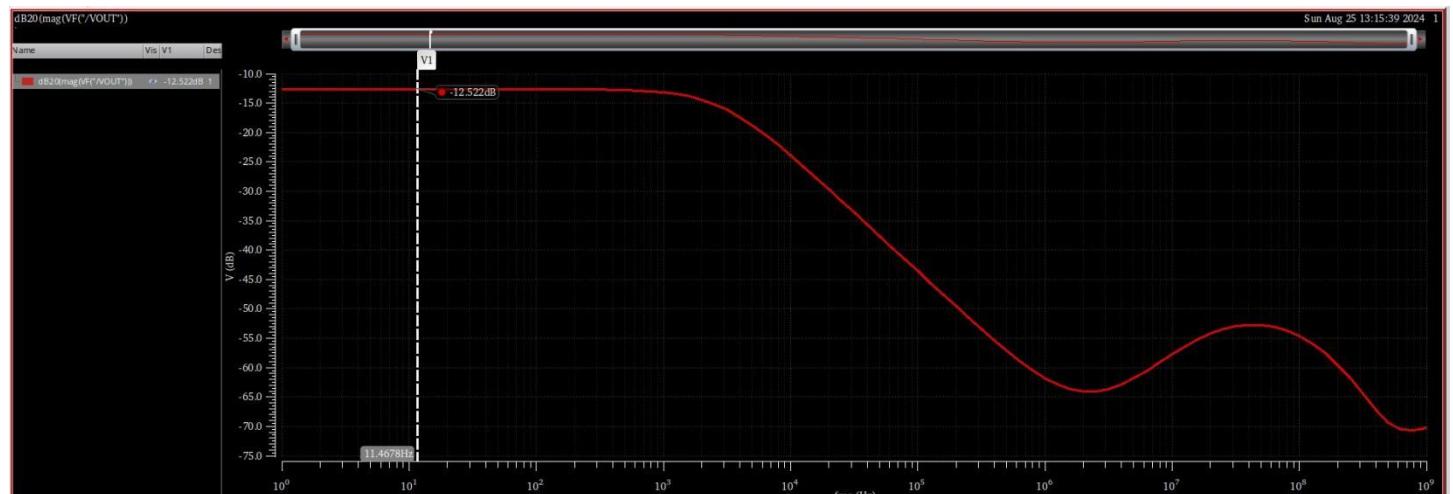
$$GBW = A_{OL} BW = 2457 \times 2930 = 7.2 \text{ MHz}$$

$$A_{OL}(S) = \frac{A_{OL}}{\sqrt{1 + (\frac{S}{\omega_{p1}})^2}} = 1, S = \omega_{p1} \sqrt{(A_{OL}^2 - 1)} = 7.2 \text{ MHz}$$

	Hand analysis	simulation
A _{OL}	2457 67.8 dB	2449 67.77 dB
BW	2930 Hz	2820 Hz
GBW	7.2 MHz	6.9 MHz
UGF	7.2 MHz	6.6 MHz

CM small signal:

CM gain in dB VS frequency:



Results from simulation:

Test	Output	Nominal	Spec	Weight	Pass/Fail
two_stage_OTA:test_bench_final:1	VF("/VOUT")				
two_stage_OTA:test_bench_final:1	Ao	236.5m			
two_stage_OTA:test_bench_final:1	BW	2.82k			
two_stage_OTA:test_bench_final:1	Ao_dB	-12.52			
two_stage_OTA:test_bench_final:1	GBW	667.2			
two_stage_OTA:test_bench_final:1	UGF	eval err			
two_stage_OTA:test_bench_final:1	dB20(mag(VF("/VOUT")))				

Hand analysis:

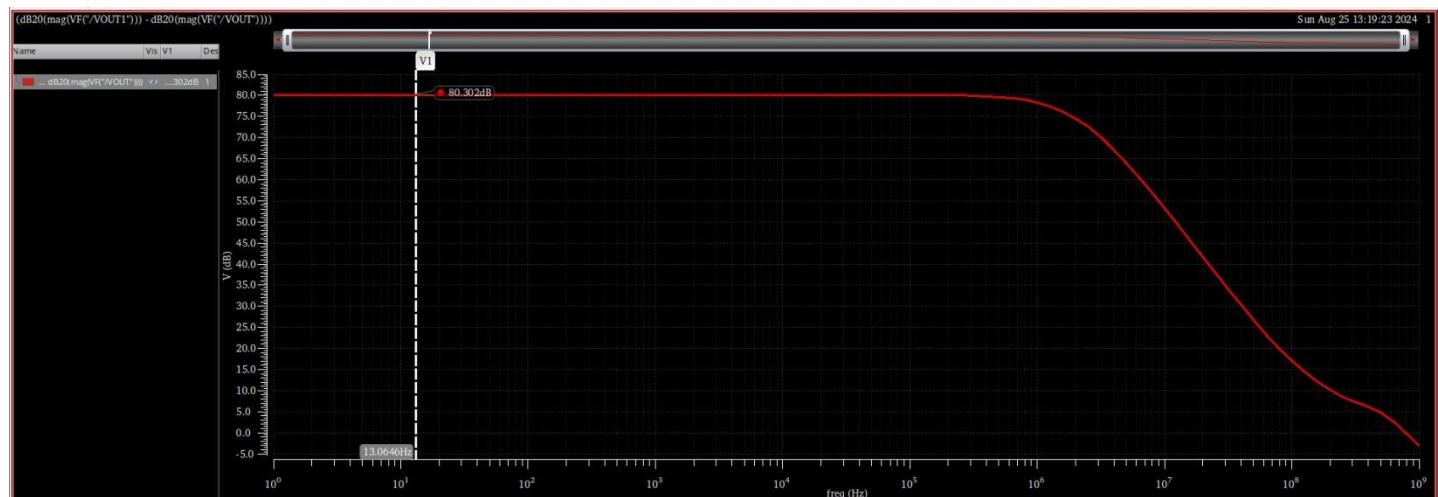
$$|A_{CM}| = \frac{g_{m1,2} \cdot A_{V2}}{1 + 2g_{m1,2}r_{o5} g_{m3,4}} \frac{1}{1 + 2 \times 95\mu \times \frac{1}{1.374\mu}} \frac{95\mu \times 37.38}{106\mu} = 240m = -12.39dB$$

$$GBW = A_{OL}BW = 240m \times 2930 = 703 \text{ Hz}$$

	Hand analysis	Simulation
A _{CM}	240m -12.39 dB	236.5m -12.52 dB
BW	2930 Hz	2820 Hz
GBW	703 Hz	667 Hz

CMRR simulation:

CMRR in dB VS frequency:



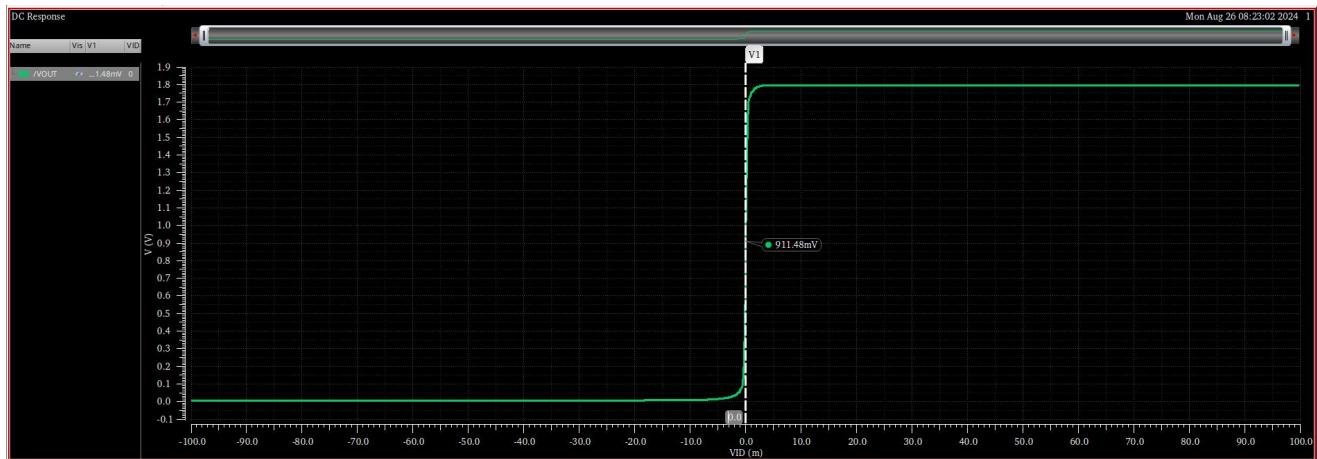
Hand analysis:

$$CMRR = 2g_{m1,2}(r_{o2}/r_{o4})r_{o5}g_{m3,4} = 10129 = 80.11 \text{ dB}$$

	Hand analysis	Simulation
CMRR	10129 80.11 dB	10350 80.3 dB

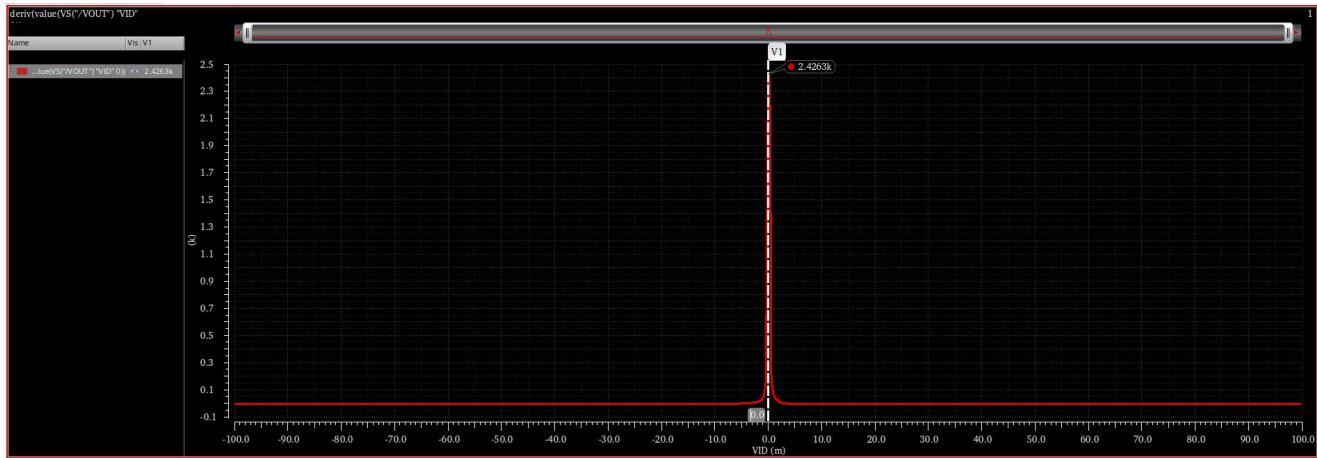
Diff large signal:

V_{OUT} VS V_{ID} :



From the graph, $V_{OUT} = 911$ mV at $V_{ID} = 0$, which is the same as DC OP simulation.

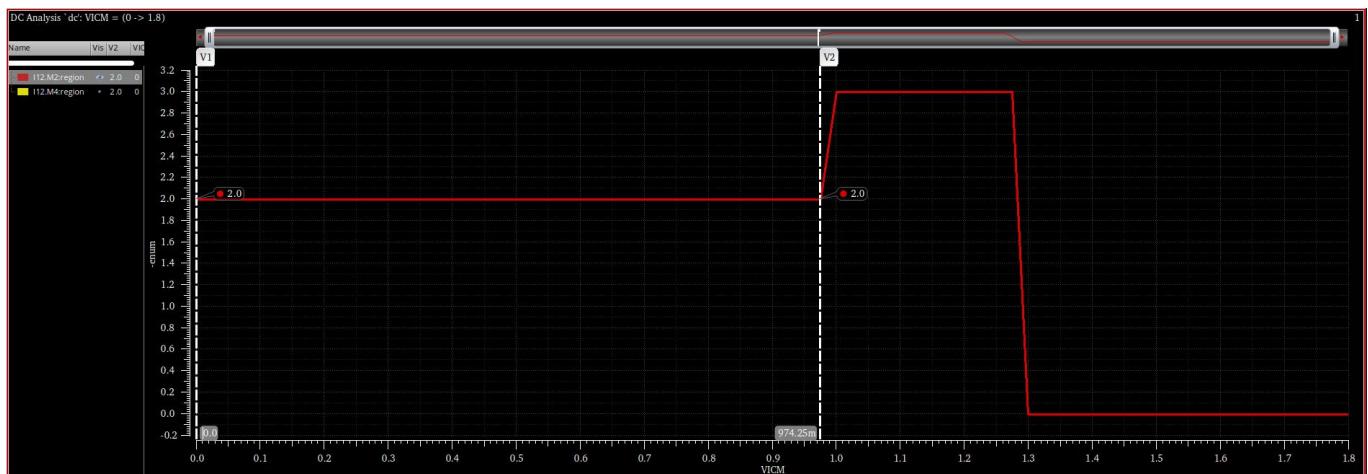
Derivative of V_{OUT} VS V_{ID} :



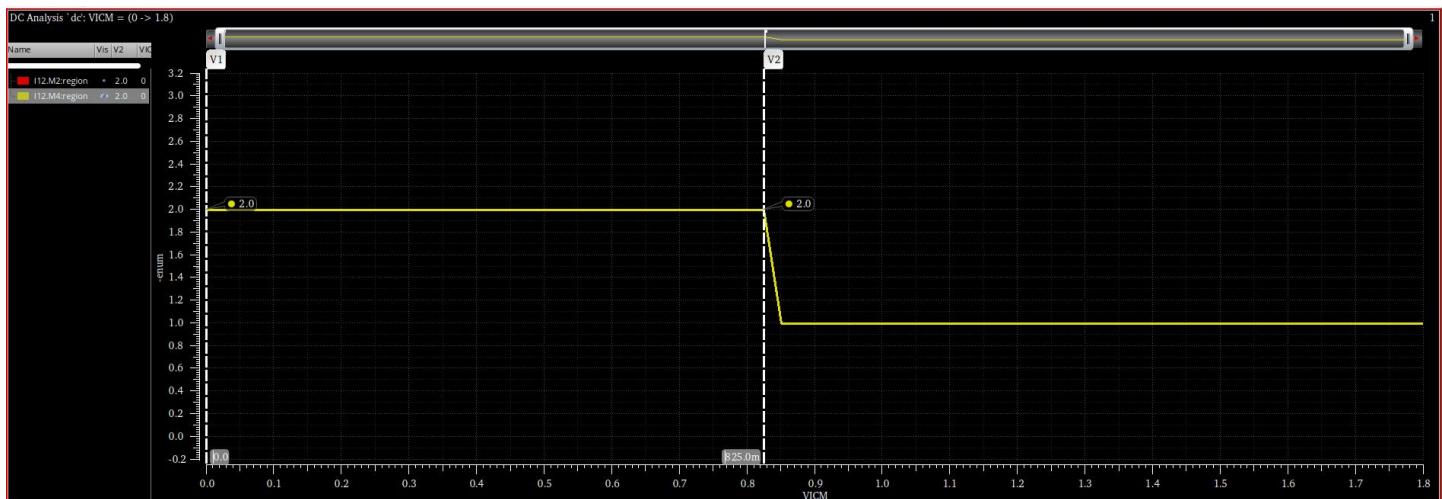
The gain from the graph is a little bit smaller than one from the AC analysis, because derivative of V_{OUT} has some error as the step increase, because the gain is not linear at all, then as we use a smaller step, the gain get closer to the AC value.

CM large signal analysis (region VS VINCM):

Region OP of the input pair VS VINCM:



Region OP of the tail current source VS VINCM:



Hand analysis:

$$V_{IN,MIN} = -V_{SG1,2} + V_{DSAT,1,2} + V_{GS3,4}$$

$$V_{IN,MIN} = -0.014 \text{ mV}$$

$$V_{IN,MAX} = V_{DD} - V_{SG1,2} - V_{DSAT5}$$

$$V_{IN,MAX} = 0.833 \text{ mV}$$

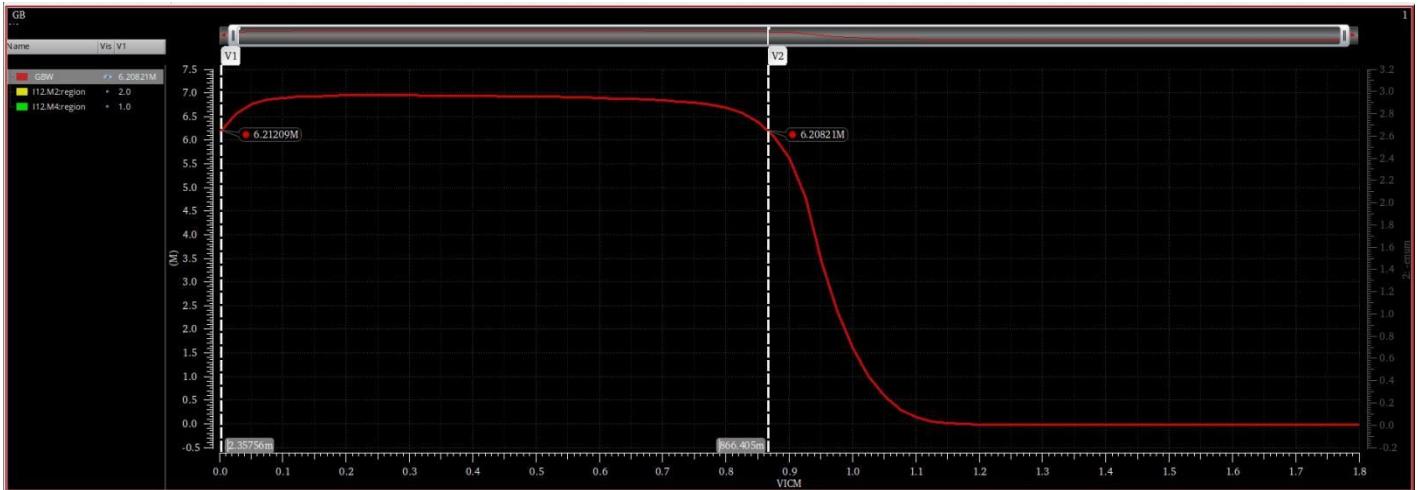
	Hand analysis	Simulation
$V_{INCM,MAX}$	833 mV	825 mV
$V_{INCM,MIN}$	-14 mV	0 V

CM large signal analysis (GBW VS VINCM):

GBW with region parameter for input pair and tail CS overlaid VS VICM:

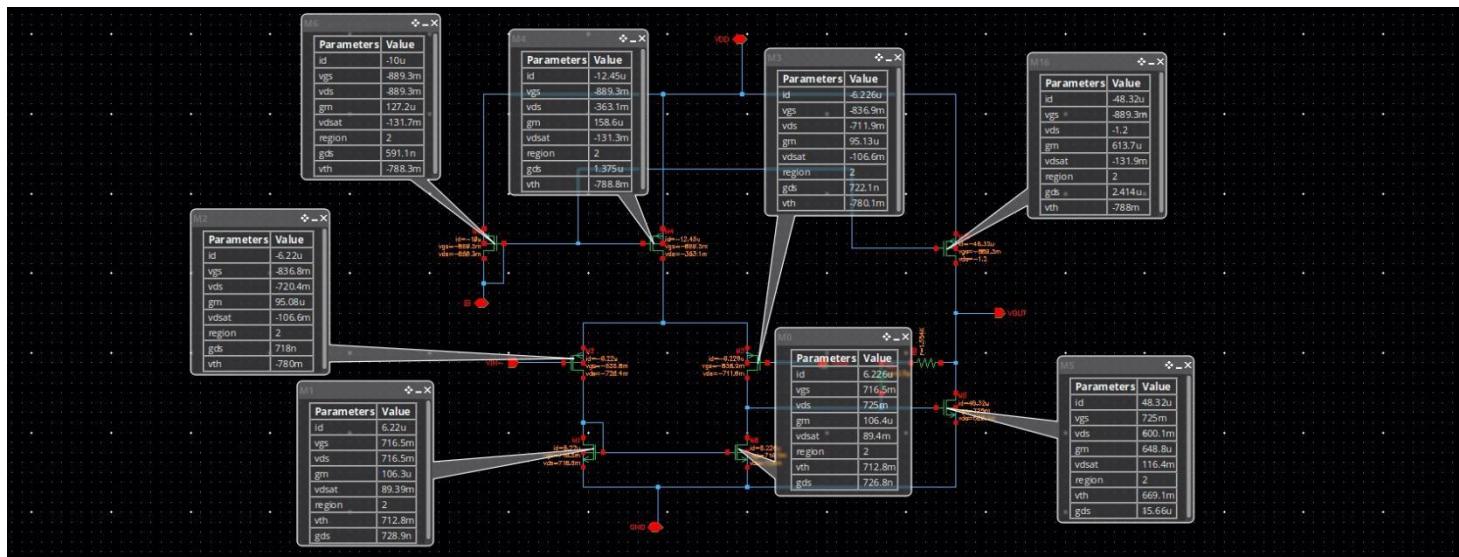


GBW VS VINCM:



From the graph, the range of VINCM is from 2 mV to 866 mV

PART 4: Closed-Loop OTA Simulation



The voltages at the input terminals are almost the same, as the open loop gain is very high, then the error signal ($V_{IN+} - V_{IN-}$) tends to zero, we can see it from another point of view, as the open loop gain get higher, then the closed loop gain get closer to 1 (ideal buffer), so which mean V_{OUT} is equal to V_{IN-} by buffer connection, then $V_{IN+} = V_{IN-}$

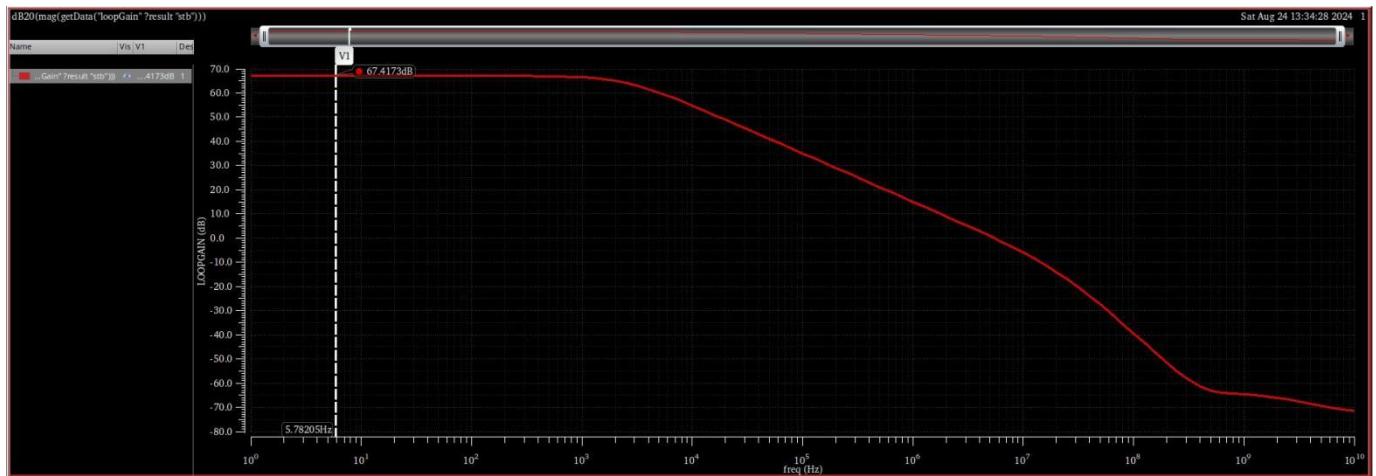
two_stage_OTA:test_bench_final:1	VDC("VIN-")	600.1m	
two_stage_OTA:test_bench_final:1	VDC("VIN+")	600m	

There is a small change in the DC voltage at output node of the first stage, and the reason for that is V_{error} is not equal to zero, that little error will lead to change in V_{DS} of the input pairs, then change in the V_{DS} of the current mirror load, also the output node will no longer follow the V_{GS} of the diode connected current mirror load, which did not change from the open loop DC OP simulaiton.

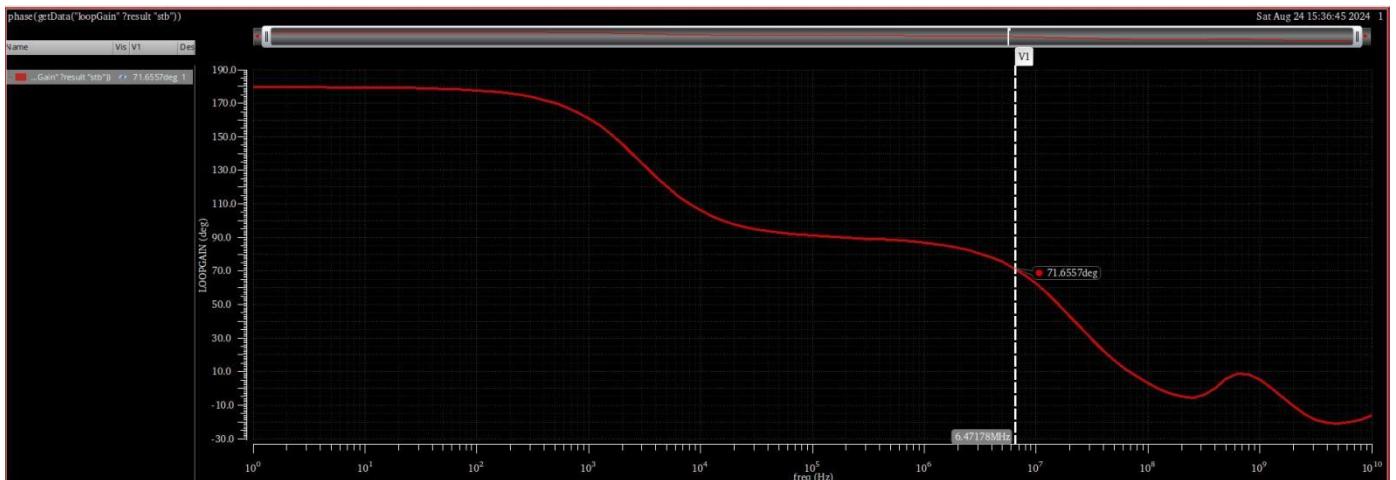
The current and g_m for input pairs is not exactly equal, and this error exists because there is a very small difference between them (V_{error} is not equal to zero), also the output node will no longer follow the V_{GS} of the diode connected current mirror load, then not necessary that the currents are equal, then g_m are not equal.

Loop gain simulation:

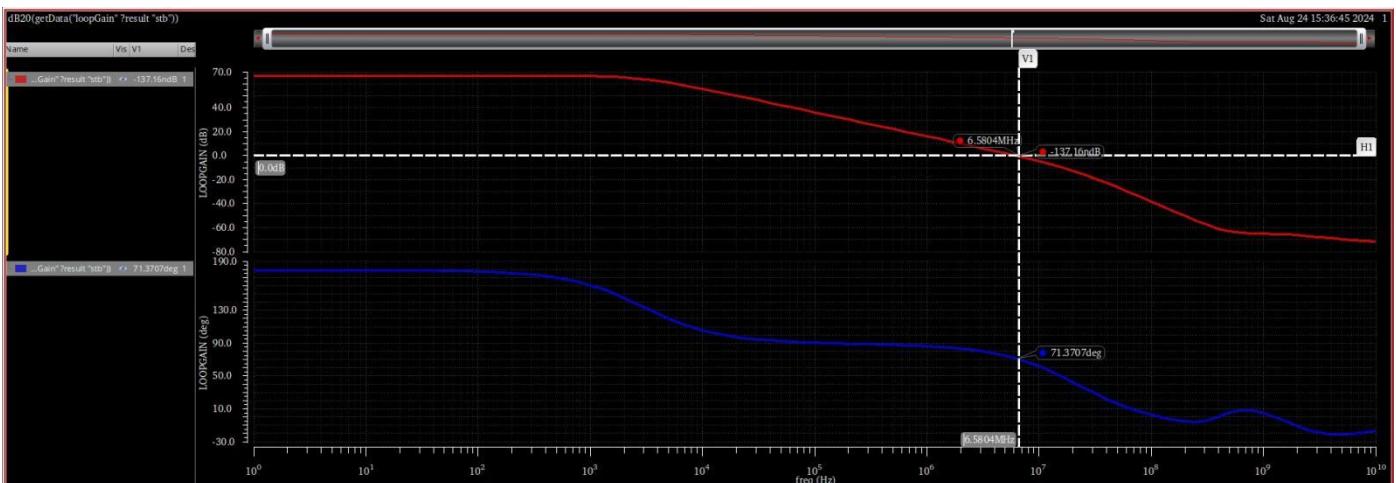
Loop gain VS frequency:



Phase of the loop gain VS frequency:



Phase margin when loop gain = 0 dB



two_stage OTA:test_bench_final:1	bandwidth(getData("loopGain" ?result "stb") 3 "low")	2.936k		
two_stage OTA:test_bench_final:1	ymax(mag(getData("loopGain" ?result "stb")))	2.349k		
two_stage OTA:test_bench_final:1	(ymax(mag(getData("loopGain" ?result "stb")))) * bandwidth(getData(...	6.897M		
two_stage OTA:test_bench_final:1	unityGainFreq(getData("loopGain" ?result "stb"))	6.61M		

	Open loop	Closed loop
$A_{OL} = A_{LG}$	2449 67.77 dB	2349 67.41 dB
BW	2820 Hz	2936 Hz
GBW	6.9 MHz	6.89 MHz
UGF	6.6 MHz	6.6 MHz

We can notice that the band width increased, and the the loop gain has decreased, although it is a buffer. Then the GBW and UGF are almost the same.

The loop gain has decreased because of the loading effect, then the band width has increased, so that GBW is constant.

PM from the simulation:

$$PM = 71.4 \text{ deg}$$

Hand analysis:

$$PM = 180 - \tan^{-1}\left(\frac{\omega}{\omega_{p1}}\right) - \tan^{-1}\left(\frac{\omega}{\omega_{p2}}\right)$$

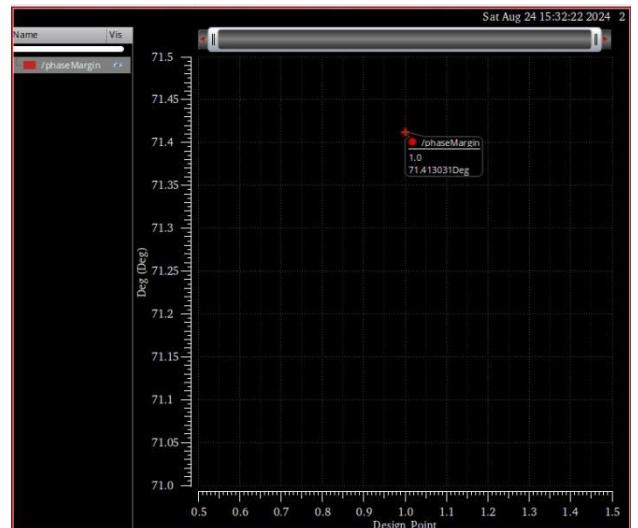
The unity gain frequency = 41.3 M rad/sec

$$\omega_{p1} = BW = 18447 \text{ rad/sec}$$

$$\omega_{p2} = \frac{g_m^2}{C_L} = 128.6 \text{ M rad/sec}$$

$$PM = 180 - \tan^{-1}\left(\frac{41.3 \text{ M}}{18447}\right) - \tan^{-1}\left(\frac{41.3 \text{ M}}{128.61 \text{ M}}\right)$$

$$PM = 180 - 90 - 17.9 = 72 \text{ deg}$$



Hand analysis of the DC gain, BW, GBW and UGF is the same as open loop

	Hand analysis	Simulation
A_{OL}	2457 67.8 dB	2349 67.41dB
BW	2930 Hz	2936 Hz
GBW	7.2 MHz	6.89 MHz
UGF	7.2 MHz	6.6 MHz
PM	72 deg	71.4 deg

Slew rate simulation:

V_{IN} and V_{OUT} overlaid VS time:



Test	Output	Nominal	Spec	Weight	Pass/Fail
two_stage_OTA:test_bench_final:1	VT("VOUT")				
two_stage_OTA:test_bench_final:1	VT("VIN+")				
two_stage_OTA:test_bench_final:1	ymax(deriv(VT("VOUT")))	5.367M			

Hand analysis:

$$SR = \frac{I_{MAX}}{C_C} = 5.9 \text{ V}/\mu\text{S}$$

	Hand analysis	Simulation
SR	5.9 V/ μ S	5.367 V/ μ S

Settling time simulation:

V_{IN} and V_{OUT} overlaid VS time:



The rise time for V_{OUT} :

Test	Output	Nominal	Spec	Weight	Pass/Fail
two_stage_OTA:test_bench_final:1	VT("/VOUT")				
two_stage_OTA:test_bench_final:1	VT("/VIN+")				
two_stage_OTA:test_bench_final:1	riseTime(VT("/VOUT")) 0.6 nil 0.6...	34.92 n			

$$\text{Rise time} = 2.2\tau = \frac{2.2}{\text{BW}_{\text{CL}}} = \frac{2.2}{2930 \times (1 + 2457)} = 48.6 \text{ ns}$$

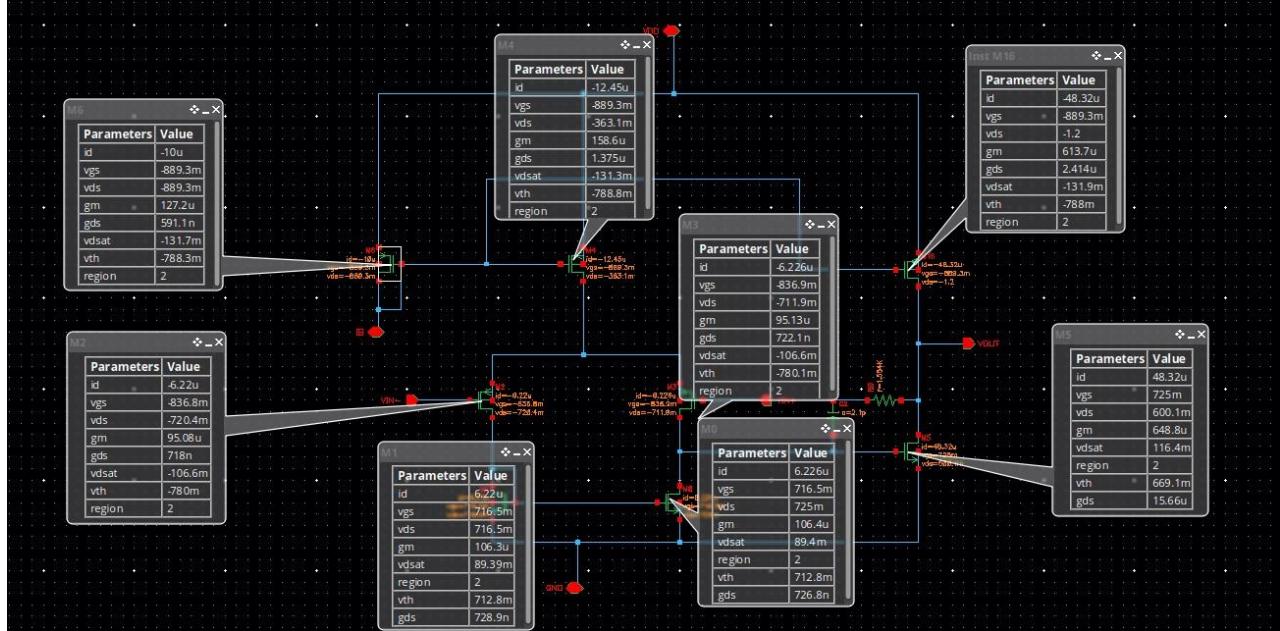
	Hand analysis	Simulation
Rise time	34.9 ns	48.6 ns

There is an overshoot in the output, and the reason for that is the system is not a critical damped system, it is an under damped system, the critical one has PM about 76 deg, so that there is an overshoot in the output.

The rise time hand analysis has some error, since the rule used is for a first order system, but we deal with a second order one, so it is faster.

Part 5 : DC Closed Loop AC Open-Loop OTA Simulation

DC OP analysis:



The currents and g_m of the input pairs are not exactly equal, and that is because output node of the first stage is no longer follow the node V_G of the diode connected current mirror load, so the currents and g_m will be different, also the input voltage of the input pairs are slightly different, as V_{ERROR} does not equal to zero.

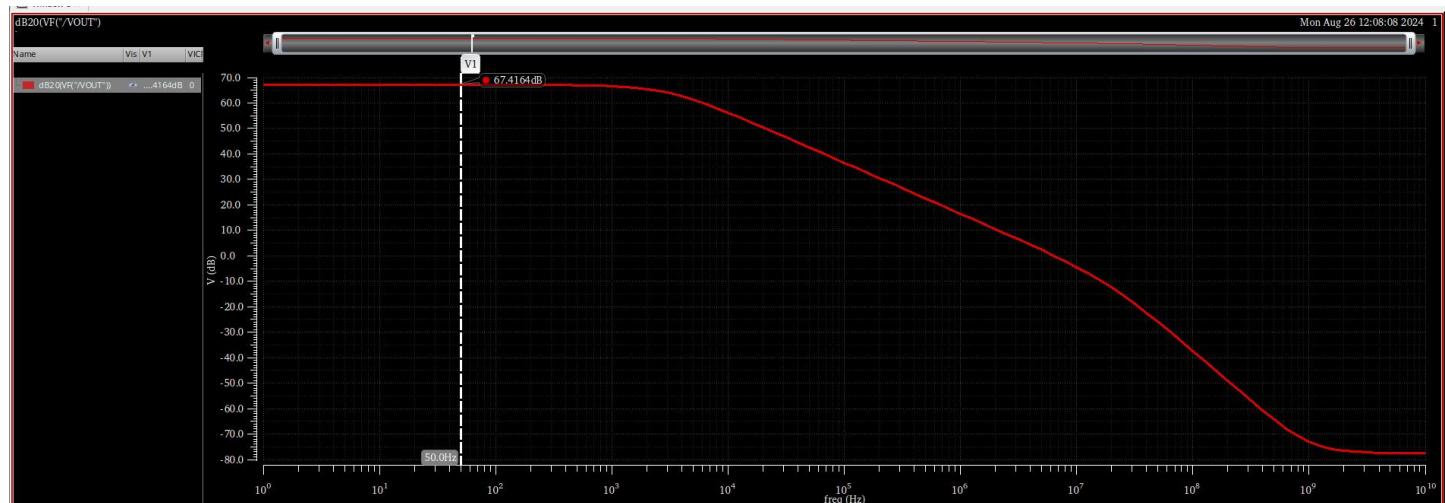
The DC output voltage of the first stage, $V_{OUT1} = 725$ mV

It should follow the node will mentioned above, but it slightly changed ($V_G = 716.5$ mV)

The DC output voltage of the second stage, $V_{OUT2} = 600.1$ mV, as V_{OUT2} follows V_{IN} .

Diff small signal analysis:

Diff gain in dB VS frequency:



Test	Output	Nominal	Spec	Weight	Pass/Fail
two_stageOTA:test_bench_final:1	bandwidth(VF("/VOUT") 3 "low")	2.936k			
two_stageOTA:test_bench_final:1	ymax(mag(VF("/VOUT")))	2.349k			
two_stageOTA:test_bench_final:1	(ymax(mag(VF("/VOUT")))) * ban...	6.897M			
two_stageOTA:test_bench_final:1	unityGainFreq(VF("/VOUT"))	6.615M			
two_stageOTA:test_bench_final:1	ymax(dB20(VF("/VOUT")))	67.42			

Hand analysis:

$$A_{OL} = A_{v1} \times A_{v2} = (g_{m1,2}(r_{o1,2}/r_{o3,4})).(g_{m6}(r_{o6}/r_{o7}))$$

$$A_{OL} = (95.11\mu \times (\frac{1}{718n}/\frac{1}{729n})).(643\mu \times (\frac{1}{2.81\mu}/\frac{1}{14.39\mu})) = 2457 = 67.8 \text{ dB}$$

$$BW = \frac{1}{2\pi R_{OUT1} R_{OUT2} G_{m2} C_C} = \frac{1}{2\pi \times 58139 \times 691085 \times 643\mu \times 2.1p} = 2.93 \text{ kHz}$$

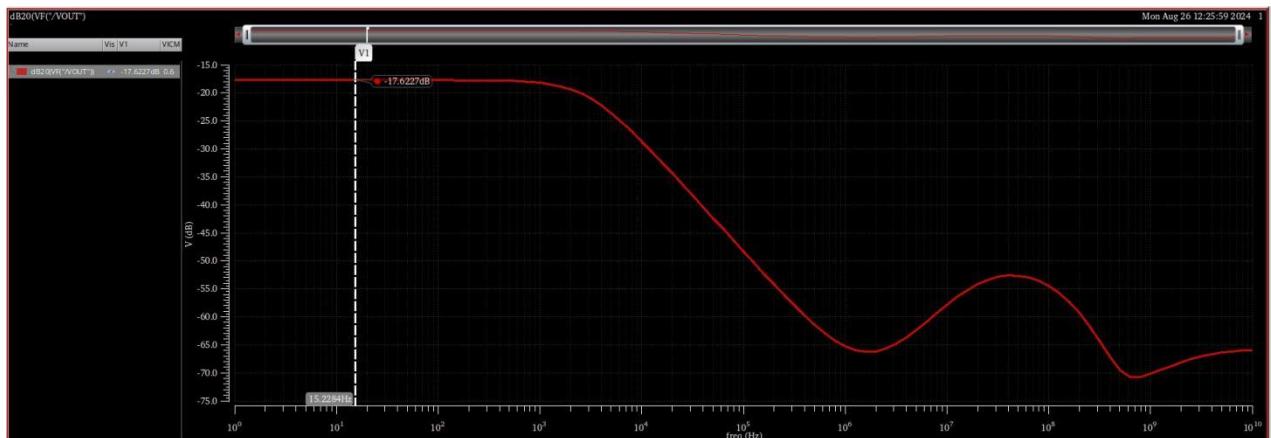
$$GBW = A_{OL} BW = 2457 \times 2930 = 7.2 \text{ MHz}$$

$$A_{OL}(S) = \frac{A_{OL}}{\sqrt{1 + (\frac{S}{\omega_{p1}})^2}} = 1, S = \omega_{p1} \sqrt{(A_{OL}^2 - 1)} = 7.2 \text{ MHz}$$

	Hand analysis	simulation
A _{OL}	2457 67.8 dB	2349 67.42 dB
BW	2930 Hz	2936 Hz
GBW	7.2 MHz	6.897 MHz
UGF	7.2 MHz	6.6 MHz

CM small signal:

CM gain in dB VS frequency:



Results from simulation:

Test	Output	Nominal	Spec	Weight	Pass/Fail
two_stage_OTA:test_bench_final:1	bandwidth(VF("VOUT") 3 "low")	2.936k			
two_stage_OTA:test_bench_final:1	ymax(mag(VF("VOUT")))	131.5m			
two_stage_OTA:test_bench_final:1	(ymax(mag(VF("VOUT")) * ban...)	386.1			
two_stage_OTA:test_bench_final:1	unityGainFreq(VF("VOUT"))	eval err			
two_stage_OTA:test_bench_final:1	ymax(dB20(VF("VOUT")))	-17.62			
two_stage_OTA:test_bench_final:1	dB20(VF("VOUT"))				

Hand analysis:

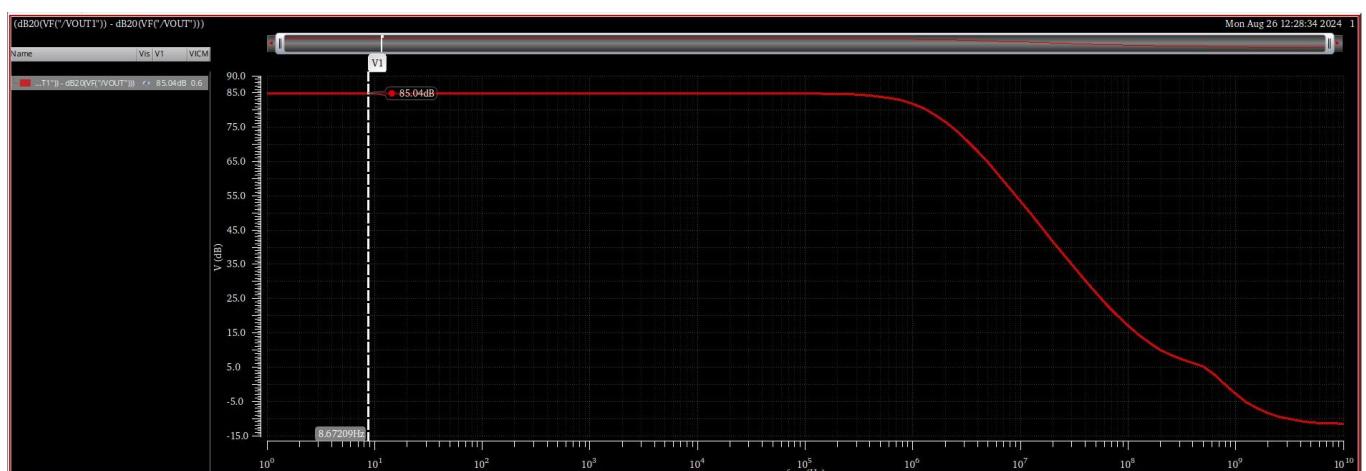
$$|A_{CM}| = \frac{g_{m1,2} \cdot A_{V2}}{1 + 2g_{m1,2}r_{o5}} \frac{1}{g_{m3,4}} = \frac{95\mu \times 37.38}{1 + 2 \times 95\mu \times \frac{1}{1.374\mu}} \frac{1}{106\mu} = 240m = -12.39dB$$

$$\text{GBW} = A_{OL} \text{BW} = 240m \times 2930 = 703 \text{ Hz}$$

	Hand analysis	Simulation
A _{CM}	240m -12.39 dB	131m -17.65 dB
BW	2930 Hz	2936 Hz
GBW	703 Hz	386 Hz

CMRR simulation:

CMRR in dB VS frequency:



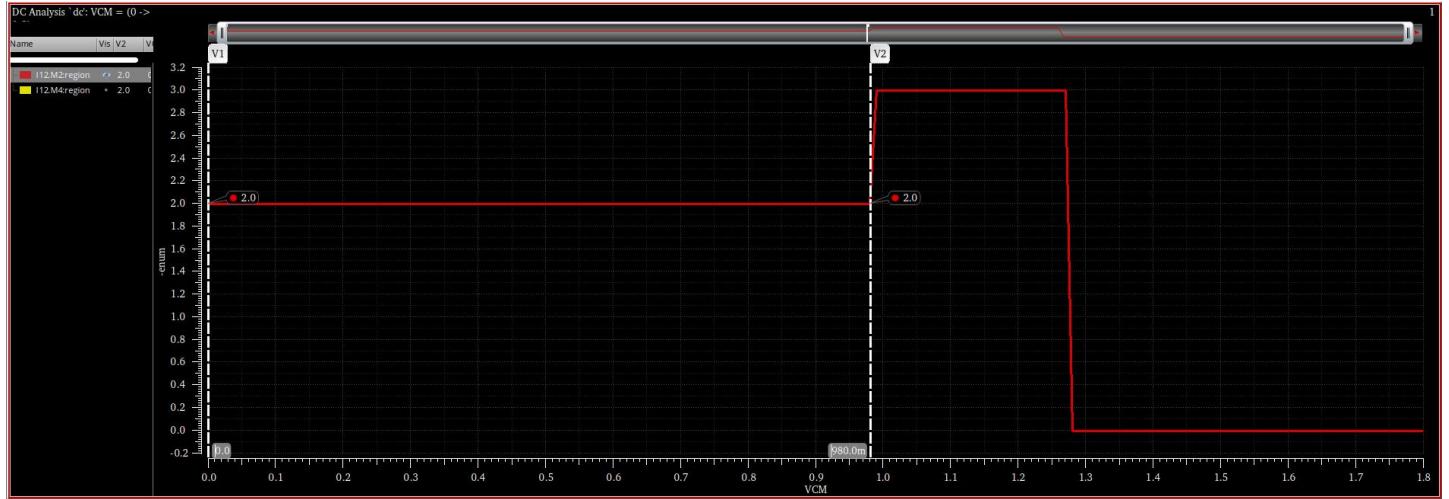
Hand analysis:

$$\text{CMRR} = 2g_{m1,2}(r_{o2}/r_{o4})r_{o5}g_{m3,4} = 10129 = 80.11 \text{ dB}$$

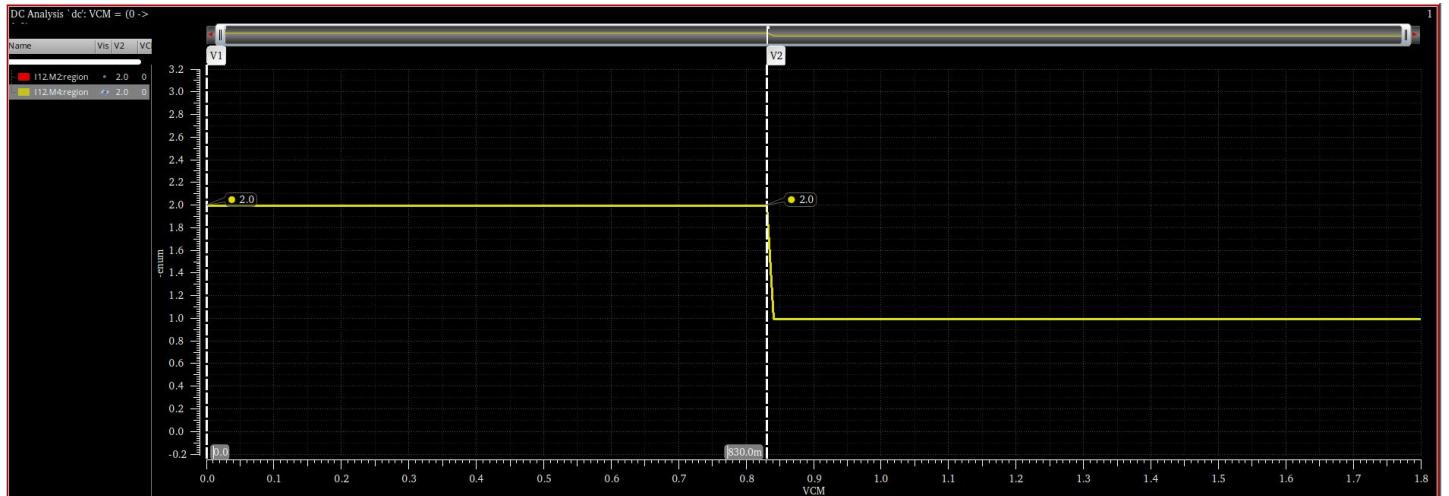
	Hand analysis	Simulation
CMRR	10129 80.11 dB	17782 85 dB

CM large signal analysis (region VS VINCM):

Region OP of the input pair VS VINCM:



Region OP of the tail current source VS VINCM:



Hand analysis:

$$V_{IN,MIN} = -V_{SG1,2} + V_{DSAT,1,2} + V_{GS3,4}$$

$$V_{IN,MIN} = -0.014 \text{ mV}$$

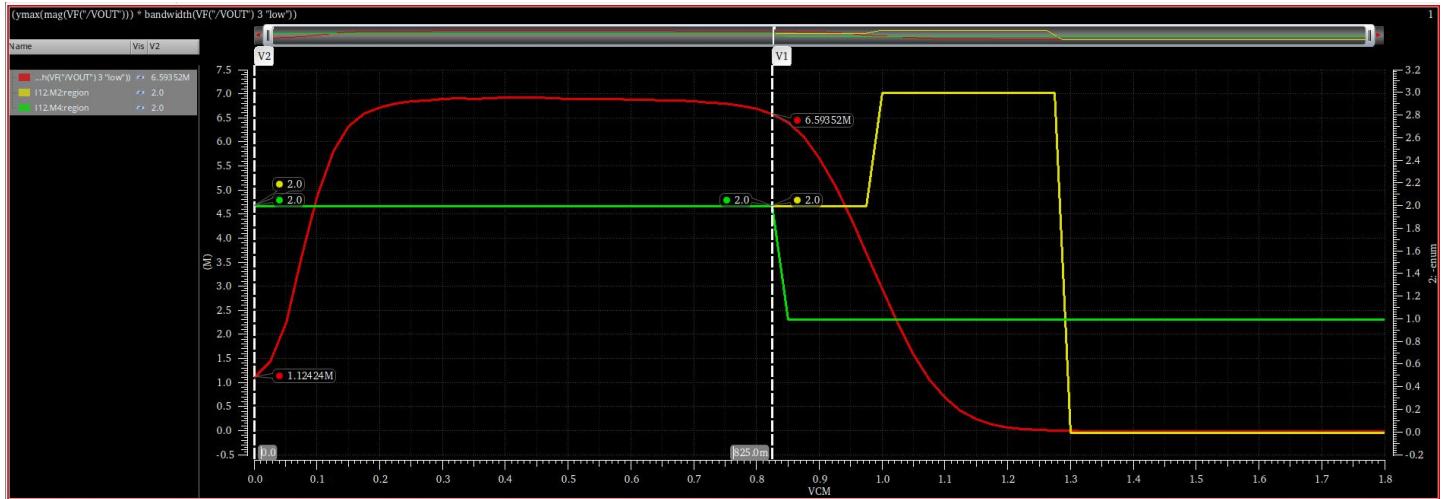
$$V_{IN,MAX} = V_{DD} - V_{SG1,2} - V_{DSAT5}$$

$$V_{IN,MAX} = 0.833 \text{ mV}$$

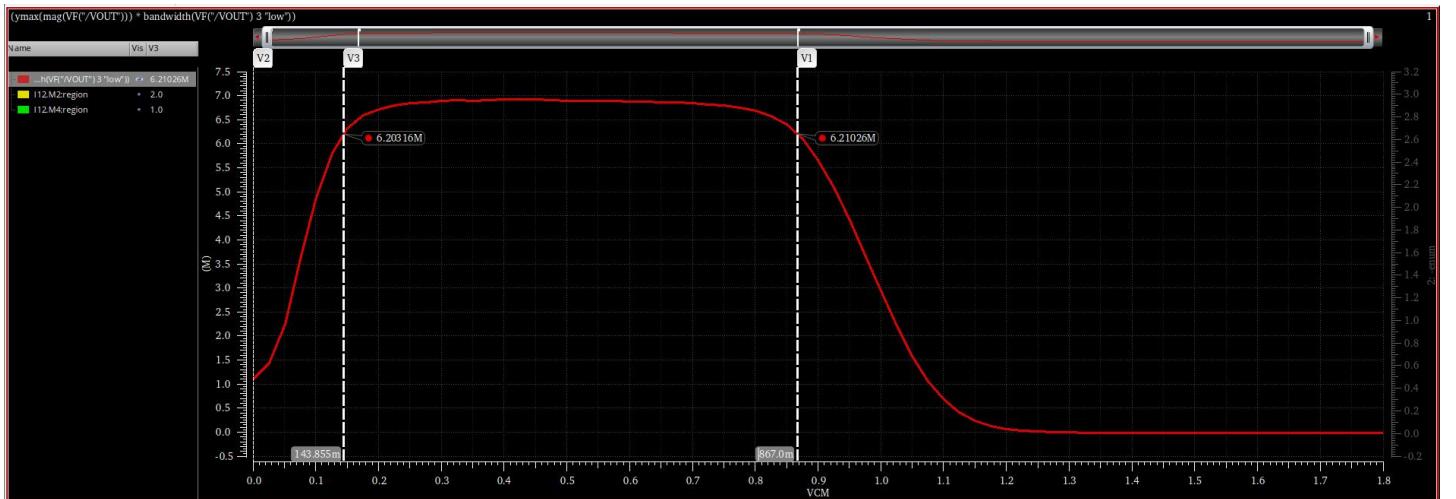
	Hand analysis	Simulation
$V_{INCM,MAX}$	833 mV	830 mV
$V_{INCM,MIN}$	-14 mV	0 V

CM large signal analysis (GBW VS VINCM):

GBW with region parameter for input pair and tail CS overlaid VS VICM:



GBW VS VINCM:



From the graph, the range of VICM is from 143 mV to 867 mV