FWC RTL Assignment 1

Mohamed Hamdan

FWC220007

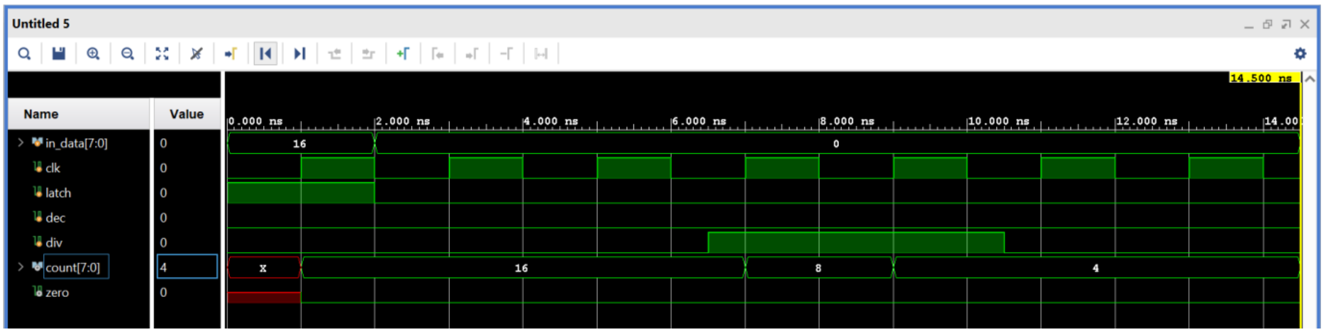
1) **Module code**

```
`timescale 1ns / 1ps

module down_counter_8bit(
// Inputs
input   wire    [7:0]   in_data,
input   wire            clk,
input   wire            latch,
input   wire            dec,
input   wire            div,
// Outputs
output  reg     [7:0]   count,
output  wire            zero
);

always @(posedge clk)
begin
    if(latch)
        count <= in_data;
    else if(dec)
        count <= (count==8'd0) ? 8'd0 : count-1;
    else if(div)
        count <= count >> 1;
end

assign zero = (count == 0);

endmodule
```

2) **Testbench code**

```
`timescale 1ns / 1ps

module down_counter_8bit_tb;
reg     [7:0]   in_data;
reg             clk, latch, dec, div;
wire    [7:0]   count;
wire            zero;

down_counter_8bit UUT(
    .in_data(in_data),
    .clk(clk),
    .latch(latch),
    .dec(dec),
    .div(div),
    .count(count),
    .zero(zero)
);

initial begin
    clk = 1'b0;
    forever #1 clk = ~clk;
end

initial begin
    in_data = 8'd16; latch = 1'b1; dec = 1'b0; div = 1'b0;
    #2 in_data = 8'd0; latch = 1'b0;
    #4.5 div = 1'b1;
    #4 div = 1'b0;
    #4 $finish;
end
endmodule
```

3) Timing diagram


Untitled 5
14.500 ns
Name
Value
in_data[7:0]
0
clk
0
latch
0
dec
0
div
0
count[7:0]
4
zero
0
0.000 ns
2.000 ns
4.000 ns
6.000 ns
8.000 ns
10.000 ns
12.000 ns
14.00
16
0
X
16
8
4