GPIO configuration for M4 access on Vaman LC board

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1 IO structure on EOSS3

According to the EOSS3 Technical Reference Manual (TRM), the ARM M4-F core can only access 7 IO pins through inbuilt registers. The FPGA/fabric can access all 46 IO pins provided the IO Multiplexer (IO-Mux) is configured appropriately by the M4. The IO-Mux is used to share a single IO pin between multiple functions like Fabric IO (FBIO), SPI master and slave bus, I2C bus and debug ports. In order for an IO pin to be accessible by the FPGA:

1. The function must be selected as FBIO. By default, all IO pins except IO_0, IO_1, IO_15 and IO_17 are configured as FBIO pins.
2. If the IO pin is used as output, its driver must be set to FPGA.
3. If the IO pin is used as input, its driver must be set to a register belonging to the Always-On power domain

The above configurations can be done by writing appropiate values to the PAD_x_CTRL registers. If an IO controller is present on the FPGA, the M4 can access all the IO pins by writing to and reading from a few registers present in the IO controller.

The C-function definition to configure the IO pins (PyHal_GPIO_Set) can be found in below link (lines 134-166):

`https://github.com/Muhammed-Hamdan/iith-fwc-2022-23/blob/main/fwc_arm/setup/gpio_fix/src/main.c`