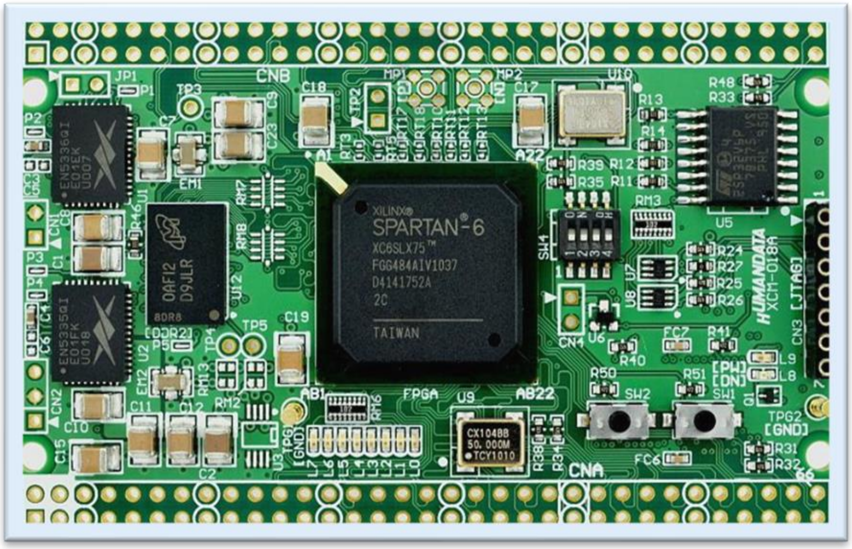
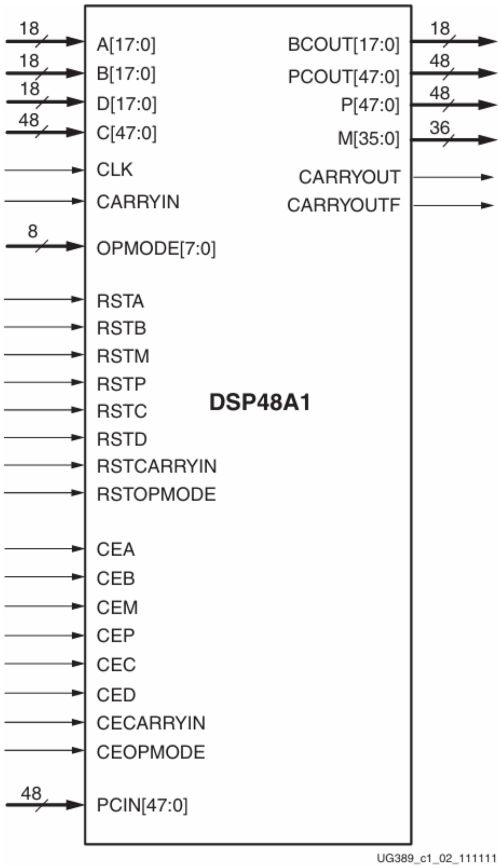
# Spartan6 - DSP48A1

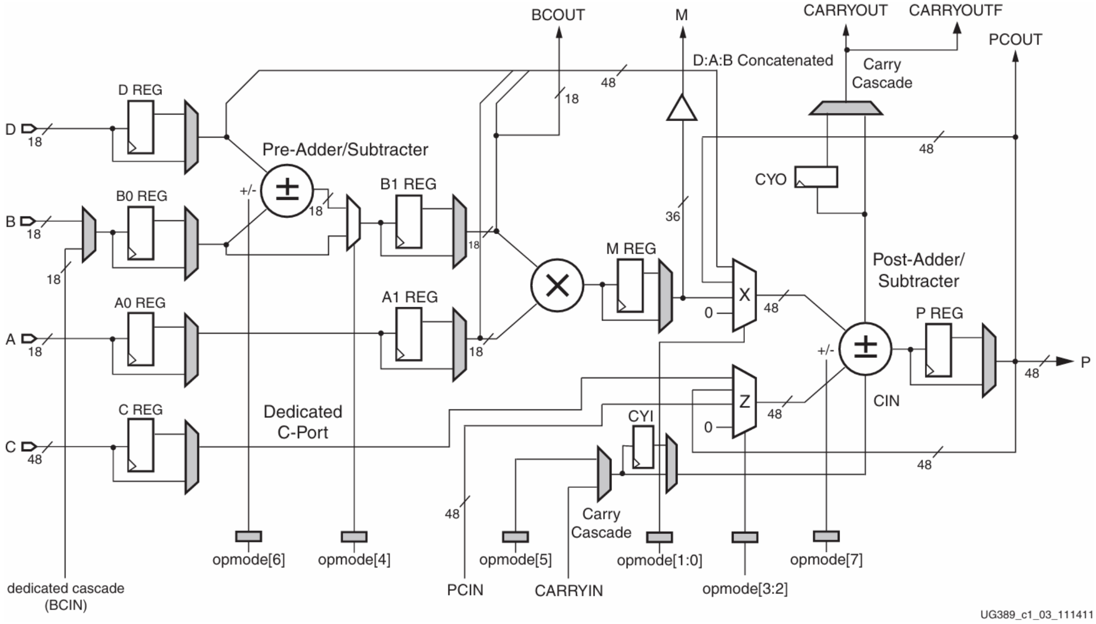


**Prepared by :** Mohamed Karam Mohamed

# Contents

RTL code ........ 4
DSP48A1.v ........ 4
MUX.v ........ 9
DFF.v ........ 9
Testbench code ........ 10
Do file ........ 13
QuestaSim snippets ........ 14
Verify Reset Operation ........ 14
Verify DSP Path 1 ........ 14
Verify DSP Path 2 ........ 15
Verify DSP Path 3 ........ 16
Verify DSP Path 4 ........ 17
Constraint file ........ 18
Elaboration ........ 18
Messages ........ 18
Schematic ........ 19
Synthesis ........ 21
Messages ........ 21
Utilization report ........ 22
timing report ........ 22
Schematic ........ 22
Implementation ........ 24
Messages ........ 24
Utilization report ........ 25
timing report ........ 25
Device ........ 25
Linting ........ 26


18
A[17:0]
18
B[17:0]
18
D[17:0]
48
C[47:0]
CLK
CARRYIN
8
OPMODE[7:0]
RSTA
RSTB
RSTM
RSTP
RSTC
RSTD
RSTCARRYIN
RSTOPMODE
CEA
CEB
CEM
CEP
CEC
CED
CECARRYIN
CEOPMODE
48
PCIN[47:0]
DSP48A1
18
BCOUT[17:0]
48
PCOUT[47:0]
48
P[47:0]
36
M[35:0]
CARRYOUT
CARRYOUTF
UG389_c1_02_111111


BCOUT
M
CARRYOUT
CARRYOUTF
PCOUT
D:A:B Concatenated
Carry
Cascade
48
18
D REG
D
18
Pre-Adder/Subtracter
+/-
±
18
B1 REG
B0 REG
B
18
18
18
CYO
48
36
M REG
X
0
48
Post-Adder/
Subtracter
P REG
A0 REG
A
18
A1 REG
18
+/-
±
CIN
P
48
C REG
C
48
Dedicated
C-Port
Z
48
0
CYI
48
Carry
Cascade
48
opmode[6]
opmode[4]
opmode[5]
opmode[1:0]
opmode[3:2]
opmode[7]
PCIN
CARRYIN
dedicated cascade
(BCIN)
UG389_c1_03_111411

# RTL CODE

## DSP48A1.v

```
module DSP48A1 (
                A, B, C, D, CARRYIN,
                M, P, CARRYOUT, CARRYOUTF,
                CLK, OPMODE,
                CEA, CEB, CEC, CECARRYIN, CED, CEM, CEOPMODE, CEP,
                RSTA, RSTB, RSTC, RSTCARRYIN, RSTD, RSTM, RSTOPMODE, RSTP,
                BCIN, BCOUT, PCIN, PCOUT
        );

    parameter A0REG = 0, A1REG = 1;
    parameter B0REG = 0, B1REG = 1;
    parameter CREG = 1, DREG = 1, MREG = 1, PREG = 1;
    parameter CARRYINREG = 1, CARRYOUTREG = 1, OPMODEREG = 1;
    parameter CARRYINSEL = "OPMODE5", B_INPUT = "DIRECT", RSTTYPE = "SYNC";

    // Data Input Ports
    input [17:0] A, B, D;
    input [47:0] C;
    input CARRYIN;
    // Data Output Ports
    output [35:0] M;
    output [47:0] P;
    output CARRYOUT, CARRYOUTF;
    // Control Ports
    input CLK;
    input [7:0] OPMODE;
    // Clock Enable Ports
    input CEA, CEB, CEC, CED, CEM, CEP;
    input CECARRYIN, CEOPMODE;
    // Reset Ports (Active High)
    input RSTA, RSTB, RSTC, RSTD, RSTM, RSTP;
    input RSTCARRYIN, RSTOPMODE;
    // Cascade Ports
    input [17:0] BCIN;
    output [17:0] BCOUT;
    input [47:0] PCIN;
    output [47:0] PCOUT;

    // Internal Wires
    wire [17:0] a0_out, a1_out, a0_reg_out, a1_reg_out;
    wire [17:0] b0_out, b1_out, b_mux_out, b0_reg_out, b1_reg_out;
    wire [47:0] c_out, c_reg_out;
    wire [17:0] d_out, d_reg_out;
    wire [7:0] opmode_out, opmode_reg_out;
    wire carryin_mux_out, carryin_reg_out, cyi_out;
```

```verilog
wire carryout_wire, carryout_reg_out;
wire [17:0] pre_add_sub_out;
wire [17:0] opmode4_mux_out;
wire [35:0] mult_out, m_out, m_reg_out;
wire [47:0] concatenated_buses;
wire [47:0] x_mux_out, z_mux_out;
wire [47:0] post_add_sub_out;
wire [47:0] p_reg_out;

// ==============Input Pipeline Registers==============
// -----------------------A Path-----------------------
// A0 Register and Mux
DFF #(.WIDTH(18), .RSTTYPE(RSTTYPE)) a0_reg (
      .clk(CLK), .rst(RSTA), .CE(CEA), .D(A), .Q(a0_reg_out)
);
MUX #(.WIDTH(18), .INPUTS(2)) a0_mux (
    .in0(A),           // Direct input
    .in1(a0_reg_out),  // Registered input
    .in2(18'b0), .in3(18'b0),  // Unused
    .sel(A0REG[0]), .out(a0_out)
);
// A1 Register and Mux
DFF #(.WIDTH(18), .RSTTYPE(RSTTYPE)) a1_reg (
    .clk(CLK), .rst(RSTA), .CE(CEA), .D(a0_out), .Q(a1_reg_out)
);
MUX #(.WIDTH(18), .INPUTS(2)) a1_mux (
    .in0(a0_out),      // Direct input
    .in1(a1_reg_out),  // Registered input
    .in2(18'b0), .in3(18'b0),  // Unused
    .sel(A1REG[0]), .out(a1_out)
);

// -----------------------B Path-----------------------
// B input port mux
MUX #(.WIDTH(18), .INPUTS(2)) b_input_mux (
    .in0(B),     // DIRECT
    .in1(BCIN),  // CASCADE
    .in2(18'b0), .in3(18'b0),  // Unused
    .sel(B_INPUT == "CASCADE"), .out(b_mux_out)
);
// B0 Register and Mux
DFF #(.WIDTH(18), .RSTTYPE(RSTTYPE)) b0_reg (
    .clk(CLK), .rst(RSTB), .CE(CEB), .D(b_mux_out), .Q(b0_reg_out)
);
MUX #(.WIDTH(18), .INPUTS(2)) b0_mux (
    .in0(b_mux_out),   // Direct input
    .in1(b0_reg_out),  // Registered input
    .in2(18'b0), .in3(18'b0),  // Unused
    .sel(B0REG[0]), .out(b0_out)
);
```

```verilog
// B1 Register and Mux
DFF #(.WIDTH(18), .RSTTYPE(RSTTYPE)) b1_reg (
    .clk(CLK), .rst(RSTB), .CE(CEB), .D(opmode4_mux_out), .Q(b1_reg_out)
);
MUX #(.WIDTH(18), .INPUTS(2)) b1_mux (
    .in0(opmode4_mux_out),    // Direct input
    .in1(b1_reg_out),        // Registered input
    .in2(18'b0), .in3(18'b0),       // Unused
    .sel(B1REG[0]), .out(b1_out)
);
assign BCOUT = b1_out;

// -----------------------C Path-----------------------
// C Register and Mux
DFF #(.WIDTH(48), .RSTTYPE(RSTTYPE)) c_reg (
    .clk(CLK), .rst(RSTC), .CE(CEC), .D(C), .Q(c_reg_out)
);
MUX #(.WIDTH(48), .INPUTS(2)) c_mux (
    .in0(C),          // Direct input
    .in1(c_reg_out),  // Registered input
    .in2(48'b0), .in3(48'b0), // Unused
    .sel(CREG[0]), .out(c_out)
);

// -----------------------D Path-----------------------
// D Register and Mux
DFF #(.WIDTH(18), .RSTTYPE(RSTTYPE)) d_reg (
    .clk(CLK), .rst(RSTD), .CE(CED), .D(D), .Q(d_reg_out)
);
MUX #(.WIDTH(18), .INPUTS(2)) d_mux (
    .in0(D),          // Direct input
    .in1(d_reg_out),  // Registered input
    .in2(18'b0), .in3(18'b0),  // Unused
    .sel(DREG[0]), .out(d_out)
);

// ====================================================
// -----------------------OPMODE-----------------------
// OPMODE Register and Mux
DFF #(.WIDTH(8), .RSTTYPE(RSTTYPE)) opmode_reg (
     .clk(CLK), .rst(RSTOPMODE), .CE(CEOPMODE), .D(OPMODE),
  .Q(opmode_reg_out)
);
MUX #(.WIDTH(8), .INPUTS(2)) opmode_mux (
    .in0(OPMODE),         // Direct input
    .in1(opmode_reg_out), // Registered input
    .in2(8'b0), .in3(8'b0),  // Unused
    .sel(OPMODEREG[0]), .out(opmode_out)
);
```

```
// -----------------Pre-Adder/Subtracter-----------------
assign pre_add_sub_out = opmode_out[6] ? (d_out - b0_out) : (d_out + b0_out);

// --------------------OPMODE[4] Mux---------------------
assign opmode4_mux_out = opmode_out[4] ? pre_add_sub_out : b0_out;

// -----Multiplier ((A * B) or (A * pre_add_sub_out))----
assign mult_out = a1_out * b1_out;

// M Register and Mux
DFF #(.WIDTH(36), .RSTTYPE(RSTTYPE)) m_reg (
    .clk(CLK), .rst(RSTM), .CE(CEM), .D(mult_out), .Q(m_reg_out)
);
MUX #(.WIDTH(36), .INPUTS(2)) m_mux (
    .in0(mult_out),   // Direct input
    .in1(m_reg_out),  // Registered input
    .in2(36'b0), .in3(36'b0),  // Unused
    .sel(MREG[0]), .out(m_out)
);
assign M = m_out;

// -----Concatenated Buses D[11:0], A[17:0], B[17:0]------
assign concatenated_buses = {d_out[11:0], a1_out, b1_out};

// --------------------X Mux---------------------
MUX #(.WIDTH(48), .INPUTS(4)) x_mux (
    .in0(48'b0),
    .in1({{12{1'b0}}, m_out}), // Extended with zeros
    .in2(P), // P feedback
    .in3(concatenated_buses),
    .sel(opmode_out[1:0]), .out(x_mux_out)
);

// --------------------Z Mux---------------------
MUX #(.WIDTH(48), .INPUTS(4)) z_mux (
    .in0(48'b0),
    .in1(PCIN),
    .in2(P), // P feedback
    .in3(c_out),
    .sel(opmode_out[3:2]), .out(z_mux_out)
);

// -----------------Carry Input------------------
// Carry input mux (CARRYIN or OPMODE5)
MUX #(.WIDTH(1), .INPUTS(2)) carryin_mux (
    .in0(CARRYIN),
    .in1(opmode_out[5]),
    .in2(1'b0), .in3(1'b0),  // Unused
    .sel(CARRYINSEL == "OPMODE5"), .out(carryin_mux_out)
);
```

```
    // Carry Input Register and Mux (CYI)
    DFF #(.WIDTH(1), .RSTTYPE(RSTTYPE)) carryin_reg (
        .clk(CLK), .rst(RSTCARRYIN), .CE(CECARRYIN), .D(carryin_mux_out),
.Q(carryin_reg_out)
    );
    MUX #(.WIDTH(1), .INPUTS(2)) carryin_reg_mux (
        .in0(carryin_mux_out),   // Direct input
        .in1(carryin_reg_out), // Registered input
        .in2(1'b0), .in3(1'b0),  // Unused
        .sel(CARRYINREG[0]), .out(cyi_out)
    );

    // ------------Post-Adder/Subtracter-------------
    assign {carryout_wire, post_add_sub_out} = opmode_out[7] ?
            (z_mux_out - (x_mux_out + cyi_out)) :
            (z_mux_out + x_mux_out + cyi_out);

    // --------------P Output Register---------------
    // P Register and Mux
    DFF #(.WIDTH(48), .RSTTYPE(RSTTYPE)) p_reg (
        .clk(CLK), .rst(RSTP), .CE(CEP), .D(post_add_sub_out), .Q(p_reg_out)
    );
    MUX #(.WIDTH(48), .INPUTS(2)) p_mux (
        .in0(post_add_sub_out), // Direct input
        .in1(p_reg_out),        // Registered input
        .in2(48'b0), .in3(48'b0),  // Unused
        .sel(PREG[0]), .out(P)
    );
    assign PCOUT = P;

    // ------------Carry Output Register-------------
    // Carry Output Register and Mux (CYO)
    DFF #(.WIDTH(1), .RSTTYPE(RSTTYPE)) carryout_reg (
        .clk(CLK), .rst(RSTCARRYIN), .CE(CECARRYIN),
        .D(carryout_wire), .Q(carryout_reg_out)
    );
    MUX #(.WIDTH(1), .INPUTS(2)) carryout_mux (
        .in0(carryout_wire), // Direct input
        .in1(carryout_reg_out),  // Registered input
        .in2(1'b0), .in3(1'b0),  // Unused
        .sel(CARRYOUTREG[0]), .out(CARRYOUT)
    );
    assign CARRYOUTF = CARRYOUT;

endmodule
```

## MUX.v

```
module MUX(in0, in1, in2, in3, sel, out);
    parameter WIDTH = 1;
    parameter INPUTS = 2;
    input [WIDTH-1:0] in0;
    input [WIDTH-1:0] in1;
    input [WIDTH-1:0] in2;
    input [WIDTH-1:0] in3;
    input [$clog2(INPUTS)-1:0] sel;
    output reg [WIDTH-1:0] out;
    always @(*) begin
        case (sel)
            0 : out = in0;
            1 : out = in1;
            2 : out = in2;
            3 : out = in3;
        endcase
    end
endmodule
```

## DFF.v

```
module DFF(clk, Q, D, rst, CE);
    parameter WIDTH = 1;
    parameter RSTTYPE = "SYNC";
    input clk, rst, CE;
    input [WIDTH-1:0] D;
    output reg [WIDTH-1:0] Q;
    generate
        if (RSTTYPE == "ASYNC") begin
            always @(posedge clk or posedge rst) begin
                if (rst)
                    Q <= {WIDTH{1'b0}};
                else if (CE)
                    Q <= D;
            end
        end
        else begin // If -> RSTTYPE = "SYNC"
            always @(posedge clk) begin
                if (rst)
                    Q <= {WIDTH{1'b0}};
                else if (CE)
                    Q <= D;
            end
        end
    endgenerate
endmodule
```

# TESTBENCH CODE

```verilog
module DSP48A1_tb();
    // Data Input Ports
    reg [17:0] A, B, D;
    reg [47:0] C;
    reg CARRYIN;
    // Data Output Ports
    wire [35:0] M;
    wire [47:0] P;
    wire CARRYOUT, CARRYOUTF;
    // Control Ports
    reg CLK;
    reg [7:0] OPMODE;
    // Clock Enable Ports
    reg CEA, CEB, CEC, CED, CEM, CEP;
    reg CECARRYIN, CEOPMODE;
    // Reset Ports (Active High)
    reg RSTA, RSTB, RSTC, RSTD, RSTM, RSTP;
    reg RSTCARRYIN, RSTOPMODE;
    // Cascade Ports
    reg [17:0] BCIN;
    wire [17:0] BCOUT;
    reg [47:0] PCIN;
    wire [47:0] PCOUT;
    // previous P and CARRYOUT for comparison
    reg [47:0] prev_P;
    reg prev_CARRYOUT;

    // Clock generation
    initial begin
        CLK = 0;
        forever
            #1 CLK = ~CLK;
    end
    // DUT instantiation with default parameters
    DSP48A1 #(
        .A0REG(0), .A1REG(1), .B0REG(0), .B1REG(1),
        .CREG(1), .DREG(1), .MREG(1), .PREG(1),
        .CARRYINREG(1), .CARRYOUTREG(1), .OPMODEREG(1),
        .CARRYINSEL("OPMODE5"), .B_INPUT("DIRECT"), .RSTTYPE("SYNC")
    ) dut (
            A, B, C, D, CARRYIN,
            M, P, CARRYOUT, CARRYOUTF,
            CLK, OPMODE,
            CEA, CEB, CEC, CECARRYIN, CED, CEM, CEOPMODE, CEP,
            RSTA, RSTB, RSTC, RSTCARRYIN, RSTD, RSTM, RSTOPMODE, RSTP,
            BCIN, BCOUT, PCIN, PCOUT
    );
```

```
// Test stimulus
initial begin
    // Initialize inputs
    A = 0; B = 0; C = 0; D = 0; CARRYIN = 0;
    OPMODE = 0; BCIN = 0; PCIN = 0; prev_P = 0; prev_CARRYOUT = 0;
    //====================================================================
    // Verify Reset Operation
    $display("Verify Reset Operation");
    RSTA = 1; RSTB = 1; RSTC = 1; RSTD = 1; RSTM = 1; RSTP = 1;
    RSTCARRYIN = 1; RSTOPMODE = 1;

    A = $random; B = $random; C = $random; D = $random;
    CARRYIN = $random; OPMODE = $random; BCIN = $random; PCIN = $random;
    CEA = $random; CEB = $random; CEC = $random; CED = $random;
    CEM = $random; CEP = $random; CECARRYIN = $random; CEOPMODE =$random;

    @(negedge CLK);

    if (M == 0 && P == 0 && CARRYOUT == 0 && CARRYOUTF == 0 &&
        BCOUT == 0 && PCOUT == 0) begin
        $display("Reset test - All outputs are zero");
    end
    else begin
        $display("Error: Reset test - Outputs not zero:\n",
               "M=%h, P=%h, CARRYOUT=%b, CARRYOUTF=%b, BCOUT=%h, PCOUT=%h",
                  M, P, CARRYOUT, CARRYOUTF, BCOUT, PCOUT);
        $stop;
    end

    RSTA = 0; RSTB = 0; RSTC = 0; RSTD = 0; RSTM = 0; RSTP = 0;
    RSTCARRYIN = 0; RSTOPMODE = 0;
    CEA = 1; CEB = 1; CEC = 1; CED = 1; CEM = 1; CEP = 1;
    CECARRYIN = 1; CEOPMODE = 1;
    //====================================================================
    // Verify DSP Path 1
    $display("Verify DSP Path 1");
    OPMODE = 8'b11011101;
    A = 20; B = 10; C = 350; D = 25;
    BCIN = $random; PCIN = $random; CARRYIN = $random;

    repeat(4) @(negedge CLK);

    if (BCOUT == 18'hf && M == 36'h12c && P == 48'h32 && PCOUT == 48'h32
    && CARRYOUT == 0 && CARRYOUTF == 0) begin
        $display("DSP Path 1 test passed");
    end
    else begin
        $display("Error: DSP Path 1 test failed");
        $stop;
    end
```

```
//===================================================================
// Verify DSP Path 2
$display("Verify DSP Path 2");
OPMODE = 8'b00010000;
A = 20; B = 10; C = 350; D = 25;
BCIN = $random; PCIN = $random; CARRYIN = $random;

repeat(3) @(negedge CLK);

if (BCOUT == 18'h23 && M == 36'h2bc && P == 48'h0 && PCOUT == 48'h0
&& CARRYOUT == 0 && CARRYOUTF == 0) begin
    $display("DSP Path 2 test passed");
end
else begin
    $display("Error: DSP Path 2 test failed");
    $stop;
end
//===================================================================
// Verify DSP Path 3
$display("Verify DSP Path 3");
prev_P = P; prev_CARRYOUT = CARRYOUT;

OPMODE = 8'b00001010;
A = 20; B = 10; C = 350; D = 25;
BCIN = $random; PCIN = $random; CARRYIN = $random;

repeat(3) @(negedge CLK);

if (BCOUT == 18'ha && M == 36'hc8 && P == prev_P &&
    CARRYOUT == prev_CARRYOUT) begin
    $display("DSP Path 3 test passed");
end
else begin
    $display("Error: DSP Path 3 test failed");
    $stop;
End
```

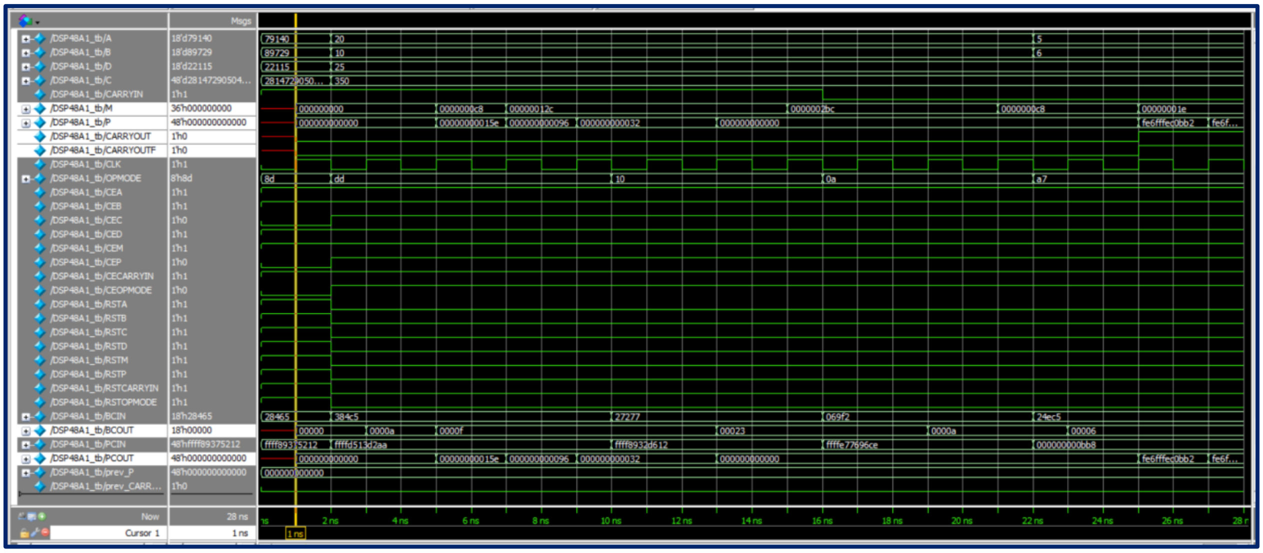
```verilog
        //===================================================================
        // Verify DSP Path 4
        $display("Verify DSP Path 4");
        OPMODE = 8'b10100111;
        A = 5; B = 6; C = 350; D = 25; PCIN = 3000;
        BCIN = $random; CARRYIN = $random;

        repeat(3) @(negedge CLK);

        if (BCOUT == 18'h6 && M == 36'h1e && P == 48'hfe6fffec0bb1 &&
            PCOUT == 48'hfe6fffec0bb1 &&
            CARRYOUT == 1 && CARRYOUTF == 1) begin
            $display("DSP Path 4 test passed");
        end
        else begin
            $display("Error: DSP Path 4 test failed");
            $stop;
        end

        $stop;
        end
endmodule
```

## DO FILE

```
vlib work

vlog DFF.v

vlog MUX.v

vlog DSP48A1.v

vlog DSP48A1_tb.v

vsim -voptargs=+acc work.DSP48A1_tb

add wave *

run -all

#quit -sim
```

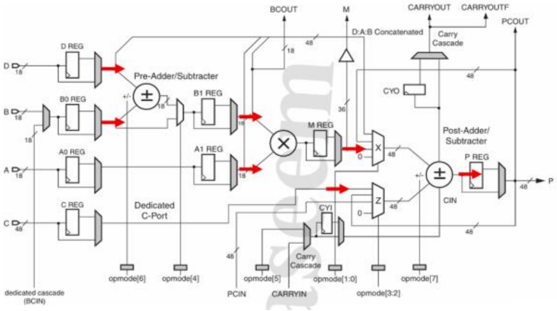
# QUESTASIM SNIPPETS

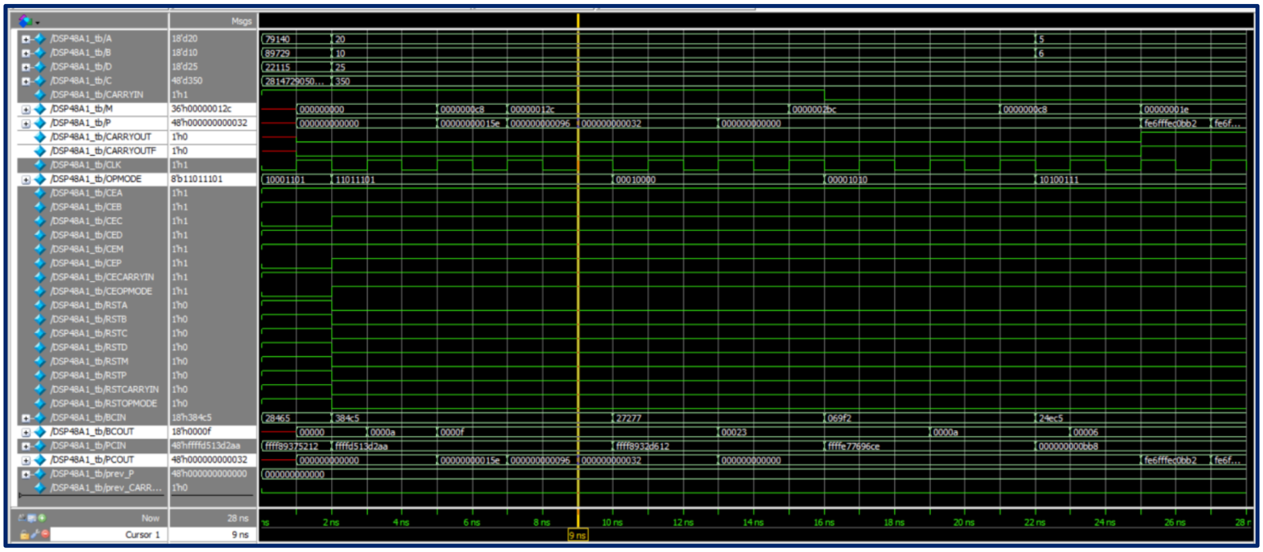
## Verify Reset Operation



| | Msgs |
|---|---|
| /DSP48A1_tb/A | 18'd79140 |
| /DSP48A1_tb/B | 18'd89729 |
| /DSP48A1_tb/D | 18'd22115 |
| /DSP48A1_tb/C | 48'd28147290504... |
| /DSP48A1_tb/CARRYIN | 1'h1 |
| /DSP48A1_tb/M | 36'h000000000 |
| /DSP48A1_tb/P | 48'h000000000000 |
| /DSP48A1_tb/CARRYOUT | 1'h0 |
| /DSP48A1_tb/CARRYOUTF | 1'h0 |
| /DSP48A1_tb/CLK | 1'h1 |
| /DSP48A1_tb/OPMODE | 8'h8d |
| /DSP48A1_tb/CEA | 1'h1 |
| /DSP48A1_tb/CEB | 1'h1 |
| /DSP48A1_tb/CEC | 1'h0 |
| /DSP48A1_tb/CED | 1'h1 |
| /DSP48A1_tb/CEM | 1'h1 |
| /DSP48A1_tb/CEP | 1'h0 |
| /DSP48A1_tb/CECARRYIN | 1'h1 |
| /DSP48A1_tb/CEOPMODE | 1'h0 |
| /DSP48A1_tb/RSTA | 1'h1 |
| /DSP48A1_tb/RSTB | 1'h1 |
| /DSP48A1_tb/RSTC | 1'h1 |
| /DSP48A1_tb/RSTD | 1'h1 |
| /DSP48A1_tb/RSTM | 1'h1 |
| /DSP48A1_tb/RSTP | 1'h1 |
| /DSP48A1_tb/RSTCARRYIN | 1'h1 |
| /DSP48A1_tb/RSTOPMODE | 1'h1 |
| /DSP48A1_tb/BCIN | 18'h28465 |
| /DSP48A1_tb/BCOUT | 18'h00000 |
| /DSP48A1_tb/PCIN | 48'hffff89375212 |
| /DSP48A1_tb/PCOUT | 48'h000000000000 |
| /DSP48A1_tb/prev_P | 48'h000000000000 |
| /DSP48A1_tb/prev_CARR... | 1'h0 |
| Now | 28 ns |
| Cursor 1 | 1 ns |

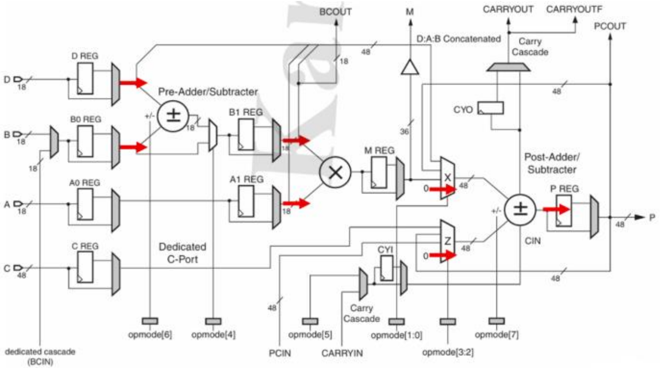
## Verify DSP Path 1

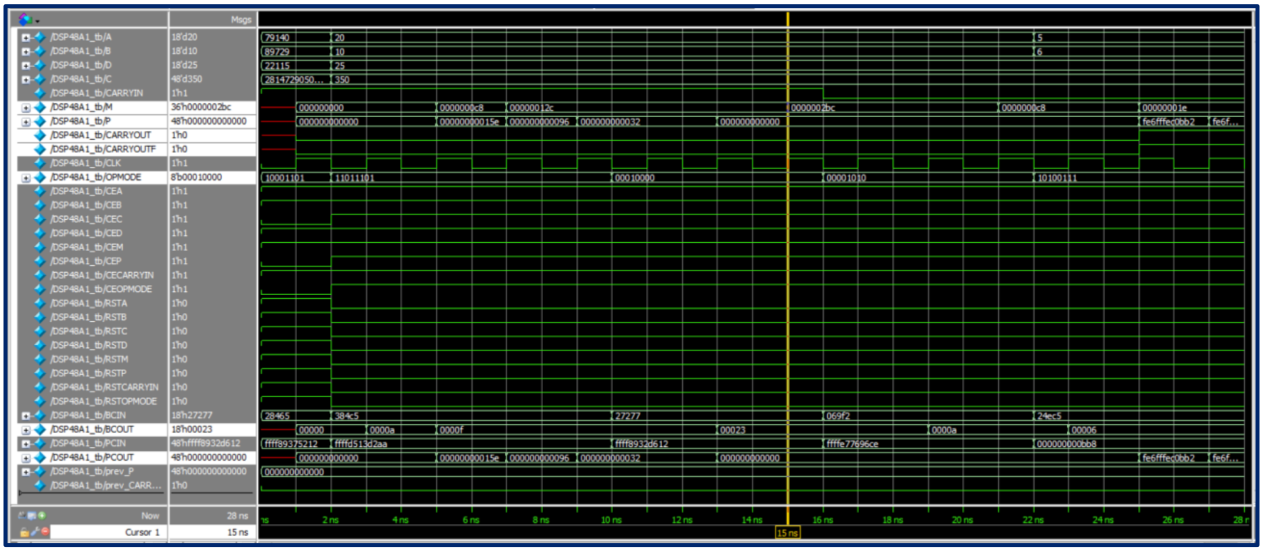




| | Msgs |
|---|---|
| /DSP48A1_tb/A | 18'd20 |
| /DSP48A1_tb/B | 18'd10 |
| /DSP48A1_tb/D | 18'd25 |
| /DSP48A1_tb/C | 48'd350 |
| /DSP48A1_tb/CARRYIN | 1'h1 |
| /DSP48A1_tb/M | 36'h00000012c |
| /DSP48A1_tb/P | 48'h000000000032 |
| /DSP48A1_tb/CARRYOUT | 1'h0 |
| /DSP48A1_tb/CARRYOUTF | 1'h0 |
| /DSP48A1_tb/CLK | 1'h1 |
| /DSP48A1_tb/OPMODE | 8'b11011101 |
| /DSP48A1_tb/CEA | 1'h1 |
| /DSP48A1_tb/CEB | 1'h1 |
| /DSP48A1_tb/CEC | 1'h1 |
| /DSP48A1_tb/CED | 1'h1 |
| /DSP48A1_tb/CEM | 1'h1 |
| /DSP48A1_tb/CEP | 1'h1 |
| /DSP48A1_tb/CECARRYIN | 1'h1 |
| /DSP48A1_tb/CEOPMODE | 1'h1 |
| /DSP48A1_tb/RSTA | 1'h0 |
| /DSP48A1_tb/RSTB | 1'h0 |
| /DSP48A1_tb/RSTC | 1'h0 |
| /DSP48A1_tb/RSTD | 1'h0 |
| /DSP48A1_tb/RSTM | 1'h0 |
| /DSP48A1_tb/RSTP | 1'h0 |
| /DSP48A1_tb/RSTCARRYIN | 1'h0 |
| /DSP48A1_tb/RSTOPMODE | 1'h0 |
| /DSP48A1_tb/BCIN | 18'h384c5 |
| /DSP48A1_tb/BCOUT | 18'h0000f |
| /DSP48A1_tb/PCIN | 48'hffffd513d2aa |
| /DSP48A1_tb/PCOUT | 48'h000000000032 |
| /DSP48A1_tb/prev_P | 48'h000000000000 |
| /DSP48A1_tb/prev_CARR... | 1'h0 |
| Now | 28 ns |
| Cursor 1 | 9 ns |

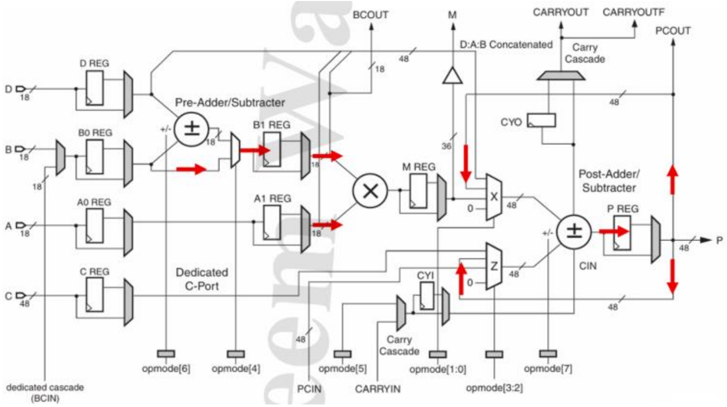
## Verify DSP Path 2

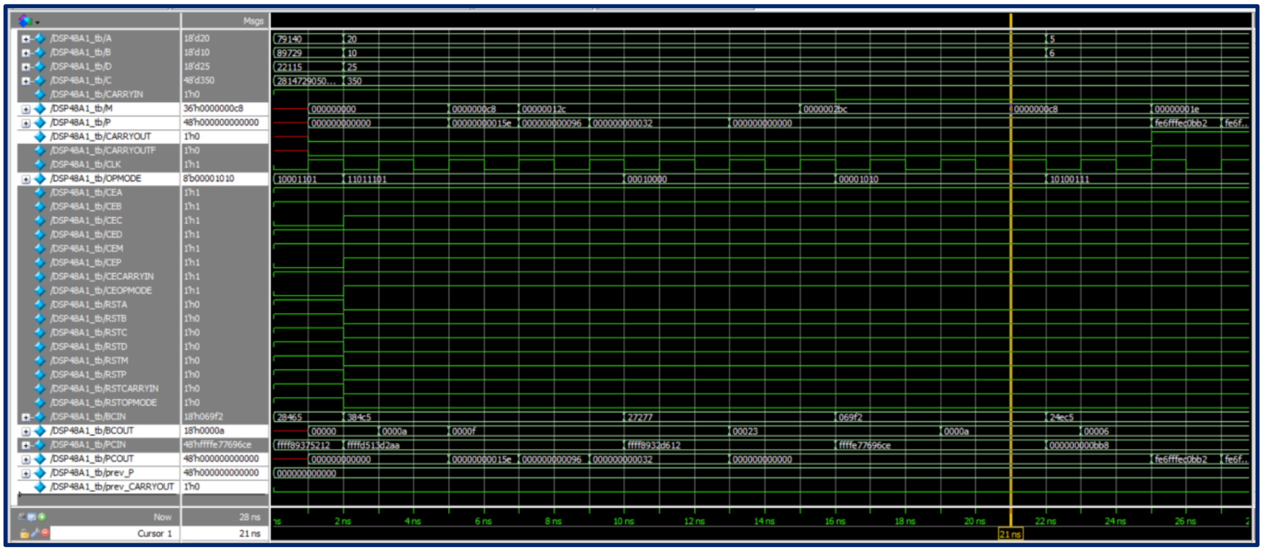




| | Msgs |
|---|---|
| /DSP48A1_tb/A | 18'd20 |
| /DSP48A1_tb/B | 18'd10 |
| /DSP48A1_tb/D | 18'd25 |
| /DSP48A1_tb/C | 48'd350 |
| /DSP48A1_tb/CARRYIN | 1'h1 |
| /DSP48A1_tb/M | 36'h0000002bc |
| /DSP48A1_tb/P | 48'h000000000000 |
| /DSP48A1_tb/CARRYOUT | 1'h0 |
| /DSP48A1_tb/CARRYOUTF | 1'h0 |
| /DSP48A1_tb/CLK | 1'h1 |
| /DSP48A1_tb/OPMODE | 8'b00010000 |
| /DSP48A1_tb/CEA | 1'h1 |
| /DSP48A1_tb/CEB | 1'h1 |
| /DSP48A1_tb/CEC | 1'h1 |
| /DSP48A1_tb/CED | 1'h1 |
| /DSP48A1_tb/CEM | 1'h1 |
| /DSP48A1_tb/CEP | 1'h1 |
| /DSP48A1_tb/CECARRYIN | 1'h1 |
| /DSP48A1_tb/CEOPMODE | 1'h1 |
| /DSP48A1_tb/RSTA | 1'h0 |
| /DSP48A1_tb/RSTB | 1'h0 |
| /DSP48A1_tb/RSTC | 1'h0 |
| /DSP48A1_tb/RSTD | 1'h0 |
| /DSP48A1_tb/RSTM | 1'h0 |
| /DSP48A1_tb/RSTP | 1'h0 |
| /DSP48A1_tb/RSTCARRYIN | 1'h0 |
| /DSP48A1_tb/RSTOPMODE | 1'h0 |
| /DSP48A1_tb/BCIN | 18'h27277 |
| /DSP48A1_tb/BCOUT | 18'h00023 |
| /DSP48A1_tb/PCIN | 48'hffff8932d612 |
| /DSP48A1_tb/PCOUT | 48'h000000000000 |
| /DSP48A1_tb/prev_P | 48'h000000000000 |
| /DSP48A1_tb/prev_CARR... | 1'h0 |
| Now | 28 ns |
| Cursor 1 | 15 ns |

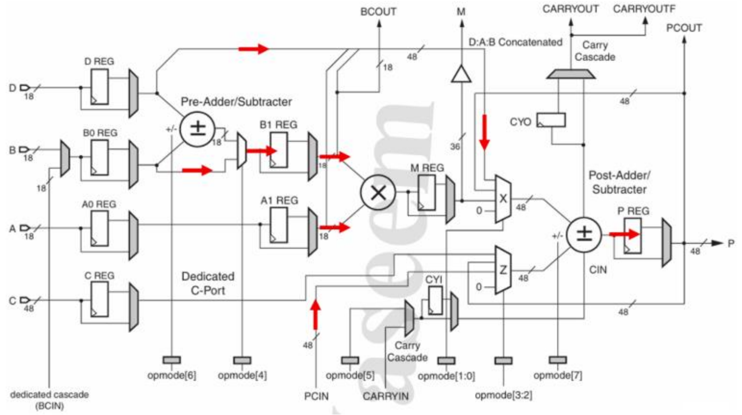
## Verify DSP Path 3

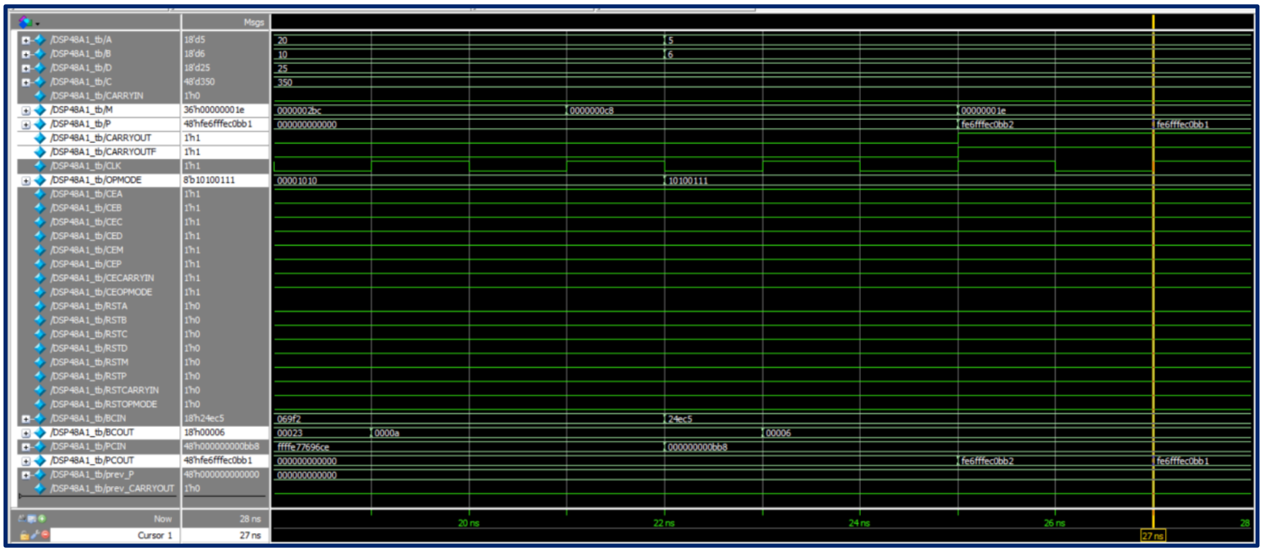



79140 20 5
89729 10 6
22115 25
2814729050... 350
000000000 0000000c8 00000012c 0000002bc 0000000c8 00000001e
000000000000 00000000015e 000000000096 000000000032 000000000000 fe6fffec0bb2 fe6f...
10001101 11011101 00010000 00001010 10100111
28465 384c5 27277 069f2 24ec5
00000 0000a 0000f 00023 0000a 00006
ffff89375212 ffffd513d2aa ffff8932d612 ffffe77696ce 000000000bb8
000000000000 00000000015e 000000000096 000000000032 000000000000 fe6fffec0bb2 fe6f...
000000000000
ns 2 ns 4 ns 6 ns 8 ns 10 ns 12 ns 14 ns 16 ns 18 ns 20 ns 22 ns 24 ns 26 ns
21 ns

| | Msgs |
|---|---|
| /DSP48A1_tb/A | 18'd20 |
| /DSP48A1_tb/B | 18'd10 |
| /DSP48A1_tb/D | 18'd25 |
| /DSP48A1_tb/C | 48'd350 |
| /DSP48A1_tb/CARRYIN | 1'h0 |
| /DSP48A1_tb/M | 36'h0000000c8 |
| /DSP48A1_tb/P | 48'h000000000000 |
| /DSP48A1_tb/CARRYOUT | 1'h0 |
| /DSP48A1_tb/CARRYOUTF | 1'h0 |
| /DSP48A1_tb/CLK | 1'h1 |
| /DSP48A1_tb/OPMODE | 8'b00001010 |
| /DSP48A1_tb/CEA | 1'h1 |
| /DSP48A1_tb/CEB | 1'h1 |
| /DSP48A1_tb/CEC | 1'h1 |
| /DSP48A1_tb/CED | 1'h1 |
| /DSP48A1_tb/CEM | 1'h1 |
| /DSP48A1_tb/CEP | 1'h1 |
| /DSP48A1_tb/CECARRYIN | 1'h1 |
| /DSP48A1_tb/CEOPMODE | 1'h1 |
| /DSP48A1_tb/RSTA | 1'h0 |
| /DSP48A1_tb/RSTB | 1'h0 |
| /DSP48A1_tb/RSTC | 1'h0 |
| /DSP48A1_tb/RSTD | 1'h0 |
| /DSP48A1_tb/RSTM | 1'h0 |
| /DSP48A1_tb/RSTP | 1'h0 |
| /DSP48A1_tb/RSTCARRYIN | 1'h0 |
| /DSP48A1_tb/RSTOPMODE | 1'h0 |
| /DSP48A1_tb/BCIN | 18'h069f2 |
| /DSP48A1_tb/BCOUT | 18'h0000a |
| /DSP48A1_tb/PCIN | 48'hffffe77696ce |
| /DSP48A1_tb/PCOUT | 48'h000000000000 |
| /DSP48A1_tb/prev_P | 48'h000000000000 |
| /DSP48A1_tb/prev_CARRYOUT | 1'h0 |
| Now | 28 ns |
| Cursor 1 | 21 ns |

## Verify DSP Path 4





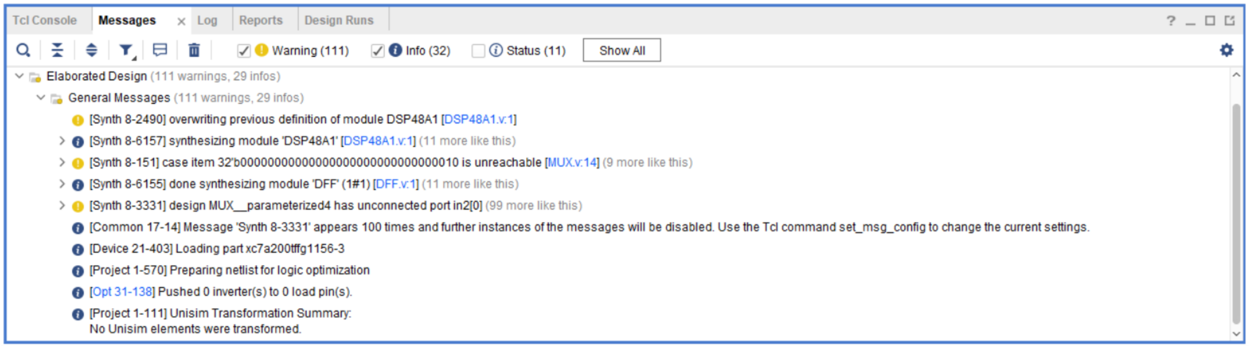
| | Msgs |
|---|---|
| /DSP48A1_tb/A | 18'd5 |
| /DSP48A1_tb/B | 18'd6 |
| /DSP48A1_tb/D | 18'd25 |
| /DSP48A1_tb/C | 48'd350 |
| /DSP48A1_tb/CARRYIN | 1'h0 |
| /DSP48A1_tb/M | 36'h00000001e |
| /DSP48A1_tb/P | 48'hfe6fffec0bb1 |
| /DSP48A1_tb/CARRYOUT | 1'h1 |
| /DSP48A1_tb/CARRYOUTF | 1'h1 |
| /DSP48A1_tb/CLK | 1'h1 |
| /DSP48A1_tb/OPMODE | 8'b10100111 |
| /DSP48A1_tb/CEA | 1'h1 |
| /DSP48A1_tb/CEB | 1'h1 |
| /DSP48A1_tb/CEC | 1'h1 |
| /DSP48A1_tb/CED | 1'h1 |
| /DSP48A1_tb/CEM | 1'h1 |
| /DSP48A1_tb/CEP | 1'h1 |
| /DSP48A1_tb/CECARRYIN | 1'h1 |
| /DSP48A1_tb/CEOPMODE | 1'h1 |
| /DSP48A1_tb/RSTA | 1'h0 |
| /DSP48A1_tb/RSTB | 1'h0 |
| /DSP48A1_tb/RSTC | 1'h0 |
| /DSP48A1_tb/RSTD | 1'h0 |
| /DSP48A1_tb/RSTM | 1'h0 |
| /DSP48A1_tb/RSTP | 1'h0 |
| /DSP48A1_tb/RSTCARRYIN | 1'h0 |
| /DSP48A1_tb/RSTOPMODE | 1'h0 |
| /DSP48A1_tb/BCIN | 18'h24ec5 |
| /DSP48A1_tb/BCOUT | 18'h00006 |
| /DSP48A1_tb/PCIN | 48'h000000000bb8 |
| /DSP48A1_tb/PCOUT | 48'hfe6fffec0bb1 |
| /DSP48A1_tb/prev_P | 48'h000000000000 |
| /DSP48A1_tb/prev_CARRYOUT | 1'h0 |
| Now | 28 ns |
| Cursor 1 | 27 ns |

# CONSTRAINT FILE

```
# DSP48A1 Constraint File for xc7a200tffg1156-3 FPGA
# Clock constraint: 100 MHz clock on pin W5

## Clock signal
set_property -dict { PACKAGE_PIN W5   IOSTANDARD LVCMOS33 } [get_ports CLK]
create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports CLK]

## Configuration options, can be used for all designs
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property CFGBVS VCCO [current_design]

## SPI configuration mode options for QSPI boot, can be used for all designs
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.CONFIGRATE 33 [current_design]
set_property CONFIG_MODE SPIx4 [current_design]
```

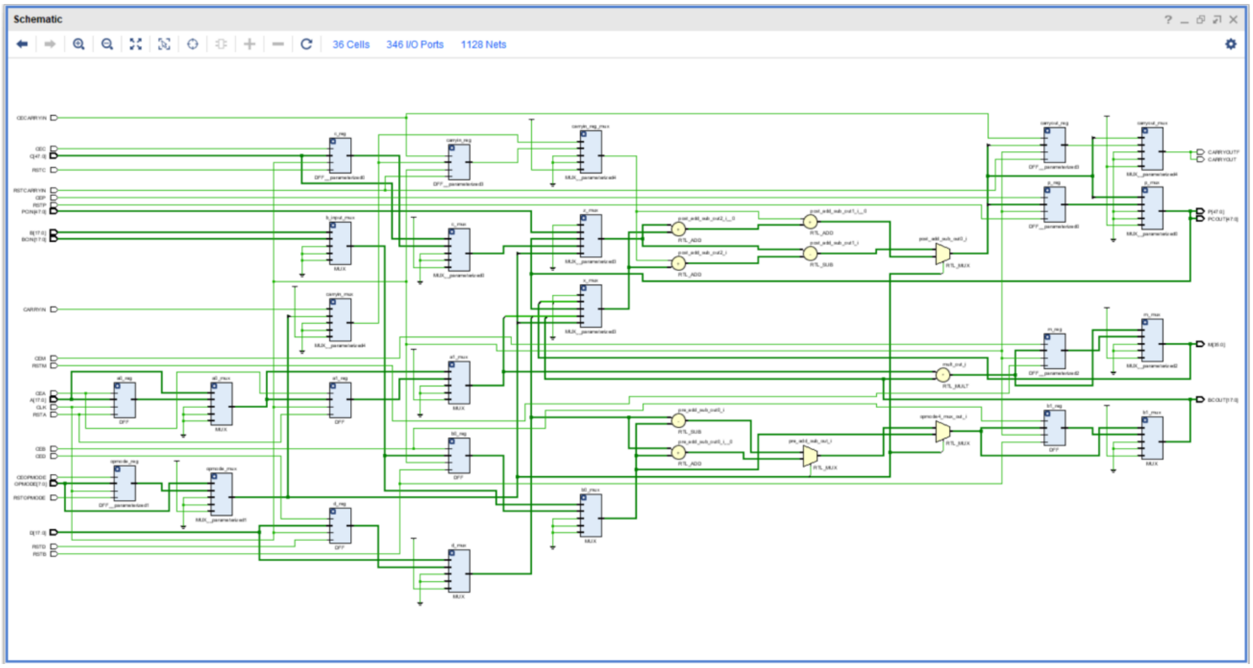
# ELABORATION

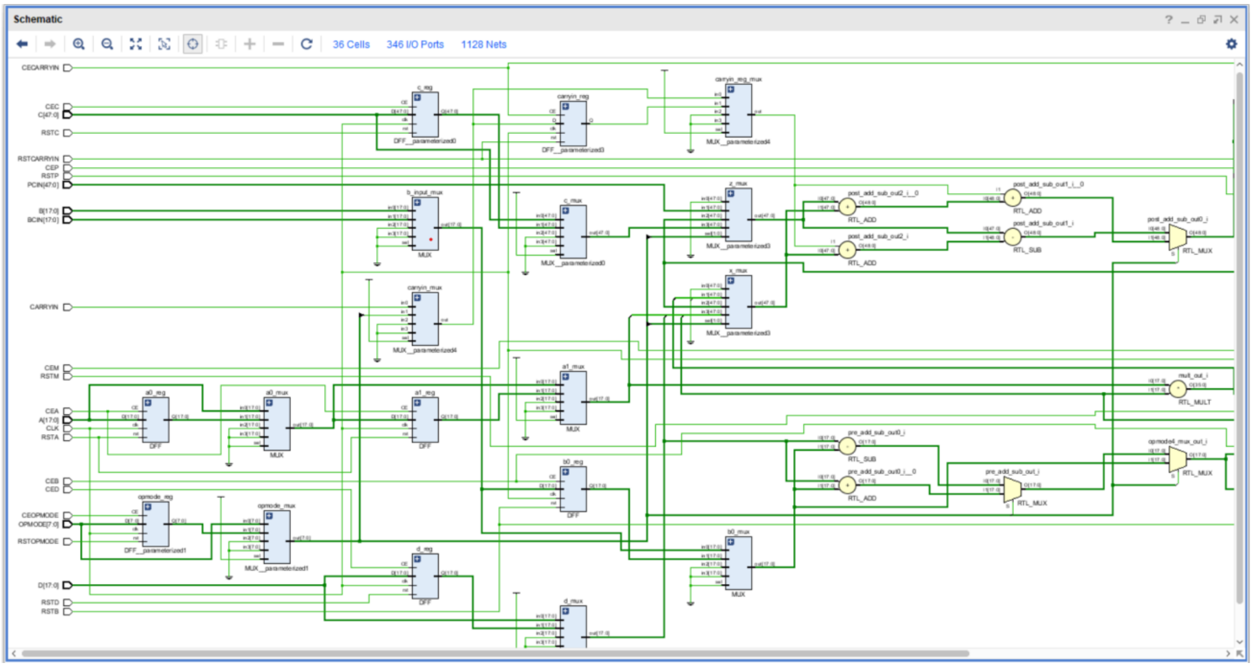
## Messages

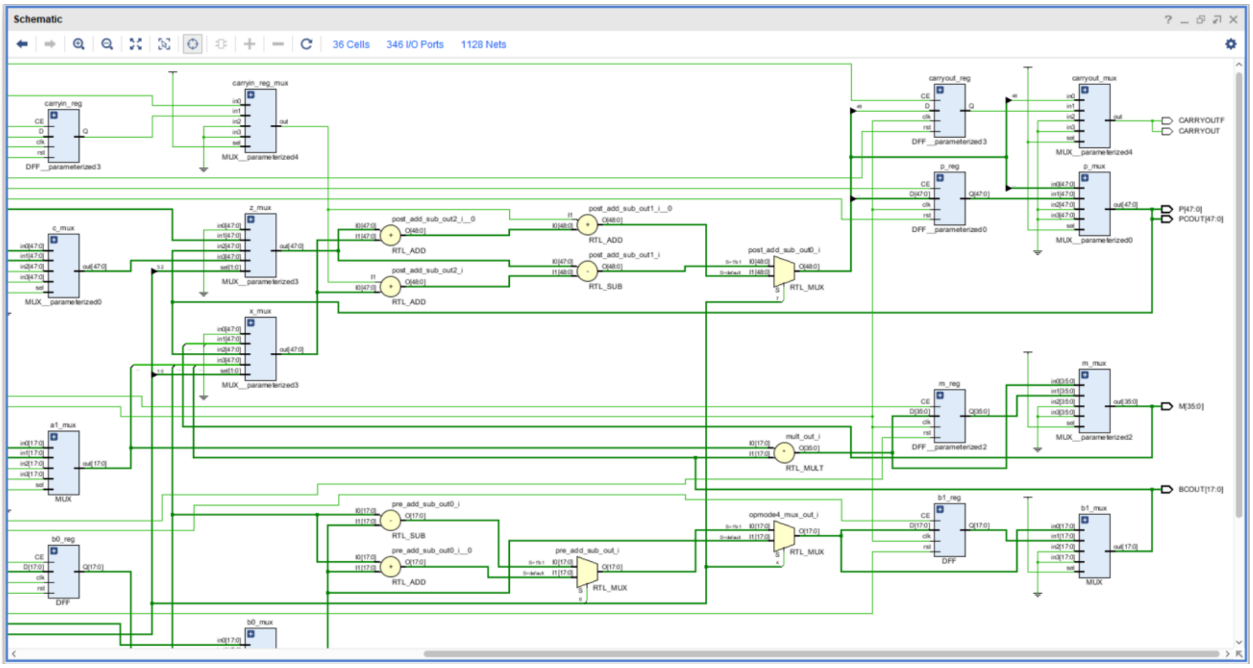


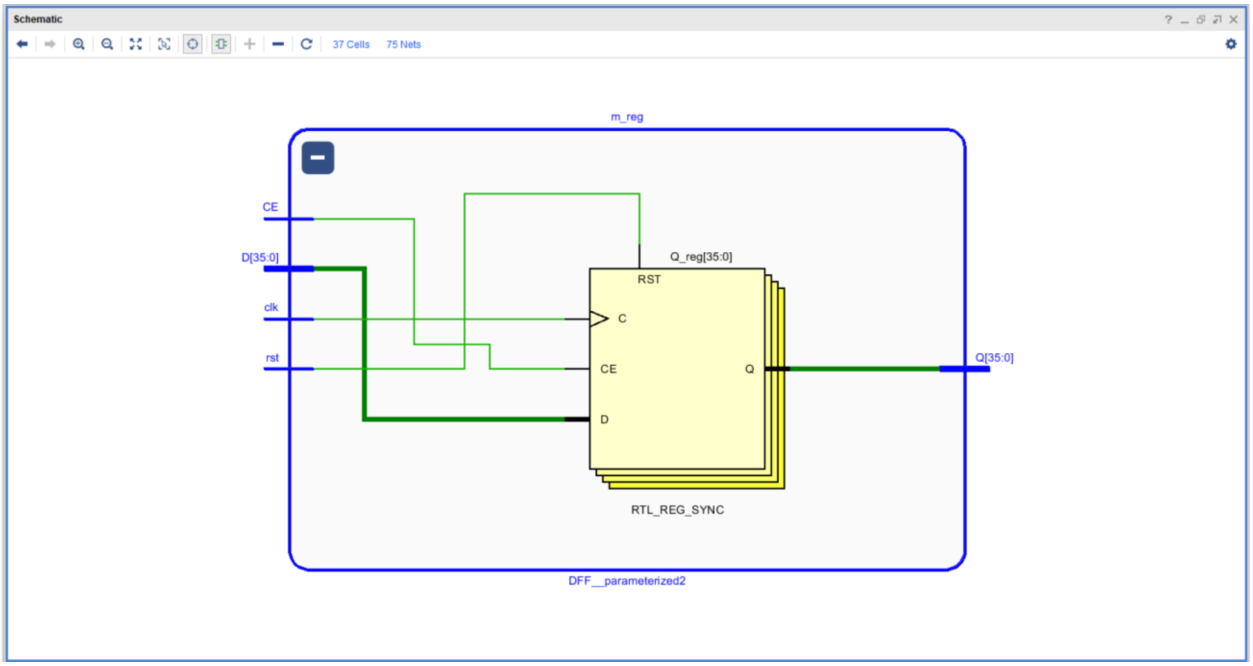
```
Elaborated Design (111 warnings, 29 infos)
  General Messages (111 warnings, 29 infos)
    [Synth 8-2490] overwriting previous definition of module DSP48A1 [DSP48A1.v:1]
  > [Synth 8-6157] synthesizing module 'DSP48A1' [DSP48A1.v:1] (11 more like this)
  > [Synth 8-151] case item 32'b00000000000000000000000000000010 is unreachable [MUX.v:14] (9 more like this)
  > [Synth 8-6155] done synthesizing module 'DFF' (1#1) [DFF.v:1] (11 more like this)
  > [Synth 8-3331] design MUX__parameterized4 has unconnected port in2[0] (99 more like this)
    [Common 17-14] Message 'Synth 8-3331' appears 100 times and further instances of the messages will be disabled. Use the Tcl command set_msg_config to change the current settings.
    [Device 21-403] Loading part xc7a200tffg1156-3
    [Project 1-570] Preparing netlist for logic optimization
    [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
    [Project 1-111] Unisim Transformation Summary:
    No Unisim elements were transformed.
```

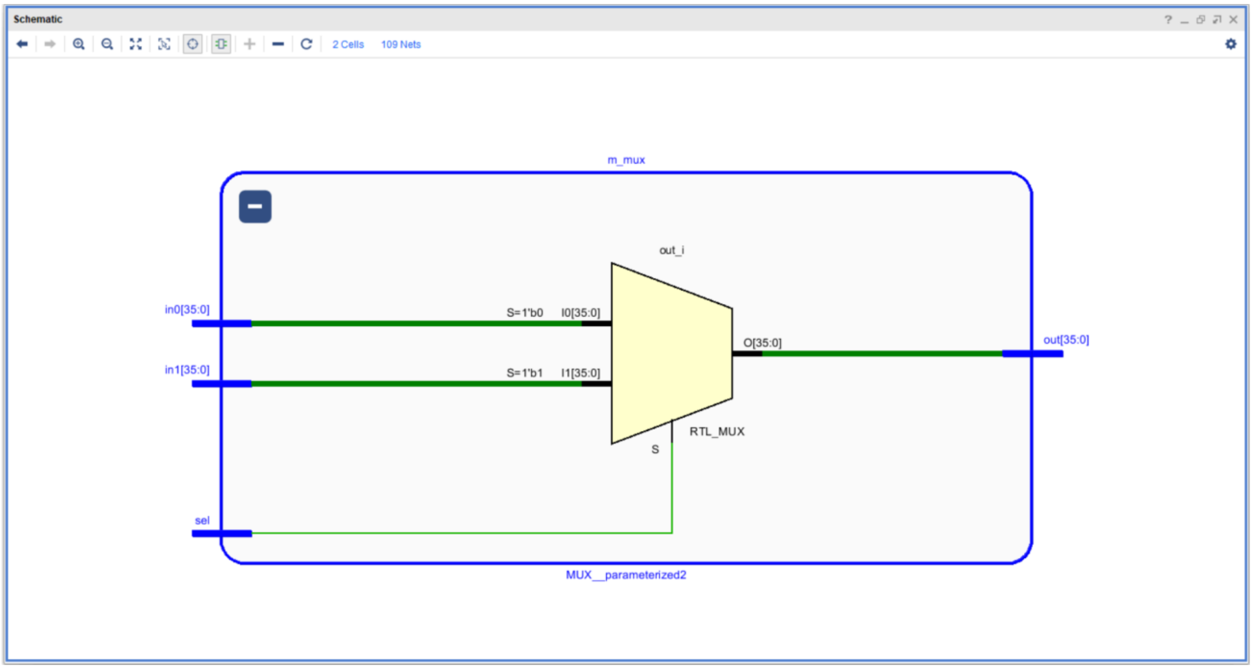
## Schematic


Schematic
36 Cells
346 I/O Ports
1128 Nets
CECARRYIN
CEC
C[47:0]
RSTC
RSTCARRYIN
CEP
RSTP
PCIN[47:0]
B[17:0]
BCIN[17:0]
CARRYIN
CEM
RSTM
CEA
A[17:0]
CLK
RSTA
CEB
CED
CEOPMODE
OPMODE[7:0]
RSTOPMODE
D[17:0]
RSTD
RSTB
c_reg
carryin_reg
carryin_reg_mux
carryout_reg
carryout_mux
p_reg
p_mux
m_reg
m_mux
b1_reg
b1_mux
CARRYOUTF
CARRYOUT
P[47:0]
PCOUT[47:0]
M[35:0]
BCOUT[17:0]
RTL_ADD
RTL_SUB
RTL_MUX
RTL_MULT


Schematic
36 Cells
346 I/O Ports
1128 Nets
CECARRYIN
CEC
C[47:0]
RSTC
RSTCARRYIN
CEP
RSTP
PCIN[47:0]
B[17:0]
BCIN[17:0]
CARRYIN
CEM
RSTM
CEA
A[17:0]
CLK
RSTA
CEB
CED
CEOPMODE
OPMODE[7:0]
RSTOPMODE
D[17:0]
RSTD
RSTB
c_reg
DFF__parameterized0
carryin_reg
DFF__parameterized3
carryin_reg_mux
MUX__parameterized4
b_input_mux
MUX
c_mux
MUX__parameterized0
z_mux
MUX__parameterized3
carryin_mux
MUX__parameterized4
x_mux
MUX__parameterized3
a0_reg
DFF
a0_mux
MUX
a1_reg
DFF
a1_mux
MUX
b0_reg
DFF
opmode_reg
DFF__parameterized1
opmode_mux
MUX__parameterized1
d_reg
DFF
b0_mux
MUX
d_mux
post_add_sub_out2_i__0
RTL_ADD
post_add_sub_out2_i
RTL_ADD
post_add_sub_out1_i__0
RTL_ADD
post_add_sub_out1_i
RTL_SUB
post_add_sub_out0_i
RTL_MUX
mult_out_i
RTL_MULT
pre_add_sub_out0_i
RTL_SUB
pre_add_sub_out0_i__0
RTL_ADD
pre_add_sub_out_i
RTL_MUX
opmode4_mux_out_i
RTL_MUX

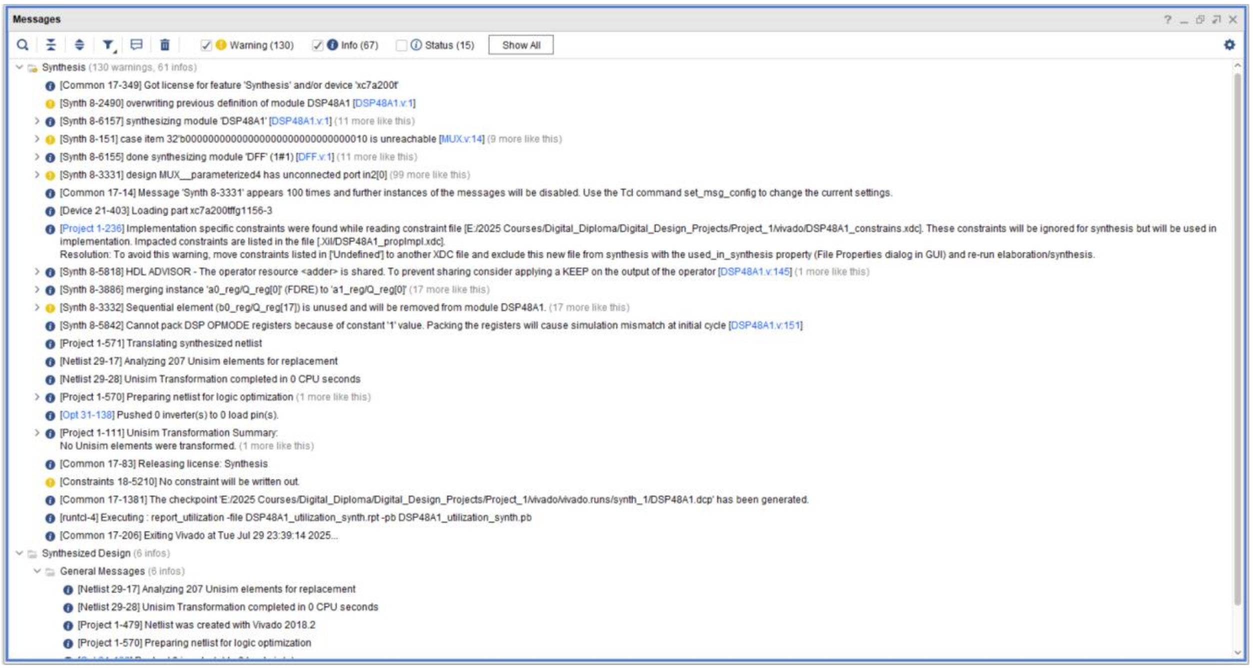

Schematic
36 Cells
346 I/O Ports
1128 Nets
carryin_reg
DFF__parameterized3
carryin_reg_mux
MUX__parameterized4
c_mux
MUX__parameterized0
z_mux
MUX__parameterized3
x_mux
MUX__parameterized3
a1_mux
MUX
b0_reg
DFF
b0_mux
post_add_sub_out2_i__0
RTL_ADD
post_add_sub_out2_i
RTL_ADD
post_add_sub_out1_i__0
RTL_ADD
post_add_sub_out1_i
RTL_SUB
post_add_sub_out0_i
RTL_MUX
pre_add_sub_out0_i
RTL_SUB
pre_add_sub_out0_i__0
RTL_ADD
pre_add_sub_out_i
RTL_MUX
mult_out_i
RTL_MULT
opmode4_mux_out_i
RTL_MUX
carryout_reg
DFF__parameterized3
carryout_mux
MUX__parameterized4
CARRYOUTF
CARRYOUT
p_reg
DFF__parameterized0
p_mux
MUX__parameterized0
P[47:0]
PCOUT[47:0]
m_reg
DFF__parameterized2
m_mux
MUX__parameterized2
M[35:0]
b1_reg
DFF
b1_mux
MUX
BCOUT[17:0]


Schematic
37 Cells
75 Nets
m_reg
CE
D[35:0]
clk
rst
Q_reg[35:0]
RST
C
CE
Q
D
RTL_REG_SYNC
Q[35:0]
DFF__parameterized2



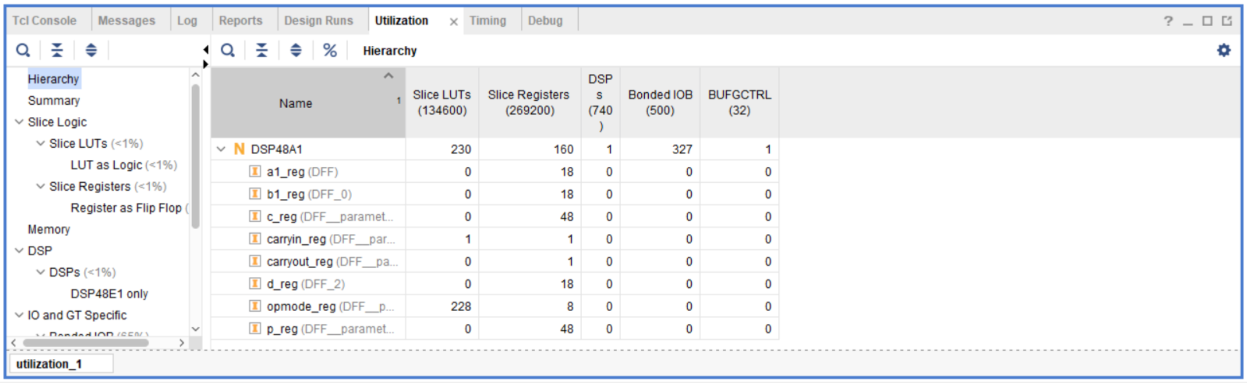
# SYNTHESIS

## Messages



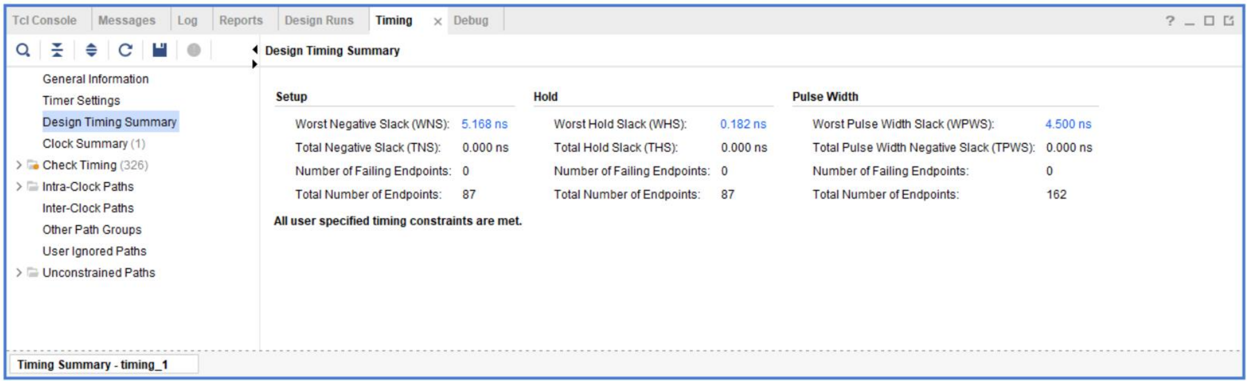
```
Synthesis (130 warnings, 61 infos)
    [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a200t'
    [Synth 8-2490] overwriting previous definition of module DSP48A1 [DSP48A1.v:1]
  > [Synth 8-6157] synthesizing module 'DSP48A1' [DSP48A1.v:1] (11 more like this)
  > [Synth 8-151] case item 32'b00000000000000000000000000000010 is unreachable [MUX.v:14] (9 more like this)
  > [Synth 8-6155] done synthesizing module 'DFF' (1#1) [DFF.v:1] (11 more like this)
  > [Synth 8-3331] design MUX__parameterized4 has unconnected port in2[0] (99 more like this)
    [Common 17-14] Message 'Synth 8-3331' appears 100 times and further instances of the messages will be disabled. Use the Tcl command set_msg_config to change the current settings.
    [Device 21-403] Loading part xc7a200tffg1156-3
    [Project 1-236] Implementation specific constraints were found while reading constraint file [E:/2025 Courses/Digital_Diploma/Digital_Design_Projects/Project_1/vivado/DSP48A1_constrains.xdc]. These constraints will be ignored for synthesis but will be used in
    implementation. Impacted constraints are listed in the file [.Xil/DSP48A1_propImpl.xdc].
    Resolution: To avoid this warning, move constraints listed in ['Undefined'] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
  > [Synth 8-5818] HDL ADVISOR - The operator resource <adder> is shared. To prevent sharing consider applying a KEEP on the output of the operator [DSP48A1.v:145] (1 more like this)
  > [Synth 8-3886] merging instance 'a0_reg/Q_reg[0]' (FDRE) to 'a1_reg/Q_reg[0]' (17 more like this)
  > [Synth 8-3332] Sequential element (b0_reg/Q_reg[17]) is unused and will be removed from module DSP48A1. (17 more like this)
    [Synth 8-5842] Cannot pack DSP OPMODE registers because of constant '1' value. Packing the registers will cause simulation mismatch at initial cycle [DSP48A1.v:151]
    [Project 1-571] Translating synthesized netlist
    [Netlist 29-17] Analyzing 207 Unisim elements for replacement
    [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
  > [Project 1-570] Preparing netlist for logic optimization (1 more like this)
    [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
  > [Project 1-111] Unisim Transformation Summary:
    No Unisim elements were transformed. (1 more like this)
    [Common 17-83] Releasing license: Synthesis
    [Constraints 18-5210] No constraint will be written out.
    [Common 17-1381] The checkpoint 'E:/2025 Courses/Digital_Diploma/Digital_Design_Projects/Project_1/vivado/vivado.runs/synth_1/DSP48A1.dcp' has been generated.
    [runtcl-4] Executing : report_utilization -file DSP48A1_utilization_synth.rpt -pb DSP48A1_utilization_synth.pb
    [Common 17-206] Exiting Vivado at Tue Jul 29 23:39:14 2025...
Synthesized Design (6 infos)
  General Messages (6 infos)
      [Netlist 29-17] Analyzing 207 Unisim elements for replacement
      [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
      [Project 1-479] Netlist was created with Vivado 2018.2
      [Project 1-570] Preparing netlist for logic optimization
```

## Utilization report



| Name | Slice LUTs (134600) | Slice Registers (269200) | DSPs (740) | Bonded IOB (500) | BUFGCTRL (32) |
|---|---|---|---|---|---|
| DSP48A1 | 230 | 160 | 1 | 327 | 1 |
| a1_reg (DFF) | 0 | 18 | 0 | 0 | 0 |
| b1_reg (DFF_0) | 0 | 18 | 0 | 0 | 0 |
| c_reg (DFF__paramet... | 0 | 48 | 0 | 0 | 0 |
| carryin_reg (DFF__par... | 1 | 1 | 0 | 0 | 0 |
| carryout_reg (DFF__pa... | 0 | 1 | 0 | 0 | 0 |
| d_reg (DFF_2) | 0 | 18 | 0 | 0 | 0 |
| opmode_reg (DFF__p... | 228 | 8 | 0 | 0 | 0 |
| p_reg (DFF__paramet... | 0 | 48 | 0 | 0 | 0 |

## timing report



Design Timing Summary

**Setup**

Worst Negative Slack (WNS): 5.168 ns
Total Negative Slack (TNS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 87

**Hold**

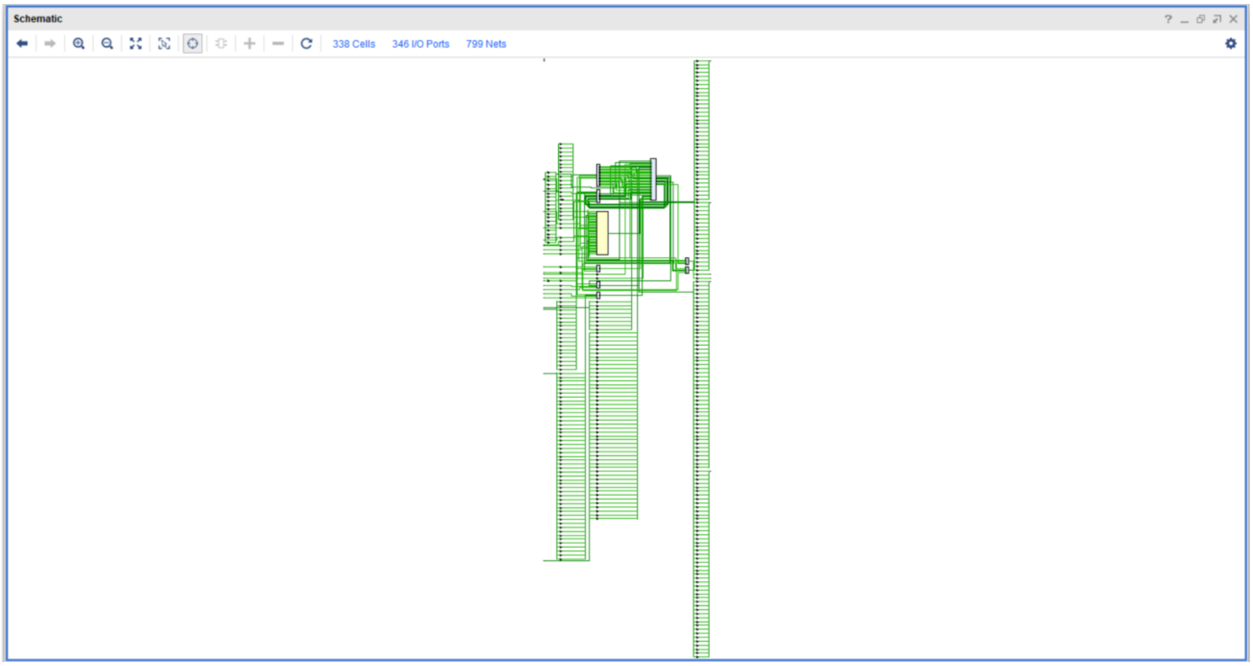
Worst Hold Slack (WHS): 0.182 ns
Total Hold Slack (THS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 87

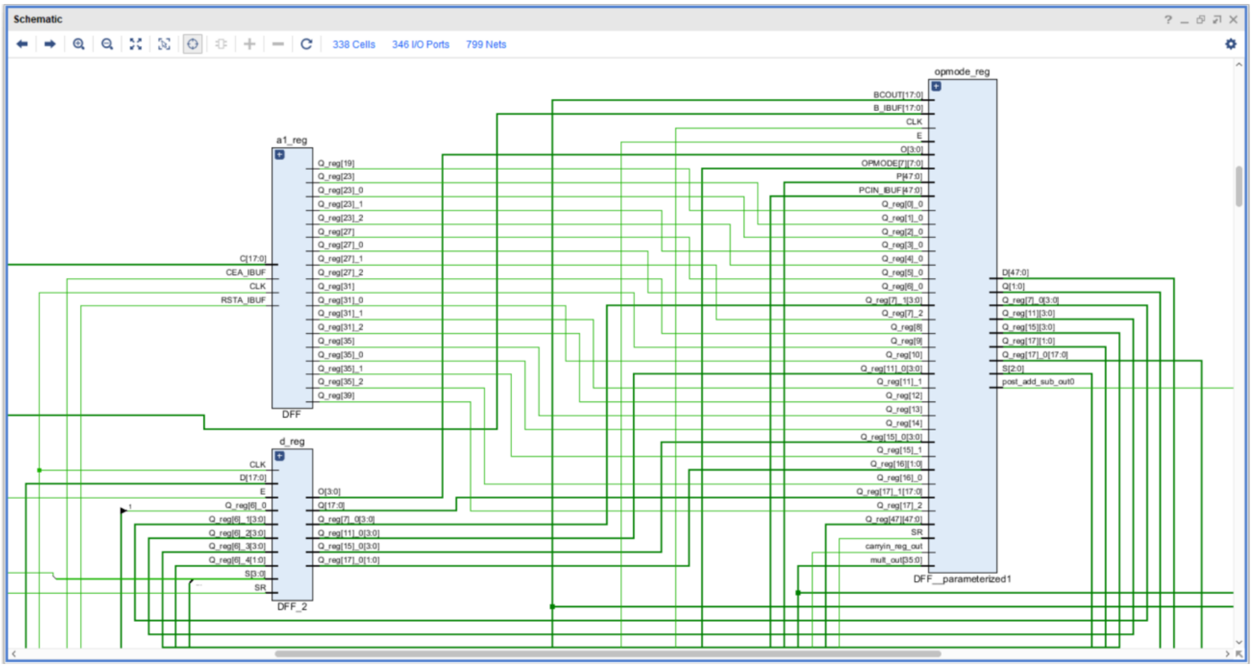
**Pulse Width**

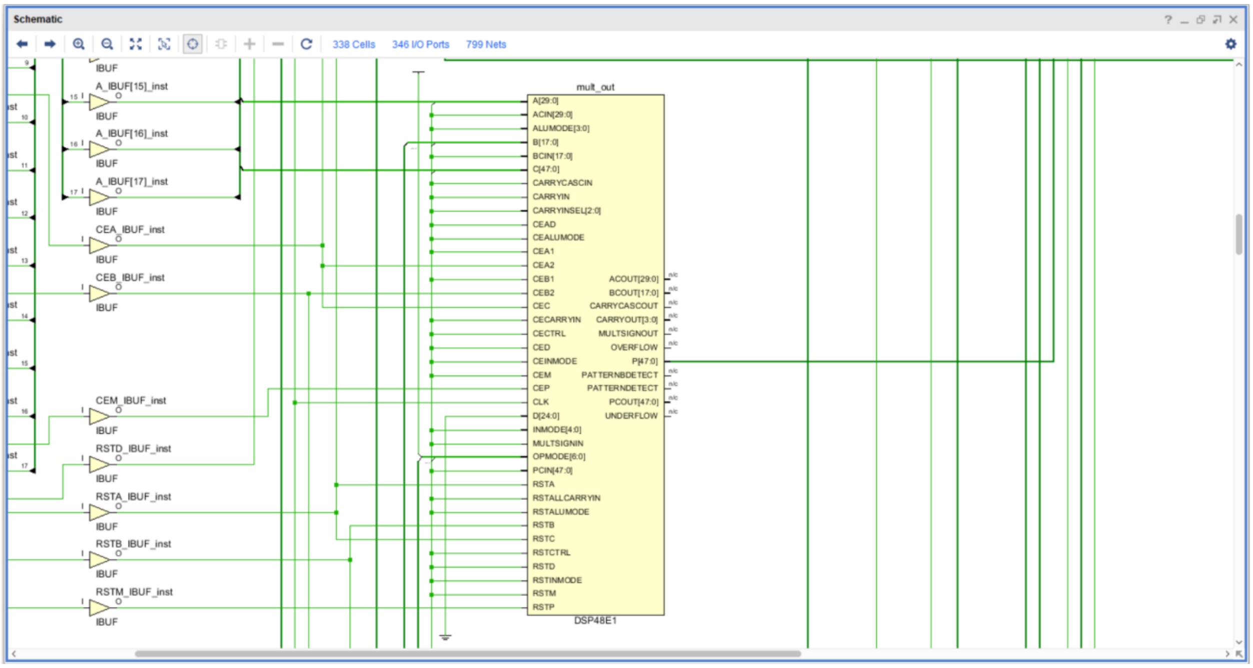
Worst Pulse Width Slack (WPWS): 4.500 ns
Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 162

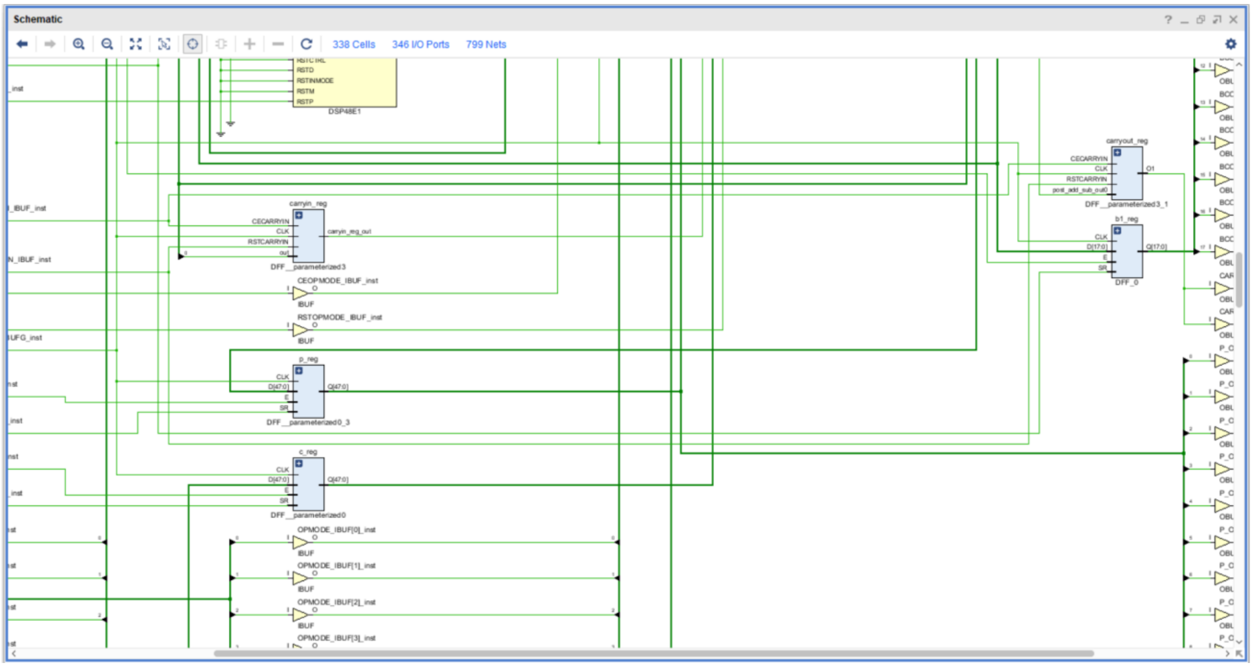
**All user specified timing constraints are met.**

## Schematic



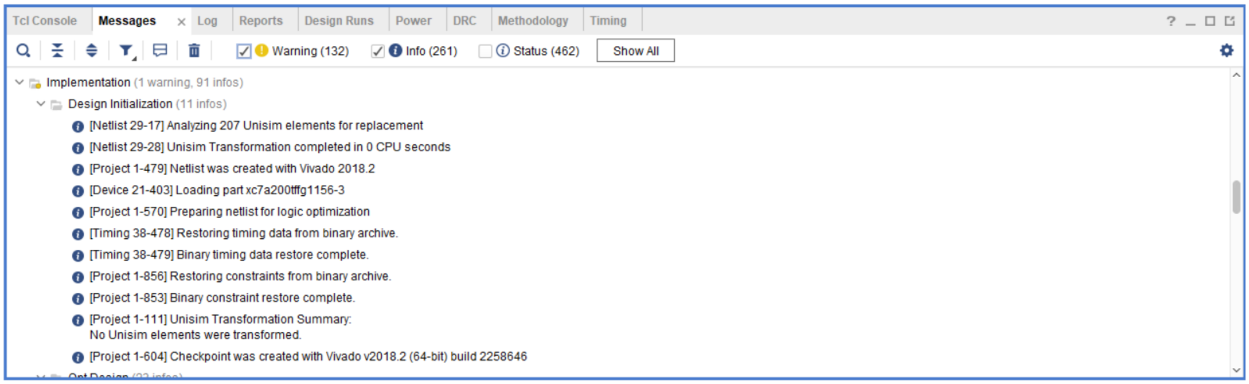

Schematic
338 Cells
346 I/O Ports
799 Nets
a1_reg
C[17:0]
CEA_IBUF
CLK
RSTA_IBUF
Q_reg[19]
Q_reg[23]
Q_reg[23]_0
Q_reg[23]_1
Q_reg[23]_2
Q_reg[27]
Q_reg[27]_0
Q_reg[27]_1
Q_reg[27]_2
Q_reg[31]
Q_reg[31]_0
Q_reg[31]_1
Q_reg[31]_2
Q_reg[35]
Q_reg[35]_0
Q_reg[35]_1
Q_reg[35]_2
Q_reg[39]
DFF
d_reg
CLK
D[17:0]
E
Q_reg[6]_0
Q_reg[6]_1[3:0]
Q_reg[6]_2[3:0]
Q_reg[6]_3[3:0]
Q_reg[6]_4[1:0]
S[3:0]
SR
O[3:0]
Q[17:0]
Q_reg[7]_0[3:0]
Q_reg[11]_0[3:0]
Q_reg[15]_0[3:0]
Q_reg[17]_0[1:0]
DFF_2
opmode_reg
BCOUT[17:0]
B_IBUF[17:0]
CLK
E
O[3:0]
OPMODE[7][7:0]
P[47:0]
PCIN_IBUF[47:0]
Q_reg[0]_0
Q_reg[1]_0
Q_reg[2]_0
Q_reg[3]_0
Q_reg[4]_0
Q_reg[5]_0
Q_reg[6]_0
Q_reg[7]_1[3:0]
Q_reg[7]_2
Q_reg[8]
Q_reg[9]
Q_reg[10]
Q_reg[11]_0[3:0]
Q_reg[11]_1
Q_reg[12]
Q_reg[13]
Q_reg[14]
Q_reg[15]_0[3:0]
Q_reg[15]_1
Q_reg[16][1:0]
Q_reg[16]_0
Q_reg[17]_1[17:0]
Q_reg[17]_2
Q_reg[47][47:0]
SR
carryin_reg_out
mult_out[35:0]
D[47:0]
Q[1:0]
Q_reg[7]_0[3:0]
Q_reg[11][3:0]
Q_reg[15][3:0]
Q_reg[17][1:0]
Q_reg[17]_0[17:0]
S[2:0]
post_add_sub_out0
DFF__parameterized1


Schematic
338 Cells
346 I/O Ports
799 Nets
IBUF
A_IBUF[15]_inst
IBUF
A_IBUF[16]_inst
IBUF
A_IBUF[17]_inst
IBUF
CEA_IBUF_inst
IBUF
CEB_IBUF_inst
IBUF
CEM_IBUF_inst
IBUF
RSTD_IBUF_inst
IBUF
RSTA_IBUF_inst
IBUF
RSTB_IBUF_inst
IBUF
RSTM_IBUF_inst
IBUF
mult_out
A[29:0]
ACIN[29:0]
ALUMODE[3:0]
B[17:0]
BCIN[17:0]
C[47:0]
CARRYCASCIN
CARRYIN
CARRYINSEL[2:0]
CEAD
CEALUMODE
CEA1
CEA2
CEB1
CEB2
CEC
CECARRYIN
CECTRL
CED
CEINMODE
CEM
CEP
CLK
D[24:0]
INMODE[4:0]
MULTSIGNIN
OPMODE[6:0]
PCIN[47:0]
RSTA
RSTALLCARRYIN
RSTALUMODE
RSTB
RSTC
RSTCTRL
RSTD
RSTINMODE
RSTM
RSTP
ACOUT[29:0]
BCOUT[17:0]
CARRYCASCOUT
CARRYOUT[3:0]
MULTSIGNOUT
OVERFLOW
P[47:0]
PATTERNBDETECT
PATTERNDETECT
PCOUT[47:0]
UNDERFLOW
DSP48E1



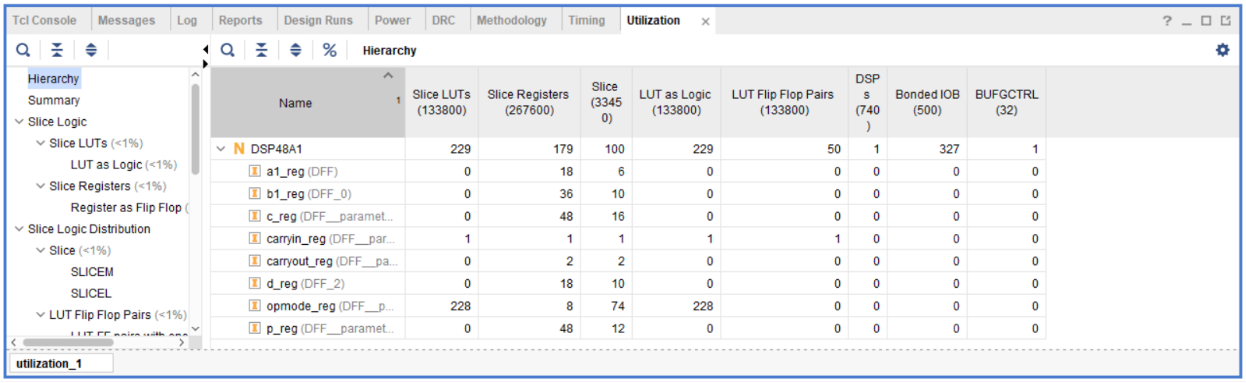
# IMPLEMENTATION

## Messages



```
Implementation (1 warning, 91 infos)
  Design Initialization (11 infos)
    [Netlist 29-17] Analyzing 207 Unisim elements for replacement
    [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
    [Project 1-479] Netlist was created with Vivado 2018.2
    [Device 21-403] Loading part xc7a200tffg1156-3
    [Project 1-570] Preparing netlist for logic optimization
    [Timing 38-478] Restoring timing data from binary archive.
    [Timing 38-479] Binary timing data restore complete.
    [Project 1-856] Restoring constraints from binary archive.
    [Project 1-853] Binary constraint restore complete.
    [Project 1-111] Unisim Transformation Summary:
    No Unisim elements were transformed.
    [Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646
  Opt Design (22 infos)
```

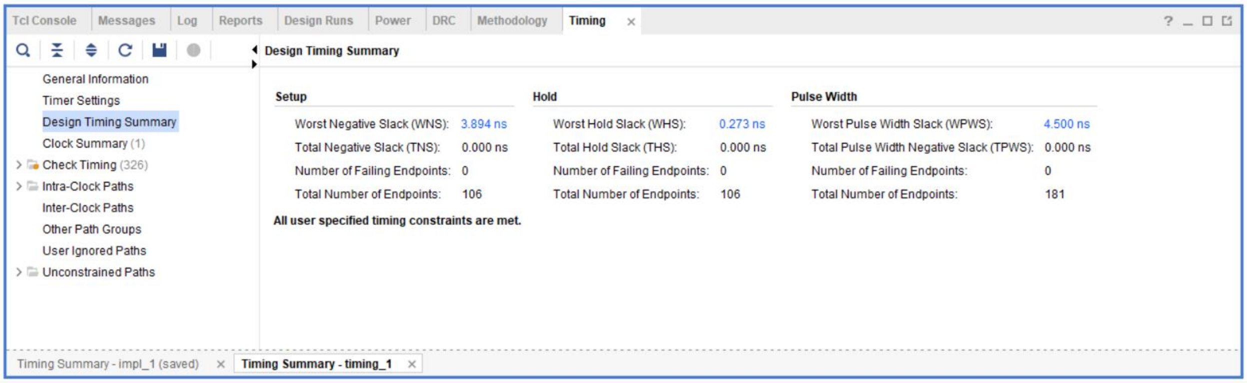
## Utilization report



Hierarchy

| Name | Slice LUTs (133800) | Slice Registers (267600) | Slice (33450) | LUT as Logic (133800) | LUT Flip Flop Pairs (133800) | DSPs (740) | Bonded IOB (500) | BUFGCTRL (32) |
|---|---|---|---|---|---|---|---|---|
| DSP48A1 | 229 | 179 | 100 | 229 | 50 | 1 | 327 | 1 |
| a1_reg (DFF) | 0 | 18 | 6 | 0 | 0 | 0 | 0 | 0 |
| b1_reg (DFF_0) | 0 | 36 | 10 | 0 | 0 | 0 | 0 | 0 |
| c_reg (DFF__paramet... | 0 | 48 | 16 | 0 | 0 | 0 | 0 | 0 |
| carryin_reg (DFF__par... | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| carryout_reg (DFF__pa... | 0 | 2 | 2 | 0 | 0 | 0 | 0 | 0 |
| d_reg (DFF_2) | 0 | 18 | 10 | 0 | 0 | 0 | 0 | 0 |
| opmode_reg (DFF__p... | 228 | 8 | 74 | 228 | 0 | 0 | 0 | 0 |
| p_reg (DFF__paramet... | 0 | 48 | 12 | 0 | 0 | 0 | 0 | 0 |

## timing report

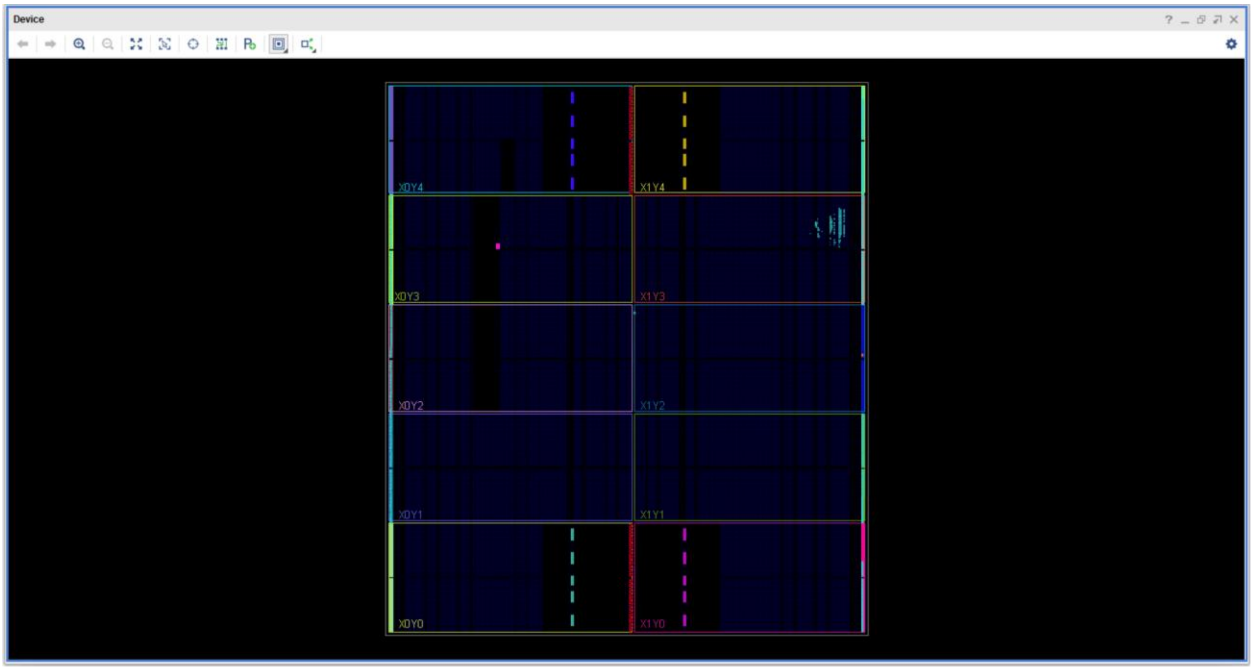


Design Timing Summary

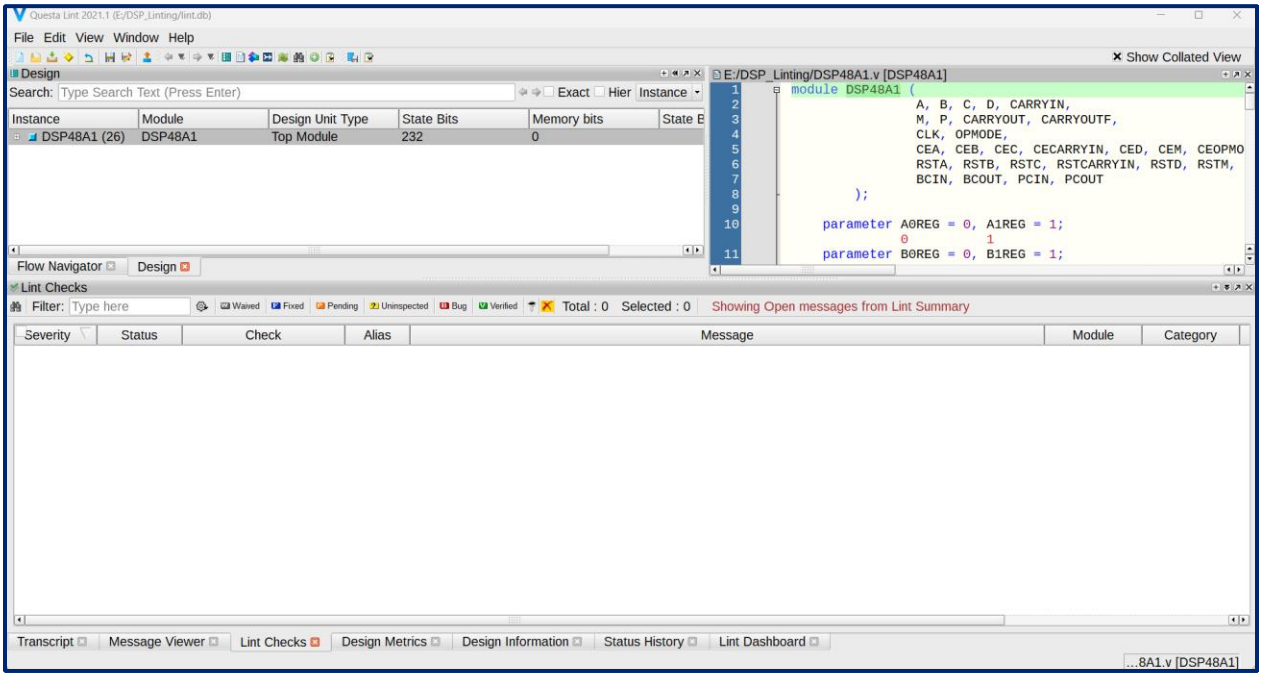
| Setup | | Hold | | Pulse Width | |
|---|---|---|---|---|---|
| Worst Negative Slack (WNS): | 3.894 ns | Worst Hold Slack (WHS): | 0.273 ns | Worst Pulse Width Slack (WPWS): | 4.500 ns |
| Total Negative Slack (TNS): | 0.000 ns | Total Hold Slack (THS): | 0.000 ns | Total Pulse Width Negative Slack (TPWS): | 0.000 ns |
| Number of Failing Endpoints: | 0 | Number of Failing Endpoints: | 0 | Number of Failing Endpoints: | 0 |
| Total Number of Endpoints: | 106 | Total Number of Endpoints: | 106 | Total Number of Endpoints: | 181 |

**All user specified timing constraints are met.**

## Device



# LINTING



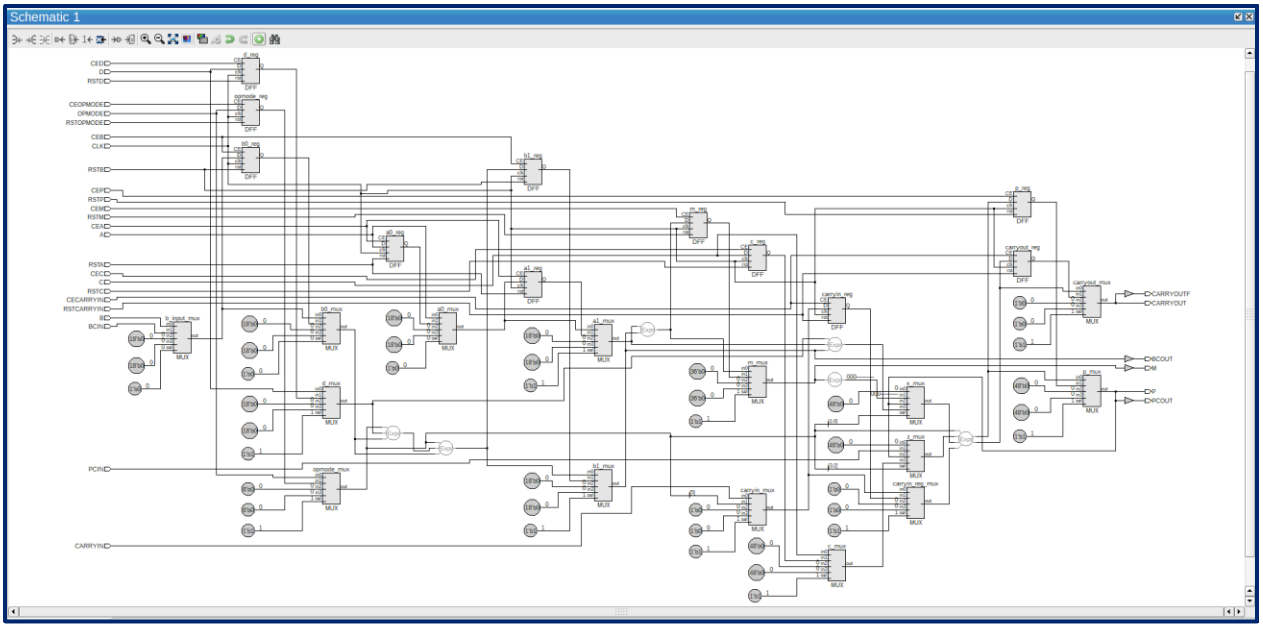
| Instance | Module | Design Unit Type | State Bits | Memory bits | State B |
|---|---|---|---|---|---|
| DSP48A1 (26) | DSP48A1 | Top Module | 232 | 0 | |

E:/DSP_Linting/DSP48A1.v [DSP48A1]

```
module DSP48A1 (
                A, B, C, D, CARRYIN,
                M, P, CARRYOUT, CARRYOUTF,
                CLK, OPMODE,
                CEA, CEB, CEC, CECARRYIN, CED, CEM, CEOPMO
                RSTA, RSTB, RSTC, RSTCARRYIN, RSTD, RSTM,
                BCIN, BCOUT, PCIN, PCOUT
        );

    parameter A0REG = 0, A1REG = 1;
              0          1
    parameter B0REG = 0, B1REG = 1;
```

Total : 0    Selected : 0    Showing Open messages from Lint Summary

| Severity | Status | Check | Alias | Message | Module | Category |
|---|---|---|---|---|---|---|


Schematic 1
CED
D
RSTD
CEOPMODE
OPMODE
RSTOPMODE
CEB
CLK
RSTB
CEP
RSTP
CEM
RSTM
CEA
A
RSTA
CEC
C
RSTC
CECARRYIN
RSTCARRYIN
B
BCIN
PCIN
CARRYIN
d_reg
opmode_reg
b0_reg
b1_reg
a0_reg
a1_reg
m_reg
c_reg
p_reg
carryout_reg
carryin_reg
DFF
b_input_mux
b0_mux
a0_mux
a1_mux
b1_mux
d_mux
opmode_mux
m_mux
x_mux
z_mux
c_mux
carryin_mux
carryin_reg_mux
carryout_mux
p_mux
MUX
CARRYOUTF
CARRYOUT
BCOUT
M
P
PCOUT