Report Generated by Test Manager

Title: **Test**
Author: **SONKO Muhammed Rahim**
Date: **12-Jun-2024 18:24:49**

Test Environment

Platform: PCWIN64
MATLAB: (R2022b)

Summary

Name	Outcome	Duration (Seconds)
Results: 2024-Jun-12 18:23:28	5 ✓	16.038
SimuPro/Subsystem/speed conditions	5 ✓	15.403
TC01_SpeedConditions	✓	2.646
TC02_ExternalWeightConditions	✓	2.652
TC03_RoadTypeConditions	✓	3.274
TC04_ACConditions	✓	2.765
TC05_AlertSystem	✓	2.029

Results: 2024-Jun-12 18:23:28

Result Type: Result Set
Parent: None
Start Time: 12-Jun-2024 18:23:31
End Time: 12-Jun-2024 18:23:47
Outcome: Total: 5, Passed: 5

Aggregated Coverage Results

Analyzed Model	Sim Mode	Complexity	Decision	Execution
SimuPro/Subsystem/speed conditions	Normal	4	67%	100%
SimuPro/Subsystem/road type condition	Normal	2	100%	100%
SimuPro/Subsystem/external weight condition	Normal	2	50%	100%
SimuPro/Subsystem/Air conditioning condition	Normal	2	100%	100%
SimuPro1/Alerts sys	Normal	0	--	100%

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SimuPro/Subsystem/speed conditions

Test Result Information

Result Type: Test Suite Result
Parent: Results: 2024-Jun-12 18:23:28
Start Time: 12-Jun-2024 18:23:31
End Time: 12-Jun-2024 18:23:46
Outcome: Total: 5, Passed: 5

Test Suite Information

Name: SimuPro/Subsystem/speed conditions

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TC01_SpeedConditions

Test Result Information

Result Type: Test Case Result
Parent: SimuPro/Subsystem/speed conditions

Start Time: 12-Jun-2024 18:23:31
End Time: 12-Jun-2024 18:23:33
Outcome: Passed

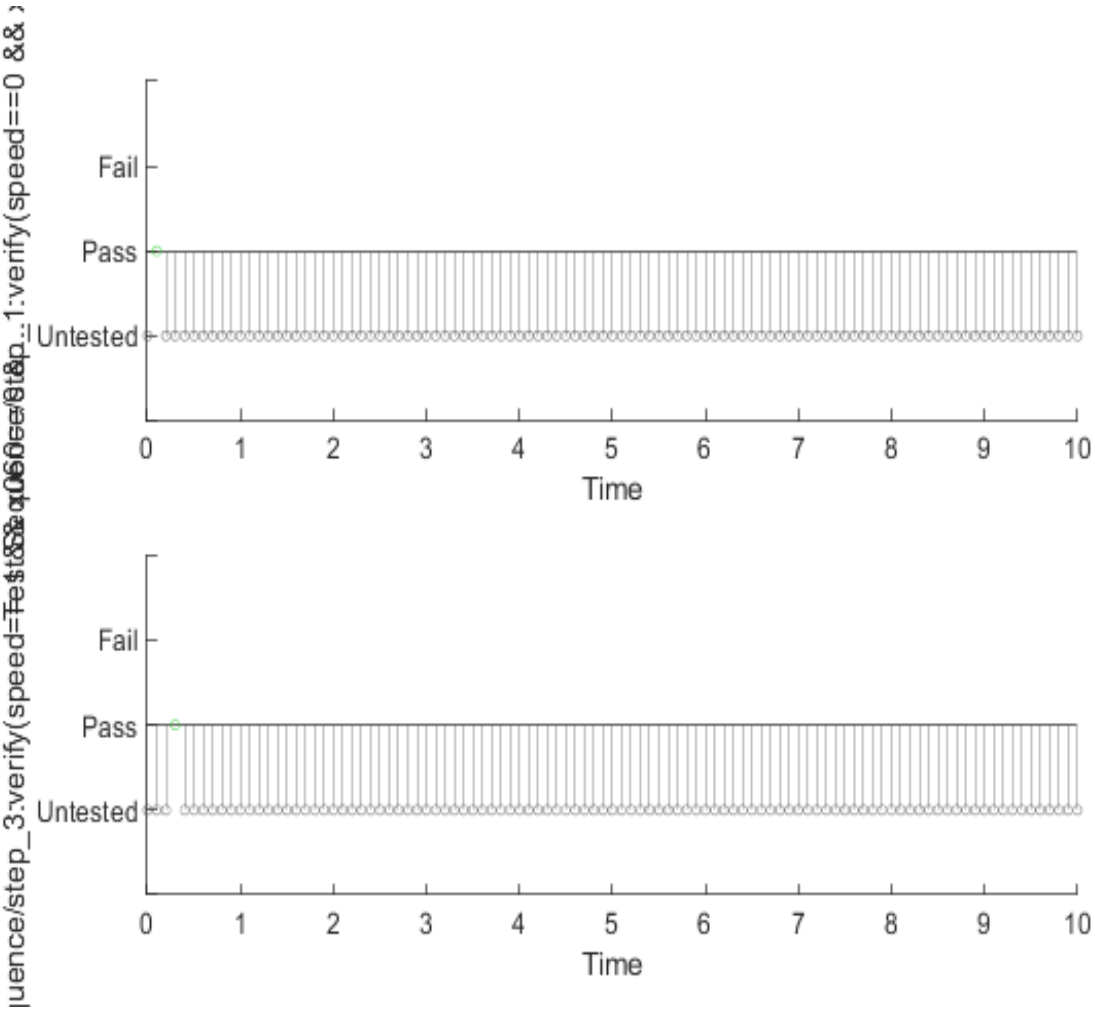
Test Case Information

Name: TC01_SpeedConditions
Type: Simulation Test

Verify Result

Name	Link to Plot
Test Sequence/step_1:verify(speed==0 && x060==0)	Link
Test Sequence/step_3:verify(speed==-1 && x060==0 && x60100==0 && x100140==0)	Link
Test Sequence/step_5:verify(speed==80 && x060==0 && x60100==2)	Link
Test Sequence/step_7:verify(speed==180 && x060==0 && x60100==0 && x100140==0)	Link

Name
Test Sequence/step_1:verify(speed==0 && x060==0)
Test Sequence/step_3:verify(speed==-1 && x060==0 && x60100==0 && x100140==0)



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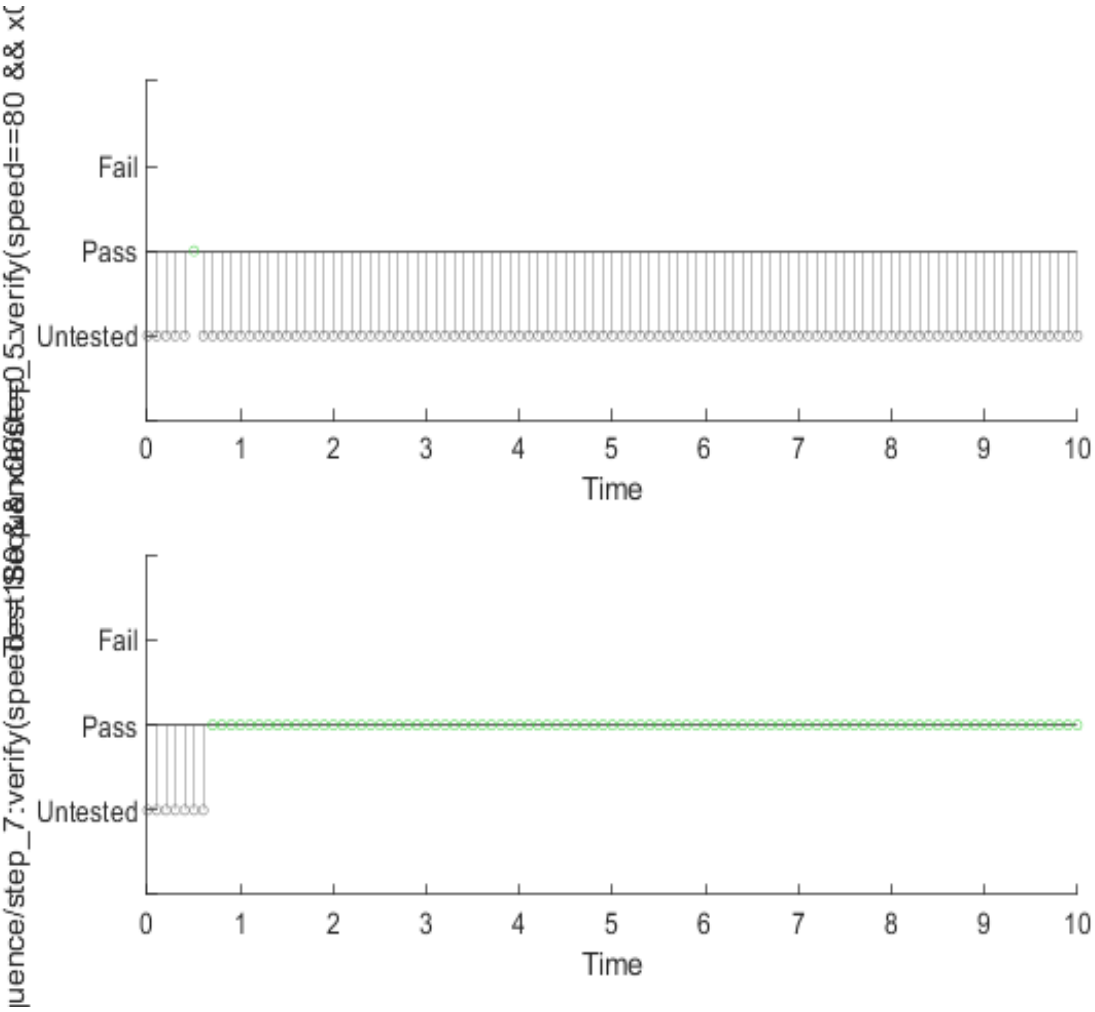
Name
Test Sequence/step_5:verify(speed==80 && x060==0 && x60100==2)
Test Sequence/step_7:verify(speed==180 && x060==0 && x60100==0 && x100140==0)



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Simulation

System Under Test Information

Model:	SimuPro
Harness:	SimuPro_Harness2
Harness Owner:	SimuPro/Subsystem/speed conditions
Release:	Current
Simulation Mode:	normal

Override SIL or PIL Mode:	0
Configuration Set:	QuickStart_50024_6_10_16_0_35086
Start Time:	0
Stop Time:	10
Checksum:	3875966644 1663385870 2200393798 729344302
Simulink Version:	10.6
Model Version:	1.1
Model Author:	muham
Date:	Wed Jun 12 17:34:22 2024
User ID:	muham
Model Path:	C:\Users\muham\Downloads\SimuPro.slx
Machine Name:	DESKTOP-OF247DK
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2024-06-12 18:23:31
Simulation Stop Time:	2024-06-12 18:23:33
Platform:	PCWIN64

Simulation Logs:
'Speed' is defined, but is never used in the Test Sequence block. Delete this object.

Using the '==' operator to compare expressions of type double in the 'verify' statement can produce unexpected results. Step 'step_1' in Test Sequence 'SimuPro_Harness2/Test Sequence': verify(speed==0 && x060==0);

Using the '==' operator to compare expressions of type double in the 'verify' statement can produce unexpected results. Step 'step_1' in Test Sequence 'SimuPro_Harness2/Test Sequence': verify(speed==0 && x060==0);

Using the '==' operator to compare expressions of type double in the 'verify' statement can produce unexpected results. Step 'step_3' in Test Sequence 'SimuPro_Harness2/Test Sequence': verify(speed==-1 && x060==0 && x60100==0 && x100140==0);

Using the '==' operator to compare expressions of type double in the 'verify' statement can produce unexpected results. Step 'step_3' in Test Sequence 'SimuPro_Harness2/Test Sequence': verify(speed==-1 && x060==0 && x60100==0 && x100140==0);

Using the '==' operator to compare expressions of type double in the 'verify' statement can produce unexpected results. Step 'step_3' in Test Sequence 'SimuPro_Harness2/Test Sequence': verify(speed==-1 && x060==0 && x60100==0 && x100140==0);

Using the '==' operator to compare expressions of type double in the 'verify' statement can produce unexpected results. Step 'step_3' in Test Sequence 'SimuPro_Harness2/Test Sequence': verify(speed==-1 && x060==0 && x60100==0 && x100140==0);

Using the '==' operator to compare expressions of type double in the 'verify' statement can produce unexpected results. Step 'step_5' in Test Sequence 'SimuPro_Harness2/Test Sequence': verify(speed==80 && x060==0 && x60100==2);

Using the '==' operator to compare expressions of type double in the 'verify' statement can produce unexpected results. Step 'step_5' in Test Sequence 'SimuPro_Harness2/Test Sequence': verify(speed==80 && x060==0 && x60100==2);

Using the '==' operator to compare expressions of type double in the 'verify' statement can produce unexpected results. Step 'step_5' in Test Sequence 'SimuPro_Harness2/Test Sequence': verify(speed==80 && x060==0 && x60100==2);

Using the '==' operator to compare expressions of type double in the 'verify' statement can produce unexpected results. Step 'step_7' in Test Sequence 'SimuPro_Harness2/Test Sequence': verify(speed==180 && x060==0 && x60100==0 && x100140==0);

Using the '==' operator to compare expressions of type double in the 'verify' statement can produce unexpected results. Step 'step_7' in Test

Sequence 'SimuPro_Harness2/Test Sequence': verify(speed==180 && x060==0 && x60100==0 && x100140==0);

Using the '==' operator to compare expressions of type double in the 'verify' statement can produce unexpected results. Step 'step_7' in Test Sequence 'SimuPro_Harness2/Test Sequence': verify(speed==180 && x060==0 && x60100==0 && x100140==0);

Using the '==' operator to compare expressions of type double in the 'verify' statement can produce unexpected results. Step 'step_7' in Test Sequence 'SimuPro_Harness2/Test Sequence': verify(speed==180 && x060==0 && x60100==0 && x100140==0);

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TC02_ExternalWeightConditions

Test Result Information

Result Type:	Test Case Result
Parent:	SimuPro/Subsystem/speed conditions
Start Time:	12-Jun-2024 18:23:34
End Time:	12-Jun-2024 18:23:36
Outcome:	Passed

Test Case Information

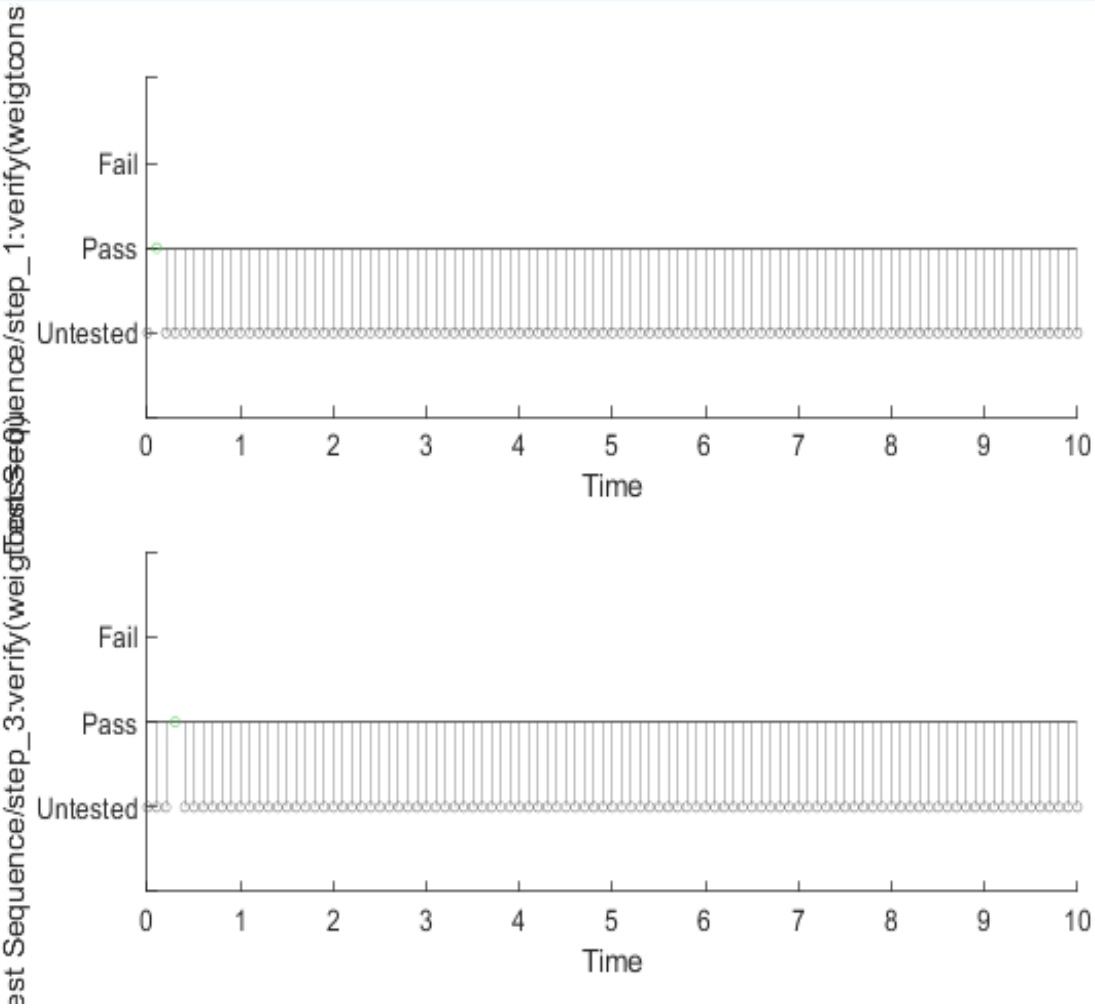
Name:	TC02_ExternalWeightConditions
Type:	Simulation Test

Verify Result

Name	Link to Plot
Test Sequence/step_1:verify(weigtcons==0)	Link
Test Sequence/step_3:verify(weigtcons==0)	Link

Test Sequence/step_5:verify(weigtcons==0)	Link
Test Sequence/step_7:verify(weigtcons-2<1e-5)	Link

Name
Test Sequence/step_1:verify(weigtcons==0)
Test Sequence/step_3:verify(weigtcons==0)



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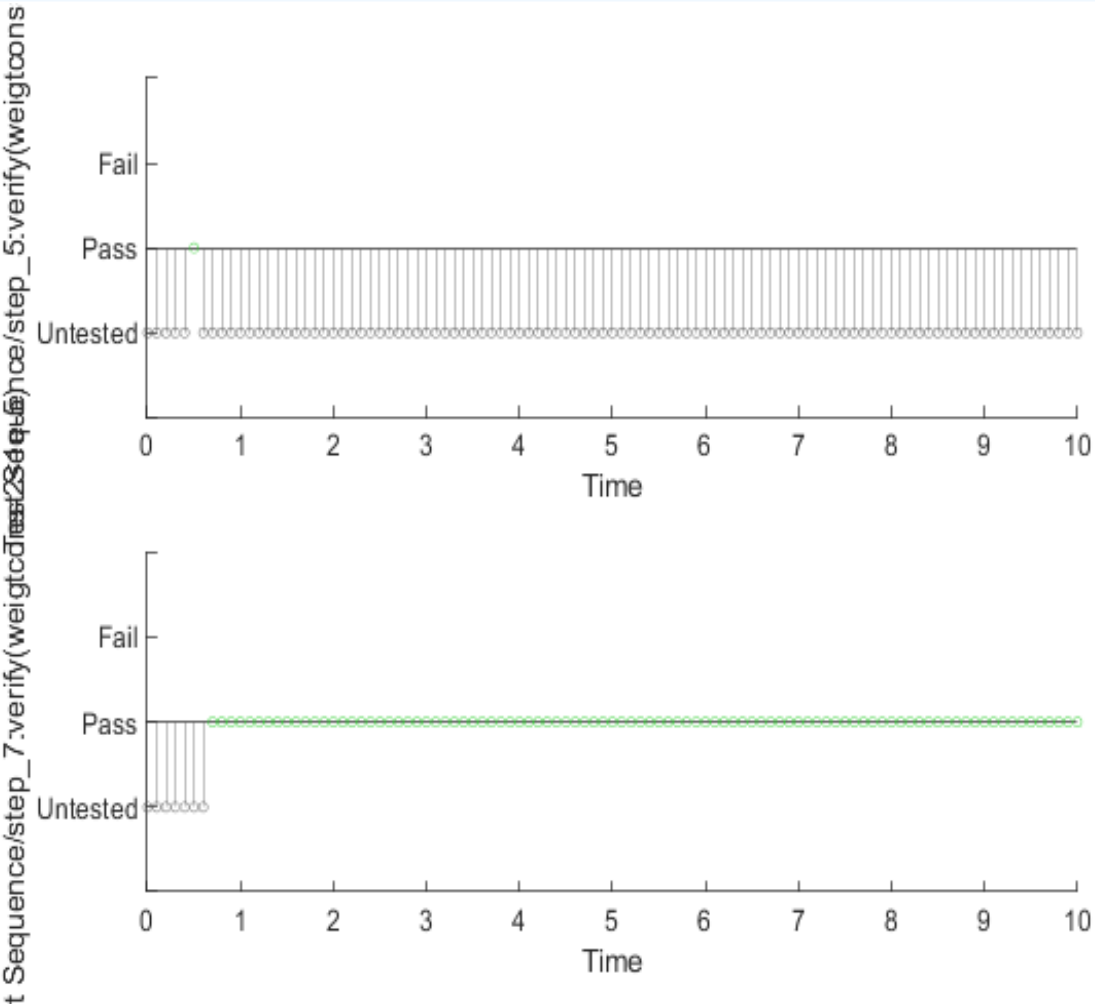
Name
Test Sequence/step_5:verify(weigtcons==0)
Test Sequence/step_7:verify(weigtcons-2<1e-5)



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Simulation

System Under Test Information

Model:	SimuPro
Harness:	SimuPro_Harness3

Harness Owner:	SimuPro/Subsystem/external weight condition
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	QuickStart_50024_6_10_16_0_35086
Start Time:	0
Stop Time:	10
Checksum:	3458630580 1420125270 538765184 2139412649
Simulink Version:	10.6
Model Version:	1.1
Model Author:	muham
Date:	Wed Jun 12 17:34:48 2024
User ID:	muham
Model Path:	C:\Users\muham\Downloads\SimuPro.slx
Machine Name:	DESKTOP-OF247DK
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2024-06-12 18:23:34
Simulation Stop Time:	2024-06-12 18:23:36
Platform:	PCWIN64

Simulation Logs:
Using the '==' operator to compare expressions of type double in the 'verify' statement can produce unexpected results.

Step 'step_1' in Test Sequence 'SimuPro_Harness3/Test Sequence':

```
verify(weigtcons==0);
```

Using the '==' operator to compare expressions of type double in the 'verify' statement can produce unexpected results.

Step 'step_3' in Test Sequence 'SimuPro_Harness3/Test Sequence':

verify(**weigtcons==0**);

Using the '==' operator to compare expressions of type double in the 'verify' statement can produce unexpected results.

Step 'step_5' in Test Sequence 'SimuPro_Harness3/Test Sequence':

verify(**weigtcons==0**);

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TC03_RoadTypeConditions

Test Result Information

Result Type:	Test Case Result
Parent:	SimuPro/Subsystem/speed conditions
Start Time:	12-Jun-2024 18:23:37
End Time:	12-Jun-2024 18:23:40
Outcome:	Passed

Test Case Information

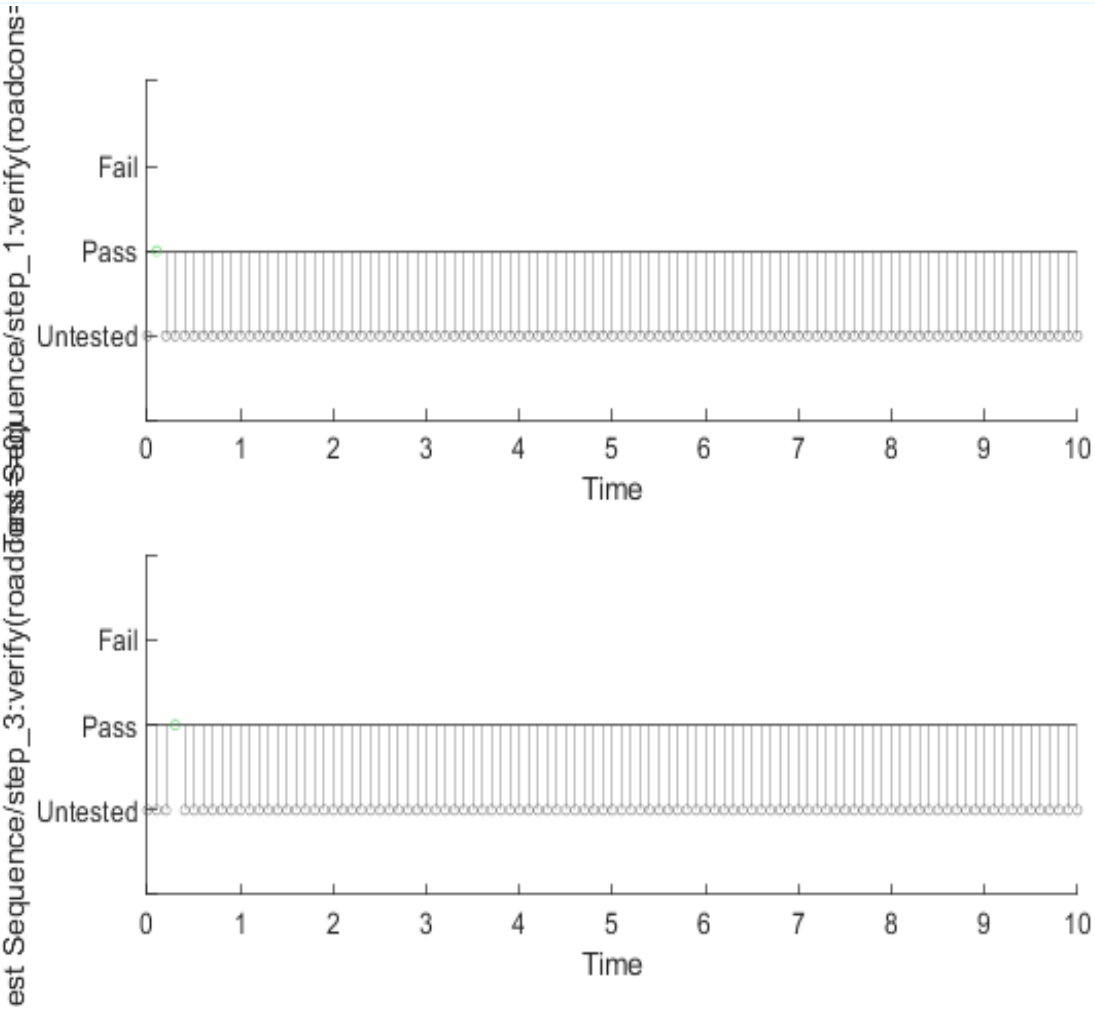
Name:	TC03_RoadTypeConditions
Type:	Simulation Test

Verify Result

Name	Link to Plot
Test Sequence/step_1:verify(roadcons==0)	Link

Test Sequence/step_3:verify(roadcons==0)	Link
Test Sequence/step_5:verify(roadcons==1)	Link
Test Sequence/step_7:verify(roadcons==0)	Link

Name
Test Sequence/step_1:verify(roadcons==0)
Test Sequence/step_3:verify(roadcons==0)



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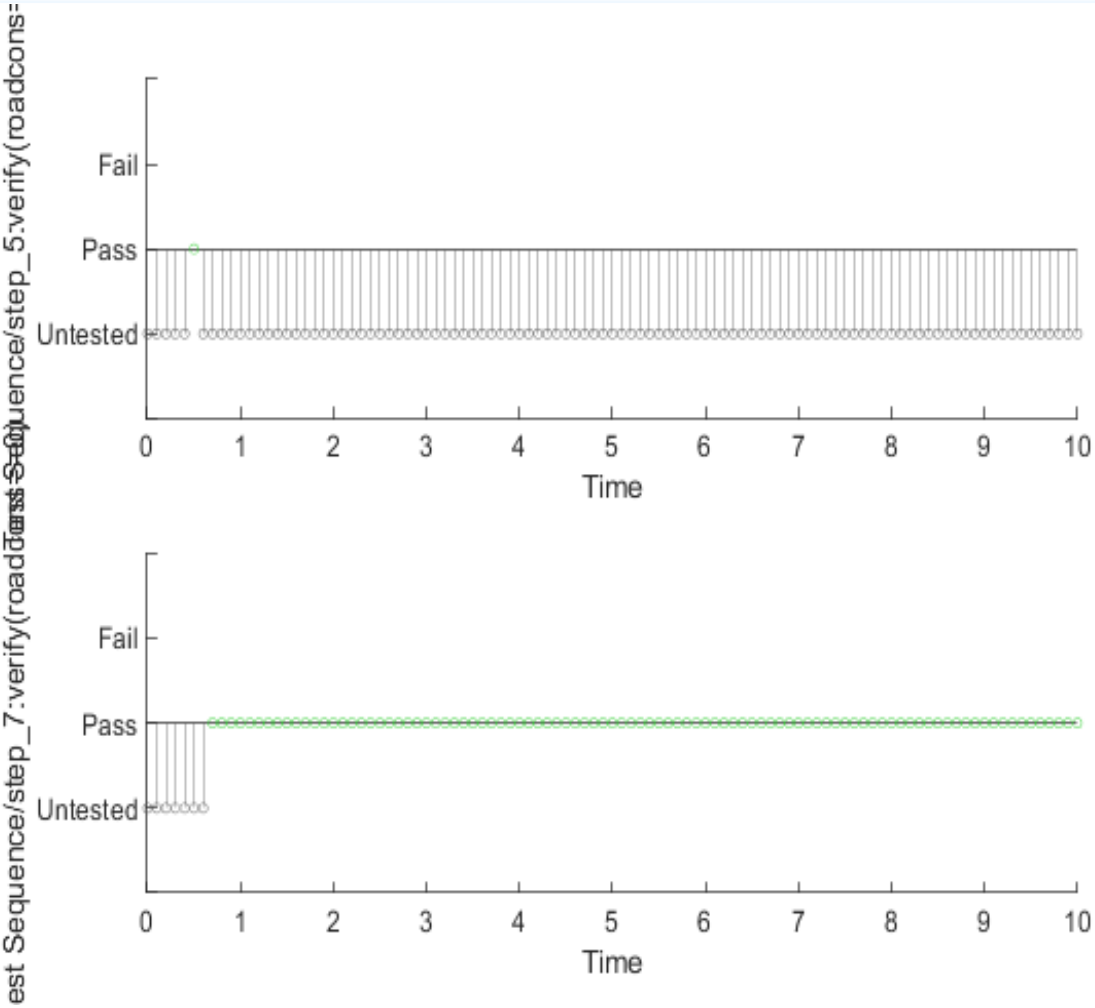
Name
Test Sequence/step_5:verify(roadcons==1)
Test Sequence/step_7:verify(roadcons==0)



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Simulation

System Under Test Information

Model: SimuPro

Harness:	SimuPro_Harness4
Harness Owner:	SimuPro/Subsystem/road type condition
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	QuickStart_50024_6_10_16_0_35086
Start Time:	0
Stop Time:	10
Checksum:	1208371333 3105066444 3811563408 3408272972
Simulink Version:	10.6
Model Version:	1.1
Model Author:	muham
Date:	Wed Jun 12 17:35:17 2024
User ID:	muham
Model Path:	C:\Users\muham\Downloads\SimuPro.slx
Machine Name:	DESKTOP-OF247DK
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2024-06-12 18:23:37
Simulation Stop Time:	2024-06-12 18:23:40
Platform:	PCWIN64

Simulation Logs:
Using the '==' operator to compare expressions of type double in the 'verify' statement can produce unexpected results.

Step 'step_1' in Test Sequence 'SimuPro_Harness4/Test Sequence':

verify(**roadcons**==**0**);

Using the '==' operator to compare expressions of type double in the 'verify' statement can produce unexpected results.

Step 'step_3' in Test Sequence 'SimuPro_Harness4/Test Sequence':

verify(**roadcons**==**0**);

Using the '==' operator to compare expressions of type double in the 'verify' statement can produce unexpected results.

Step 'step_5' in Test Sequence 'SimuPro_Harness4/Test Sequence':

verify(**roadcons**==**1**);

Using the '==' operator to compare expressions of type double in the 'verify' statement can produce unexpected results.

Step 'step_7' in Test Sequence 'SimuPro_Harness4/Test Sequence':

verify(**roadcons**==**0**);

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TC04_ACConditions

Test Result Information

Result Type:	Test Case Result
Parent:	SimuPro/Subsystem/speed conditions
Start Time:	12-Jun-2024 18:23:41
End Time:	12-Jun-2024 18:23:44

Outcome: Passed

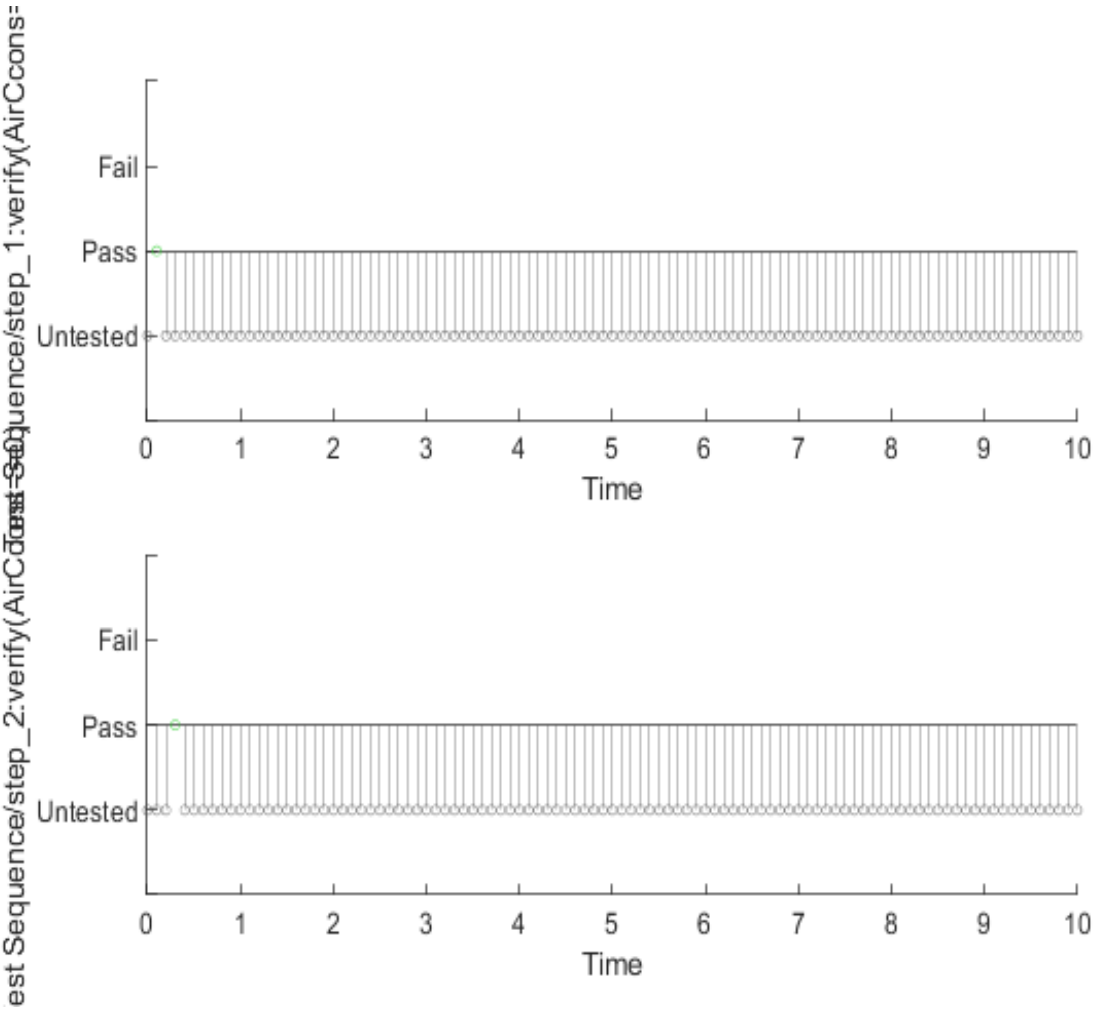
Test Case Information

Name: TC04_ACConditions
Type: Simulation Test

Verify Result

Name	Link to Plot
Test Sequence/step_1:verify(AirCcons==0)	Link
Test Sequence/step_2:verify(AirCcons==0)	Link
Test Sequence/step_3:verify(AirCcons==0)	Link
Test Sequence/step_4:verify(AirCcons==1)	Link

Name
Test Sequence/step_1:verify(AirCcons==0)
Test Sequence/step_2:verify(AirCcons==0)



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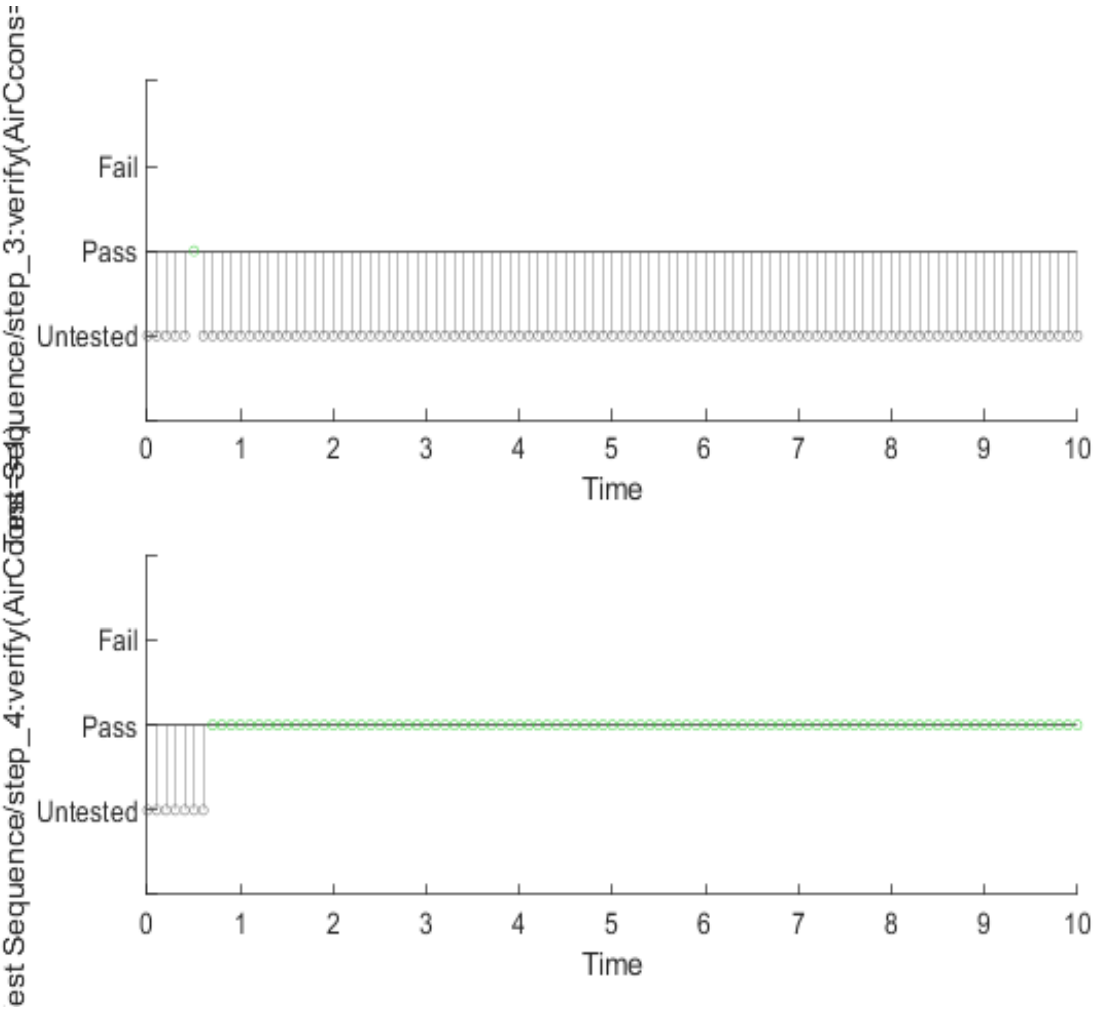
Name
Test Sequence/step_3:verify(AirCcons==0)
Test Sequence/step_4:verify(AirCcons==1)



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Simulation

System Under Test Information

Model:	SimuPro
Harness:	SimuPro_Harness1
Harness Owner:	SimuPro/Subsystem/Air conditioning condition
Release:	Current
Simulation Mode:	normal

Override SIL or PIL Mode:	0
Configuration Set:	QuickStart_50024_6_10_16_0_35086
Start Time:	0
Stop Time:	10
Checksum:	60770625 4107569560 1366862281 3745393648
Simulink Version:	10.6
Model Version:	1.2
Model Author:	muham
Date:	Wed Jun 12 17:35:57 2024
User ID:	muham
Model Path:	C:\Users\muham\Downloads\SimuPro.slx
Machine Name:	DESKTOP-OF247DK
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2024-06-12 18:23:41
Simulation Stop Time:	2024-06-12 18:23:43
Platform:	PCWIN64

Simulation Logs:
Using the '==' operator to compare expressions of type double in the 'verify' statement can produce unexpected results.

Step 'step_1' in Test Sequence 'SimuPro_Harness1/Test Sequence':

verify(**AirCcons**==**0**);

Using the '==' operator to compare expressions of type double in the 'verify' statement can produce unexpected results.

Step 'step_2' in Test Sequence 'SimuPro_Harness1/Test Sequence':

verify(**AirCcons**==**0**);

Using the '==' operator to compare expressions of type double in the 'verify' statement can produce unexpected results.

Step 'step_3' in Test Sequence 'SimuPro_Harness1/Test Sequence':

verify(**AirCcons**==**0**);

Using the '==' operator to compare expressions of type double in the 'verify' statement can produce unexpected results.

Step 'step_4' in Test Sequence 'SimuPro_Harness1/Test Sequence':

verify(**AirCcons**==**1**);

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TC05_AlertSystem

Test Result Information

Result Type:	Test Case Result
Parent:	SimuPro/Subsystem/speed conditions
Start Time:	12-Jun-2024 18:23:44
End Time:	12-Jun-2024 18:23:46
Outcome:	Passed

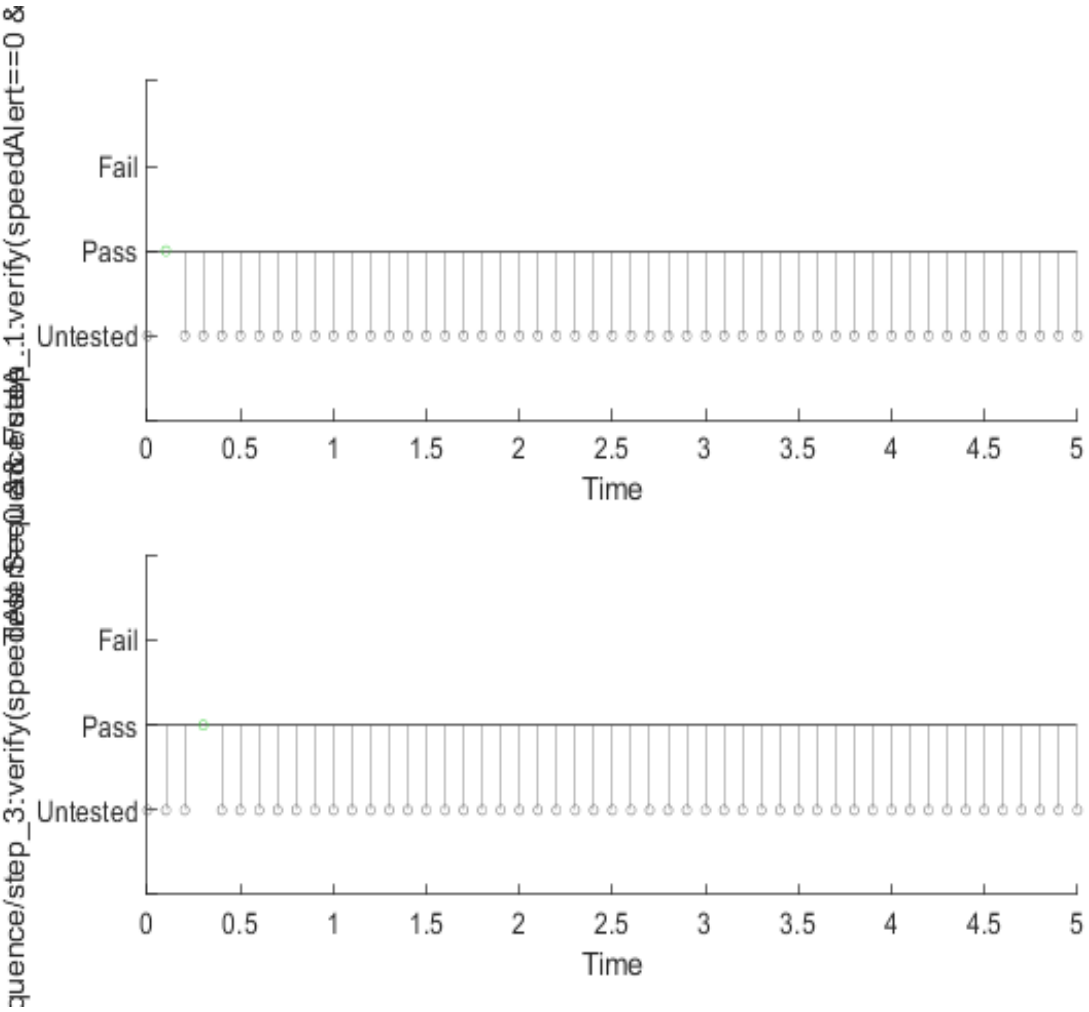
Test Case Information

Name: TC05_AlertSystem
Type: Simulation Test

Verify Result

Name	Link to Plot
Test Sequence/step_1:verify(speedAlert==0 && FuelAlert==1)	Link
Test Sequence/step_3:verify(speedAlert==0 && FuelAlert==1)	Link
Test Sequence/step_5:verify(speedAlert==1 && FuelAlert==1)	Link
Test Sequence/step_7:verify(speedAlert==1 && FuelAlert==0)	Link

Name
Test Sequence/step_1:verify(speedAlert==0 && FuelAlert==1)
Test Sequence/step_3:verify(speedAlert==0 && FuelAlert==1)



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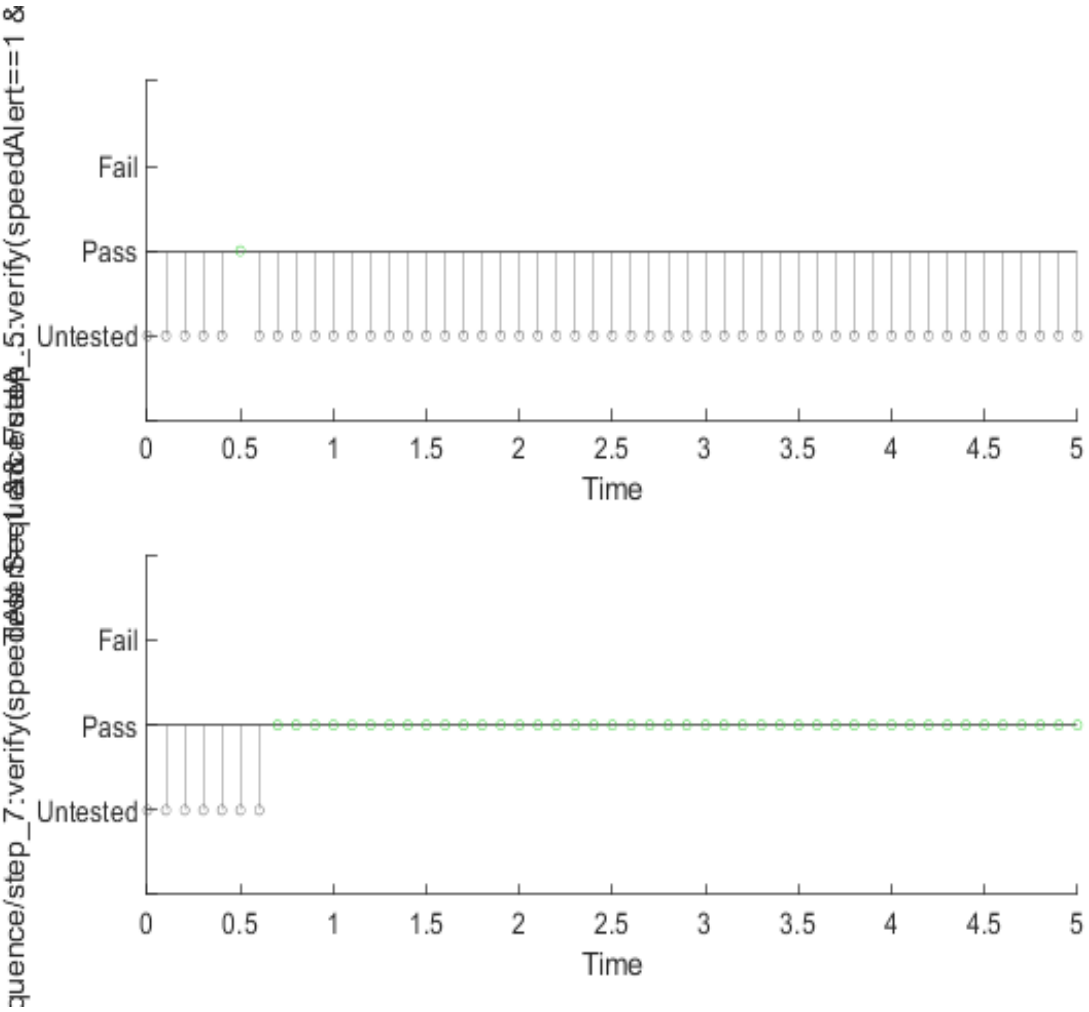
Name
Test Sequence/step_5:verify(speedAlert==1 && FuelAlert==1)
Test Sequence/step_7:verify(speedAlert==1 && FuelAlert==0)



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Simulation

System Under Test Information

Model:	SimuPro1
Harness:	ALERTharness
Harness Owner:	SimuPro1/Alerts sys
Release:	Current
Simulation Mode:	normal

Override SIL or PIL Mode:	0
Configuration Set:	QuickStart_50024_6_10_16_0_35086
Start Time:	0
Stop Time:	5
Checksum:	449538767 3137062810 3835609670 1469163749
Simulink Version:	10.6
Model Version:	1.3
Model Author:	muham
Date:	Wed Jun 12 18:22:23 2024
User ID:	muham
Model Path:	C:\Users\muham\Downloads\SimuPro1.slx
Machine Name:	DESKTOP-OF247DK
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.10000000000000001
Simulation Start Time:	2024-06-12 18:23:44
Simulation Stop Time:	2024-06-12 18:23:45
Platform:	PCWIN64