

# Report Generated by Test Manager

**Title:** Test  
**Author:** Sonko Muhammed R.  
**Date:** 29-Oct-2024 12:13:07

## Test Environment

Platform: PCWIN64  
MATLAB: (R2022b)

## Summary

Name

Outcome

Duration  
(Seconds)

 [DiagReq2](#)



4.724

# DiagReq2

## Test Result Information

Result Type:Test Case Result

Parent:None

Start Time:29-Oct-2024 11:34:13

End Time:29-Oct-2024 11:34:17

Outcome:Passed

## Test Case Information

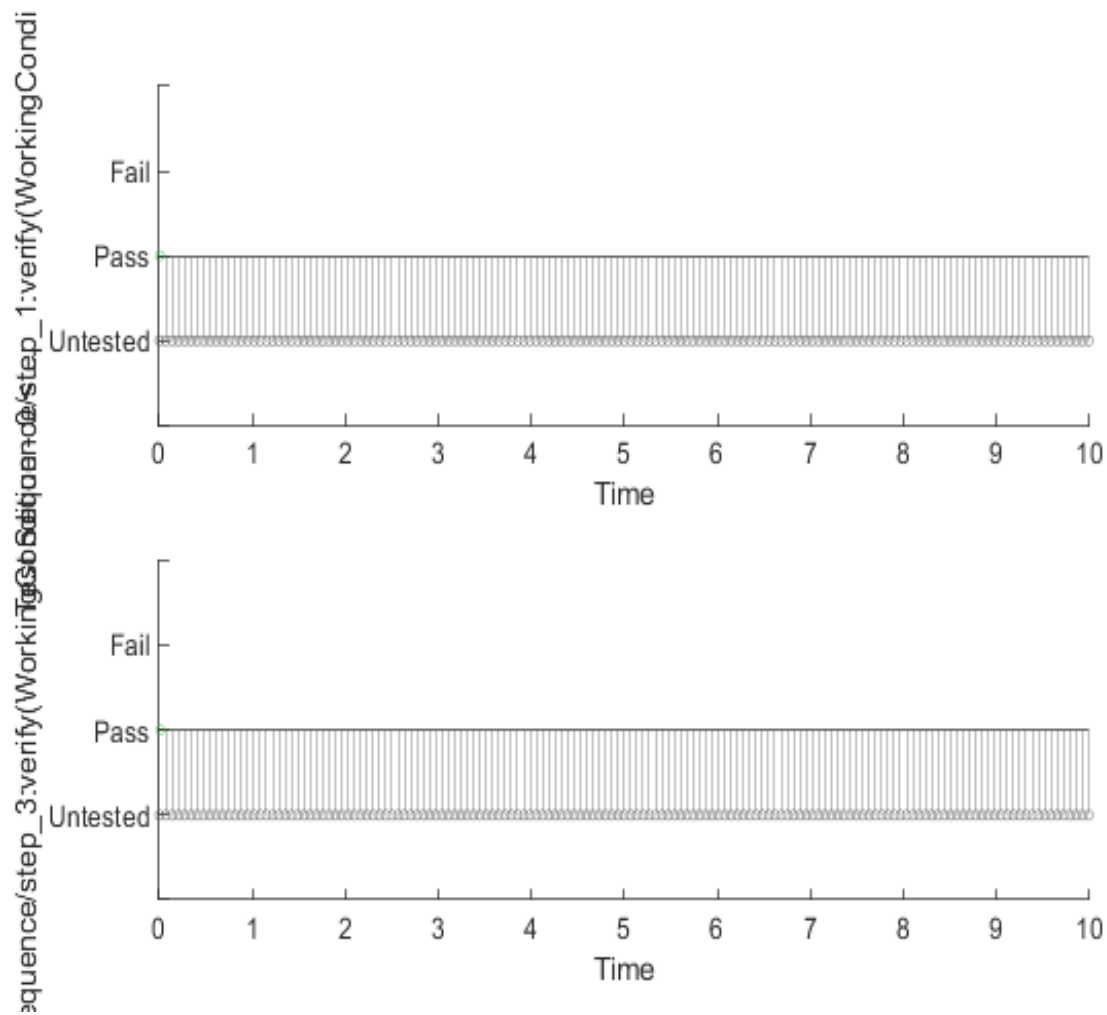
Name:DiagReq2

Type:Simulation Test

## Verify Result

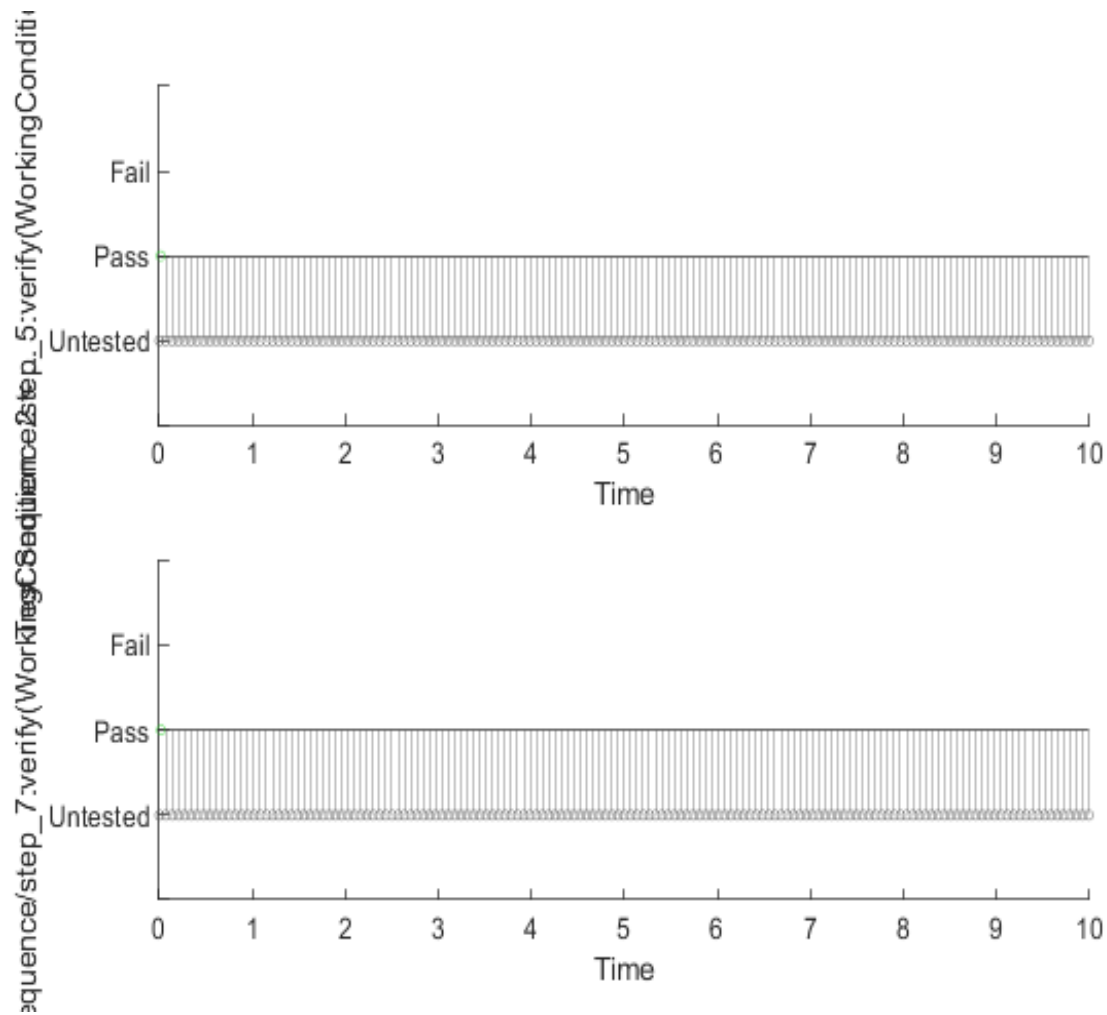
Name	Link to Plot
<div>✔ Test Sequence/step_1.verify(WorkingCondition==0)</div>	<a href="#">Link</a>
<div>✔ Test Sequence/step_3.verify(WorkingCondition - 0 &lt; 0.0001)</div>	<a href="#">Link</a>
<div>✔ Test Sequence/step_5.verify(WorkingCondition - 1 &lt; 0.0001)</div>	<a href="#">Link</a>
<div>✔ Test Sequence/step_7.verify(WorkingCondition - 2 &lt; 0.0001)</div>	<a href="#">Link</a>
<div>✔ Test Sequence/step_9.verify(WorkingCondition - 3 &lt; 0.0001)</div>	<a href="#">Link</a>
<div>✔ Test Sequence/step_11.verify(WorkingCondition - 4 &lt; 0.0001)</div>	<a href="#">Link</a>
<div>✔ Test Sequence/step_13.verify(WorkingCondition - 5 &lt; 0.0001)</div>	<a href="#">Link</a>

Name
<div>✔ Test Sequence/step_1.verify(WorkingCondition==0)</div>
<div>✔ Test Sequence/step_3.verify(WorkingCondition - 0 &lt; 0.0001)</div>



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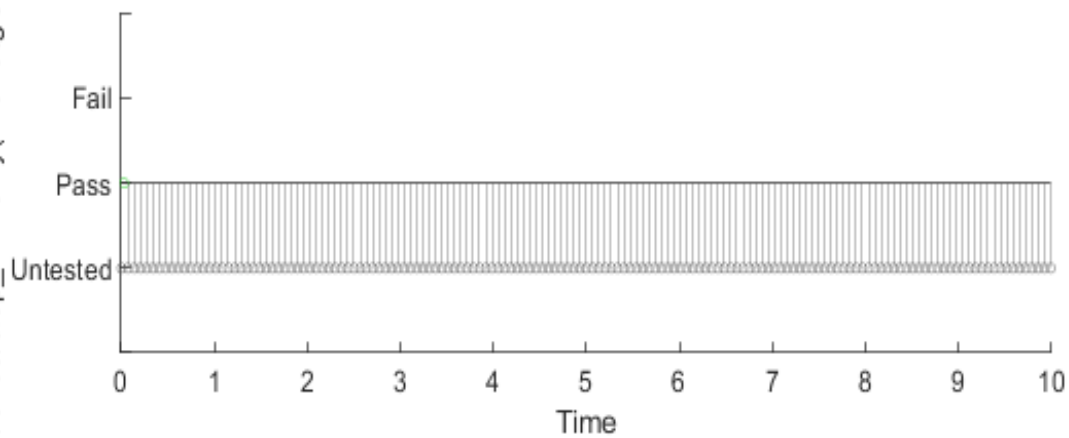
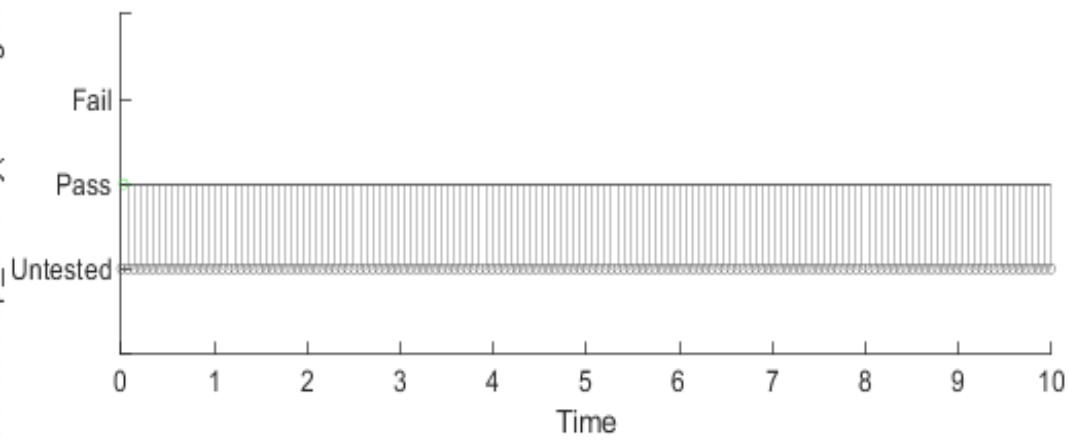
Name	
✓	Test Sequence/step_5:verify(WorkingCondition - 1 < 0.0001)
✓	Test Sequence/step_7:verify(WorkingCondition - 2 < 0.0001)



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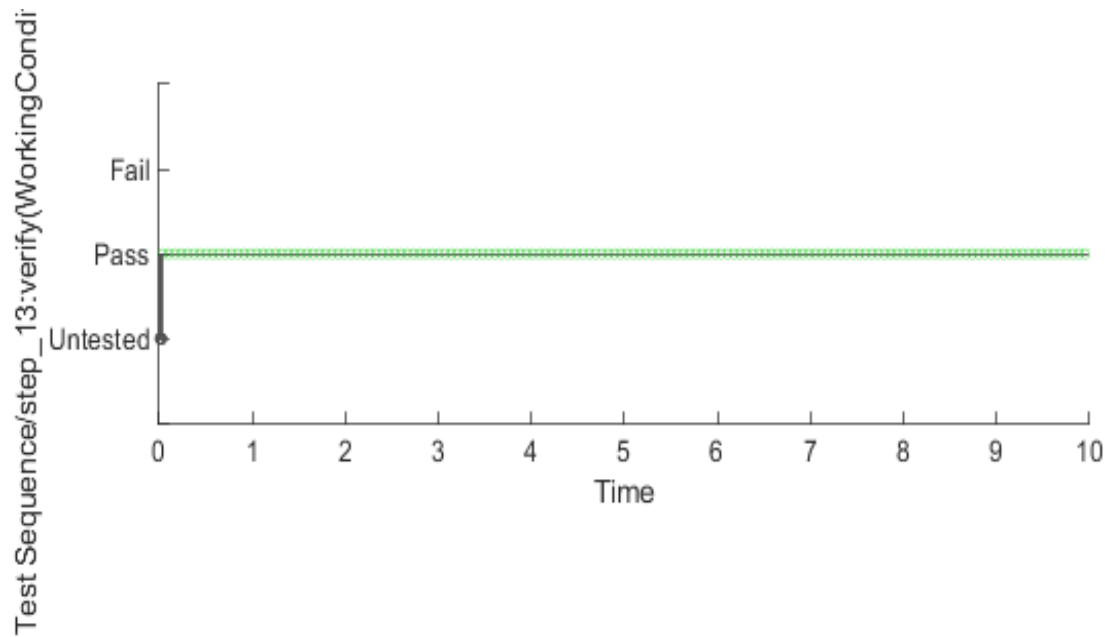
Name	
✔	Test Sequence/step_9:verify(WorkingCondition - 3 < 0.0001)
✔	Test Sequence/step_11:verify(WorkingCondition - 4 < 0.0001)

Test Sequence/step\_9:verify(WorkingCondition



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Name	
✓	Test Sequence/step_13:verify(WorkingCondition - 5 < 0.0001)



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## Simulation

### System Under Test Information

Model:	InitDiag
Harness:	InitDiag_Harness1
Harness Owner:	InitDiag/Subsystem/Subsystem
Release:	Current
Simulation Mode:	normal

Override SIL or PIL	0
Mode:	
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	10
Checksum:	4017348971 3731191896 4271648242 2229109967
Simulink Version:	10.6
Model Version:	1.0
User ID:	muham
Model Path:	C:\Users\muham\Desktop\MST_IESE_2023\M2_S1\Traitement_Num_Image\TNI_TP\InitDiag.slx
Machine Name:	DESKTOP-OF247DK
Solver Name:	VariableStepDiscrete
Solver Type:	Variable-Step
Max Step Size:	0.0025000000000000001
Simulation Start Time:	2024-10-29 11:34:13
Simulation Stop Time:	2024-10-29 11:34:16
Platform:	PCWIN64

#### Simulation Logs:

Using the '==' operator to compare expressions of type double in the 'verify' statement can produce unexpected results.

Step '[step\\_1](#)' in Test Sequence '[InitDiag\\_Harness1/Test Sequence](#)':

```
verify(WorkingCondition==0);
```

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