REGISTER 10-1: **T0CON: TIMER0 CONTROL REGISTER**

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TMR0ON	T08BIT	T0CS	T0SE	PSA	T0PS2	T0PS1	T0PS0
bit 7							bit 0

bit 7   **TMR0ON:** Timer0 On/Off Control bit

1 = Enables Timer0
0 = Stops Timer0

bit 6   **T08BIT**: Timer0 8-bit/16-bit Control bit

1 = Timer0 is configured as an 8-bit timer/counter
0 = Timer0 is configured as a 16-bit timer/counter

bit 5   **T0CS**: Timer0 Clock Source Select bit

1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (CLKO)

bit 4   **T0SE**: Timer0 Source Edge Select bit

1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin

bit 3   **PSA**: Timer0 Prescaler Assignment bit

1 = TImer0 prescaler is NOT assigned. Timer0 clock input bypasses prescaler.
0 = Timer0 prescaler is assigned. Timer0 clock input comes from prescaler output.

bit 2-0   **T0PS2:T0PS0**: Timer0 Prescaler Select bits

111 = 1:256 prescale value
110 = 1:128 prescale value
101 = 1:64 prescale value
100 = 1:32 prescale value
011 = 1:16 prescale value
010 = 1:8 prescale value
001 = 1:4 prescale value
000 = 1:2 prescale value

REGISTER 11-1: **T1CON: TIMER1 CONTROL REGISTER**

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RD16	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON
bit 7							bit 0

bit 7   **RD16:** 16-bit Read/Write Mode Enable bit

1 = Enables register Read/Write of Timer1 in one 16-bit operation
0 = Enables register Read/Write of Timer1 in two 8-bit operations

bit 6   **Unimplemented:** Read as '0'

bit 5-4   **T1CKPS1:T1CKPS0**: Timer1 Input Clock Prescale Select bits

11 = 1:8 Prescale value
10 = 1:4 Prescale value
01 = 1:2 Prescale value
00 = 1:1 Prescale value

bit 3   **T1OSCEN:** Timer1 Oscillator Enable bit

1 = Timer1 Oscillator is enabled
0 = Timer1 Oscillator is shut-off
    The oscillator inverter and feedback resistor are turned off to eliminate power drain.

bit 2   **T1SYNC**: Timer1 External Clock Input Synchronization Select bit

When TMR1CS = 1:
1 = Do not synchronize external clock input
0 = Synchronize external clock input
When TMR1CS = 0:
This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.

bit 1   **TMR1CS**: Timer1 Clock Source Select bit

1 = External clock from pin RC0/T1OSO/T13CKI (on the rising edge)
0 = Internal clock (Fosc/4)

bit 0   **TMR1ON:** Timer1 On bit

1 = Enables Timer1
0 = Stops Timer1

REGISTER 12-1: **T2CON: TIMER2 CONTROL REGISTER**

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0
bit 7							bit 0

bit 7   **Unimplemented:** Read as '0'

bit 6-3   **TOUTPS3:TOUTPS0**: Timer2 Output Postscale Select bits

 0000 = 1:1 Postscale
 0001 = 1:2 Postscale
 •
 •
 •
 1111 = 1:16 Postscale

bit 2   **TMR2ON**: Timer2 On bit

 1 = Timer2 is on
 0 = Timer2 is off

bit 1-0   **T2CKPS1:T2CKPS0**: Timer2 Clock Prescale Select bits

 00 = Prescaler is 1
 01 = Prescaler is 4
 1x = Prescaler is 16

REGISTER 13-1: **T3CON: TIMER3 CONTROL REGISTER**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RD16	T3CCP2	T3CKPS1	T3CKPS0	T3CCP1	T3SYNC	TMR3CS	TMR3ON
bit 7							bit 0

bit 7   **RD16:** 16-bit Read/Write Mode Enable bit

 1 = Enables register Read/Write of Timer3 in one 16-bit operation
 0 = Enables register Read/Write of Timer3 in two 8-bit operations

bit 6-3   **T3CCP2:T3CCP1:** Timer3 and Timer1 to CCPx Enable bits

 1x = Timer3 is the clock source for compare/capture CCP modules
 01 = Timer3 is the clock source for compare/capture of CCP2,
      Timer1 is the clock source for compare/capture of CCP1
 00 = Timer1 is the clock source for compare/capture CCP modules

bit 5-4   **T3CKPS1:T3CKPS0:** Timer3 Input Clock Prescale Select bits

 11 = 1:8 Prescale value
 10 = 1:4 Prescale value
 01 = 1:2 Prescale value
 00 = 1:1 Prescale value

bit 2   **T3SYNC:** Timer3 External Clock Input Synchronization Control bit
             (Not usable if the system clock comes from Timer1/Timer3)

 When TMR3CS = 1:
 1 = Do not synchronize external clock input
 0 = Synchronize external clock input
 When TMR3CS = 0:
 This bit is ignored. Timer3 uses the internal clock when TMR3CS = 0.

bit 1   **TMR3CS:** Timer3 Clock Source Select bit

 1 = External clock input from Timer1 oscillator or T1CKI
     (on the rising edge after the first falling edge)
 0 = Internal clock (Fosc/4)

bit 0   **TMR3ON:** Timer3 On bit

 1 = Enables Timer3
 0 = Stops Timer3

REGISTER 14-1:   CCP1CON REGISTER/CCP2CON REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DCxB1	DCxB0	CCPxM3	CCPxM2	CCPxM1	CCPxM0

bit 7   bit 0

bit 7-6   **Unimplemented:** Read as '0'

bit 5-4   **DCxB1:DCxB0**: PWM Duty Cycle bit1 and bit0

<u>Capture mode:</u>
Unused

<u>Compare mode:</u>
Unused

<u>PWM mode:</u>
These bits are the two LSbs (bit1 and bit0) of the 10-bit PWM duty cycle. The upper eight bits (DCx9:DCx2) of the duty cycle are found in CCPRxL.

bit 3-0   **CCPxM3:CCPxM0**: CCPx Mode Select bits

0000 = Capture/Compare/PWM disabled (resets CCPx module)
0001 = Reserved
0010 = Compare mode, toggle output on match (CCPxIF bit is set)
0011 = Reserved
0100 = Capture mode, every falling edge
0101 = Capture mode, every rising edge
0110 = Capture mode, every 4th rising edge
0111 = Capture mode, every 16th rising edge
1000 = Compare mode,
         Initialize CCP pin Low, on compare match force CCP pin High (CCPIF bit is set)
1001 = Compare mode,
         Initialize CCP pin High, on compare match force CCP pin Low (CCPIF bit is set)
1010 = Compare mode,
         Generate software interrupt on compare match (CCPIF bit is set, CCP pin is unaffected)
1011 = Compare mode,
         Trigger special event (CCPIF bit is set)
11xx = PWM mode

REGISTER 17-1:   ADCON0 REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	—	ADON

bit 7   bit 0

bit 7-6   **ADCS1:ADCS0**: A/D Conversion Clock Select bits (ADCON0 bits in **bold**)

ADCON1 <ADCS2>	ADCON0 <ADCS1:ADCS0>	Clock Conversion
0	00	Fosc/2
0	01	Fosc/8
0	10	Fosc/32
0	11	Frc (clock derived from the internal A/D RC oscillator)
1	00	Fosc/4
1	01	Fosc/16
1	10	Fosc/64
1	11	Frc (clock derived from the internal A/D RC oscillator)

bit 5-3   **CHS2:CHS0**: Analog Channel Select bits

000 = channel 0, (AN0)
001 = channel 1, (AN1)
010 = channel 2, (AN2)
011 = channel 3, (AN3)
100 = channel 4, (AN4)
101 = channel 5, (AN5)
110 = channel 6, (AN6)
111 = channel 7, (AN7)

Note: The PIC18F2X2 devices do not implement the full 8 A/D channels; the unimplemented selections are reserved. Do not select any unimplemented channel.

bit 2   **GO/DONE:** A/D Conversion Status bit

<u>When ADON = 1:</u>
1 = A/D conversion in progress (setting this bit starts the A/D conversion which is automatically cleared by hardware when the A/D conversion is complete)
0 = A/D conversion not in progress

bit 1   **Unimplemented:** Read as '0'

bit 0   **ADON:** A/D On bit

1 = A/D converter module is powered up
0 = A/D converter module is shut-off and consumes no operating current

REGISTER 17-2: ADCON1 REGISTER

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	ADCS2	—	—	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

bit 7   **ADFM:** A/D Result Format Select bit
1 = Right justified. Six (6) Most Significant bits of ADRESH are read as '0'.
0 = Left justified. Six (6) Least Significant bits of ADRESL are read as '0'.

bit 6   **ADCS2:** A/D Conversion Clock Select bit (ADCON1 bits in **bold**)

ADCON1 <ADCS2>	ADCON0 <ADCS1:ADCS0>	Clock Conversion
0	00	Fosc/2
0	01	Fosc/8
0	10	Fosc/32
0	11	FRC (clock derived from the internal A/D RC oscillator)
1	00	Fosc/4
1	01	Fosc/16
1	10	Fosc/64
1	11	FRC (clock derived from the internal A/D RC oscillator)

bit 5-4   **Unimplemented:** Read as '0'

bit 3-0   **PCFG3:PCFG0:** A/D Port Configuration Control bits

PCFG <3:0>	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0	VREF+	VREF-	C / R
0000	A	A	A	A	A	A	A	A	VDD	VSS	8 / 0
0001	A	A	A	A	VREF+	A	A	A	AN3	VSS	7 / 1
0010	D	D	D	A	A	A	A	A	VDD	VSS	5 / 0
0011	D	D	D	A	VREF+	A	A	A	AN3	VSS	4 / 1
0100	D	D	D	D	A	D	A	A	VDD	VSS	3 / 0
0101	D	D	D	D	VREF+	D	A	A	AN3	VSS	2 / 1
011x	D	D	D	D	D	D	D	D	—	—	0 / 0
1000	A	A	A	A	VREF+	VREF-	A	A	AN3	AN2	6 / 2
1001	D	D	A	A	A	A	A	A	VDD	VSS	6 / 0
1010	D	D	A	A	VREF+	A	A	A	AN3	VSS	5 / 1
1011	D	D	A	A	VREF+	VREF-	A	A	AN3	AN2	4 / 2
1100	D	D	D	A	VREF+	VREF-	A	A	AN3	AN2	3 / 2
1101	D	D	D	D	VREF+	VREF-	A	A	AN3	AN2	2 / 2
1110	D	D	D	D	D	D	D	A	VDD	VSS	1 / 0
1111	D	D	D	D	VREF+	VREF-	D	A	AN3	AN2	1 / 2

A = Analog input   D = Digital I/O
C/R = # of analog input channels / # of A/D voltage references

REGISTER 8-1: INTCON REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF
bit 7							bit 0

bit 7   **GIE/GIEH:** Global Interrupt Enable bit
<u>When IPEN = 0:</u>
1 = Enables all unmasked interrupts
0 = Disables all interrupts
<u>When IPEN = 1:</u>
1 = Enables all high priority interrupts
0 = Disables all interrupts

bit 6   **PEIE/GIEL:** Peripheral Interrupt Enable bit
<u>When IPEN = 0:</u>
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts
<u>When IPEN = 1:</u>
1 = Enables all low priority peripheral interrupts
0 = Disables all low priority peripheral interrupts

bit 5   **TMR0IE:** TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 overflow interrupt
0 = Disables the TMR0 overflow interrupt

bit 4   **INT0IE:** INT0 External Interrupt Enable bit
1 = Enables the INT0 external interrupt
0 = Disables the INT0 external interrupt

bit 3   **RBIE:** RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

bit 2   **TMR0IF:** TMR0 Overflow Interrupt Flag bit
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1   **INT0IF:** INT0 External Interrupt Flag bit
1 = The INT0 external interrupt occurred (must be cleared in software)
0 = The INT0 external interrupt did not occur

bit 0   **RBIF:** RB Port Change Interrupt Flag bit
1 = At least one of the RB7:RB4 pins changed state (must be cleared in software)
0 = None of the RB7:RB4 pins have changed state

Note: A mismatch condition will continue to set this bit. Reading PORTB will end the mismatch condition and allow the bit to be cleared.

REGISTER 8-2: INTCON2 REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	U-0	R/W-1	U-0	R/W-1
RBPU	INTEDG0	INTEDG1	INTEDG2	—	TMR0IP	—	RBIP
bit 7							bit 0

bit 7   **RBPU**: PORTB Pull-up Enable bit

1 = All PORTB pull-ups are disabled
0 = PORTB pull-ups are enabled by individual port latch values

bit 6   **INTEDG0**:External Interrupt0 Edge Select bit

1 = Interrupt on rising edge
0 = Interrupt on falling edge

bit 5   **INTEDG1**: External Interrupt1 Edge Select bit

1 = Interrupt on rising edge
0 = Interrupt on falling edge

bit 4   **INTEDG2**: External Interrupt2 Edge Select bit

1 = Interrupt on rising edge
0 = Interrupt on falling edge

bit 3   **Unimplemented:** Read as '0'

bit 2   **TMR0IP**: TMR0 Overflow Interrupt Priority bit

1 = High priority
0 = Low priority

bit 1   **Unimplemented:** Read as '0'

bit 0   **RBIP**: RB Port Change Interrupt Priority bit

1 = High priority
0 = Low priority

REGISTER 8-3: INTCON3 REGISTER

R/W-1	R/W-1	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
INT2IP	INT1IP	—	INT2IE	INT1IE	—	INT2IF	INT1IF
bit 7							bit 0

bit 7   **INT2IP:** INT2 External Interrupt Priority bit

1 = High priority
0 = Low priority

bit 6   **INT1IP:** INT1 External Interrupt Priority bit

1 = High priority
0 = Low priority

bit 5   **Unimplemented:** Read as '0'

bit 4   **INT2IE:** INT2 External Interrupt Enable bit

1 = Enables the INT2 external interrupt
0 = Disables the INT2 external interrupt

bit 3   **INT1IE:** INT1 External Interrupt Enable bit

1 = Enables the INT1 external interrupt
0 = Disables the INT1 external interrupt

bit 2   **Unimplemented:** Read as '0'

bit 1   **INT2IF:** INT2 External Interrupt Flag bit

1 = The INT2 external interrupt occurred (must be cleared in software)
0 = The INT2 external interrupt did not occur

bit 0   **INT1IF:** INT1 External Interrupt Flag bit

1 = The INT1 external interrupt occurred (must be cleared in software)
0 = The INT1 external interrupt did not occur

Interrupt source	Flag bit	Enable bit	Priority bit
INT0 external	INT0IF	INT0IE	–
INT1 external	INT1IF	INT1IE	INT1IP
INT2 external	INT2IF	INT2IE	INT2IP
RB port change	RBIF	RBIE	RBIP
TMR0 overflow	TMR0IF	TMR0IE	TMR0IP
TMR1 overflow	TMR1IF	TMR1IE	TMR1IP
TMR2 match PR2	TMR2IF	TMR2IE	TMR2IP
TMR3 overflow	TMR3IF	TMR3IE	TMR3IP
A/D complete	ADIF	ADIE	ADIP
CCP1	CCP1IF	CCP1IE	CCP1IP
CCP2	CCP2IF	CCP2IE	CCP2IP
USART RCV	RCIF	RCIE	RCIP
USART TX	TXIF	TXIE	TXIP
Parallel slave port	PSPIF	PSPIE	PSPIP
Sync serial port	SSPIF	SSPIE	SSPIP
Low-voltage detect	LVDIF	LVDIE	LVDIP
Bus collision	BCLIF	BCLIE	BCLIP
EEPROM/FLASH write	EEIF	EEIE	EEIP

Graphical LCD

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
Display On/off	0	0	0	0	1	1	1	1	1	D	Controls the display ON or OFF.The internal status and the DDRAM data is not affected. D=0: OFF; D=1: ON
Set Address (Y address)	0	0	0	1	Y address (0~63)						Sets the Y address at the column address counter
Set Page (X address)	0	0	1	0	1	1	1	Page (0~7)			Sets the X address at the X address register.
Display Start Line	0	0	1	1	Display start line (0~63)						Indicates the Display Data RAM displayed at the top of the screen.

Status Read	0	1	Busy	0	ON/ OFF	Reset	0	0	0	0	Reads the internal status
											BUSY
											    0: Ready
											    1: In operation
											ON/OFF
											    0: Display ON
											    1: Display OFF
											RESET
											    0: Normal
											    1: Reset

Write Display Data	1	0	Write data								Writes data (DB[0:7]) into the DDRAM. After writing instruction, Y address is incriminated by 1 automatically
Read Display Data	1	1	Read data								Reads data (DB[0:7]) from display data RAM to the data bus.