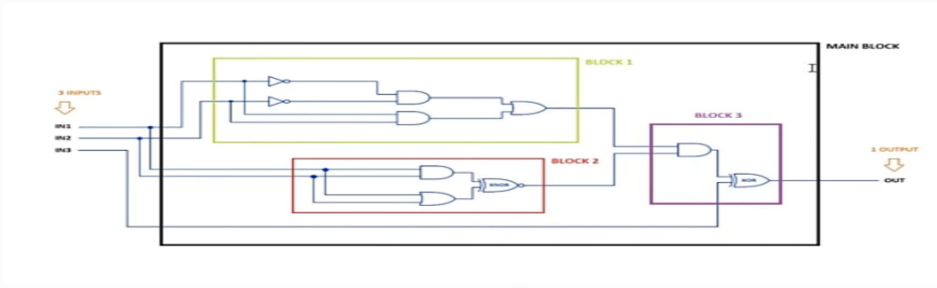

in1	in2	in3	out
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

```
1  `timescale 1ns / 1ps
2
3  module main(in1, in2, in3, out
4      );
5
6      input in1, in2, in3;
7
8      output out;
9
10     wire w1, w2;
11
12     B1 block1( .a(in1), .b(in2), .c(w1) );
13
14     B2 block2( .a(in1), .b(in2), .c(w2) );
15
16     B3 block3( .a(w1), .b(w2), .c(in3), .d(out) );
17
18
19
20
21 endmodule
```

```
1  `timescale 1ns / 1ps
2
3  module B1(a,b,c
4      );
5
6      input a,b;
7      output c;
8
9      assign c = (~a & ~b) | (a & b);
10
11
12 endmodule
13
```

```
1  `timescale 1ns / 1ps
2
3  module B2(a,b,c
4      );
5
6      input a,b;
7      output c;
8
9      assign c = ((a & b) ~^ (a | b));
10
11
12 endmodule
13
```

```
1  `timescale 1ns / 1ps
2
3  module B3(a,b,c,d
4      );
5
6
7      input a,b,c;
8      output d;
9
10     assign d = (a & b) ^ c;
11
12 endmodule
13
```

```
1  NET in1 LOC = "P11";
2  NET in2 LOC = "L3";
3  NET in3 LOC = "K3";
4  NET out LOC = "M5";
```