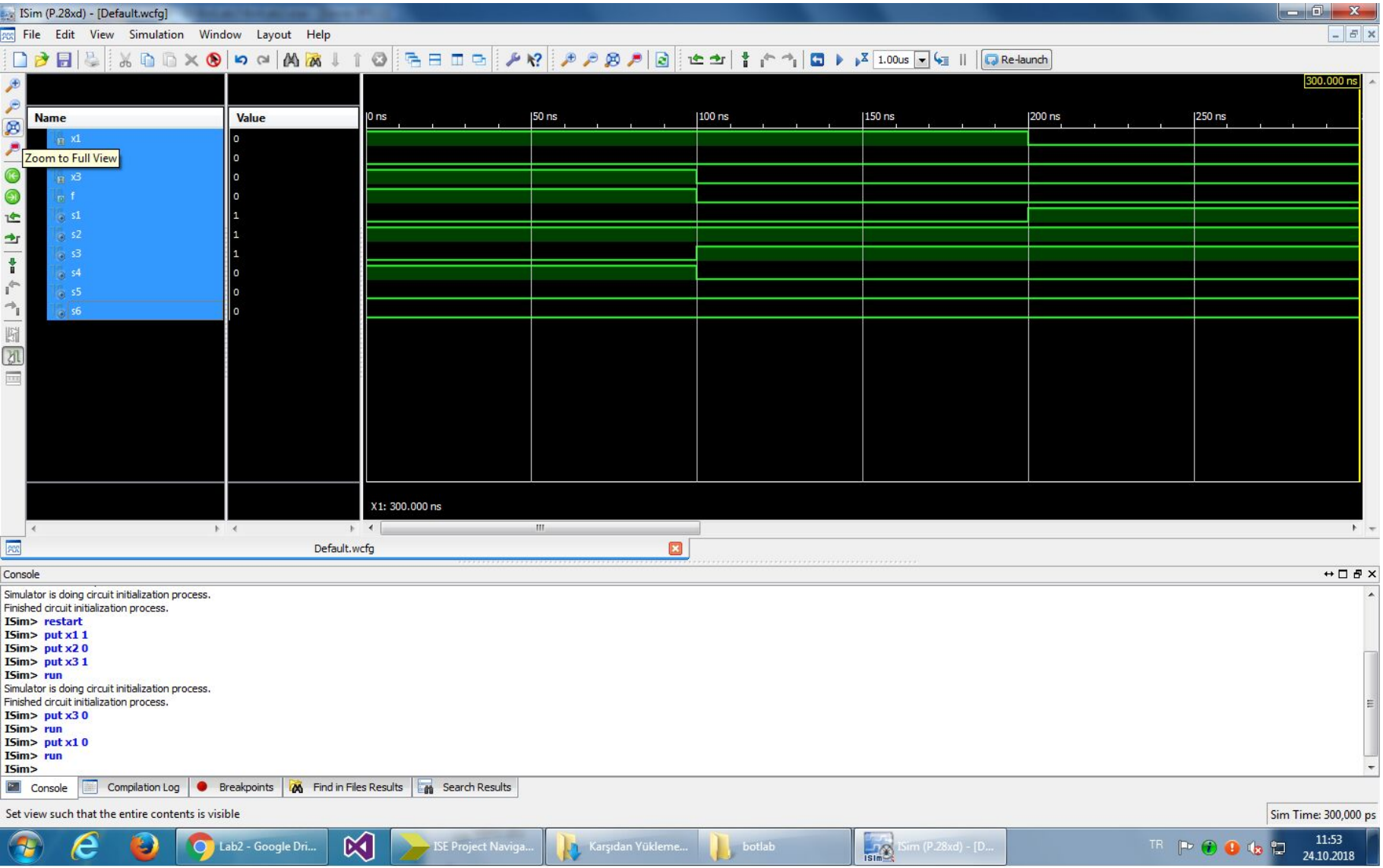
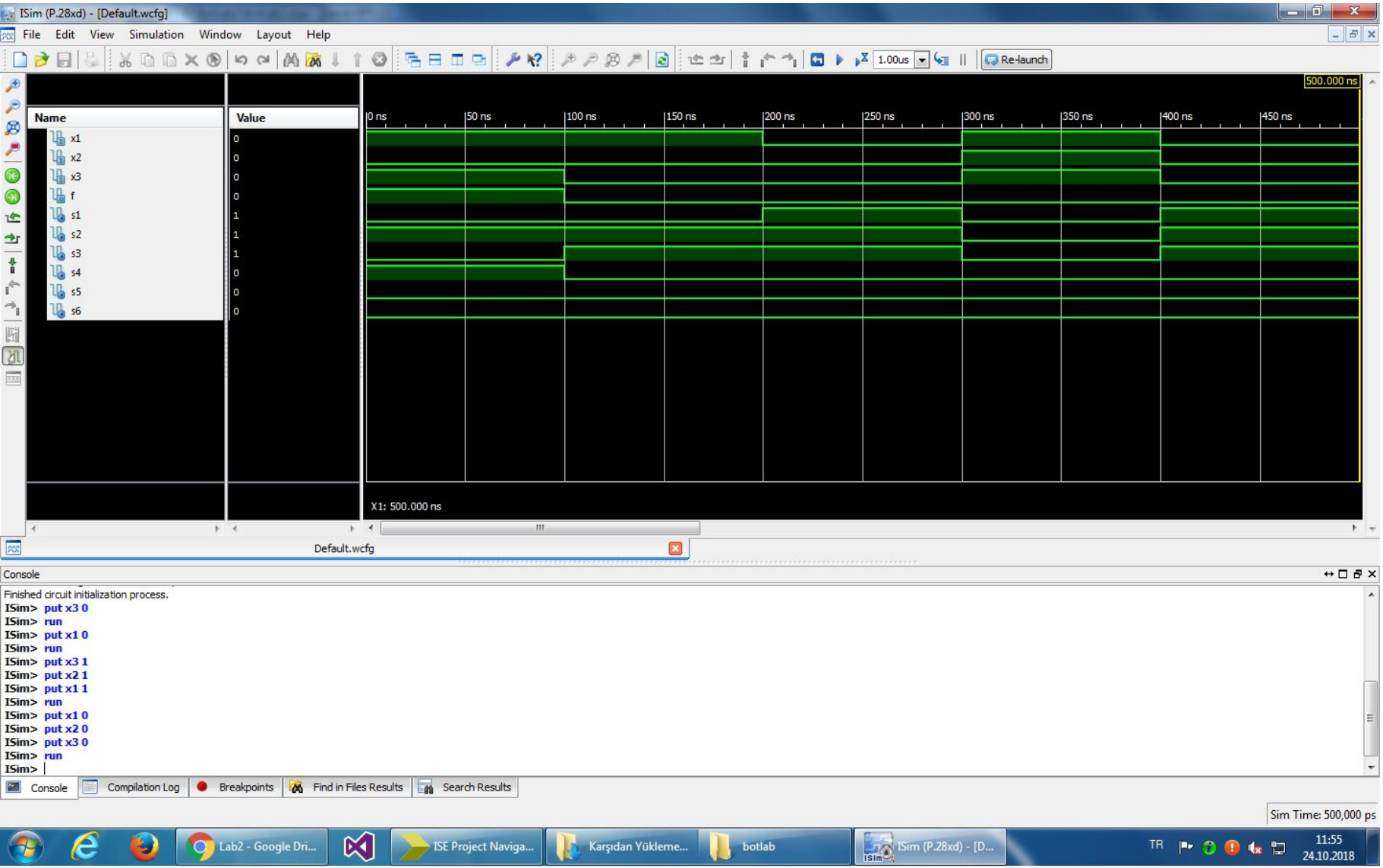
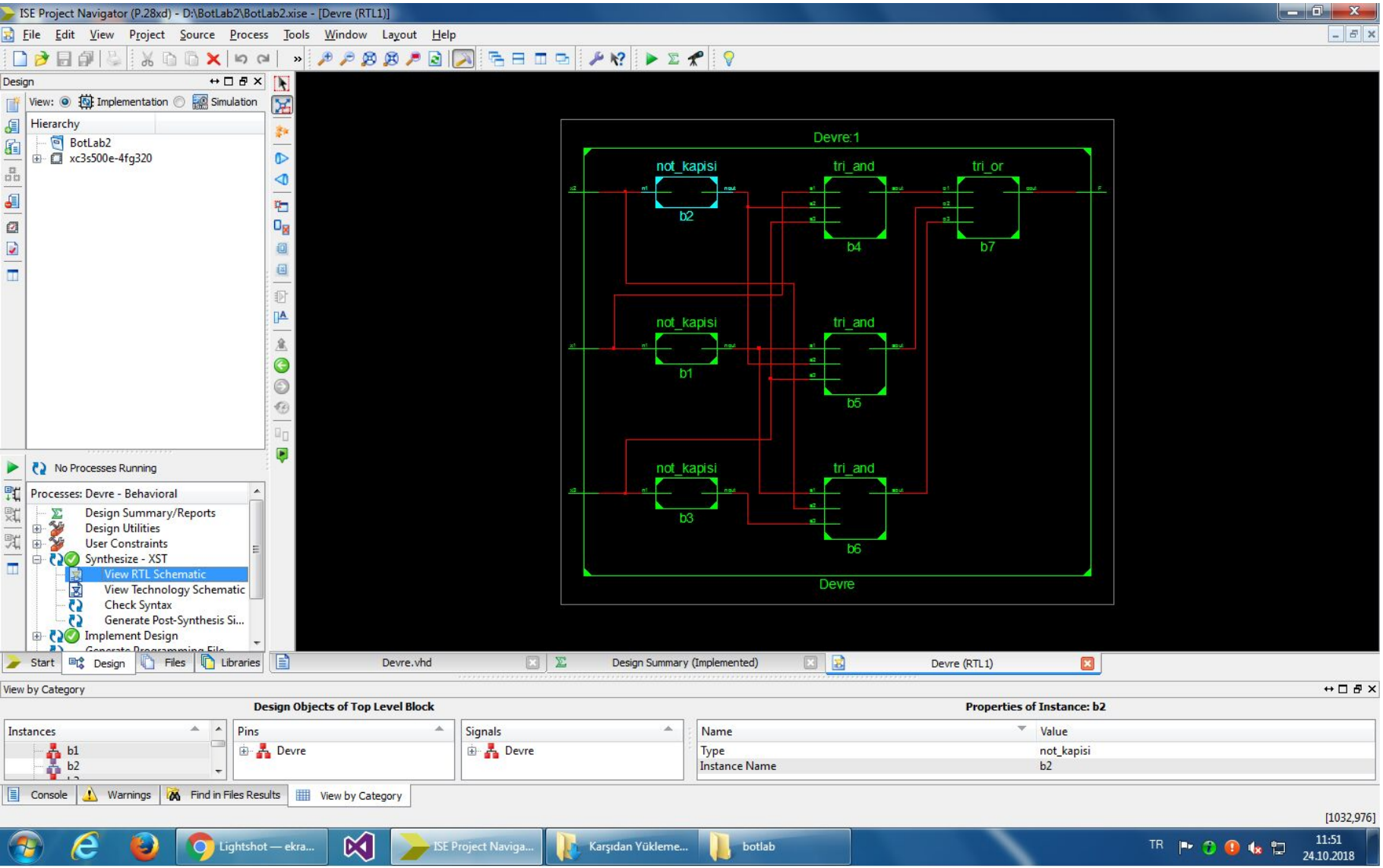

ISim (P.28xd) - [Default.wcfg]
File Edit View Simulation Window Layout Help
1.00us
Re-launch
Name
Value
x1
x3
f
s1
s2
s3
s4
s5
s6
Zoom to Full View
0
0
0
0
1
1
1
0
0
0
300.000 ns
0 ns
50 ns
100 ns
150 ns
200 ns
250 ns
X1: 300.000 ns
Default.wcfg
Console
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim> restart
ISim> put x1 1
ISim> put x2 0
ISim> put x3 1
ISim> run
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim> put x3 0
ISim> run
ISim> put x1 0
ISim> run
ISim>
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Set view such that the entire contents is visible
Sim Time: 300,000 ps
Lab2 - Google Dri...
ISE Project Naviga...
Karşıdan Yükleme...
botlab
ISim (P.28xd) - [D...
TR
11:53
24.10.2018

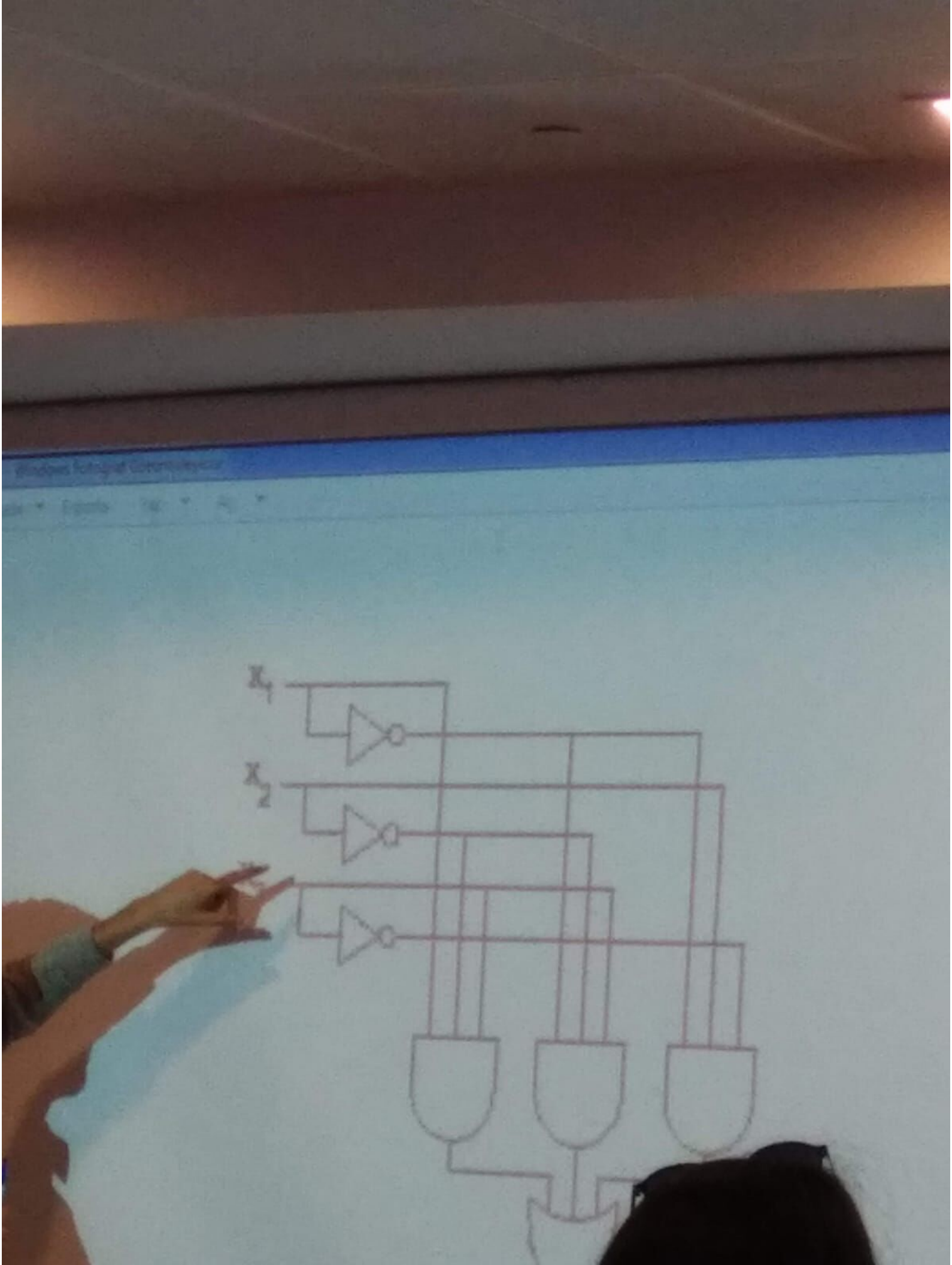

ISim (P.28xd) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Name
Value
x1
x2
x3
f
s1
s2
s3
s4
s5
s6
0 ns
50 ns
100 ns
150 ns
200 ns
250 ns
300 ns
350 ns
400 ns
450 ns
500.000 ns
X1: 500.000 ns
Default.wcfg
Console
Finished circuit initialization process.
ISim> put x3 0
ISim> run
ISim> put x1 0
ISim> run
ISim> put x3 1
ISim> put x2 1
ISim> put x1 1
ISim> run
ISim> put x1 0
ISim> put x2 0
ISim> put x3 0
ISim> run
ISim>
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 500,000 ps
Lab2 - Google Dri...
ISE Project Naviga...
Karşıdan Yükleme...
botlab
ISim (P.28xd) - [D...
TR
11:55
24.10.2018

```
----------------------------------------------------------------------------
---------
-- Company:
-- Engineer:
--
-- Create Date:    10:36:39 10/24/2018
-- Design Name:
-- Module Name:    Devre - Behavioral
-- Project Name: 2. Uygulama - D
-- Target Devices:
-- Tool versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------
---------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

-- Genel devre her þeyden baðýmsýzdýr
entity Devre is
      port(
            x1, x2, x3 :in STD_LOGIC;
            F:out STD_LOGIC
      );
end Devre;

architecture Behavioral of Devre is

-- And kapýsýnýn eklenmesi
component tri_and
      port(a1, a2, a3: in STD_LOGIC;
            aout: out STD_LOGIC
      );
end component;

-- Or kapýsýnýn eklenmesi
component tri_or
      port(o1, o2, o3:in STD_LOGIC;
            oout:out STD_LOGIC
      );
end component;

-- Not kapýsýnýn eklenmesi
component not_kapisi
      port(
```

```
            n1:in STD_LOGIC;
            nout:out STD_LOGIC
      );
end component;


-- ara kablolar (component'ten gelen kablolar)
signal s1: STD_LOGIC;
signal s2: STD_LOGIC;
signal s3: STD_LOGIC;
signal s4: STD_LOGIC;
signal s5: STD_LOGIC;
signal s6: STD_LOGIC;

begin
      -- b'ler etikettir
      b1: not_kapisi port map(x1, s1);
      b2: not_kapisi port map(x2, s2);
      b3: not_kapisi port map(x3, s3);
      b4: tri_and port map(x1, s2, x3, s4);
      b5: tri_and port map(s1, s2, x3, s5);
      b6: tri_and port map(s1, x2, s3, s6);
      b7: tri_or port map(s4, s5, s6, F);

end Behavioral;
----------------------------------------------------------------------------
---------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity tri_and is

port(a1, a2, a3: in STD_LOGIC;
      aout:out STD_LOGIC
);

end tri_and;

architecture Behavioral of tri_and is

begin
      process(a1, a2, a3)

      begin
      aout <= a1 AND a2 AND a3;
      end process;

end Behavioral;
----------------------------------------------------------------------------
---------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity tri_or is

port(o1, o2, o3: in STD_LOGIC;
      oout : out STD_LOGIC
);

end tri_or;
```

```
architecture Behavioral of tri_or is

begin
      process(o1, o2, o3)

      begin
      oout <= o1 OR o2 OR o3;
      end process;

end Behavioral;
----------------------------------------------------------------------------
---------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity not_kapisi is

port(
      n1:in STD_LOGIC;
      nout:out STD_LOGIC
);

end not_kapisi;

architecture Behavioral of not_kapisi is

begin
      process(n1)

      begin
            nout <= not n1;
      end process;

end Behavioral;
```


ISE Project Navigator (P.28xd) - D:\BotLab2\BotLab2.xise - [Devre (RTL1)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
BotLab2
xc3s500e-4fg320
No Processes Running
Processes: Devre - Behavioral
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis Si...
Implement Design
Devre:1
not_kapisi
tri_and
tri_or
b2
b4
b7
not_kapisi
tri_and
b1
b5
not_kapisi
tri_and
b3
b6
Devre
Start Design Files Libraries
Devre.vhd
Design Summary (Implemented)
Devre (RTL1)
View by Category
Design Objects of Top Level Block
Properties of Instance: b2
Instances
b1
b2
Pins
Devre
Signals
Devre
Name
Value
Type
not_kapisi
Instance Name
b2
Console Warnings Find in Files Results View by Category
[1032,976]
Lightshot — ekra...
ISE Project Naviga...
Karşıdan Yükleme...
botlab
TR
11:51
24.10.2018


x_1
x_2