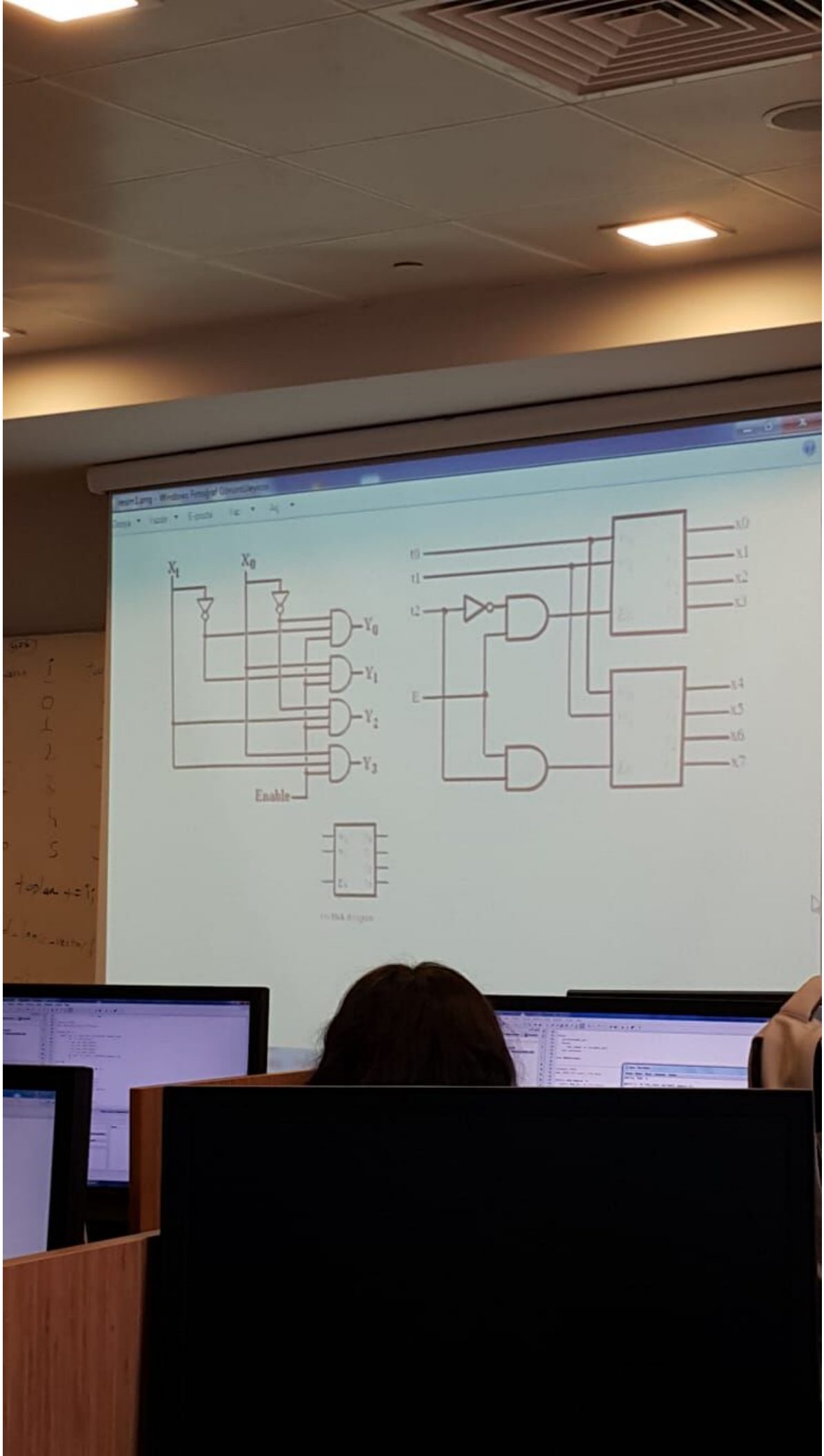
X_1
X_0
Y_0
Y_1
Y_2
Y_3
Enable

```
----------------------------------------------------------------------------
---------
-- Company:
-- Engineer: Yunus Emre Ak 1306150001 , Okan Uslu {no}
--
-- Create Date:    16:51:16 11/02/2018
-- Design Name:
-- Module Name:    Devre - Behavioral
-- Project Name:   4. Uygulama - D
-- Target Devices:
-- Tool versions:
-- Description: 4. Uygulamada çizilmesi gereken devrenin vhdl kodları
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------
---------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity NotGate is
    port(
        x0: in STD_LOGIC;
        y0: out STD_LOGIC
    );
end NotGate;

architecture Behavioral of NotGate is

begin
     process(x0)
     begin
           y0 <= not x0;
     end process;
end Behavioral;
----------------------------------------------------------------------------
--------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity AndGate is
    port(
        x0, x1: in STD_LOGIC;
        y0: out STD_LOGIC
    );
end AndGate;

architecture Behavioral of AndGate is
begin
    process(x0, x1)
    begin
        y0 <= x0 AND x1;
    end process;
end Behavioral;
----------------------------------------------------------------------------
---------
```

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity TriAndGate is
    port (
        x0, x1, x2: in STD_LOGIC;
        y0: out STD_LOGIC
    );
end TriAndGate;

architecture Behavioral of TriAndGate is
begin
    process(x0, x1, x2)

    begin
        y0 <= x0 AND x1 AND x2;
    end process;
end Behavioral;
----------------------------------------------------------------------------
---------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity Decoder is
    port(
        x0, x1, E: in STD_LOGIC;
        y0, y1, y2, y3: out STD_LOGIC
    );
end Decoder;

architecture Behavioral of Decoder is

component NotGate is
    port(
        x0: in STD_LOGIC;
        y0: out STD_LOGIC
    );
end component;

component TriAndGate is
    port(
        x0, x1, x2: in STD_LOGIC;
        y0: out STD_LOGIC
    );
end component;

signal n0: STD_LOGIC;
signal n1: STD_LOGIC;

begin
    p1: NotGate port map(x0, n0);
    p2: NotGate port map(x1, n1);
    p3: TriAndGate port map(n0, n1, E, y0);
    p4: TriAndGate port map(x0, n1, E, y1);
    p5: TriAndGate port map(n0, x1, E, y2);
    p6: TriAndGate port map(x0, x1, E, y3);

end Behavioral;
----------------------------------------------------------------------------
--------------------
```

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity Circuit is
    port(
        t0, t1, t2, E:in STD_LOGIC;
        x0, x1, x2, x3, x4, x5, x6, x7:out STD_LOGIC
    );
end Circuit;

architecture Behavioral of Circuit is

component NotGate is
    port(
        x0: in STD_LOGIC;
        y0: out STD_LOGIC
    );
end component;

component AndGate is
    port(
        x0, x1: in STD_LOGIC;
        y0: out STD_LOGIC
    );
end component;

component Decoder is
    port(
        x0, x1, E: in STD_LOGIC;
        y0, y1, y2, y3: out STD_LOGIC
    );
end component;

signal a0: STD_LOGIC;
signal n2: STD_LOGIC;
signal a1: STD_LOGIC;

begin
    p0: NotGate port map(t2, n2);
    p1: AndGate port map(n2, E, a0);
    p2: Decoder port map(t0, t1, a0, x0, x1, x2, x3);
    p3: AndGate port map(E, t2, a1);
    p4: Decoder port map(t0, t1, a1, x4, x5, x6, x7);

end Behavioral;
```