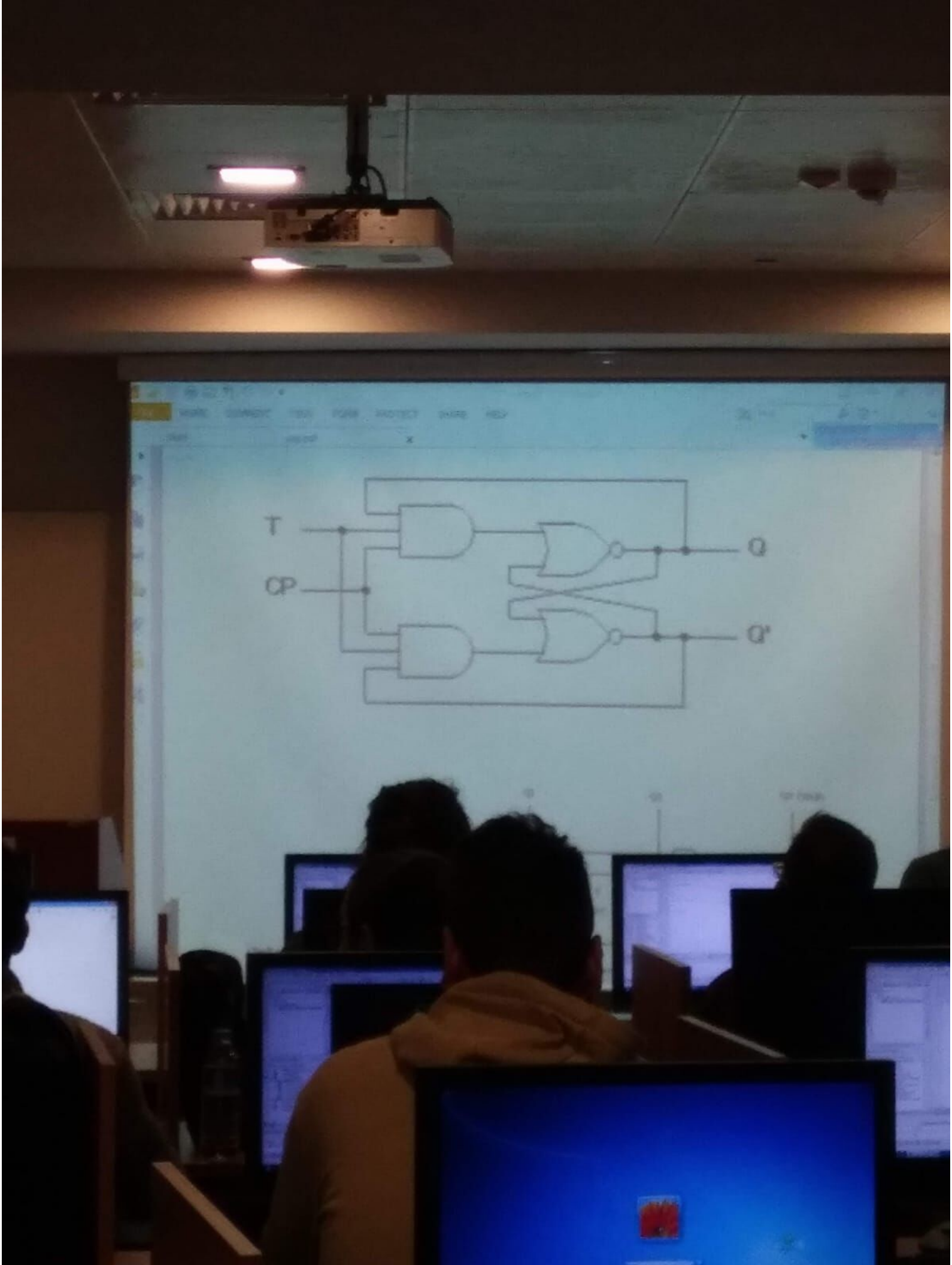
T
CP
Q
Q'

```
----------------------------------------------------------------------------
---------
-- Company:
-- Engineer: Yunus Emre Ak 1306150001 , Okan Uslu {no}
--
-- Create Date:    16:51:16 11/02/2018
-- Design Name:
-- Module Name:    Devre - Behavioral
-- Project Name:   4. Uygulama - D
-- Target Devices:
-- Tool versions:
-- Description: 4. Uygulamada çizilmesi gereken devrenin vhdl kodları
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------
---------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity JK is
    port( -- Setting input and output ports
        T, CP: in STD_LOGIC;
        Q, nQ: inout STD_LOGIC
    );
end JK;

-- Defining the behavioral of the architecture which is JK Flip-Flop
architecture Behavioral of JK is
    -- Adding TriAndGate component
    component TriAndGate is
        port(
            x0, x1, x2: in STD_LOGIC;
            y: out STD_LOGIC
        );
    end component;

    -- Adding NorGate component
    component NorGate is
        port(
            x0, x1: in STD_LOGIC;
            y: out STD_LOGIC
        );
    end component;

    -- Adding necessary signals
    signal a1: STD_LOGIC; -- First and gate output (the left up)
    signal a2: STD_LOGIC; -- Second and gate output (the left down)
    signal nor1: STD_LOGIC; -- First and gate output (the right up)
    signal nor2: STD_LOGIC; -- Second and gate output (the right down)

    begin -- Behavioral
        p0: TriAndGate port map(Q, T, CP, a1);
        p1: TriAndGate port map(CP, T, nQ, a2);
        p2: NorGate port map(a1, nQ, Q);
        p3: NorGate port map(Q, a2, nQ);
```

```
end Behavioral;

-------------------------------------------------------------------------
---------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Defining NorGate
entity NorGate is
    port( -- Setting input and output ports
        x0, x1: in STD_LOGIC;
        y: out STD_LOGIC
    );
end NorGate;

-- Defining the behavioral of the architecture which is NorGate
architecture Behavioral of NorGate is
    begin -- Behavioral
        process(x0, x1) -- Process the ports which necessary
        begin -- Process
            y <= NOT (x0 OR x1);
        end process;
end Behavioral;

-------------------------------------------------------------------------
---------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Definig TriAndGate
entity TriAndGate is
    port( -- Setting input and output ports
        x0, x1, x2: in STD_LOGIC;
        y: out STD_LOGIC
    );
end TriAndGate;

-- Defining the behavioral of the architecture which is TriAndGate
architecture Behavioral of TriAndGate is
    begin -- Behavioral
        process(x0, x1, x2) -- Process the ports which necessary
        begin -- Process
            y <= x0 AND x1 AND x2;
        end process;
end Behavioral;
```