Digital Logic Design
(EL-227)
LABORATORY MANUAL
Spring-2021

LAB 06
Half Adder, Full Adder, half Subtractor and Binary Multiplication

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STUDENT NAME ROLL NO SEC

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INSTRUCTOR SIGNATURE & DATE

MARKS AWARDED: /02

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NATIONAL UNIVERSITY OF COMPUTER AND EMERGING SCIENCES (NUCES), KARACHI

Date:22/03/2021

Lab Session 06: Half Adder, Full Adder, half Subtractor and Binary Multiplication

After completing this lab, you would be able to know

- ➢ Distinguish between Half Adder and Full Adder, their functions and logic diagrams
- ➢ Implement adder circuits using logic gate ICs
- ➢ Implement half Subtractor and Full Subtractor circuits using logic gate ICs
- ➢ Implement a 2*2 Binary Multiplier circuits using logic gate ICs
- ➢ Define some useful terminologies like CARRY, SUM, Difference and Borrow

Theory:

In electronics, an ***adder*** or ***summer*** is a digital circuit that performs addition of numbers. For single bit adders, there are two general types:

- Half Adder
- Full Adder

1. Half Adder

A **half adder** is a logic circuit which performs addition of two binary one-bit inputs and has two binary outputs as a result. The outputs are designated as **Sum (S)** and **Carry (C)**.

Circuit Diagram

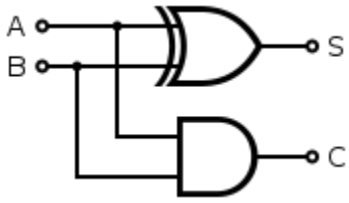
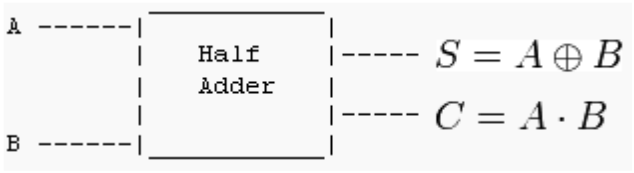


Figure 01



Truth Table:

Here is the Truth table of Half Adder,

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

2. Full Adder:

A full adder is a logic circuit performs the addition of three binary one-bit inputs and has Two binary outputs as a result. The three binary inputs include two binary input bits (A and B) and a Carry bit (Cin). The outputs of the full adder are designated as Sum (S) and Carry out (Cout). A block diagram of Full Adder implementation is as follows:

Circuit Diagram:

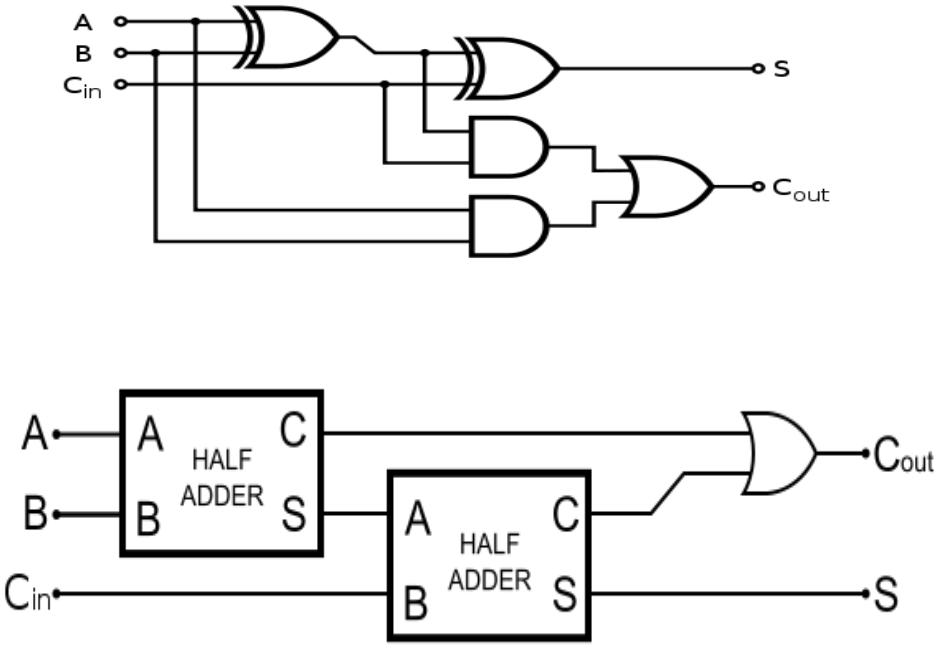


Figure 02

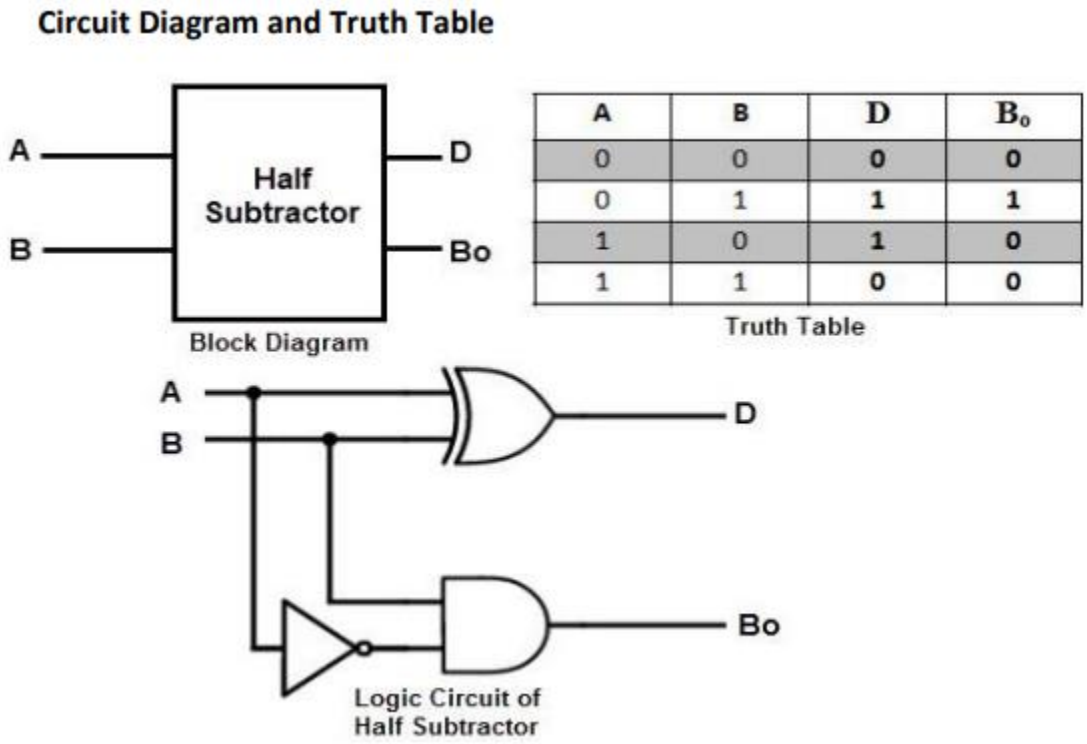
Truth Table:

TRUTH TABLE (Full Adder - 1bit)

X	Y	Cin	Cout	S
0	0	0	**0**	**0**
0	0	1	**0**	**1**
0	1	0	**0**	**1**
0	1	1	**1**	**0**
1	0	0	**0**	**1**
1	0	1	**1**	**0**
1	1	0	**1**	**0**
1	1	1	**1**	**1**

3. Half Subtractor

A half Subtractor circuit performs the subtraction of two binary inputs and has two binary outputs as a result. The outputs of the half Subtractor are designated as Difference (D) and Borrow (B). The difference and borrow are the binary difference and borrow and has either '0' or '1' logic.



A	B	D	B_o
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Truth Table

Figure 03

4. Full Subtractor

A combinational logic circuit performs a subtraction between the two binary bits by considering Borrow of the lower significant stage is called as the full subtractor. In this, subtraction of the two Digits is performed by taking into consideration whether a 1 has already borrowed by the previous Adjacent lower minuend bit or not.
It has three input terminals in which two terminals corresponds to the two bits to be subtracted (minuend A and subtrahend B), and a borrow bit Bi corresponds to the borrow operation. There are two outputs, one corresponds to the difference D output and other borrow output Bo as shown in Figure along with truth table.

A	B	B_{in}	D	B_o
0	0	0	**0**	**0**
0	0	1	**1**	**1**
0	1	0	**1**	**1**
0	1	1	**0**	**1**
1	0	0	**1**	**0**
1	0	1	**0**	**0**
1	1	0	**0**	**0**
1	1	1	**1**	**1**

Truth Table

By deriving the Boolean expression for the full subtractor from above truth table, we get the expression that tells that a full subtractor can be implemented with half subtractor with OR gate as shown in figure below.

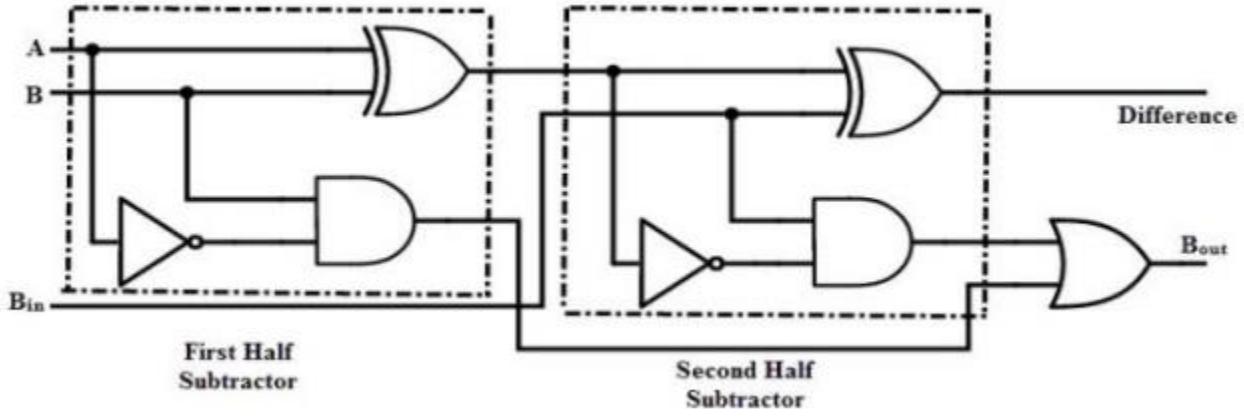


Figure 04

5. Binary Multiplication:

Multiplication in binary Number system is similar to its decimal counterpart. Two numbers *A* and *B* can be multiplied by partial products: for each digit in *B*, the product of that digit in *A* is
Calculated and written on a new line, shifted leftward so that its rightmost digit lines up with the Digit in *B* that was used. The sum of all these partial products gives the final result.
Since there are only two digits in binary, there are only two possible outcomes of each partial multiplication:

- If the digit in *B* is 0, the partial product is also 0
- If the digit in *B* is 1, the partial product is equal to *A*

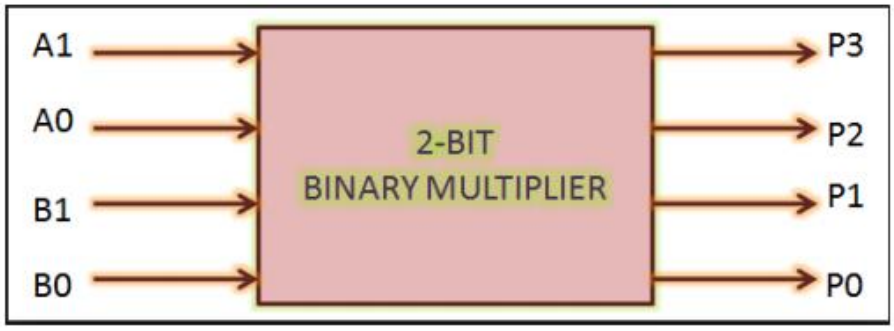
For example, the binary numbers 1011 and 1010 are multiplied as follows:

- The AND gates produce the partial products.

- For a 2-bit by 2-bit multiplier, we can just use two half adders to sum the partial products. In general, though, we'll need full adders.

Here C_3-C_0 are the product, not carries.

```
        1 0 1 1   (A)
      × 1 0 1 0   (B)
      ---------
        0 0 0 0   ← Corresponds to a zero in B
+     1 0 1 1     ← Corresponds to a one in B
+   0 0 0 0
+ 1 0 1 1
---------------
= 1 1 0 1 1 1 0
```



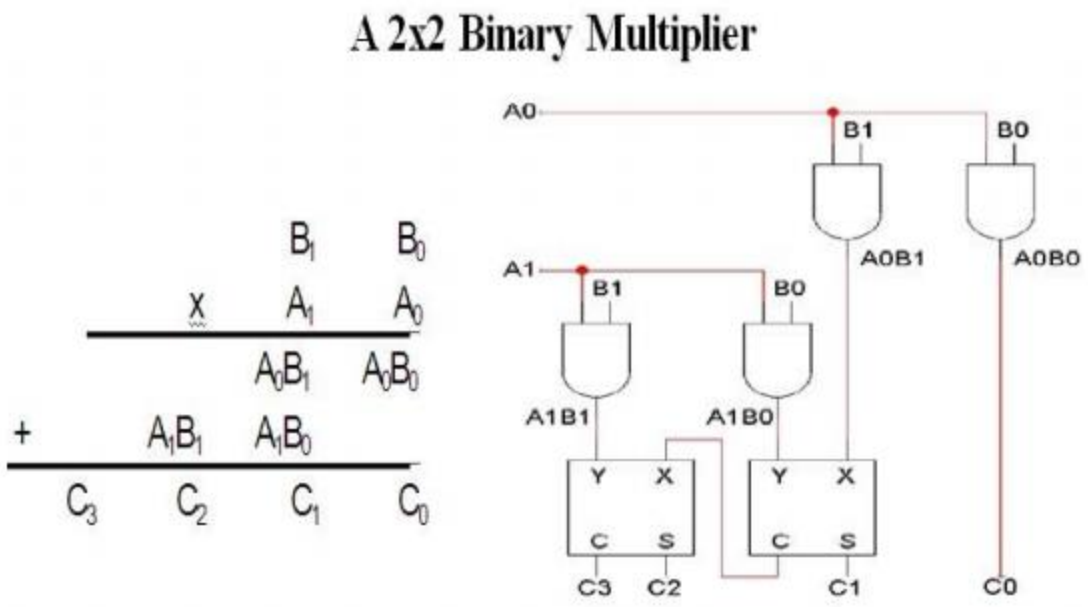


Figure 05

What are the applications of a full adder circuit?

1. Ripple carry adder, it adds n-bits at a time.
2. Carryout Multiplication -the dedicated multiplication circuit uses it.
3. ALU- Arithmetic Logic Unit (one of the circuit is a full adder).
4. To generate memory addresses inside a computer and to make the Program Counter Point to next instruction, the ALU makes use of this adder.
5. for graphics related applications, where there is a very much need of complex Computations, the GPU uses optimized ALU which is made up of full adders, other Circuits as well….
6. ALU in computers and varieties of calculators.
7. Different IC and microprocessor chips in PC n laptops
8. Ripple counter
9. Important tool in DSP (digital signal processing).

Basically, it is used in designing ALU and this ALU is used for wide variety of applications (From designing CPU to GPU).

Report for Experiment 6

Name _____ Student ID_____ Section_____ Date_____

Exercise:

Q No. 01. Design and implement Full Adder Circuit on Bread board and write down its Boolean Expression.

Q No .02 Design and implement Half Adder Circuit on Bread Board and write down its Boolean Expression.

Q No. 03. Design and implement 2*2 Bit Binary Multiplier Circuit on Bread Board.

Q No.04 Design and implement half subtractor Circuit on Bread Board and write down its Boolean Expression.

Q No. 05 Design circuit on trainer for given expressions by using either NAND or NOR gate.

1. **ABC + D' + E'**
2. **ABC + DE**

Q No. 06 Use a Karnaugh map to minimize the following standard SOP expression and design circuit on trainer.

$$A\bar{B}C + \bar{A}BC + \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C}$$

Q No. 07 Use a Karnaugh map to minimize the following standard POS expression and design circuit on trainer.

$$(B + C + D)(A + B + \bar{C} + D)(\bar{A} + B + C + \bar{D})(A + \bar{B} + C + D)(\bar{A} + \bar{B} + C + D)$$

Quote of the week

May you get all that you really deserve, be polite and observe, Give your best, and speak your mind, Success, You will definitely find, all the best!