Lab#3 Task

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Task#1

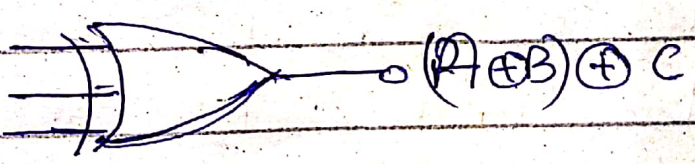
3 input XOR and XNOR Gates, Truth table and circuit diagram

3-input XOR Gate

Truth table

A	B	$A \oplus B$	C	$(A \oplus B) \oplus C$
0	0	0	0	0
0	0	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1

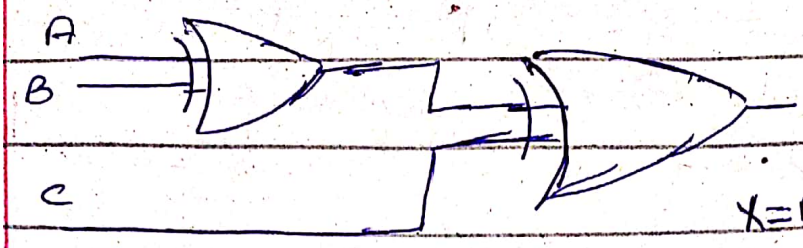
Symbol:



boolean expression.

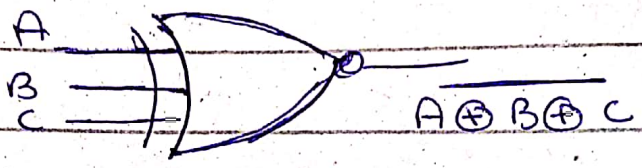
$(A \oplus B) \oplus C = A\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}C + ABC$

Circuit diagram of 3-XOR gate.



X-NOR Gate

Symbol:-



Boolean expression

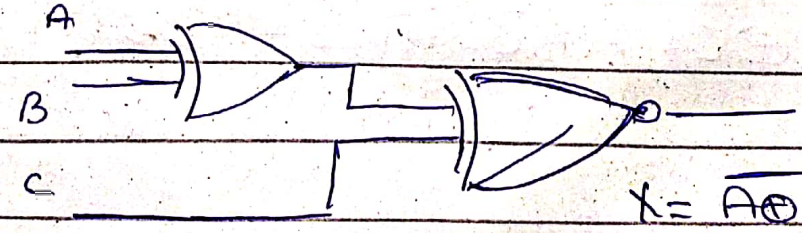
$$X = \overline{A \oplus B \oplus C} \quad \text{OR}$$

$$X = \bar{A}\bar{B}C + A\bar{B}\bar{C} + A\bar{B}C + \bar{A}BC$$

Truth table

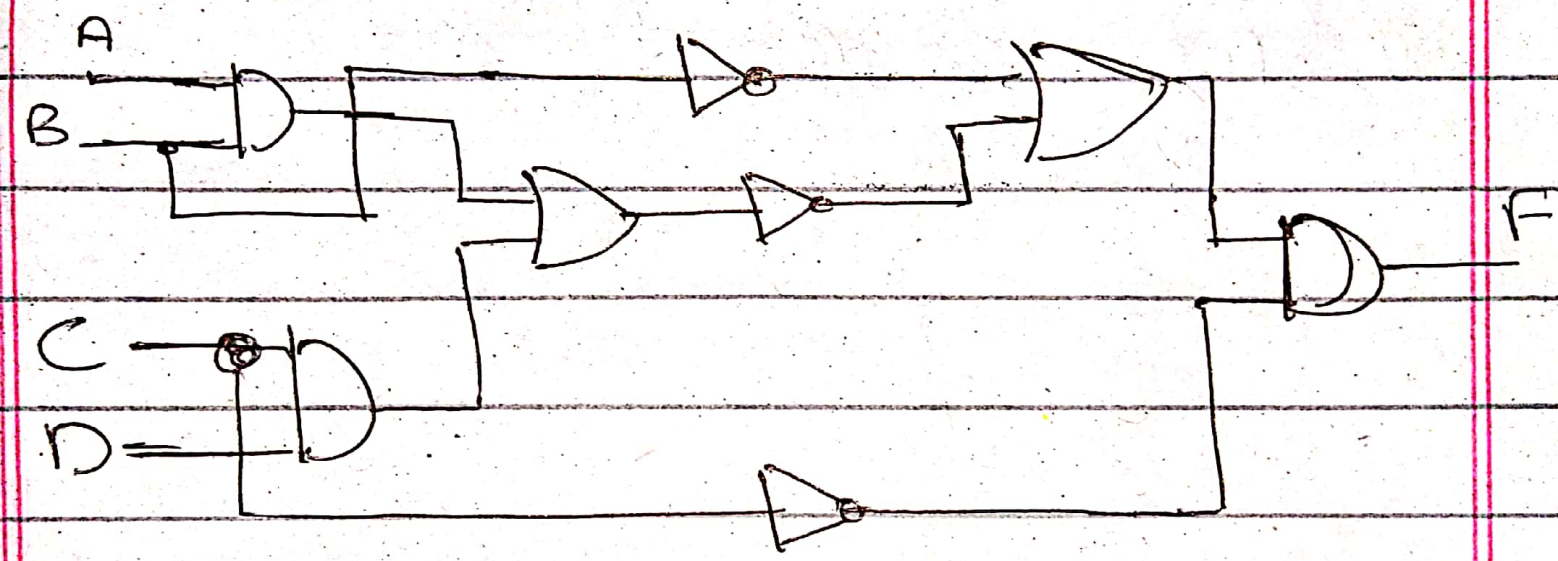
A	C	B	A⊕B	A⊕B⊕C	$\overline{A \oplus B \oplus C}$
0	0	0	0	0	1
0	1	0	0	1	0
0	0	1	1	1	0
0	1	1	1	0	1
1	0	0	1	1	0
1	1	0	0	0	1
1	0	1	1	0	1
1	1	1	1	1	0

circuit diagram



Task #2.

Write Boolean expression of logic circuit.



1st step. $(A \cdot B)$, $(C \cdot D)$

2nd " $(A \cdot B) + (C \cdot D)$

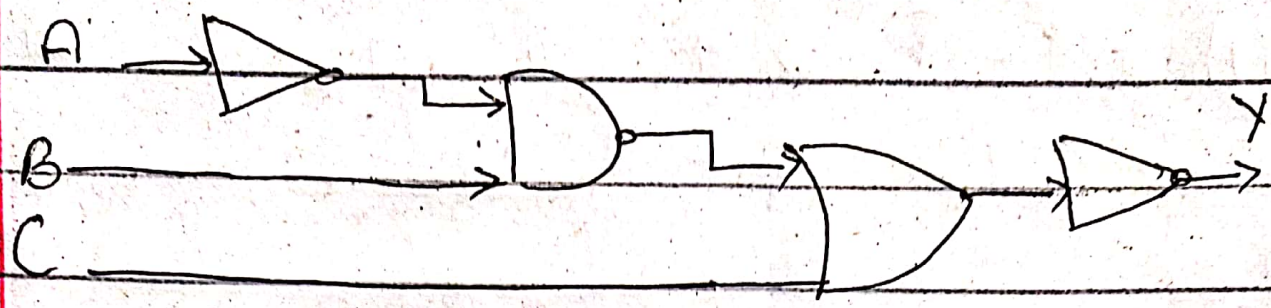
3rd " $\overline{C}$, $\overline{B}$, $\overline{(A \cdot B) + (C \cdot D)}$

4th " $\overline{(A \cdot B) + (C \cdot D)} + \overline{B}$.

5th step. $\overline{\left(\overline{(A \cdot B) + (C \cdot D)} + \overline{B}\right) \cdot \overline{C}}$

boolean expression

Task #3.



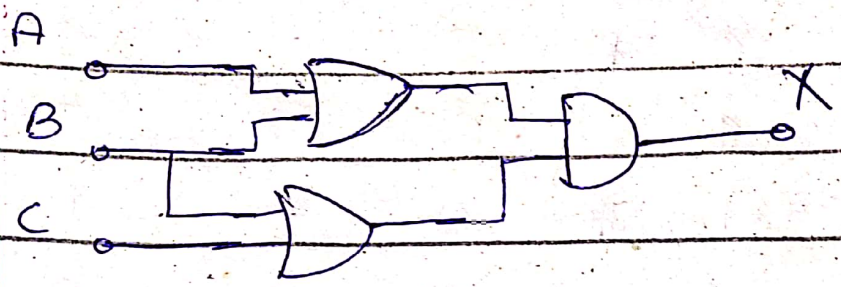
A	B	C	A'	$A \cdot B$	$(A \cdot B)'$	$(A \cdot B)' + C$	$((A \cdot B)' + C)'$
0	0	0	1	0	1	1	0
0	0	1	1	0	1	1	0
0	1	0	1	0	1	1	0
0	1	1	1	0	1	1	0
1	0	0	0	0	1	1	0
1	0	1	0	0	1	1	0
1	1	0	0	0	1	1	0
1	1	1	0	0	1	1	0

Boolean Expression.

$$\left((A' \cdot B)' + (A \cdot B)' + C \right)'$$

Task #4

1. $(A+B).(B+C)$.



Truth table

A	B	C	A+B	B+C	(A+B).(B+C)
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	1	1
0	1	1	1	1	1
1	0	0	1	0	0
1	0	1	1	1	1
1	1	0	1	1	1
1	1	1	1	1	1

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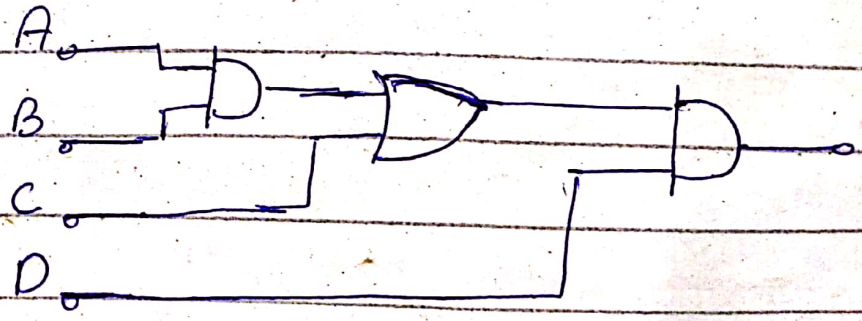
2. $(AB+C)\,D$.

circuit diagram.

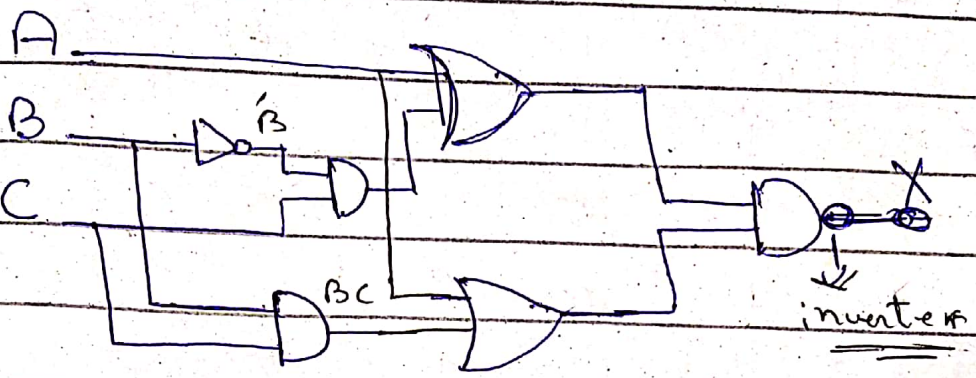


Truth Table

A (8)	B (4)	C (2)	D (1)	AB	AB+C	(AB+C).D
0	0	0	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	0	0	0
0	1	0	1	0	0	0
0	1	1	0	0	1	0
0	1	1	1	0	1	1
1	0	0	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	0	1	0
1	0	1	1	0	1	1
1	1	0	0	1	1	0
1	1	0	1	1	1	0
1	1	1	0	1	1	0
1	1	1	1	1	1	1

3. $((A+B'C).(A+BC))'$

Circuit diagram



Truth table

B'	A	B	C	BC	B'C	A+B'C	A+BC	(A+B'C).(A+BC)
1	0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0	0
0	0	1	0	0	0	0	0	0
0	0	1	1	1	0	0	1	0
1	1	0	0	0	0	1	1	1
1	1	0	1	0	1	1	1	1
0	1	1	0	0	0	1	1	1
0	1	1	1	1	0	1	1	1

$((A+B'C).(A+BC))'$

1
1
1
1
0
0
0
0

4. $A'BC + AB'C + ABC' + (ABC)''$

circuit diagram

A	B	C	A'	B'	C'	BC	A'B'
0	0	0	1	1	1	0	0
0	0	1	1	1	0	0	0
0	1	0	1	0	1	0	0
0	1	1	1	0	0	1	0
1	0	0	0	1	1	0	1
1	0	1	0	1	0	0	1
1	1	0	0	0	1	0	0
1	1	1	0	0	0	1	0

A·B	AB'C	A'BC	ABC'	A·B·C
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	1	0	0
0	0	0	0	0
0	1	0	0	0
1	0	0	1	0
1	0	0	0	1

$(A \cdot B \cdot C)'$ $(ABC)' + ABC'$ $A'BC + AB'C$

1 1 0

1 1 0

0 0 1

1 0 0

0 0 0

$(A'BC + AB'C) + (ABC' + (ABC)')$

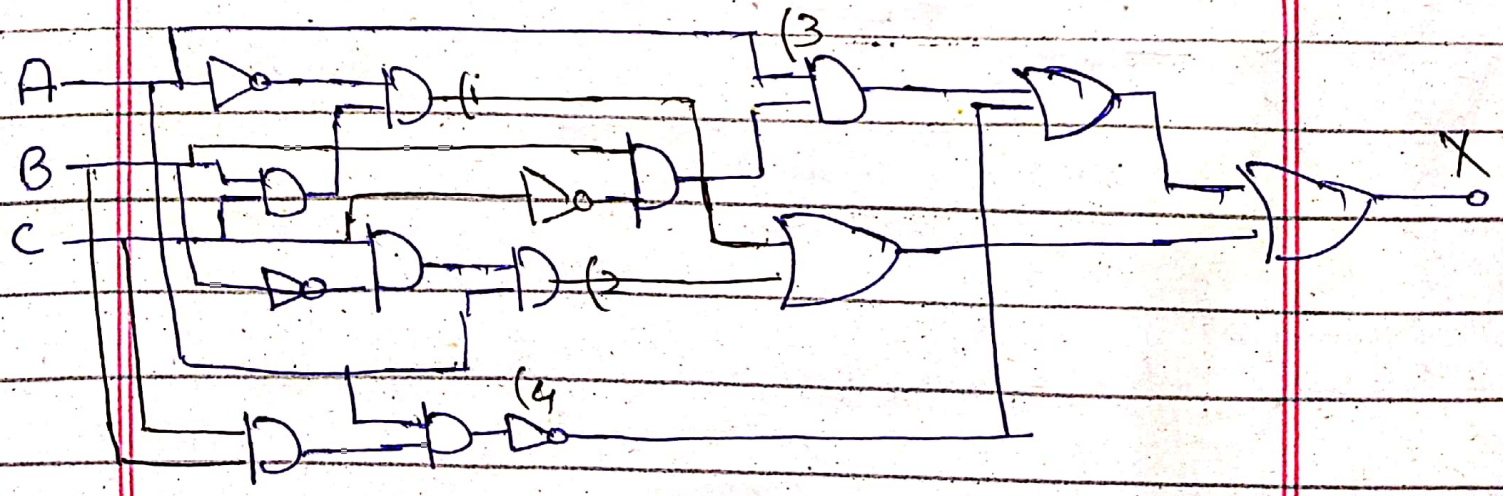
1

1

1

0

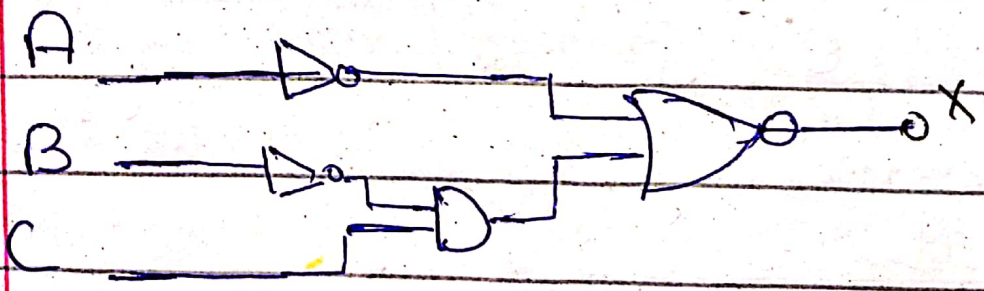
circuit diagram.



5. $(A' + B'C)'$

4	2	1					
A	B	C	A'	B'	B'C	A'+B'C	(A'+B'C)'
0	0	0	1	1	0	1	0
0	0	1	1	1	1	1	0
0	1	0	1	0	0	1	0
0	1	1	1	0	0	1	0
1	0	0	0	1	0	0	1
1	0	1	0	1	1	0	1
1	1	0	0	0	0	0	1
1	1	1	0	0	0	0	1

Circuit diagram.



Task # 5.

i) Use Nand and NOR gates

ii) Given diagram of figure 9.