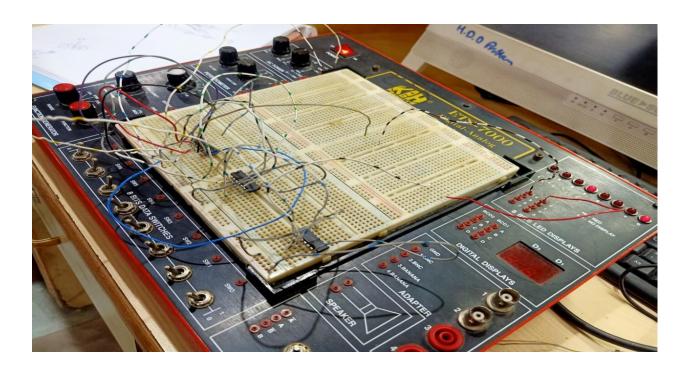
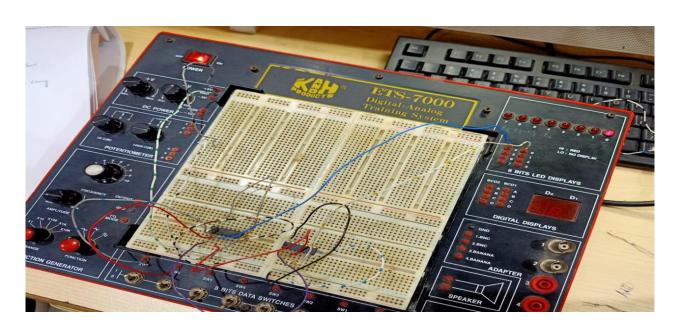
Roll no- 20k-0409

Name: Mukand Krishna

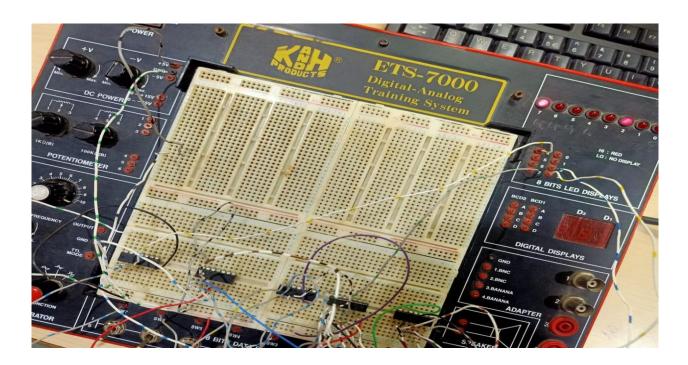
Q 1 - Full adder circuit.



Q 2 – Half adder circuit



Q3-2*2 Bit Multiplier



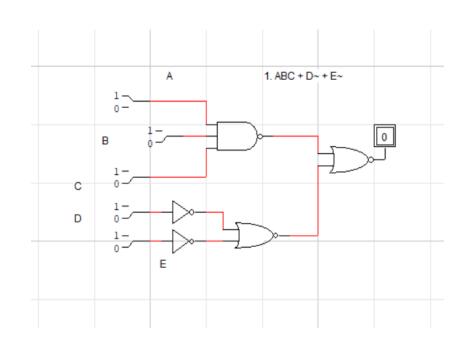
Q 4 – Half Subtractor



Q5. Design circuit on trainer for given expressions by using either NAND or NOR gate

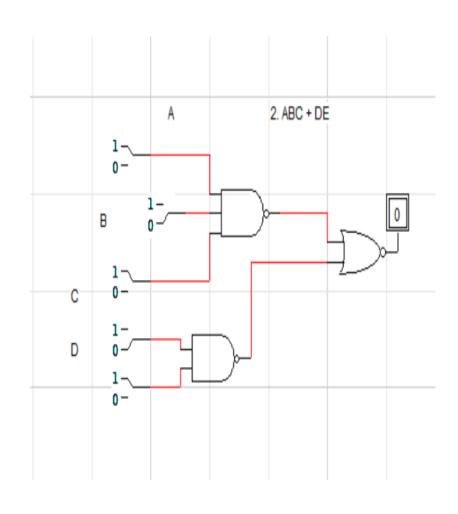
Part 1 <u>ABC + D~ + E~</u>

Α	В	С	D	E	ABC +D~+E~
0	0	0	0	0	0
0	0	0	0	1	0
0	0	0	1	0	0
0	0	0	1	1	0
0	0	1	0	0	0
0	0	1	0	1	0
0	0	1	1	0	0
0	0	1	1	1	0
0	1	0	0	0	0
0	1	0	0	1	0
0	1	0	1	0	0
0	1	0	1	1	0
0	1	1	0	0	0
0	1	1	0	1	0
0	1	1	1	0	0
0	1	1	1	1	0
1	0	0	0	0	0
1	0	0	0	1	0
1	0	0	1	0	0
1	0	0	1	1	0
1	0	1	0	0	0
1	0	1	0	1	0
1	0	1	1	0	1
1	0	1	1	1	0
1	1	0	0	0	0
1	1	0	0	1	1
1	1	0	1	0	0
1	1	0	1	1	0
1	1	1	0	0	1
1	1	1	0	1	1
1	1	1	1	0	1
1	1	1	1	1	0



Part 2. <u>ABC + DE</u>

Α	В	С	D	E	ABC +DE
0	0	0	0	0	0
0	0	0	0	1	0
0	0	0	1	0	0
0	0	0	1	1	0
0	0	1	0	0	0
0	0	1	0	1	0
0	0	1	1	0	0
0	0	1	1	1	0
0	1	0	0	0	0
0	1	0	0	1	0
0	1	0	1	0	0
0	1	0	1	1	0
0	1	1	0	0	0
0	1	1	0	1	0
0	1	1	1	0	0
0	1	1	1	1	0
1	0	0	0	0	0
1	0	0	0	1	0
1	0	0	1	0	0
1	0	0	1	1	0
1	0	1	0	0	0
1	0	1	0	1	0
1	0	1	1	0	0
1	0	1	1	1	0
1	1	0	0	0	0
1	1	0	0	1	0
1	1	0	1	0	0
1	1	0	1	1	0
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1	1	1	0	1	0
1	1	1	1	0	0
1	1	1	1	1	1

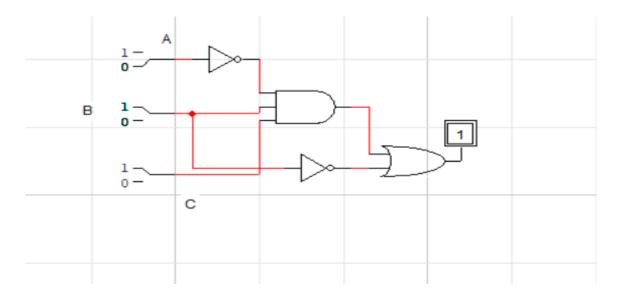


Q 6 Use a Karnaugh map to minimize the following standard SOP expression and design circuit on trainer.

Positioning 1's in the k map

	B~C~	B~C	ВС	BC~
A~	1	1	1	
Α	1	1		

Simplified expression: B~ + A~BC



Q7. Use a Karnaugh map to minimize the following standard POS expression and design circuit on trainer.

$$(B+C+D) (A+B+C^*+D) (A^*+B+C+D^*) (A^*+B+C+D^*) (A+B^*+C+D) (A^*+B^*+C+D)$$
 $(AA^*+B+C+D) (A+B+C^*+D) (A^*+B+C+D^*) (A^*+B+C+D^*) (A+B^*+C+D) (A^*+B^*+C+D)$
 $(A+B+C+D) (A^*+B+C+D) (A+B+C^*+D) (A^*+B+C+D^*) (A^*+B+C+D^*) (A+B^*+C+D) (A^*+B^*+C+D)$
Positioning 0's in the k map

	C+D	C+D ~	C~+D~	C~+D
A+B	0	0		
A+B~	0	0		0
A~+B~				
A~+B	0			
		<u> </u>	<u> </u>	<u> </u>

Simplified expression: (A + C) (A $^{\sim}$ + B + C + D $^{\sim}$) (A + B $^{\sim}$ + C + D)

