Day / Date

DLD

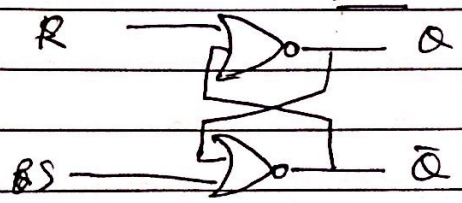
20K-1077

Lab 11

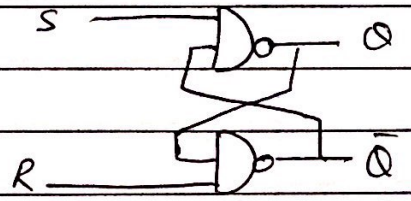
Maleeha Khan

Lab Task #1

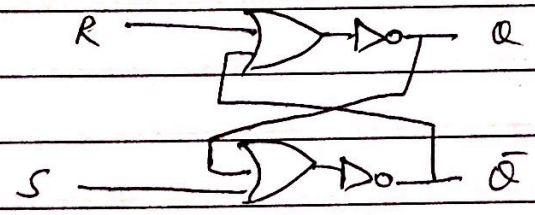
NOR



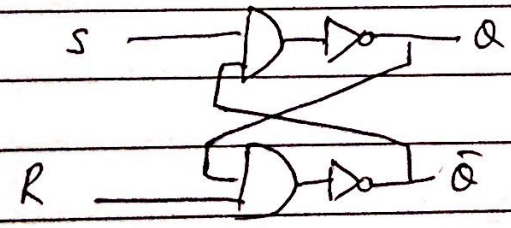
NAND



NOR gate
Using logic gates :-

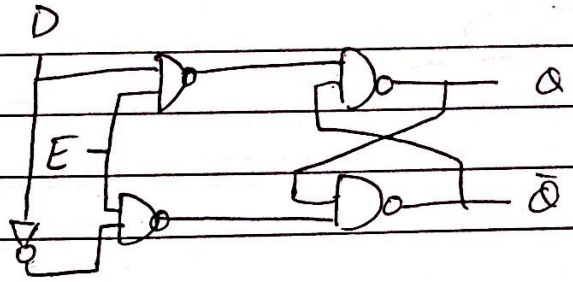


NAND using logic gates :-

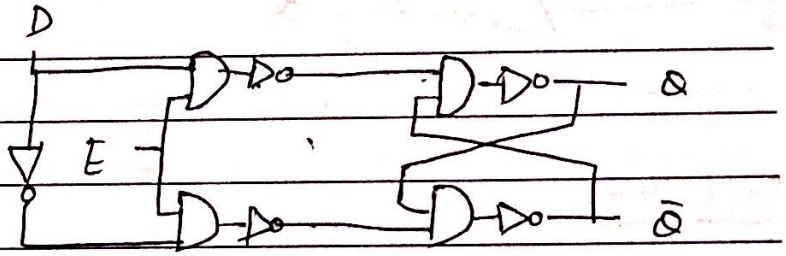


Lab Task #2

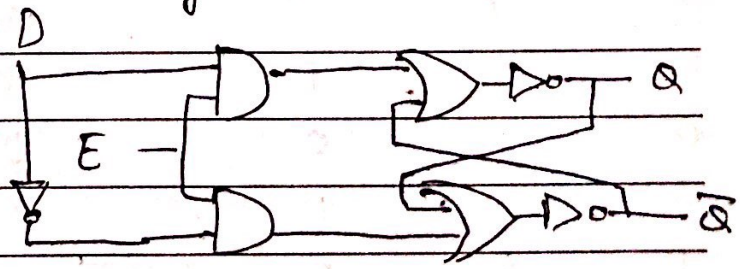
D latch



D latch using And and not:



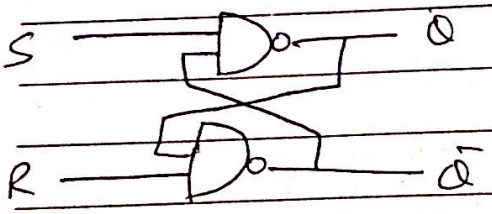
D latch using OR and not:



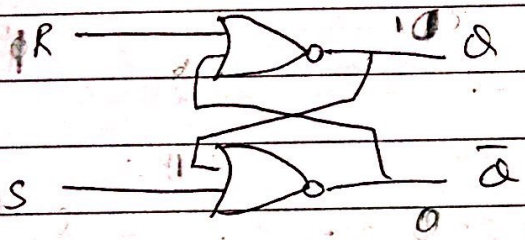
Day / Date

TASK #3

NAND



NOR



Task #4

S	R	Q_n	Q	$\bar{Q}$	
0	0	0	Memory		
0	0	1	Memory		
0	1	0	0	1	Reset
0	1	1	Invalid		
1	0	0	1	0	set
1	0	1	Invalid		
1	1	0	Invalid		
1	1	1	Invalid		