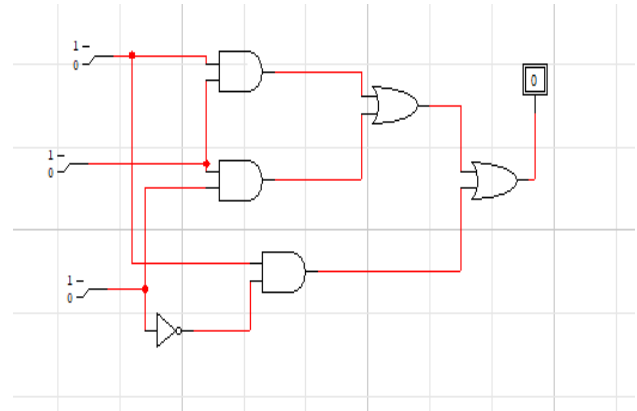


Roll no: 20k-0409

Name: MUKAND KRISHNA

EXAMPLE

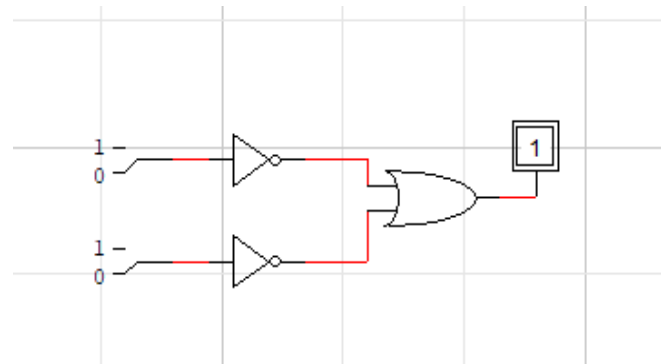
A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1



CIRCUIT# 1

A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

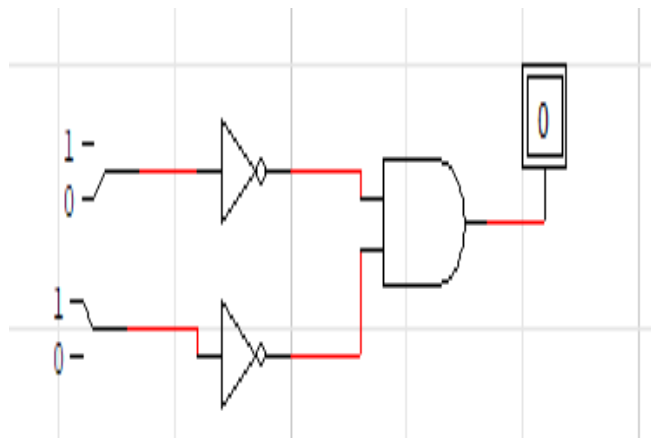
$$Z = A' + B'$$



CIRCUIT# 2

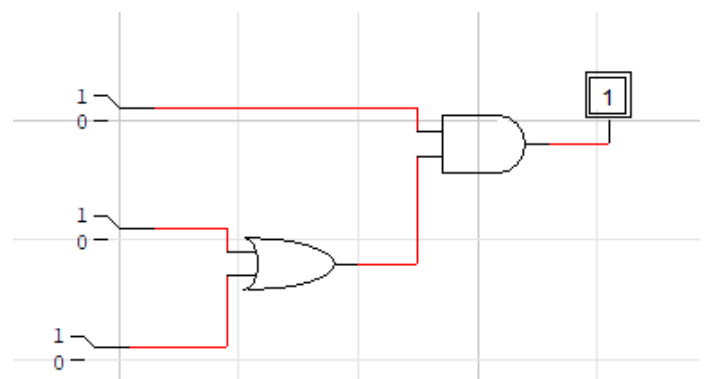
A	B	Z
0	0	1
0	1	0
1	0	0
1	1	0

$$Z = A' \cdot B'$$



CIRCUIT#3

Boolean Expression: $Z = A \cdot (B + C)$



CIRCUIT# 4

BOOLEAN EXPRESSION: $Z = A + (B.C)$

CIRCUIT# 5

EXPRESSION: $Z = (A.B) + (A.C)$

CIRCUIT# 6

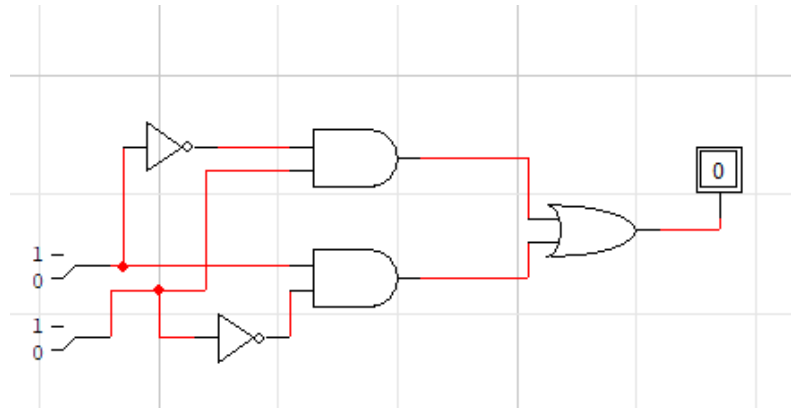
EXPRESSION: $Z = (A.B).B'$

CIRCUIT# 7

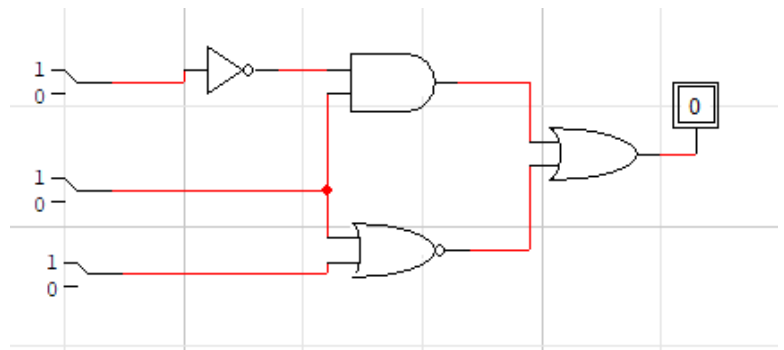
EXPRESSION: $Z = (A.B) + (C.D)$

CIRCUIT# 8 ----->>>>

EXPRESSION: $Z = (A.B') + (A'.B)$

**LOGIC CIRCUIT DIAGRAM**

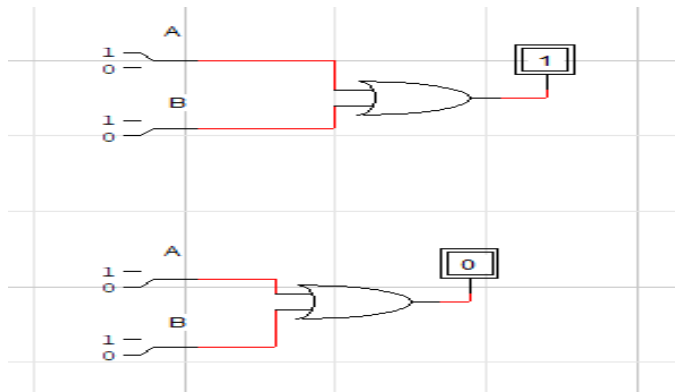
EXPRESSION: $Z = (A \sim . B) + (B + C) \sim$



A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

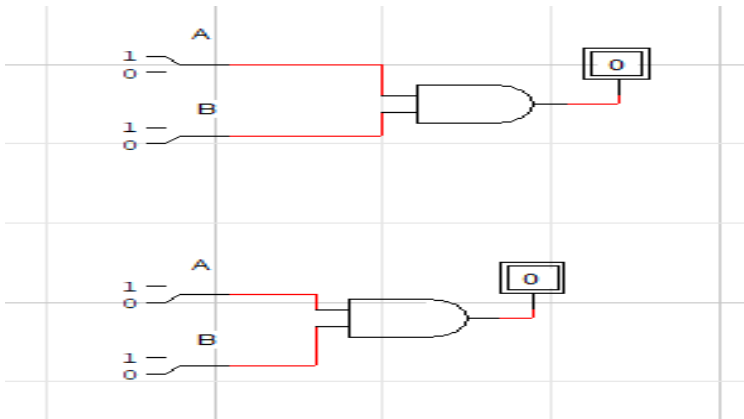
COMMUTATIVE LAW

ADDITION: $a + b = b + a$



A	B	A+B	A	B	B+A
0	0	0	0	0	0
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	1

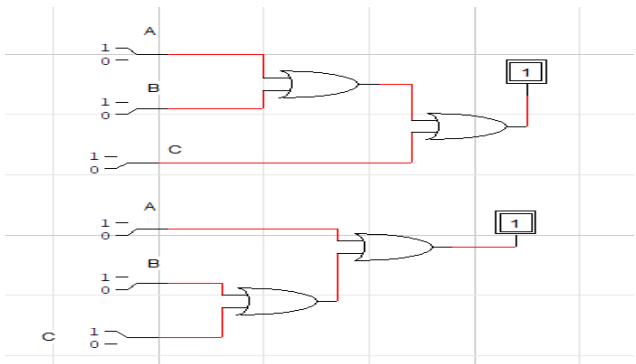
MULTIPLICATION: $ab = b.a$



A	B	A.B	A	B	A.B
0	0	0	0	0	0
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	1	1	1

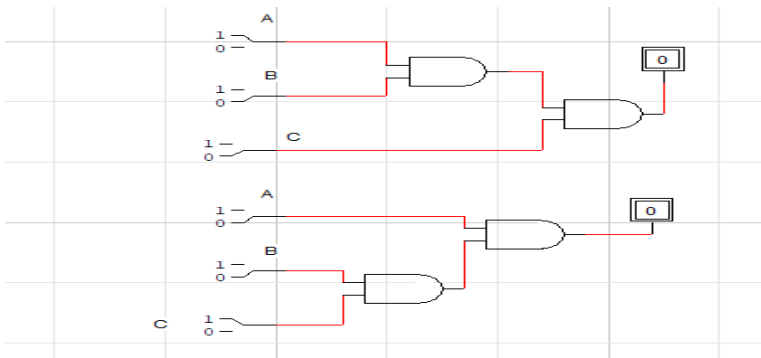
Associative law

ADDITION: $a + (b + c) = (a + b) + c$



A	B	C	(a+b)+c	A	B	C	a+(b+c)
0	0	0	0	0	0	0	0
0	0	1	1	0	0	1	1
0	1	0	1	0	1	0	1
0	1	1	1	0	1	1	1
1	0	0	1	1	0	0	1
1	0	1	1	1	0	1	1
1	1	0	1	1	1	0	1
1	1	1	1	1	1	1	1

MULTIPLICATION: $a(bc) = (a.b)c$

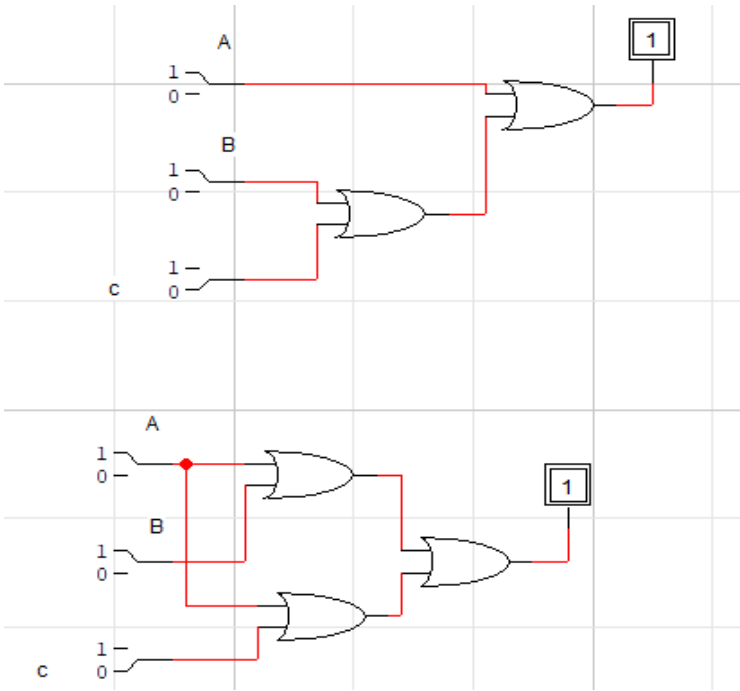
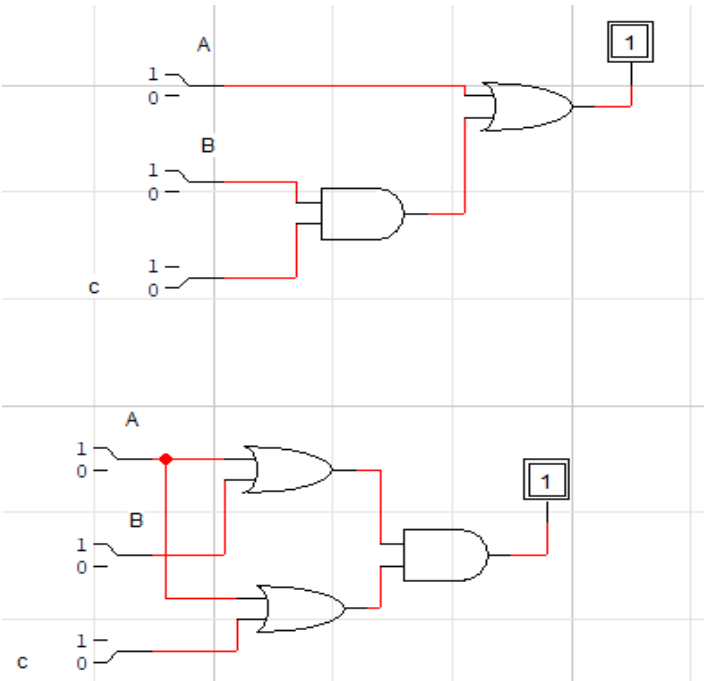


A	B	C	(a.b).c	A	B	C	(a.b)c
0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0
0	1	0	0	0	1	0	0
0	1	1	0	0	1	1	0
1	0	0	0	1	0	0	0
1	0	1	0	1	0	1	0
1	1	0	0	1	1	0	0
1	1	1	1	1	1	1	1

Distributive Law

Addition: $A+(B+C) = (A+B)+(A+C)$

Multiplication: $A+(B.C)=(A+B).(A+C)$



A	B	C	$A+(B+C)$	A	B	C	$(A+B)+(A+C)$
0	0	0	0	0	0	0	0
0	0	1	1	0	0	1	1
0	1	0	1	0	1	0	1
0	1	1	1	0	1	1	1
1	0	0	1	1	0	0	1
1	0	1	1	1	0	1	1
1	1	0	1	1	1	0	1
1	1	1	1	1	1	1	1

A	B	C	$A+(B.C)$	A	B	C	$(A+B).(A+C)$
0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0
0	1	0	0	0	1	0	0
0	1	1	1	0	1	1	1
1	0	0	1	1	0	0	1
1	0	1	1	1	0	1	1
1	1	0	1	1	1	0	1
1	1	1	1	1	1	1	1

Lab# 3 tasks

1. Design 3 input XOR and XNOR gate. Truth table, draw the circuit diagram.

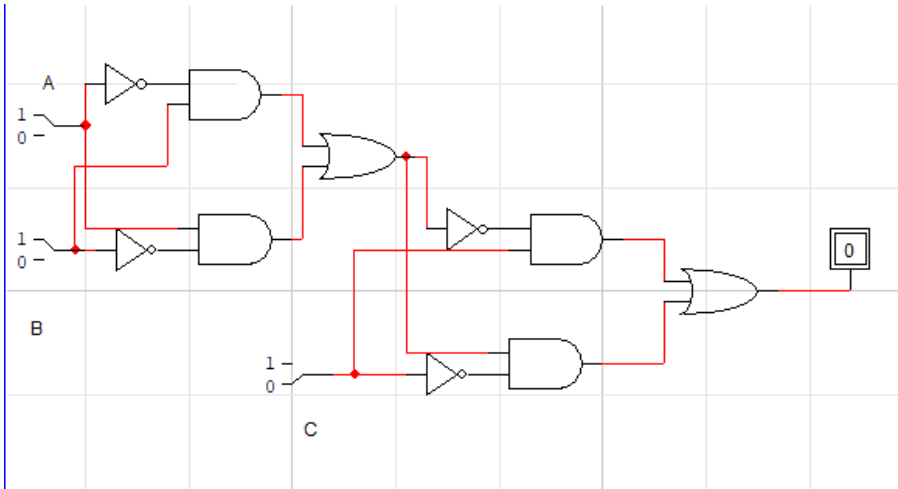
Truth Table

A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

using **and, or gate**

A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

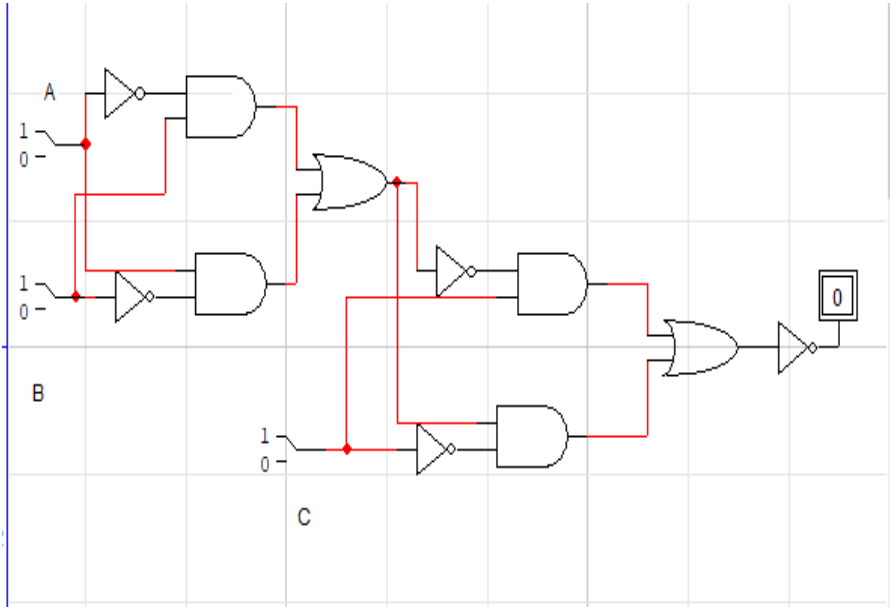
Circuit diagram of XOR gate using and, or gate



Boolean Expression: $X = ABC + A'B'C + AB'C' + A'BC'$

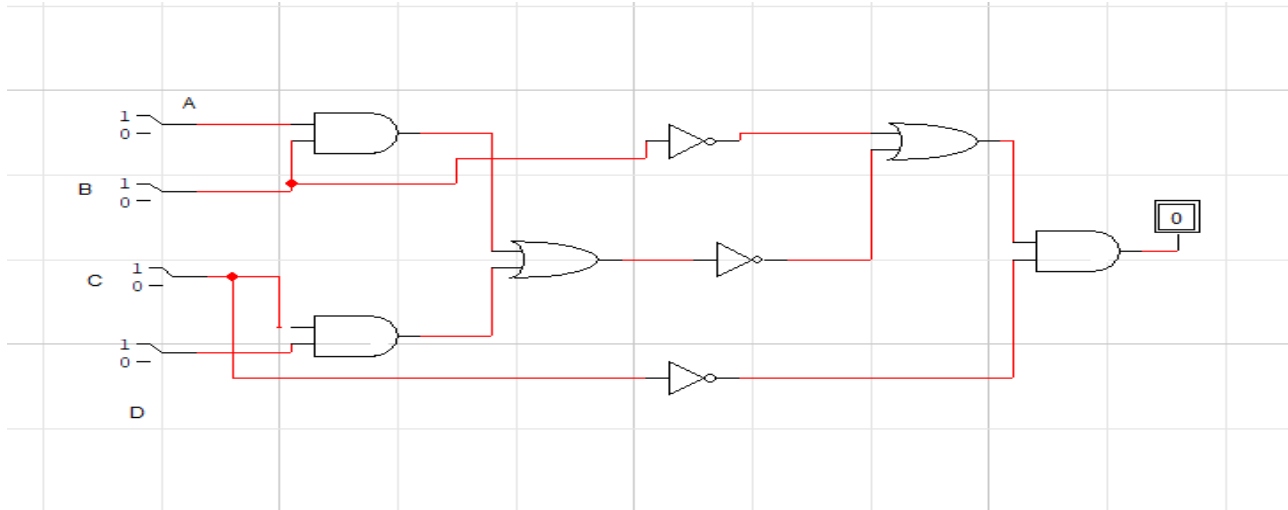
Truth Table

Circuit diagram of XNOR gate



Boolean Expression: $X = (ABC + A'B'C + AB'C' + A'BC') \sim$

2. Implement the following logic circuit on logic trainer, and write Boolean Expression.



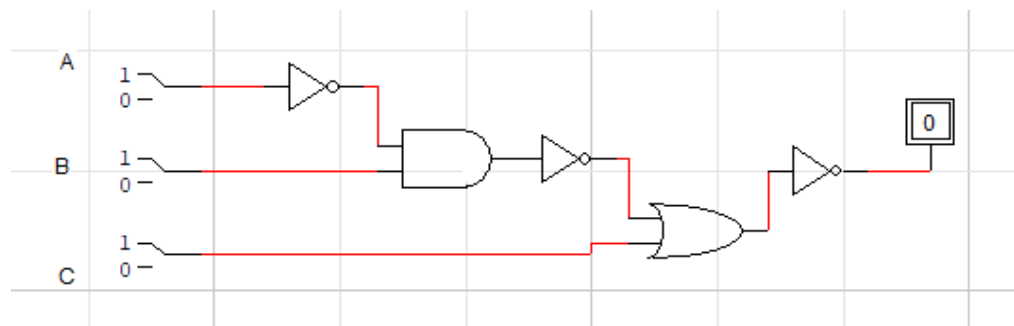
Boolean Expression: $X = (A.B) + (C.D) \sim + B \sim . C \sim$

3. Write the Boolean expression and draw Truth tables

Truth Table

A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Circuit Diagram



Boolean Expression: $((A \sim . B) \sim + C) \sim$

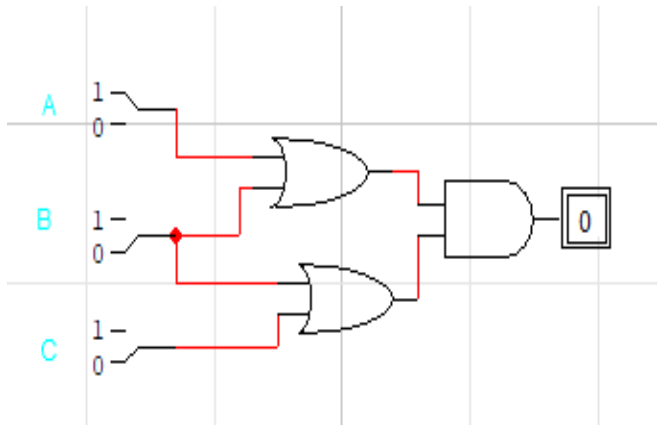
4. Draw a circuit diagram corresponding to the following Boolean expression and implement it.

Circuit # 1: Boolean Expression: $(A + B) \cdot (B + C)$

Truth table

A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Circuit Diagram

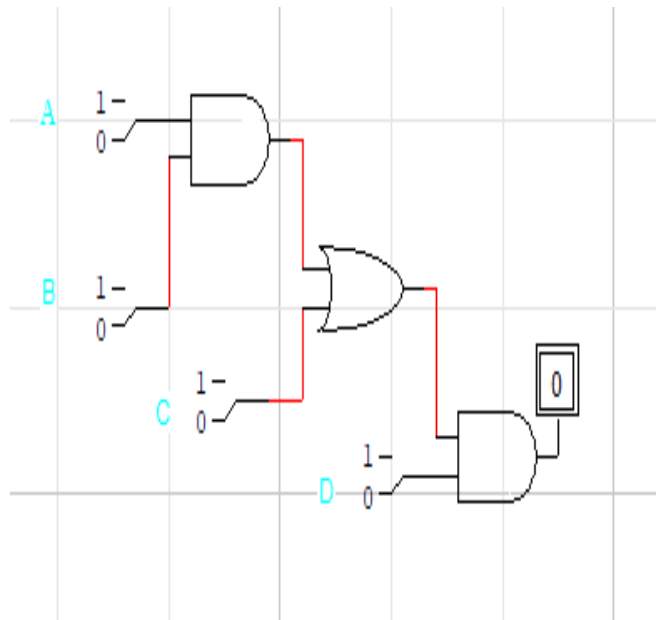


Circuit # 2: Boolean Expression: $(AB + C)D$

Truth table

A	B	C	D	X
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

Circuit Diagram

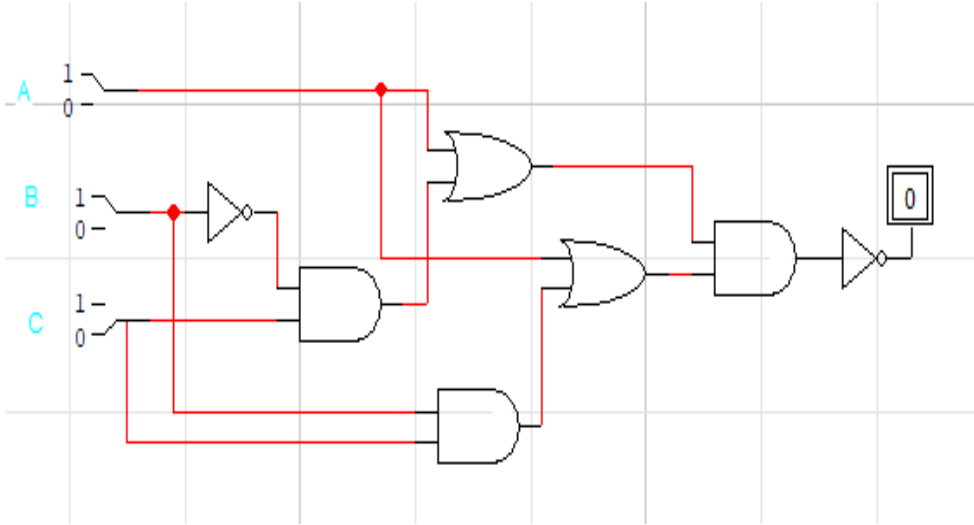


Circuit # 3: Boolean Expression: $((A + B\sim C)(A + BC))\sim$

Truth table

A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Circuit Diagram

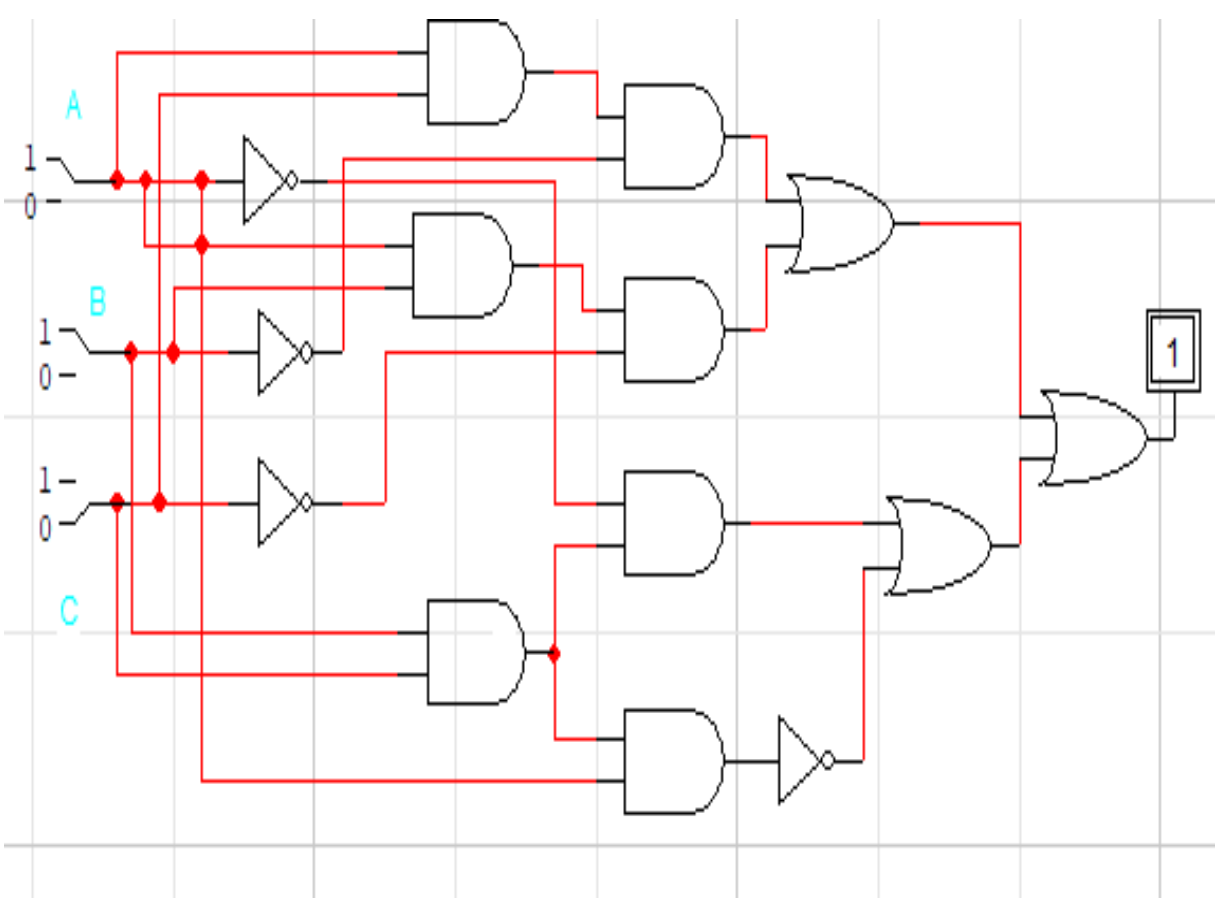


Circuit # 4: Boolean Expression: $A'BC + AB'C + ABC' + (ABC)'$

Truth table

A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Circuit Diagram

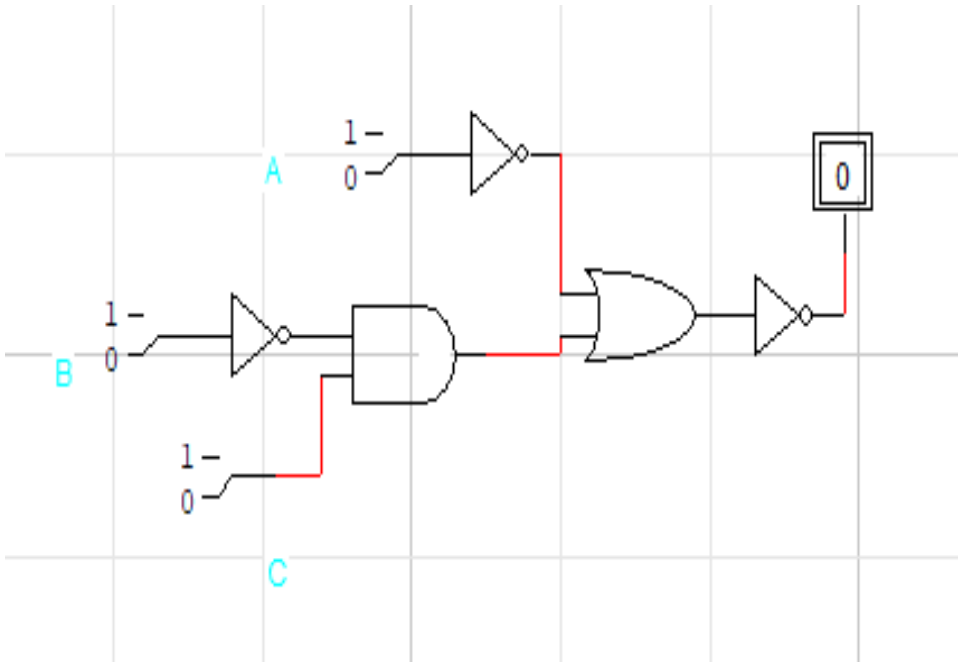


Circuit # 5: Boolean Expression: $(A\sim + BC)\sim$

Truth table

A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Circuit Diagram



5. Transform the given diagram circuit to new logic diagram using NAND /NOR gates. Implement the transformed logic circuit.

Circuit Diagram

