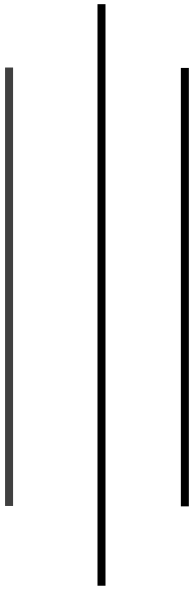
FARWESTERN UNIVERSITY

Mahendranagar, Kanchanpur

Digital Clock

Project Report



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Submitted By:

- **Mukesh Pant (29)**
- **Adarsh Joshi (2)**
- **Anil Chandra Giri (3)**
- **Dinesh Prasad Joshi (18)**

Submitted To:

Er. Kamal Lekhak

Assistant Professor

Far-Western University

Acknowledgement

I wish to express my sincere appreciation to the individuals and resources that played a pivotal role in bringing this project, "**Digital Clock**" to fruition.

First and foremost, I extend my heartfelt gratitude to my project supervisor, Er. Kamal Lekhak Sir, whose unwavering support and guidance were instrumental in shaping the project's direction and ensuring its successful execution.

I also want to acknowledge the invaluable role played by Multisim Software for providing a powerful simulation tool. This software, with its user-friendly interface and robust capabilities, greatly facilitated the design and validation process, contributing significantly to the project's success.

This report stands as a testament to the collective efforts of the individuals and resources mentioned, without whom this project would not have been possible.

ABSTRACT

This project report delves into the design, development, and implementation of a digital clock system. The study focuses on creating an accurate and user-friendly digital timekeeping solution using digital electronics and programming techniques. Through the utilization of microcontroller technology and LED display modules, the project achieves precise timekeeping and visually appealing digital display. The report outlines the objectives, methodology, and technical details of the digital clock, highlighting its functionalities and features. The findings demonstrate the successful realization of a functional digital clock, showcasing its reliability and efficiency. This project contributes to the realm of digital electronics and programming, providing practical insights into clock design in the digital era. The report concludes with suggestions for potential enhancements and real-world applications, emphasizing the significance of digital clocks in modern timekeeping systems.

TABLE OF CONTENT

INTRODUCTION

➔ In an increasingly digital world, the ubiquitous presence of clocks and timekeeping devices cannot be overstated. From the humble alarm clock by our bedside to the synchronized time systems that govern our daily lives, the importance of accurate timekeeping cannot be underestimated. This report delves into the realm of digital clock simulation, focusing on the utilization of counters as a fundamental component in the creation of digital timekeeping systems.

The concept of a digital clock may seem commonplace, but beneath its simple facade lies a complex interplay of digital electronics and mathematical precision. This report aims to provide an in-depth exploration of the design, simulation, and functionality of digital clocks built upon counter circuits. By understanding the inner workings of these systems, we gain valuable insights into not only the core principles of timekeeping but also the broader field of digital electronics and its applications.

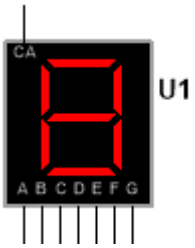
Throughout this report, we will embark on a journey through the fundamental theory of digital counters, their application in clock circuits, and the intricacies of clock signal generation. We will explore the various types of counters, such as binary counters and decade counters, and how they contribute to the accurate representation of time in a digital format.

By the end of this report, readers will have a comprehensive understanding of how digital clocks, driven by counter circuits, function and can be simulated for testing and validation. This knowledge not only serves as a valuable educational resource but also as a foundation for anyone interested in the fascinating world of digital electronics and timekeeping technology.

7-Segment Display

➔ A 7-Segment Display consist of seven individual colored LED's (called the segments), within one single display package in order to produce the required numbers or HEX characters from 0 to 9 and A to F respectively. A standard 7-segment LED display generally has eight (8) input connections, one for each LED segment and one that acts as a common terminal or connection for all the internal display segments. Some single displays have also have an additional input pin to display a decimal point in their lower right or left hand corner. One or more such display are combined to display bigger numbers. This kind of display is generally used in digital clocks, calculators, wrist watches and many more electronic devices.

Following is the segment of 7-segment display:



In electronics there are two important types of 7-segment display;

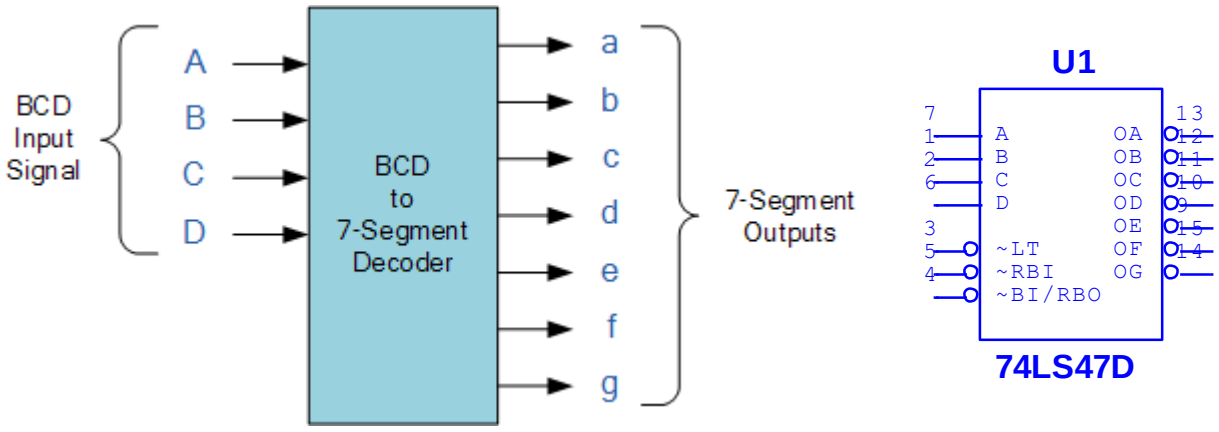
1. **The Common Cathode Display (CCD)** – In the common cathode display, all the cathode connections of the LED's are joined together to logic "0" or ground. The individual segments are illuminated by application of a "HIGH", logic "1" signal to the individual Anode terminals.

2. **The Common Anode Display (CAD)** – In the common anode display, all the anode connections of the LED's are joined together to logic "1" and the individual segments are illuminated by connecting the individual Cathode terminals to a "LOW", logic "0" signal.

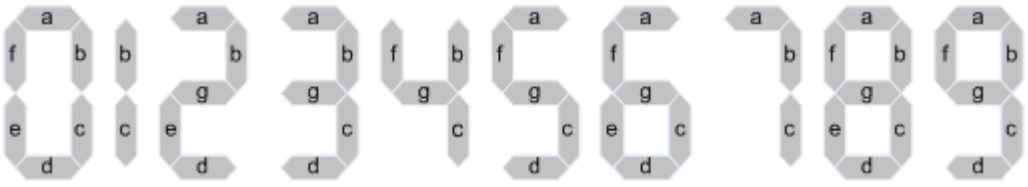
BCD TO 7-SEGMENT DISPLAY DECODER

➔ On the display the correct combination of LED segments need to be illuminated and BCD to 7-segment Display Decoders such as the 74LS47 do just that. A binary coded decimal (BCD) to 7-segment display decoder such as the TTL 74LS47 or 74LS48, have 4 BCD inputs and 7 output lines, one for each LED segment.

➔ This allows a smaller 4-bit binary number to be used to display all the decimal numbers from 0 to 9 and by adding two displays together, a full range of numbers from 00 to 99 can be displayed with just a single byte of eight data bits. Here A, B, C and D are binary inputs and OA, OB, OC, OD, OE, OF, OG are outputs which are connected to respected terminals of display.



7-Segment Display Elements for all Numbers:



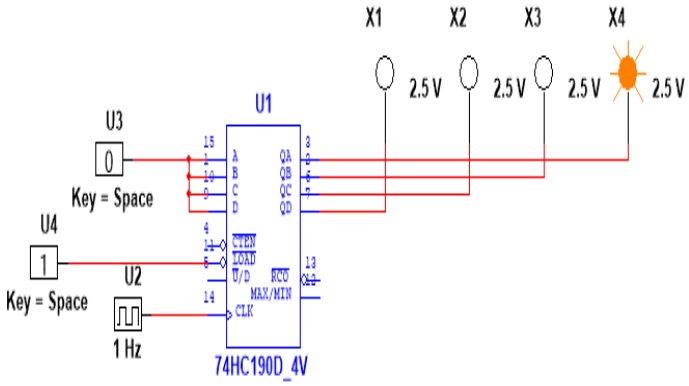
COUNTER

#MOD-10 counter (Decade counter) – A decade counter is a series type of digital counter which is designed to count ten digits. It performs the operation of resetting automatically when there is a new clock input signal. As the counter counts **ten unique combinations** of the applied input, it is termed a decade counter.

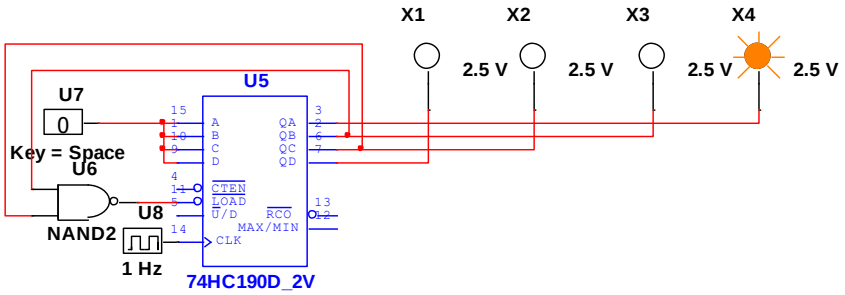
The values that a BCD counter counts are 0, 1, 2, 3, 4, 5, 6, 7, 8, and 9 in binary format. The counter which we used is 74HC190 which is a synchronous decade counter. In this counter IC A, B, C and D are load inputs which are connected to the individual flip-flops onside the counter, QB, QC and QD are the individual binary outputs representing the current count state in a four bit binary format.

CTEN is count enable, LOAD is used to whether enable or disable the counting, U'/D decides mode of counter whether it is up/down counter, CLK is clock signal, RCO is ripple clock output which can be used to cascade multiple counters as it serves as a way to signal when the counter is about to wrap around its maximum or minimum value and MAX/MIN output produces high pulse when the terminal the terminal count nine (1001) is reached in UP mode and count zero (0000) is reached in down mode.

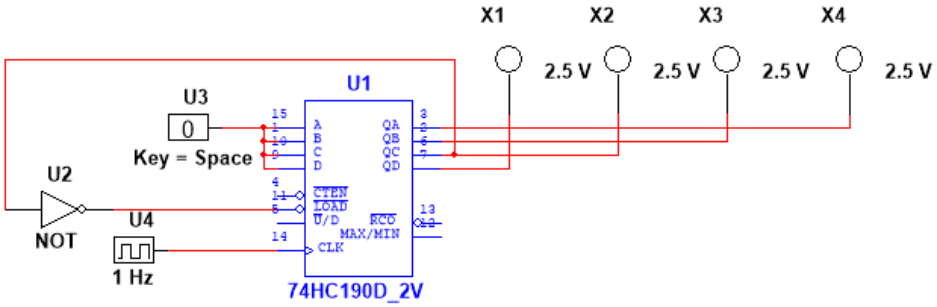
(NOTE: CTEN, LOAD and RCO are active low)



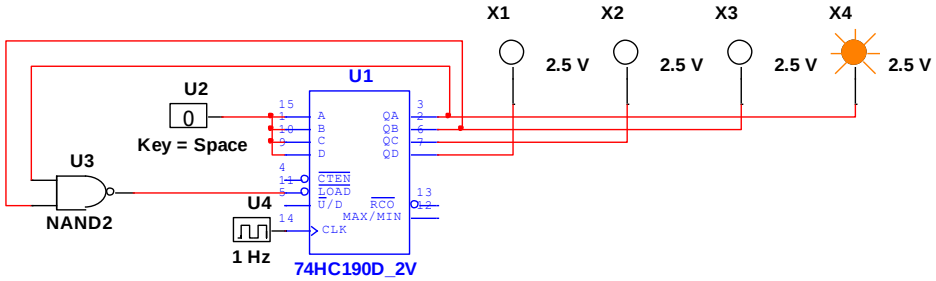
#MOD-6 counter –A modulo 6 (MOD-6) counter circuit can be made using a decade counter and feeding the NANDed output of QB and QC to the load so that whenever the count reaches **0110** i.e. 6 in decimal the count starts again from **0000** i.e. 0 in decimal.



#MOD-4 counter– A modulo 4 (MOD-4) counter circuit can be made using a decade counter and feeding the NOT output of QC to the load so that whenever the count reaches **0100** i.e. 4 in decimal the count starts again from **0000** i.e. 0 in decimal.

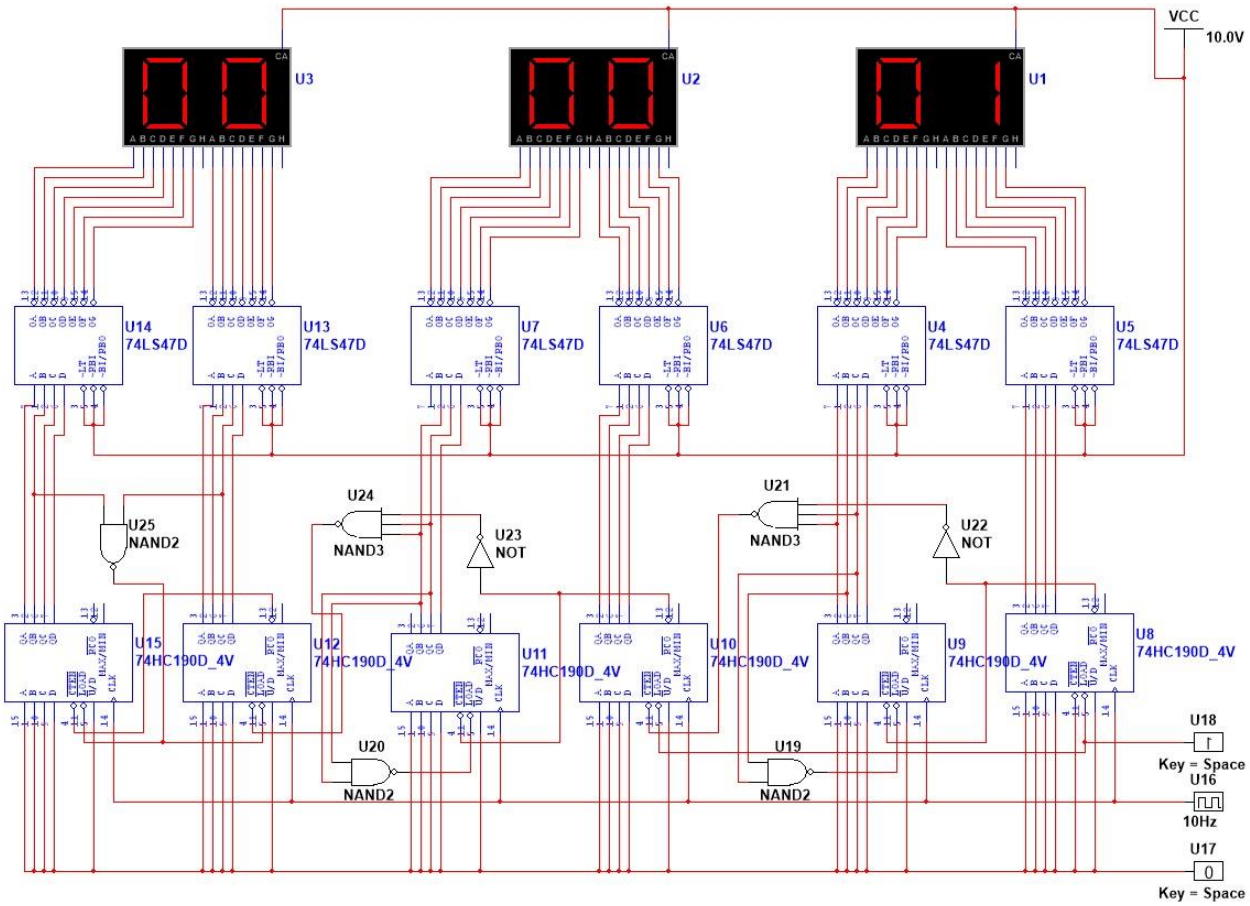


#MOD-3 counter – A modulo 3 (MOD-3) counter circuit can be made using a decade counter and feeding the NANDed output of QB and QC to the load so that whenever the count reaches 0011 i.e. 3 in decimal the count starts again from 0000 i.e. 0 in decimal.



WORKING MECHANISM

➔With the help of 7-segment display, BCD to 7-segment display decoder and counters we can simulate a digital clock as shown in figure below;



Here all together we need 6 displays so the working process is divided into six steps;

STEP 1: At first we setup first counter i.e. decade counter such that it counts 0-9 every second by providing clock signal with 1 Hz frequency, LOAD inputs A, B, C and D with low voltage (0), $\overline{\boldsymbol{LOAD}}$ with high voltage (1) and $\overline{\boldsymbol{CTEN}}$ with (0).

STEP 2: The second counter i.e. MOD-6 counter is setup such a way that the $\overline{\boldsymbol{RCO}}$ from first counter is connected to $\overline{\boldsymbol{CTEN}}$ of second

counter so that when the first counter wraps around its maximum to minimum value i.e. 9 to 0, second counter is enabled and QB and QC of the second counter are passed through NAND gate and connected to the $\overline{\boldsymbol{LOAD}}$ so that it resets when QB and QC become 1 i.e. count reaches 6 or 0110 in binary.

STEP 3: In third counter i.e. the decade counter NOT of $\overline{\boldsymbol{RCO}}$ and QB & QC from first counter are passed through NAND gate and connected to the complement of $\overline{\boldsymbol{CTEN}}$ so that when the count reaches 6 in second counter and 0 in first counter the third counter is enabled.

STEP 4: The forth counter i.e. MOD-6 counter is setup such a way that the $\overline{\boldsymbol{RCO}}$ from third counter is connected to $\overline{\boldsymbol{CTEN}}$ of forth counter so that when the third counter wraps around its maximum to minimum value i.e. 9 to 0, second counter is enabled and QB and QC of the second counter are passed through NAND gate and connected to the $\overline{\boldsymbol{LOAD}}$ so that it resets when QB and QC become 1 i.e. count reaches 6 or 0110 in binary.

STEP 5: In fifth counter i.e. MOD-4 counter NOT of $\overline{\boldsymbol{RCO}}$ and QB & QC from forth counter are passed through NAND gate and connected to $\overline{\boldsymbol{CTEN}}$ so that when the count reaches 6 in forth counter and 0 in third the fifth counter is enabled.

STEP 6: The sixth counter i.e. MOD-3 counter is setup such a way that the $\overline{\boldsymbol{RCO}}$ from fifth counter is connected to $\overline{\boldsymbol{CTEN}}$ of sixth counter so that when the fifth counter wraps around its maximum to minimum value i.e. 3 to 0, sixth counter is enabled.

(NOTE: $\overline{\boldsymbol{LOAD}}$ is given to fifth and sixth counter such a way that when the count reaches 2 in sixth counter and 4 in fifth counter they reset.)

Finally the outputs from the individual counters are connected to each BCD to 7-segment display decoder and further connected to each 7-segment displays.

CONCLUSION

➔ At last by combining all counters, decoders and displays a simulation of digital clock of 24 hour format is completed. Since the version of simulation tool i.e. multisim was old so due to some bugs we had to set frequency of the clock 10 Hz to change the count of counter by 1 secound.