MUKESH

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Leetcode Github

EDUCATION

- **National Institute of Technology, Silchar, Assam --** B.Tech in Electronics and Communication Engineering (ECE)
  July 2022 - June 2026 | CGPA: 8.34/10|| Gate Score : 561
- **Rajkiya Pratibha Vikas Vidyalaya, Lajpat Nagar, Delhi --** CBSE Class XII
  July 2019 - June 2021 | 90.2%
- **Government Boys' Senior Secondary School, Delhi --** CBSE Class X
  July 2014 - June 2019 | 92.8%

WORK EXPERIENCE

Bharat Heavy Electricals Limited (BHEL) Varanasi May 2024- July 2024

- Responsibility: Analysed and assessed the processor integration within CNC machines to enhance performance and reliability.
- Learning: Acquired in-depth knowledge of the role of processors in controlling machining operations

PROJECTS

FIR Filter Optimization | Digital Design | Digital Signal Processing(Verilog) Github

- Engineered a FIR filter using Constant Shift Register (CSR) to reduce memory usage
- Optimized coefficient implementation via Canonical Signed Digit (CSD) to minimize multipliers
- Applied Binary Common Subexpression Elimination (BCSE) to reuse logic and reduce gate count
- Leveraged heuristic search to explore efficient coefficient mappings and structure sharing
- Implemented power optimization through clock gating and operand isolation techniques
- Validated functionality with a modular testbench and signal integrity analysis

Processing SoC on Zynq | Embedded Systems (Verilog) Github

- Engineered SoC leveraging Zynq processor with DMA, DDR, and AXI bus IP for high-speed data flow
- Designed custom line buffer and image processing IPs to blur and sharpen grayscale images in hardware
- Validated system performance with test images, achieving low-latency hardware acceleration

RTL-to-GDSII Flow for RISC-V 32-bit 5-Stage Pipeline Processor | VLSI Design Github

- Implemented and simulated a 5-stage pipelined RISC-V processor RTL in Vivado.
- Automated synthesis, placement, routing, and GDSII layout generation using OpenLane flow.
- Verified physical design integrity through LVS and DRC checks, enabling tape-out readiness.

6T SRAM Characterization | Cadence Virtuoso Github

- Designed a 4-bit CPU based on fundamental computer architecture principles, integrating modules such as ALU, Register File, Program Counter, Control Unit, and Instruction Memory
- Implemented core CPU operations including instruction fetch, decode, execute, and halt with a simple instruction set
- Enabled register-based arithmetic and logic operations with cycle-by-cycle simulation output
- Modularized the CPU design into reusable components, improving clarity and scalability for hardware simulation and testing

SKILLS AND COMPETENCIES

- **Languages:** SystemVerilog (including Assertions), Verilog, C, C++, Python, Tcl.
- **Tools:** Cadence Virtuoso, Vivado, Synopsys VCS, Mentor Questa, Git, vitis, ModelSim, OpenLane,
- **Operating Systems:** Linux, Windows, macOS.
- **Concept:** RTL design, SoC Design, RTL-to-GDSII, FSM, Image Processing, UVM, CPU Microarchitecture, Computer Architecture
- **Soft Skills:** Leadership, Event Management, Public Speaking, Time Management, Problem Solving, Team Collaboration.

CERTIFICATIONS

- **Physical VLSI design** : NPTEL
- **CMOS design** : NPTEL
- **C++** : Coursera
- **Arduino** : Coursera

EXTRA-CURRICULAR ACTIVITIES

Position of Responsibility

- Moderator, Literary Society, Illuminits, NIT Silchar - Content Writer & Event Manager

Awards – 2nd Prize, State Science Exhibition (2020), 1st Prize, Centre Science Exhibition (2019)

Interests – NSS, Poetry, Running, Kabaddi, Video Editing