Figure 20-26*b* illustrates the idea of one dominant lag network. In the midband the gain is high and the phase shift is 180°. One of the stages has a dominant lag network, so that the gain breaks at a low frequency and rolls off at 20 dB per decade. A decade above this frequency, the phase shift is 270°. It stays at approximately 270° until the gain crosses the horizontal axis at f_{unity}. Beyond this point, oscillations are impossible because the loop gain is less than unity.

With monolithic op amps, the dominant lag network is usually integrated on the chip and automatically provides the 20-dB roll-off until f_{unity} is reached. For instance, the 741 uses a 30-pF compensating capacitor that is part of a Miller lag network; the gain breaks at 10 Hz and rolls off at 20 dB per decade until an f_{unity} of 1 MHz is reached.

With uncompensated op amps like the 709, you have to add external resistors and capacitors to get this 20-dB roll-off; the manufacturer's data sheet tells you the sizes of R and C to use.

20-8 THE 555 TIMER

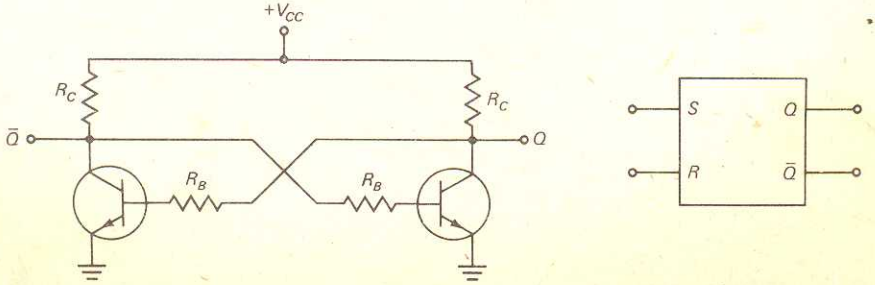
The 555 *timer* combines a relaxation oscillator, two comparators, an *RS* flip-flop, and a discharge transistor. This versatile IC has so many applications that it has become an industry standard. Once you understand how it works, you can join the many designers who are constantly finding new uses for this amazing IC.

RS FLIP-FLOP

Figure 20-27*a* shows a pair of cross-coupled transistors. Each collector drives the opposite base through a resistance R_B. In a circuit like this, one transistor is saturated and the other is cut off. For instance, if the right transistor is saturated, its collector voltage is approximately zero. This means no base drive for the left transistor, and so it goes into cutoff and its collector voltage approaches $+V_{CC}$. This high voltage produces enough base current to keep the right transistor in saturation.

On the other hand, if the right transistor is cut off, then its collector voltage drives the left transistor into saturation. The low collector voltage out of this left transistor then keeps the right transistor in cutoff.

Depending on which transistor is saturated, the Q output is either low or high. By adding more components to the circuit, we get an *RS flip-flop*, a circuit that can set



the Q output to high or reset it to low. Incidentally, a complementary (opposite) output $\overline{Q}$ is available from the collector of the other transistor.

Figure 20-27*b* shows the schematic symbol for an *RS* flip-flop of any design. Whenever you see this symbol, remember the action: The circuit latches in either of two states. A high S input sets Q to high; a high R input resets Q to low. Output Q remains in a given state until it is triggered into the opposite state.

BASIC TIMING CONCEPT

Figure 20-28*a* illustrates some basic ideas that we will need in our later discussion of the 555 timer. Assume that output Q is high. This saturates the transistor and clamps the capacitor voltage at ground. In other words, the capacitor is shorted and cannot charge.

The noninverting input voltage of the comparator is called the *threshold* voltage, and the inverting input voltage is referred to as the *control* voltage. With the *RS* flip-flop set, the saturated transistor holds the threshold voltage at 0. The control voltage, on the other hand, is fixed at +10 V because of the voltage divider.

Suppose we apply a high voltage to the R input. This resets the *RS* flip-flop. Output Q goes low and cuts off the transistor. Capacitor C is now free to charge. As the capacitor charges, the threshold voltage increases. Eventually, the threshold voltage becomes slightly greater than the control voltage (+10 V). The output of the comparator then goes high, forcing the *RS* flip-flop to set. The high Q output saturates the transistor, and this quickly discharges the capacitor. Notice the two

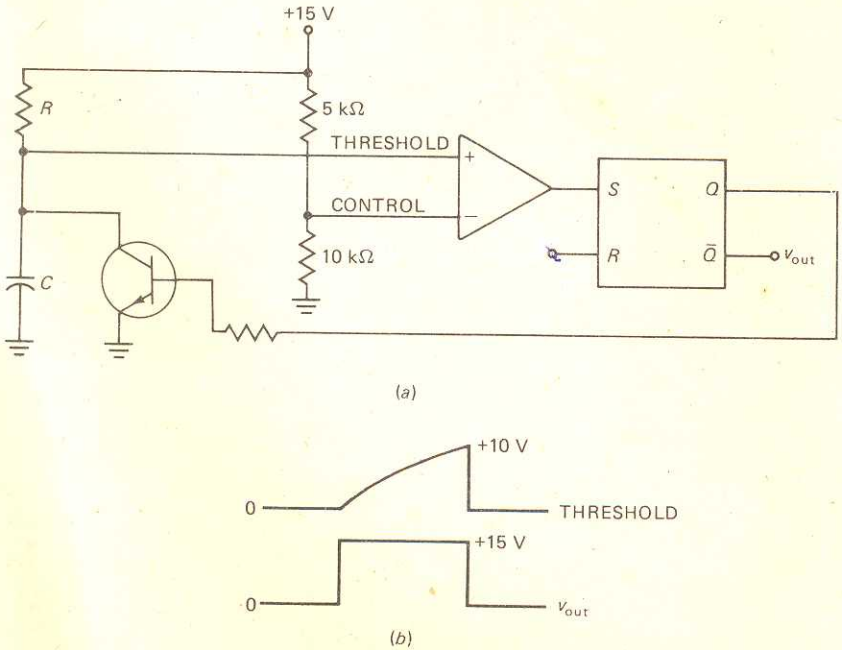


Fig. 20-28 (a) *Basic timing circuit.* (b) *Capacitor voltage is exponential and output voltage is rectangular.*

waveforms in Fig. 20-28*b*. An exponential rise is across the capacitor, and a positive-going pulse appears at the $\overline{Q}$ output.

555 BLOCK DIAGRAM

Figure 20-29 is a simplified block diagram of the NE555 timer, an 8-pin IC timer introduced by Signetics Corporation. Notice that the upper comparator has a threshold input (pin 6) and a control input (pin 5). In most applications, the control input is not used, so that the control voltage equals $+2V_{CC}/3$. As before, whenever the threshold voltage exceeds the control voltage, the high output from the comparator will set the flip-flop.

The collector of the discharge transistor goes to pin 7. When this pin is connected to an external timing capacitor, a high Q output from the flip-flop will saturate the transistor and discharge the capacitor. When Q is low, the transistor opens and the capacitor can charge as previously described.

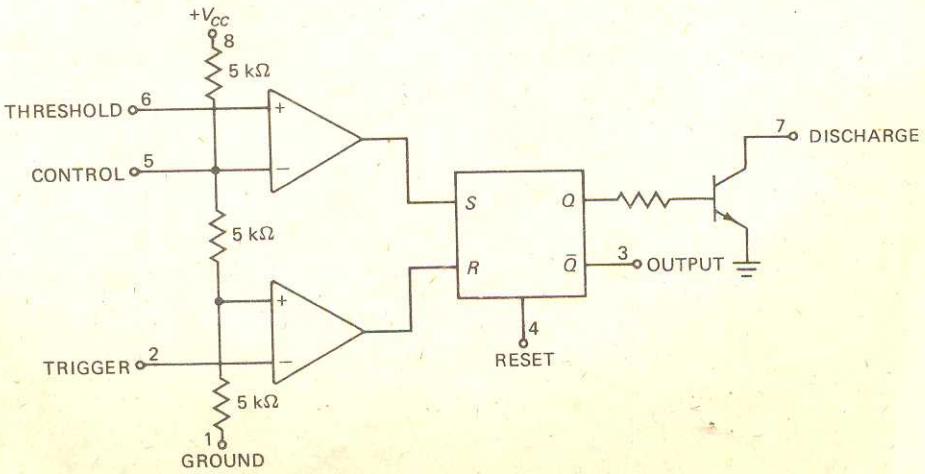
The complementary signal out of the flip-flop goes to pin 3, the output. When the external reset (pin 4) is grounded, it inhibits the device (prevents it from working). This on/off feature is sometimes useful. In most applications, however, the external reset is not used, and pin 4 is tied directly to the supply voltage.

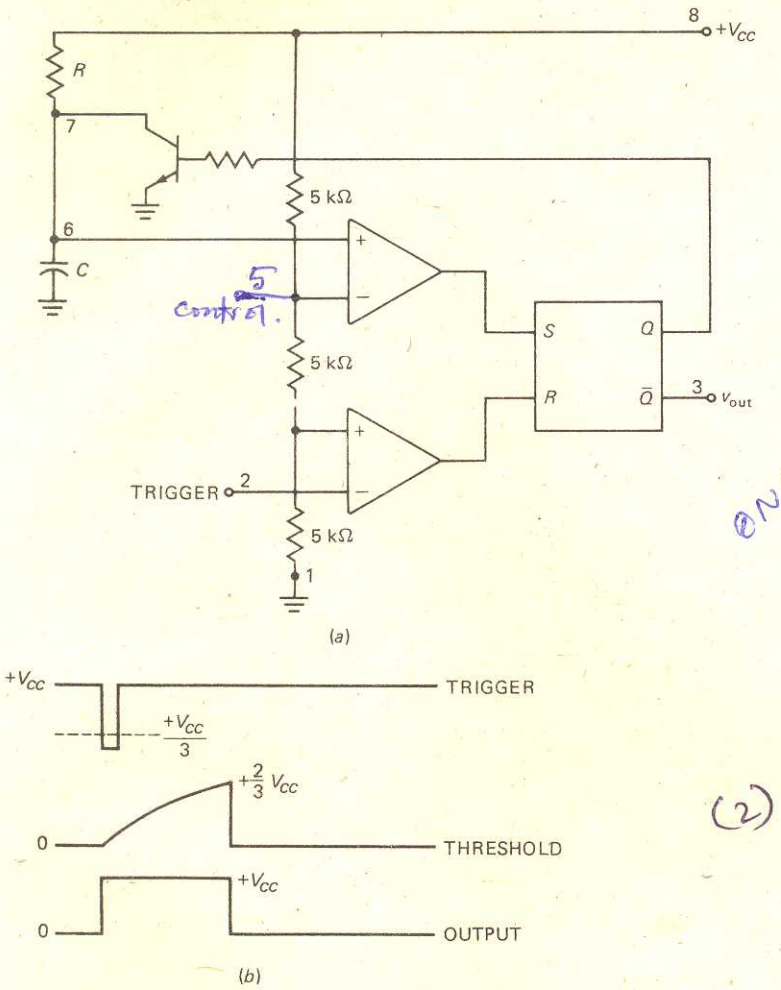
Notice the lower comparator. Its inverting input is called the *trigger* (pin 2). Because of the voltage divider, the noninverting input has a fixed voltage of $+V_{CC}/3$. When the trigger input voltage is slightly less than $+V_{CC}/3$, the op-amp output goes high and resets the flip-flop.

Finally, pin 1 is the chip ground, while pin 8 is the supply pin. The 555 timer will work with any supply voltage between 4.5 and 16 V

MONOSTABLE OPERATION

Figure 20-30*a* shows the 555 timer connected for *monostable* (also called one-shot) operation. The circuit works as follows. When the trigger input is slightly less than $+V_{CC}/3$, the lower comparator has a high output and resets the flip-flop. This cuts off





(1)

ONE SHOT.

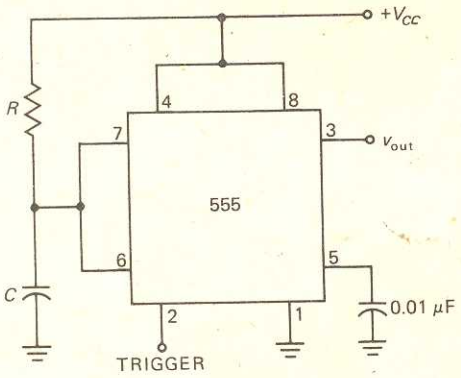
(2)

Fig. 20-30 (a) *555 timer connected as monostable multivibrator.* (b) *Trigger, output, and threshold waveforms.*

the transistor, allowing the capacitor to charge. When the capacitor voltage is slightly greater than $+2V_{CC}/3$, the upper comparator has a high output, which sets the flip-flop. As soon as Q goes high, it turns on the transistor; this quickly discharges the capacitor.

Figure 20-30*b* shows typical waveforms. The trigger input is a narrow pulse with a quiescent value of $+V_{CC}$. The pulse must drop below $+V_{CC}/3$ to reset the flip-flop and allow the capacitor to charge. When the threshold voltage slightly exceeds $+2V_{CC}/3$, the flip-flop sets; this saturates the transistor and discharges the capacitor. As a result, we get one rectangular output pulse.

The capacitor C has to charge through resistance R. The larger the RC time constant, the longer it takes for the capacitor voltage to reach $+2V_{CC}/3$. In other words, the RC time constant controls the width of the output pulse. Appendix 1



derives this formula for the pulse width:

$$W = 1.1RC \qquad (20\text{-}20)$$

For instance, if $R = 22\ \text{k}\Omega$ and $C = 0.068\ \mu\text{F}$, then

$$W = 1.1(22\ \text{k}\Omega)(0.068\ \mu\text{F}) = 1.65\ \text{ms}$$

Normally, a schematic diagram does not show the comparators, flip-flop, and other components inside the 555 timer. Rather, you will see a schematic diagram like Fig. 20-31 for the monostable 555 circuit. Only the pins and external components are shown. Incidentally, notice that pin 5 (control) is bypassed to ground through a small capacitor, typically 0.01 μF. This provides noise filtering for the control voltage.

Recall that grounding pin 4 inhibits the 555 timer. To avoid accidental reset, pin 4 is usually tied to the supply voltage, as shown in Fig. 20-31.

In summary, the monostable 555 timer produces a single pulse whose width is determined by the external R and C used in Fig. 20-31. The pulse begins with the leading edge of the negative trigger input. One-shot operation like this has a number of applications, as you will see in later studies.

ASTABLE OPERATION

Figure 20-32*a* shows the 555 timer connected for *astable* (free-running) operation. When Q is low, the transistor is cut off and the capacitor is charging through a total resistance of $R_A + R_B$. Because of this, the charging time constant is $(R_A + R_B)C$. As the capacitor charges, the threshold voltage increases. Eventually, the threshold voltage exceeds $+2V_{CC}/3$; then the upper comparator has a high output, and this sets the flip-flop. With Q high, the transistor saturates and grounds pin 7. Now the capacitor discharges through R_B. Therefore, the discharging time constant is R_BC. When the capacitor voltage drops slightly below $+V_{CC}/3$, the lower comparator has a high output, and this resets the flip-flop.

Figure 20-32*b* illustrates the waveforms. As you can see, the timing capacitor has an exponentially rising and falling voltage. The output is a rectangular wave. Since the charging time constant is longer than the discharging time constant, the output is not symmetrical; the high output state lasts longer than the low output state.

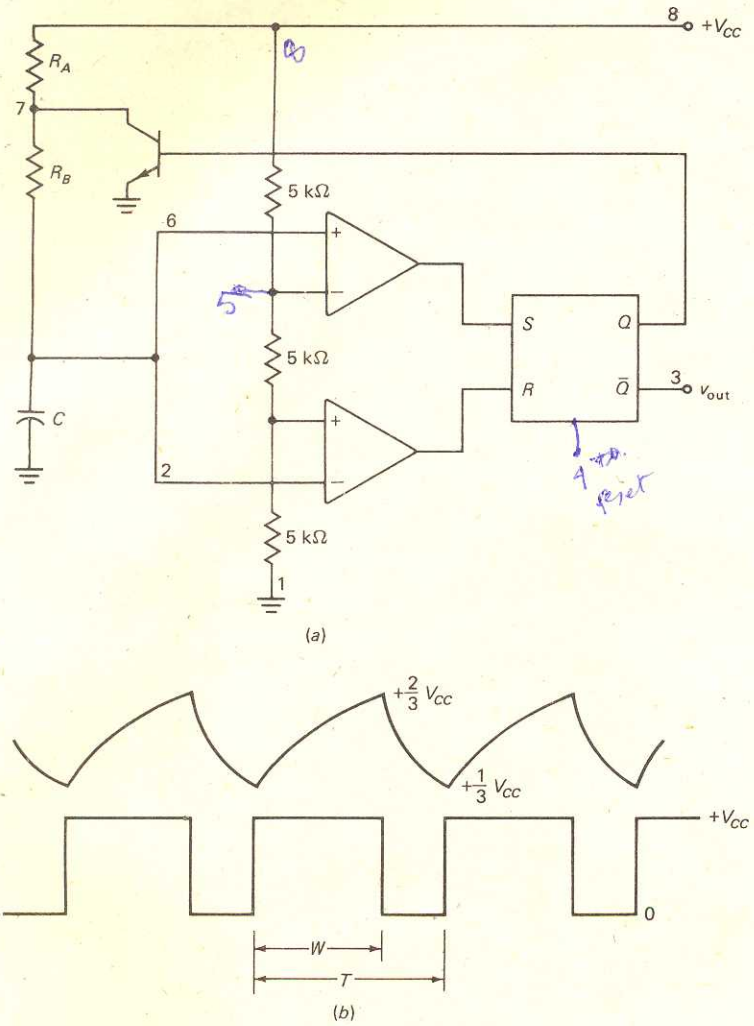


Fig. 20-32 (a) *555 timer connected as astable multivibrator.* (b) *Capacitor and output waveforms.*

To specify how unsymmetrical the output is, we will use the *duty cycle,* defined as

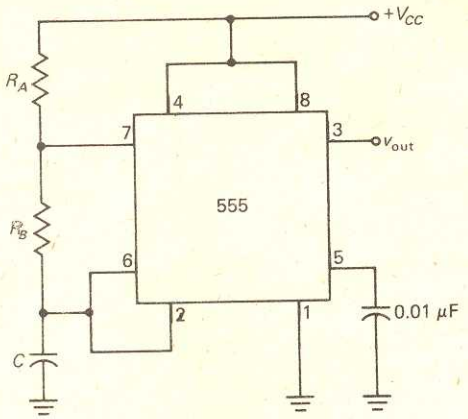
$$D = \frac{W}{T} \times 100\% \tag{20-21}$$

As an example, if $W = 2$ ms and $T = 2.5$ ms, then the duty cycle is

$$D = \frac{2 \text{ ms}}{2.5 \text{ ms}} \times 100\% = 80\%$$

Depending on resistances R_A and R_B, the duty cycle is between 50 and 100 percent.

A mathematical solution (Appendix 1) to the charging and discharging equations



gives the following formulas. The output frequency is

$$f = \frac{1.44}{(R_A + 2R_B)C} \tag{20-22}$$

and the duty cycle is

$$D = \frac{R_A + R_B}{R_A + 2R_B} \times 100\% \tag{20-23}$$

If R_A is much smaller than R_B, the duty cycle approaches 50 percent.

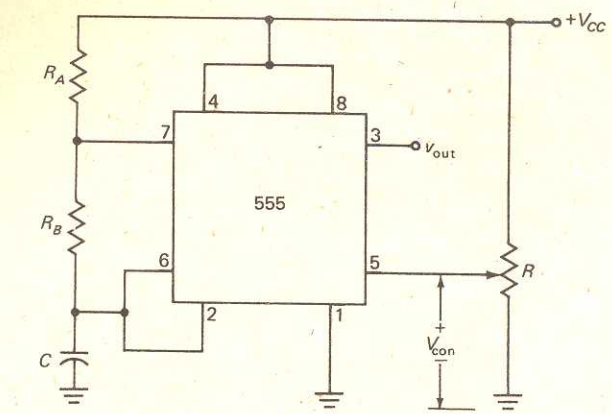
Figure 20-33 shows the astable 555 timer as it usually appears on a schematic diagram. Again notice how pin 4 (reset) is tied to the supply voltage and how pin 5 (control) is bypassed to ground through a 0.01-μF capacitor. An astable 555 timer is often called a *free-running multivibrator* because it produces a continuous train of rectangular pulses.

VOLTAGE-CONTROLLED OSCILLATOR

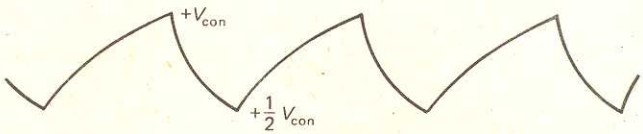
Figure 20-34*a* shows a *voltage-controlled* oscillator (VCO), one application for a 555 timer. The circuit is sometimes called a voltage-to-frequency converter because an input voltage can change the output frequency. Here is how the circuit works. Recall that pin 5 (control) connects to the inverting input of the upper comparator. Normally, the control voltage is $+2V_{CC}/3$ because of the internal voltage divider. In Fig. 20-34*a*, however, the voltage from an external potentiometer overrides the internal voltage. In other words, by adjusting the potentiometer, we can change the control voltage.

Figure 20-34*b* illustrates the voltage across the timing capacitor. Notice that it varies between $+V_{control}/2$ and $+V_{control}$. If we increase $V_{control}$, it takes the capacitor longer to charge and discharge; therefore, the frequency decreases. As a result, we can change the frequency of the circuit by varying the control voltage.

Incidentally, the control voltage may come from a potentiometer or it may be the output of a transistor circuit, op amp, or some other device. One of the more interesting applications for a VCO is the phase-locked loop (PLL), discussed in Chap. 23.



(a)



(b)

RAMP GENERATOR

Here is another application for the 555 timer. Charging a capacitor through a resistor produces an exponential waveform. If we use a constant current source to charge a capacitor, however, we get a *ramp*. This is the idea behind the circuit of Fig. 20-35*a*. Here we have replaced the resistor of previous circuits with a *pnp* current source that produces a constant charging current of

$$I_C = \frac{V_{CC} - V_E}{R_E} \tag{20-24}$$

where

$$V_E = \frac{R_2}{R_1 + R_2} V_{CC} + V_{BE} \tag{20-25}$$

For instance, if $V_{CC} = 15$ V, $R_E = 20$ kΩ, $R_1 = 5$ kΩ, $R_2 = 10$ kΩ, and $V_{BE} = 0.7$ V, then

$$V_E = 10 \text{ V} + 0.7 \text{ V} = 10.7 \text{ V}$$

and

$$I_C = \frac{15 \text{ V} - 10.7 \text{ V}}{20 \text{ k}\Omega} = 0.215 \text{ mA}$$

When a trigger starts the monostable 555 timer of Fig. 20-35*a*, the *pnp* current source forces a constant charging current into the capacitor. Therefore, the voltage across the capacitor is a ramp, as shown in Fig. 20-35*b*. As derived in Chap. 18, the

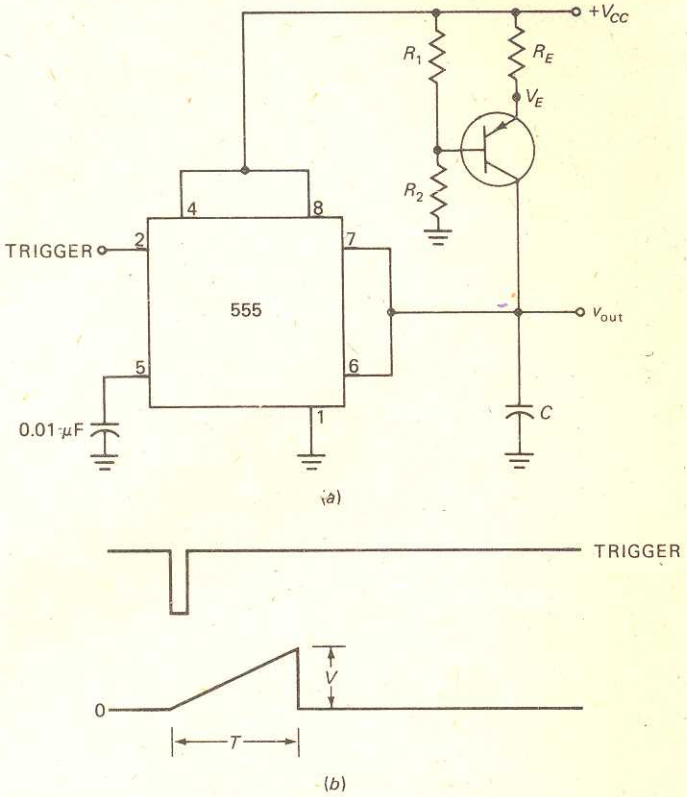


Fig. 20-35 (a) *Using a 555 timer and a bipolar current source to produce a ramp output voltage.* (b) *Trigger and ramp waveforms.*

slope S of the ramp is given by

$$S = \frac{I}{C} \tag{20-26}$$

If the charging current is 0.215 mA and the capacitance is 0.022 μF, the ramp will have a slope of

$$S = \frac{0.215 \text{ mA}}{0.022\ \mu\text{F}} = 9.77 \text{ V/ms}$$

Proof of Eq. (18-22)

The UTP has a value of $+BV_{sat}$ and the LTP a value of $-BV_{sat}$. Start with the basic switching equation that applies to any RC circuit:

$$v = v_i + (v_f - v_i)\ (1 - e^{-t/RC}) \qquad \text{(A-20)}$$

where v = instantaneous capacitor voltage
v_i = initial capacitor voltage
v_f = target capacitor voltage
t = charging time
RC = time constant

In Fig. 18-25*b*, the capacitor charge starts with an initial value of $-BV_{sat}$ and ends with a value of $+BV_{sat}$. The target voltage for the capacitor voltage is $+V_{sat}$ and the capacitor charging time is half a period, $T/2$. Substitute into Eq. (A-20) to get

$$BV_{sat} = -BV_{sat} + (V_{sat} + BV_{sat})\ (1 - e^{-T/2RC})$$

This simplifies to

$$\frac{2B}{1+B} = 1 - e^{-T/2RC}$$

By rearranging and taking the antilog, the foregoing becomes

$$T = 2RC \ln \frac{1+B}{1-B}$$

Proof of Eqs. (20-22) and (20-23)

In Fig. 20-32*b*, the capacitor upward charge takes time W. The capacitor voltage starts at $+V_{CC}/3$ and ends at $+2V_{CC}/3$ with a target voltage of $+V_{CC}$. Substitute into Eq. (A-20) to get

$$\frac{2V_{CC}}{3} = \frac{V_{CC}}{3} + \left(V_{CC} - \frac{V_{CC}}{3}\right)(1 - e^{-W/RC})$$

This simplifies to

end = start + (target − start)$(1 - e^{-t/RC})$

$$e^{-W/RC} = 0.5$$

or

$$W = 0.693RC = 0.693(R_A + R_B)C$$

The discharge equation is similar, except that R_B is used instead of $R_A + R_B$. In Fig. 20-32*b*, the discharge time is $T - W$, which leads to

$$T - W = 0.693R_BC$$

Therefore, the period is

$$T = 0.693(R_A + R_B)C + 0.693R_BC$$

and the duty cycle is

$$D = \frac{0.693(R_A + R_B)C}{0.693(R_A + R_B)C + 0.693R_BC} \times 100\%$$

or

$$D = \frac{R_A + R_B}{R_A + 2R_B} \times 100\%$$

To get the frequency, take the reciprocal of the period T:

$$f = \frac{1}{T} = \frac{1}{0.693(R_A + R_B)C + 0.693R_BC}$$

or

$$f = \frac{1.44}{(R_A + 2R_B)C}$$