ESP P3a Class AB Audio Power Amplifier

From Reverse Engineering to High-Fidelity Sound

A personal journey into mastering analog signal amplification

Designed by Rod Elliott, Reverse Engineered by Mukhtar Suleman

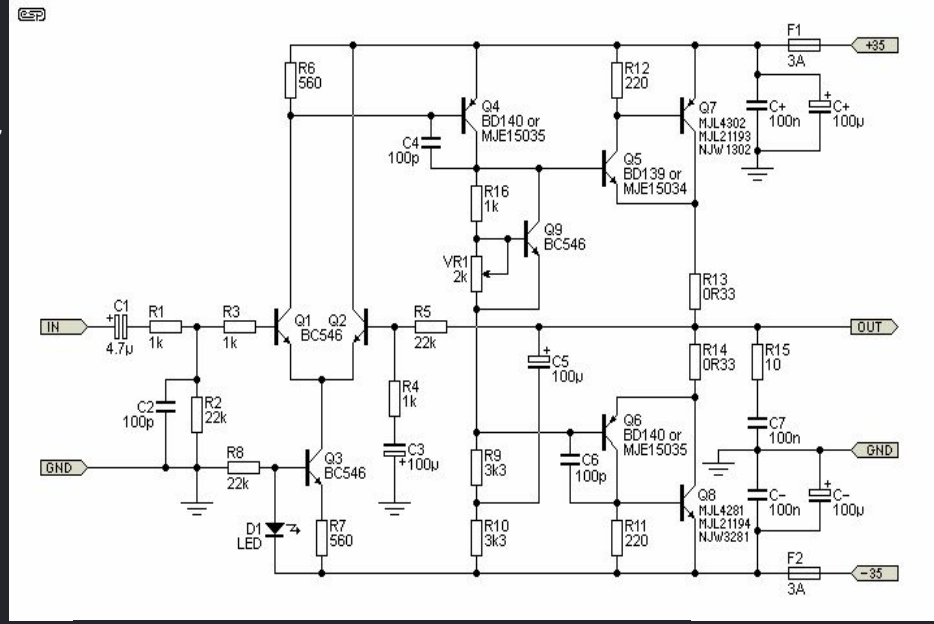
Architecture & Design Choice

The goal was to design and prototype a **100W Class AB audio amplifier** for high-fidelity speaker output — combining **clean sound** with **efficient power delivery**.

After evaluating amplifier topologies:

- **Class A** offers excellent linearity but is highly inefficient (~25%).
- **Class B** improves efficiency (~78%) but suffers from **crossover distortion**.
- **Class AB** strikes a balance — by using **diode or V_BE biasing**, both output transistors remain slightly on, reducing distortion and preserving efficiency.

I chose to reverse engineer **Rod Elliott's ESP P3a design** due to its clean schematic layout, thermal stability, and proven high-fidelity performance — making it ideal for hands-on prototyping and learning.



Spec	Target Value
Output Power	100W @ 4Ω
Voltage Rails	±35V
Frequency Response	20Hz–20kHz
THD+N	< 0.1%
Application	Home Stereo Audio

ESP P3A Design Requirements & Specifications

Parameter	Specification
Power Output	60–100 W RMS per channel
Load Impedance	8 Ω (±42 V rails) or 4 Ω (±35 V rails)
Supply Voltage (Rails)	±35 V for 4 Ω loads; ±42 V for 8 Ω loads
THD+N	< 0.05% at 1 kHz, full power
Frequency Response	10 Hz – 100 kHz (–1 dB)
Slew Rate	20 V/µs
Thermal Considerations	Large heatsink required; bias transistor mounted on heatsink for thermal tracking
Stability	Stable with capacitive loads; phase margin > 45°; gain margin > 10 dB
Application	Hi-Fi stereo, bi-amp systems, instrument amplifiers

Class AB Topology Explanation

Behavior Summary:

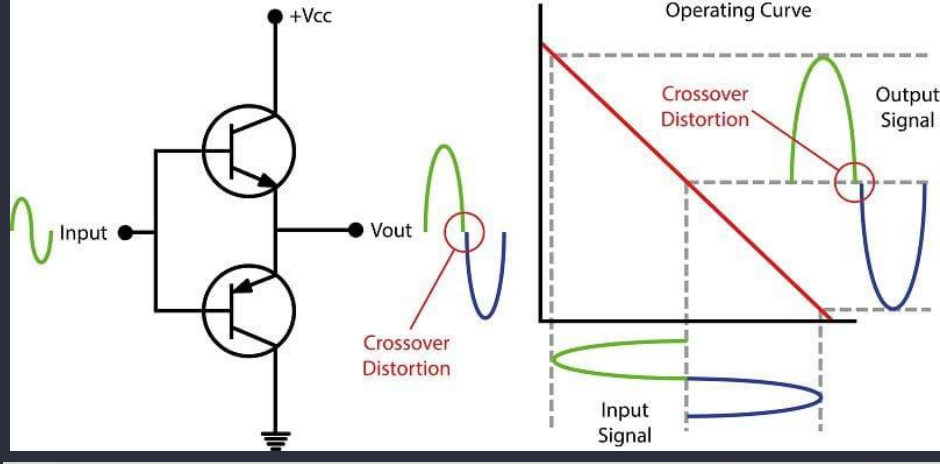
- **At Vin = 0V**
  → Both NPN and PNP slightly conduct → no distortion at zero-crossing.

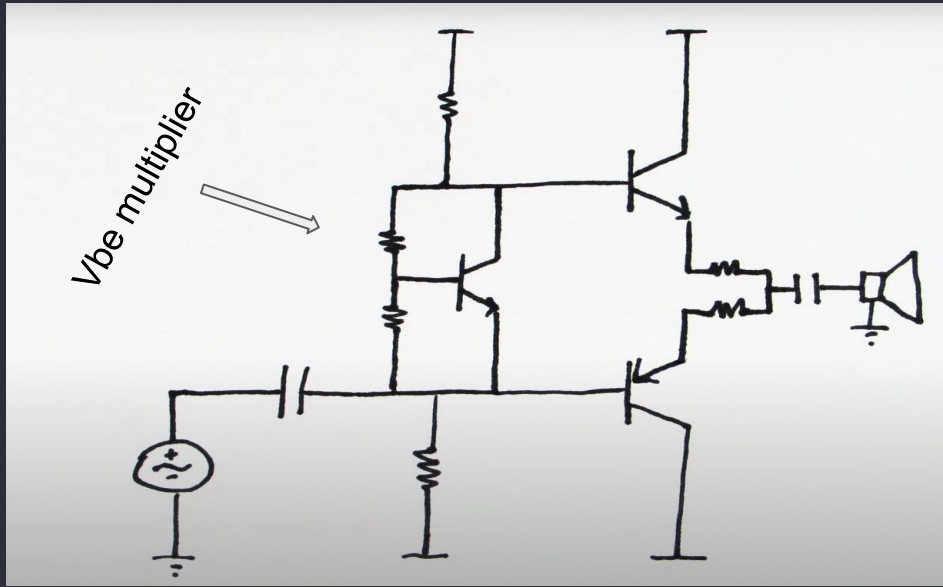
1. **Vin > 0 (Positive Half)**
   → NPN turns on more → sources current to the load.
   → PNP turns off gradually.

2. **Vin < 0 (Negative Half)**
   → PNP turns on more → sinks current from the load.
   → NPN turns off gradually.

Mitigating Crossover Distortion:

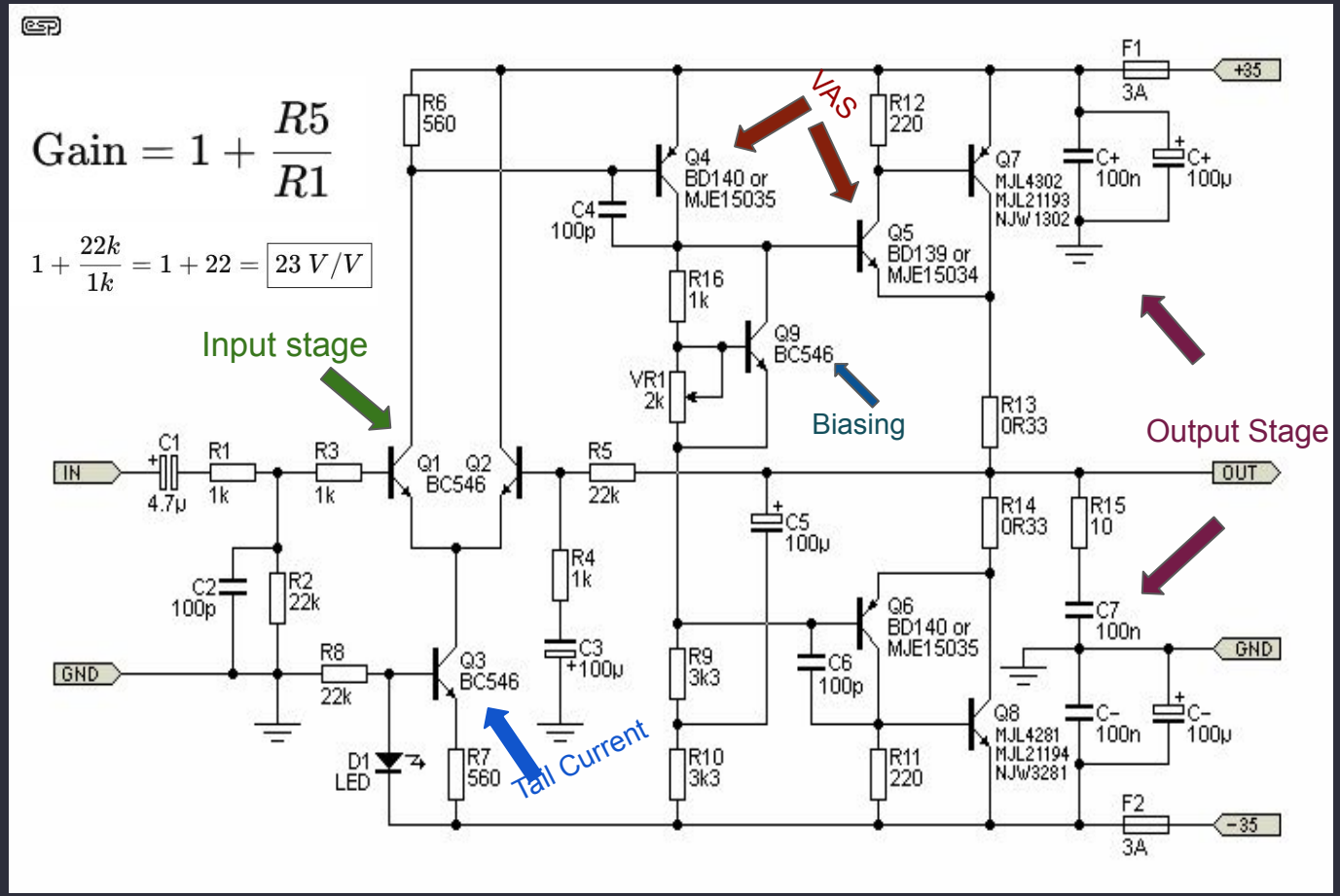
- V_BE multiplier creates a modest quiescent current (typically 50–100 mA per output transistor), just enough to avoid distortion without excessive heat.





ESP P3a schematic

Block	Components
Input Stage	Q1, Q2, R1, R2, R3, R4, R5
Tail Current Source	Q3, D1, R7
Voltage Amplification Stage (VAS)	Q4, Q5, R16, C4
Bias Control (V_BE Multiplier)	Q9, VR1, R16
Output Stage (Class AB)	Q6, Q7, Q8, R13, R14, C7
Feedback & Output Filtering	OUT node → R15, C7, trace back to R2



Simulation & Validation Process

I simulated the ESP P3a input stage in LTSpice to validate the differential pair's behavior.

To isolate the stage, I disconnected the feedback loop from Q2's base.

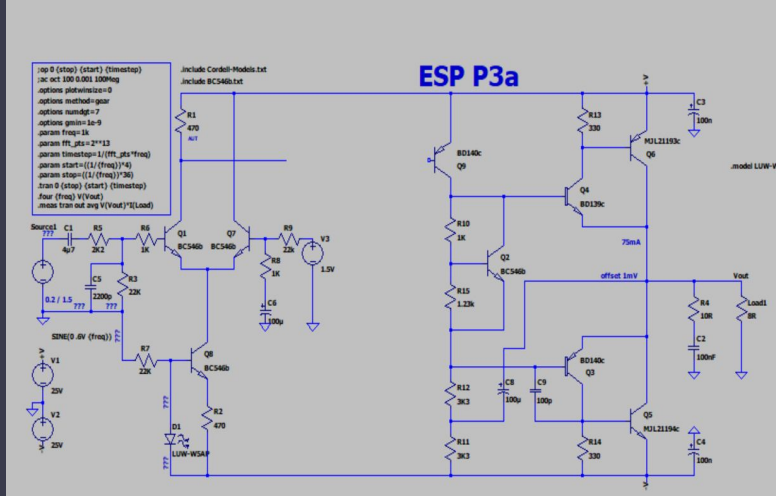
I applied a 1.5V AC signal to Q1's base to mimic an audio input.

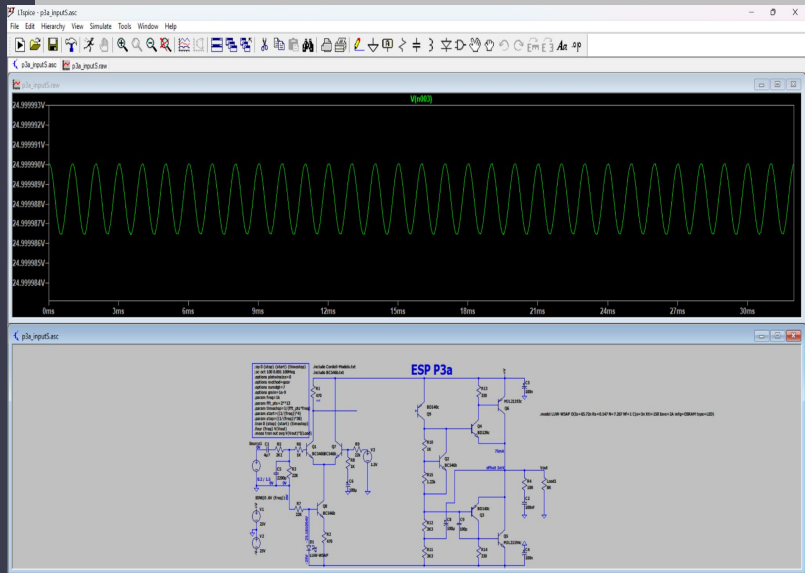
The tail current source uses a white LED (3.2V) and BJT with a 470Ω emitter resistor:

- **Tail current ≈ (3.2V - 0.7V) / 470Ω ≈ 5.3 mA**
- **≈ 2.65 mA per transistor**

Transconductance: **g□ ≈ 2.65 mA / 25 mV = 0.106 S**

Voltage gain: **A ≈ g□ × RC = 0.106 × 470 ≈ 49.8 V/V (~34 dB)**





Simulation & Validation Process

Voltage gain stage (VAS) and **Class AB driver components now added**

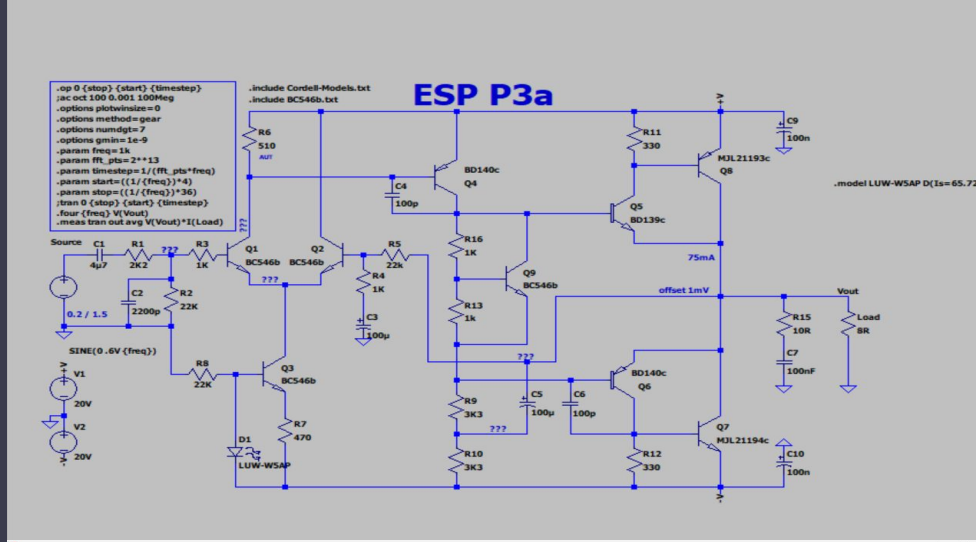
Q4 and Q5 form the core of the gain stage:

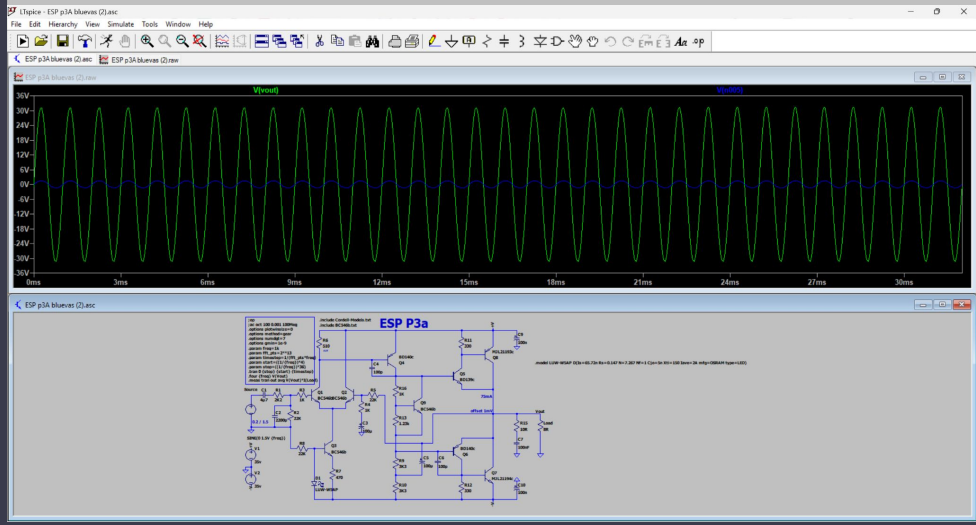
- **Q4** acts as the current source load.
- **Q5** operates as the **voltage amplification stage (VAS)**, boosting the signal from the input stage.

Q5 also drives the PNP transistor (Q8) — the upper half of the Class AB output stage.

The **Class AB output biasing** is controlled by **Q9**, which is configured as a **VBE multiplier**

- This sets the **quiescent current** between Q8 (PNP) and Q6 (NPN), helping to minimize crossover distortion
- 30Vpp > 21.2Vrms > P = (21.2)^2/8 = 56.2W or P = (21.2)^2/4 = 112.4W





Simulation Results (LTSpice)

Gain:Vout /Vin
30V/1.5 = 20

```
Direct Newton iteration for .op point succeeded.
N-Period=1
Fourier components of V(vout)
DC component:-0.0572217

Harmonic          Frequency          Fourier          Normalized
 Number             [Hz]           Component          Component
    1            1.000e+3           3.130e+1           1.000e+0
    2            2.000e+3           2.074e-3           6.627e-5
    3            3.000e+3           1.728e-3           5.522e-5
    4            4.000e+3           2.778e-4           8.876e-6
    5            5.000e+3           1.271e-4           4.061e-6
    6            6.000e+3           1.122e-4           3.586e-6
    7            7.000e+3           2.221e-5           7.098e-7
    8            8.000e+3           3.683e-5           1.177e-6
    9            9.000e+3           1.813e-5           5.795e-7
Partial Harmonic Distortion: 0.008690%
Total Harmonic Distortion:   0.008694%
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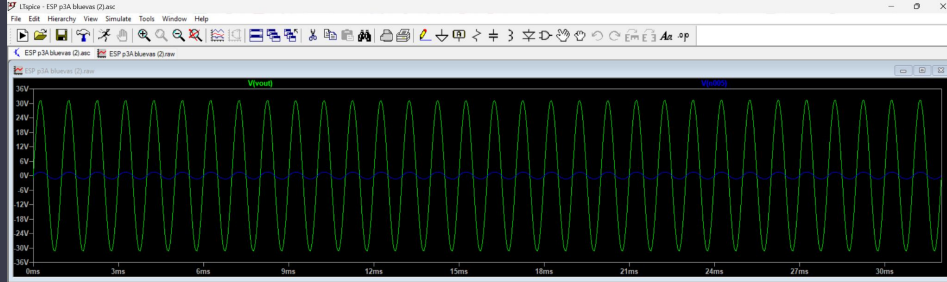
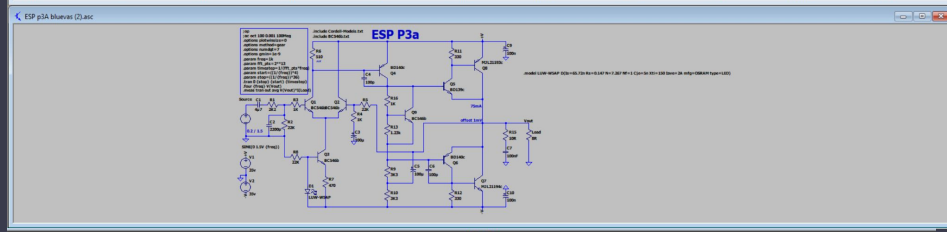
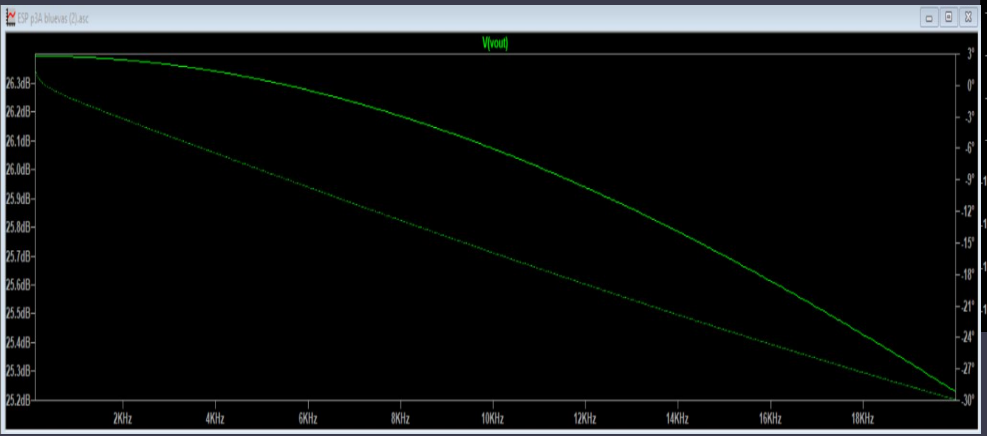
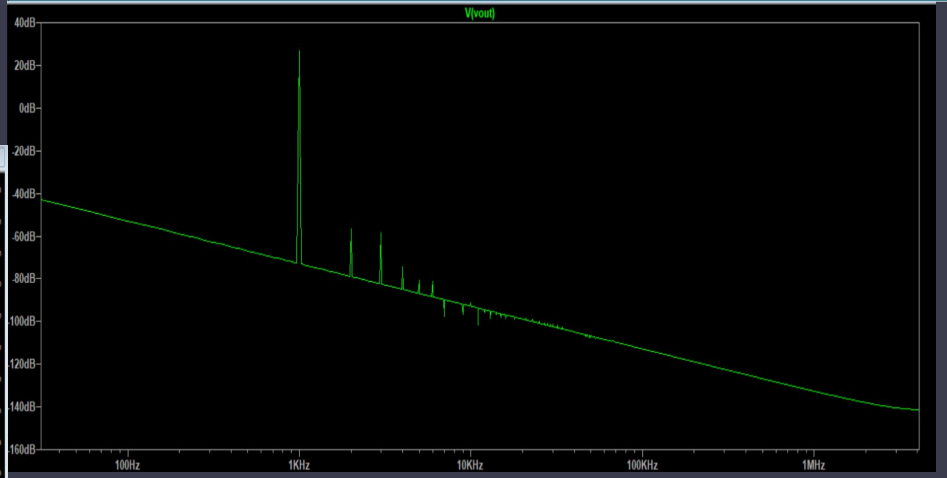




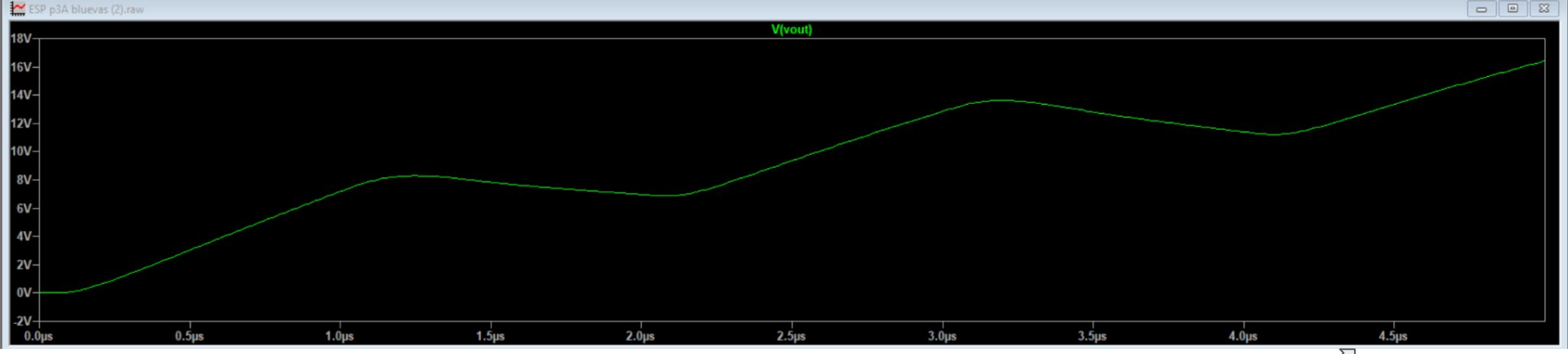
THD

Frequency response



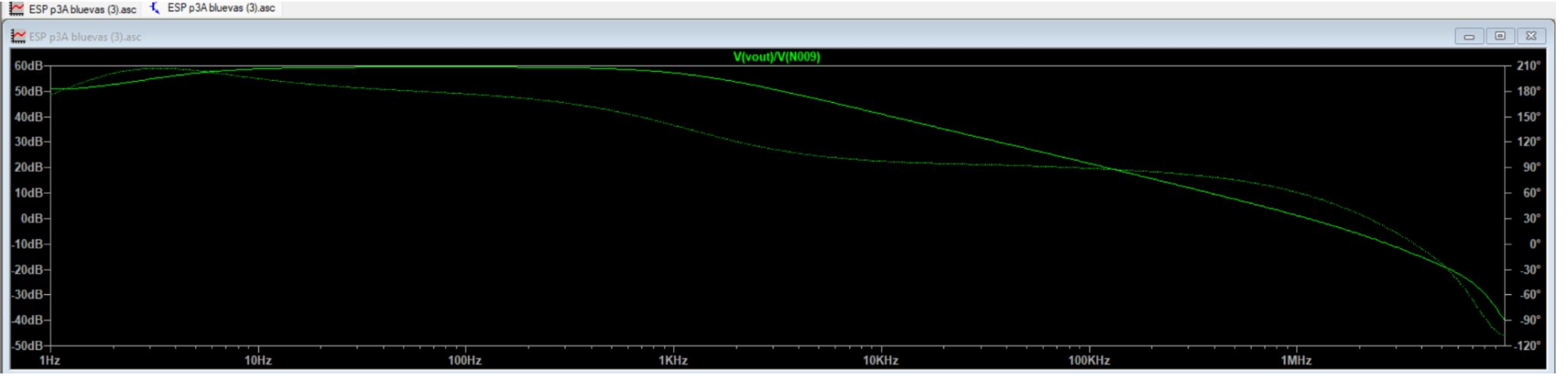


FFT

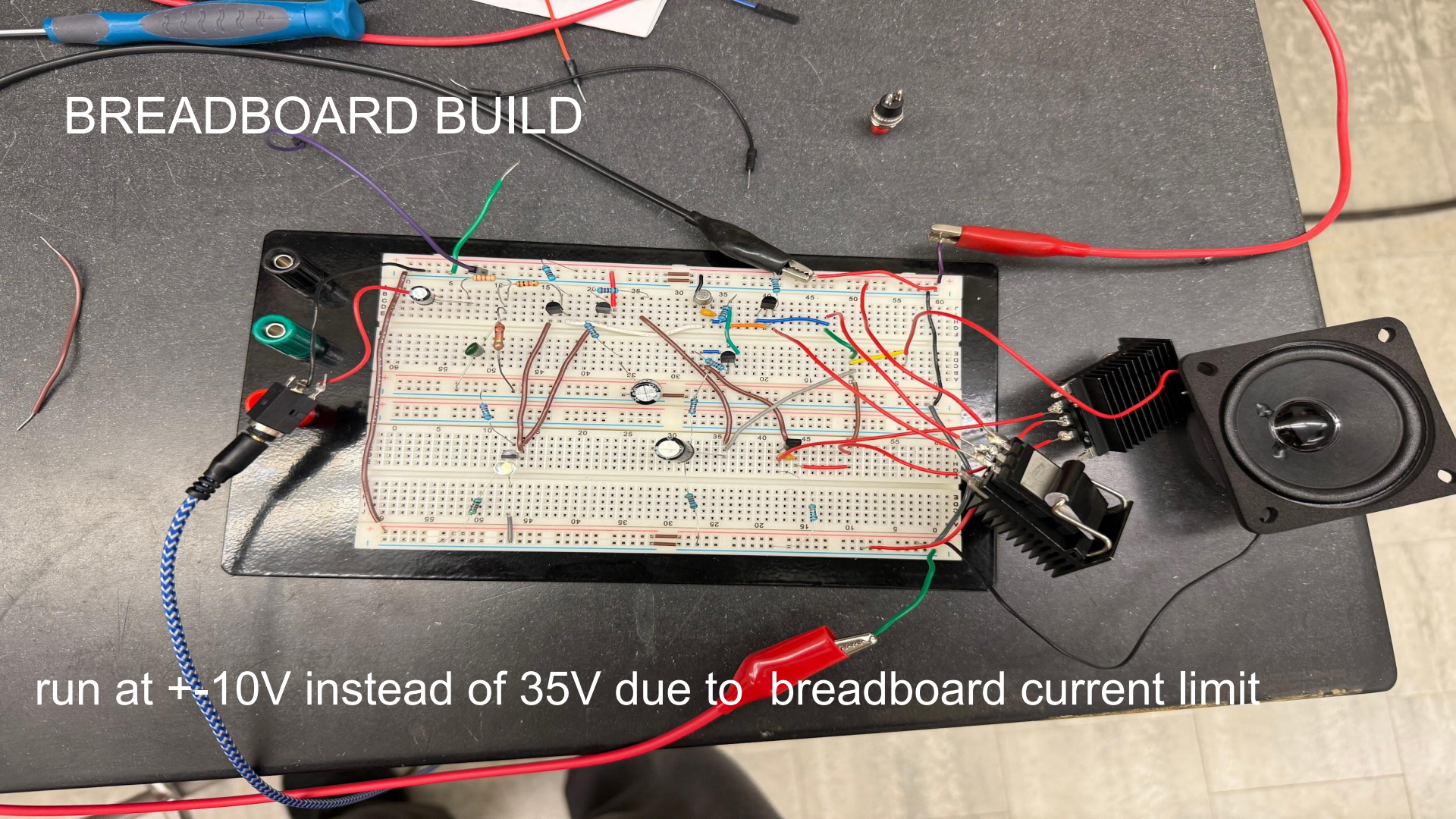


Slew rate = V/us = 3V/5us = .6V/us - pretty low for power audio amplifiers

Unity gain point frequency at 1.13Mhz, 29°



BREADBOARD BUILD



run at +-10V instead of 35V due to breadboard current limit

What I could still validate at ±10V

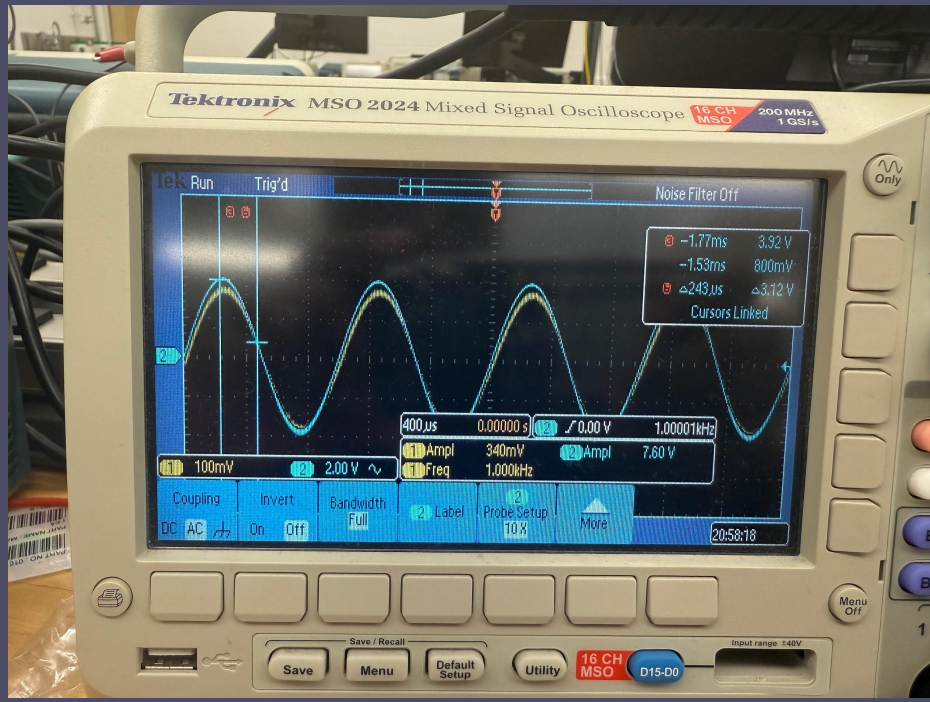
Test/Observation	What It Confirms
DC operating points	Biasing of all transistors (VAS, differential pair, output)
Quiescent current	V_BE multiplier working, output stage not oscillating
Small-signal gain	Expected voltage gain (still close to 20×, scaled output)
Waveform symmetry	Output is centered at 0V, no major offset
Crossover distortion check	Class AB smooth zero-crossing behavior
Stability	No self-oscillation at idle or with input signal

Breadboard Results

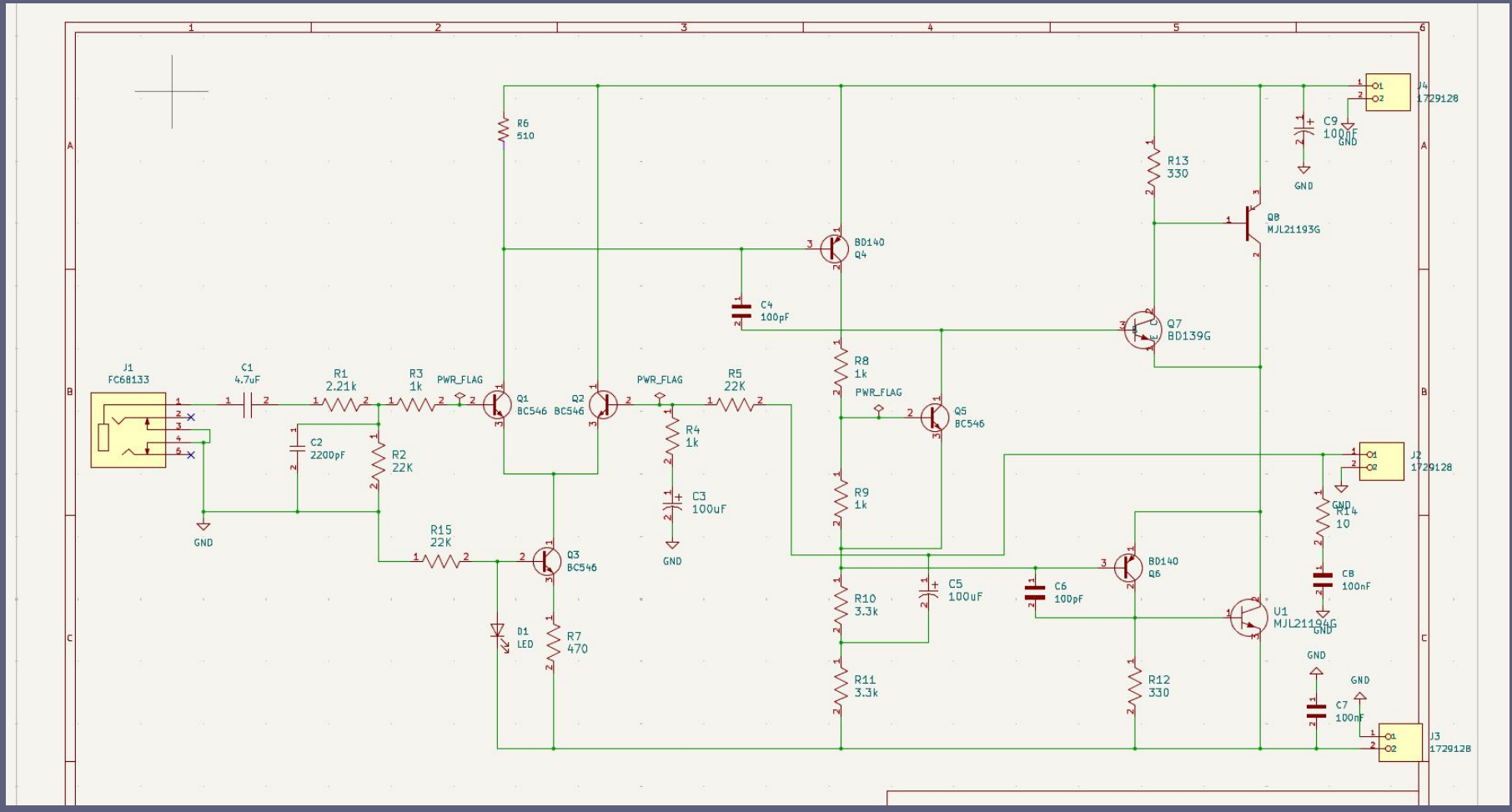
Input signal: sine 350mV 1khz yellow probe

Output: 7.60V blue probe

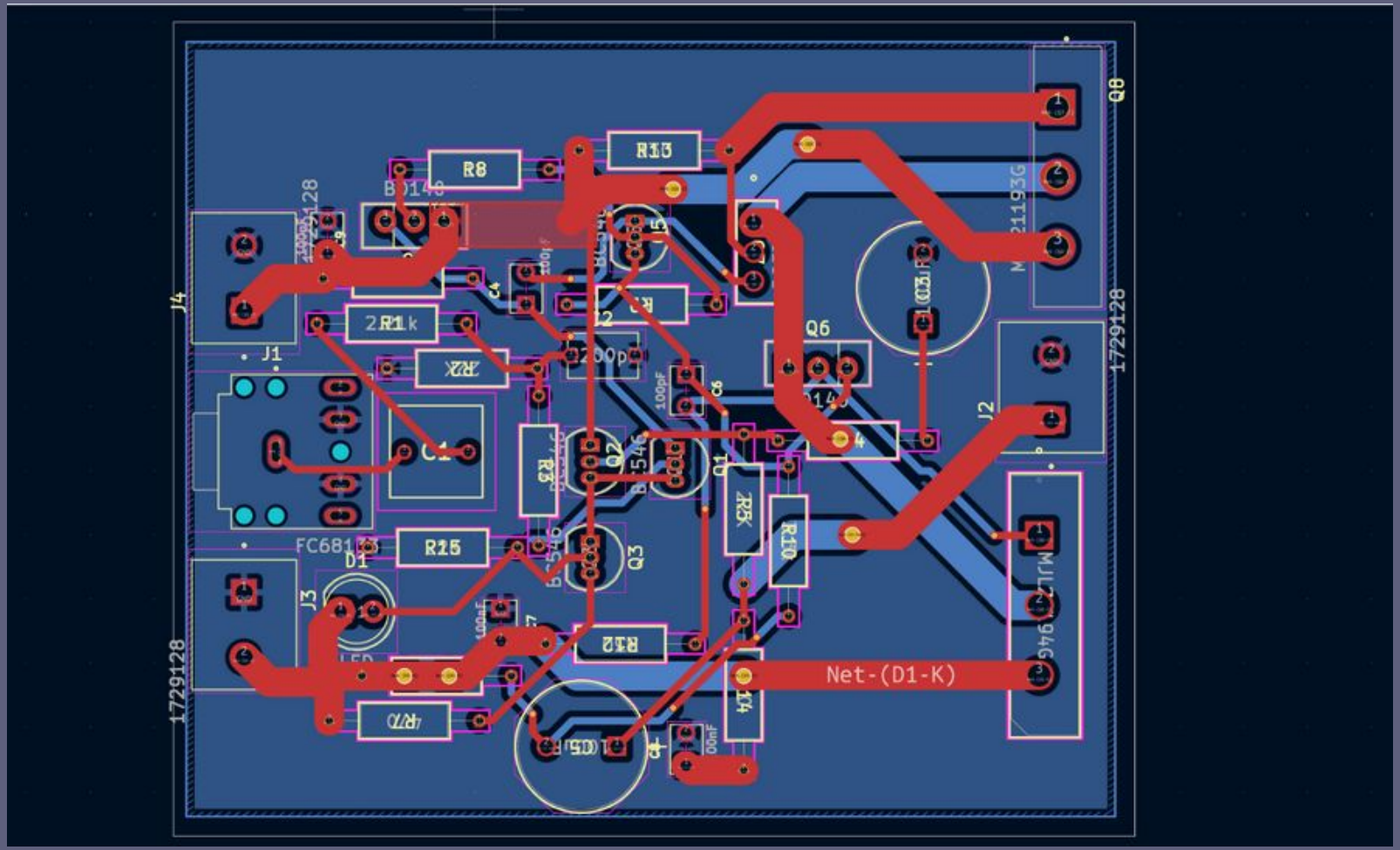
Gain = 7.6/.35 = 21.7V/V ≈ 23V/V



PCB Schematic



PCB



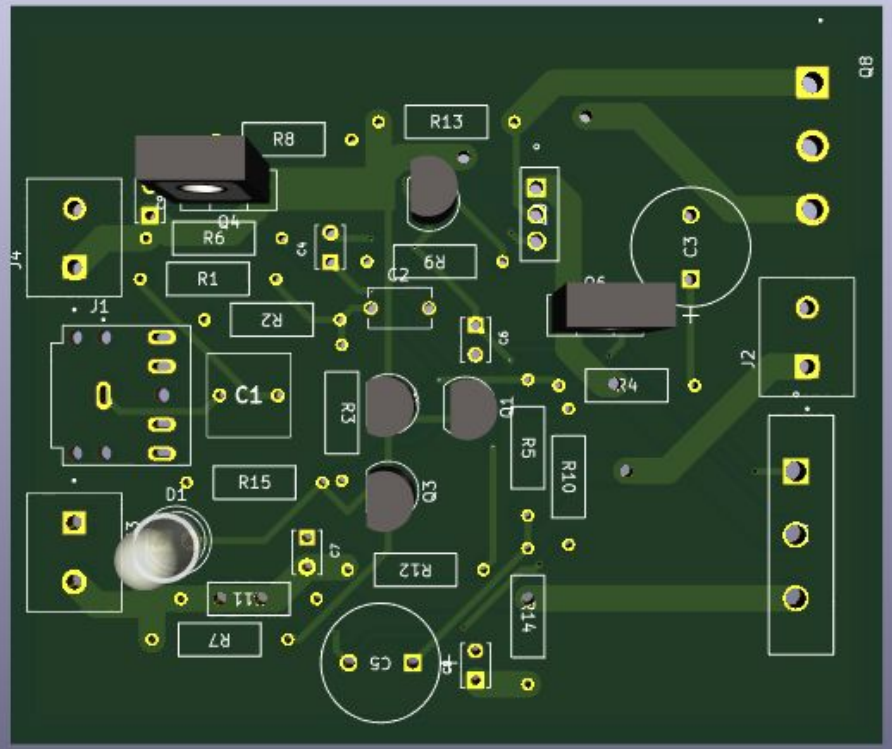
3D PCB

Software: KiCad 7.0

Layers: 2-layer board

Copper Weight: 1 oz (35µm)

Trace Width for Power Rails: 2.3 mm (Handles >3A for output stage and speaker drive)



Lessons Learned – ESP P3a Class AB Amplifier

1. PCB Layout is *Everything*

- High-current traces need to be treated like copper busbars — used **2.3 mm traces** for >3A paths (Q7/Q8 → Vout → Load)

2. **Simulation vs. Reality**

- Simulations in LTSpice showed ideal THD, slew rate, and stability
- Breadboard testing (±10V rails) revealed **subtle distortion** and thermal drift

3. Real analog design is about **debugging what simulation missed**

- Building first at **reduced voltage on breadboard** is underrated
- Every trace has a story — and analog layout is as much an art as a science