Indian Institute of Science

Bangalore, India

M. Tech Electrical Engineering

(04-03-04-10-51-23-1-23117)

Submitted To-

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PROBLEM DESCRIPTION

In this homework, you are to design a basic two-stage CMOS operational amplifier (op-amp), as shown in Figure 1, forthe specifications given inTable 1. The op-amp consists of a differential input stage (M_1 and M_2) driving a current mirror load(M_3 and M_4) followed by a common-source amplifier stage (M_7). The devices M_5 and M_7 form the tail current source for the differential stage and the current source load for thecommon- source stage. C_c and R_z are the compensation capacitor and the zero-nulling resistor.

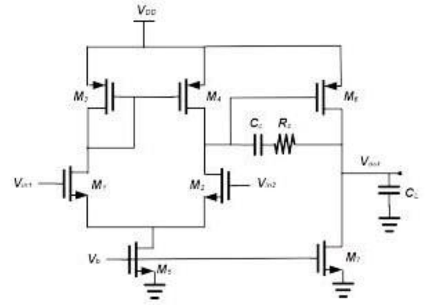


Figure 1 A basic two-stage operational amplifier.

Table 1 Design specifications @ [Supply voltage = **1.8** $\boldsymbol{V}$, Load CL = **100** $\boldsymbol{fF}$, and Temperature = **27°** $\boldsymbol{C}$]

S.N.	Parameter	Symbol		Value
1.	Open-loop, differential-mode, DC voltage gain	A_0	≥	$1000\ V/V$ $(60\ dB)$
2.	Unity-gain frequency	f_{UG}	≥	$10\ MHz$
3.	Phase margin	PM	≥	$75°$
4.	Common-mode rejection ratio	$CMRR$	≥	$50\ dB$
5.	Power dissipation	P_d	≤	$30\ \mu W$

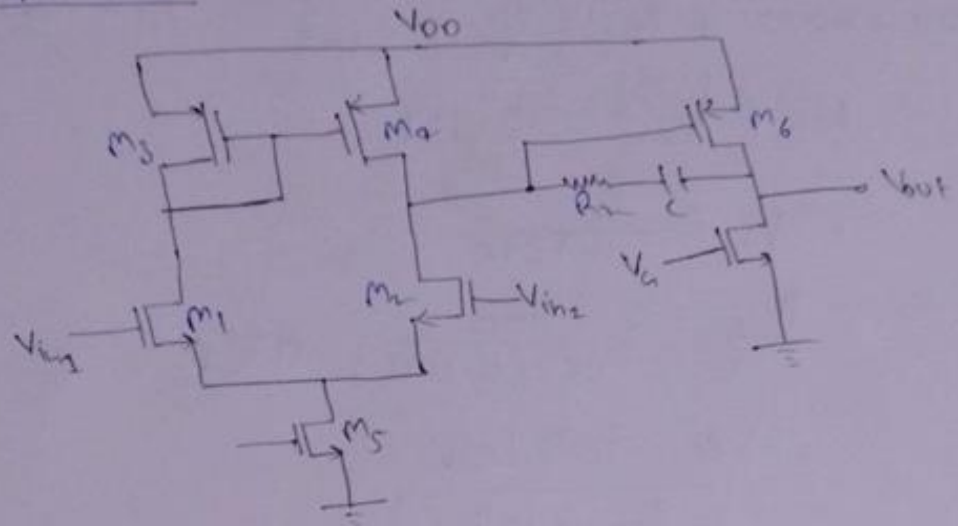
The designing of the op-amp consists of selecting device sizes and biasing conditions.

Solution:

Initial Design:

Two Stage op-amp Design :-

1) Compensated



$V_{DD} = 1.8V \quad C_L = 100fF$

given $A_v \geq 60dB$ (1000 V/V) GB (gain Bandwidth) = Constant $= f_1 \geq 10MHz$

$PM \geq 75 \quad CMRR \geq 50dB \quad P_d \leq 30mW$

Assumption $ICMR(min) = 0.8 \quad ICMR(max) = 1.6$

$0.8 \leq ICMR < 1.6 \quad S.R \geq 1V/\mu sec$

$L = 1\mu m$

Design $$G H(s) = \frac{G_1 G_2 (1 - s/z_1)}{(1+s/p_1)(1+s/p_2)}$$

where $$p_1 = \frac{1}{(r_{ds_2} \| r_{ds_4}) g_{m_6} (r_{ds_6} \| r_{ds_7}) C_c}$$

$$p_2 = \frac{g_{m_6}}{C_L}$$

$$\text{zero} \Rightarrow z_1 = \frac{g_{m_6}}{C_c}$$

$$PM = 180 + \phi$$

$$180 + \phi \Big|_{GB} \geq 75^\circ$$

$$180 + \left[-\tan^{-1}\left(\frac{GB}{z_1}\right) - \tan^{-1}\left(\frac{GB}{p_1}\right) - \tan^{-1}\left(\frac{GB}{p_2}\right)\right] \geq 75^\circ$$

$$\tan^{-1}(0.1) + \tan^{-1}(G) + \tan^{-1}\left(\frac{f_u}{p_2}\right) \leq 105^\circ$$

$(z_2 \geq 10 f_u;\ p_1 \leq 10 f_u)$

$$\therefore 5.71 + 89.7 + \tan^{-1}\left(\frac{f_u}{p_2}\right) \leq 105$$

$$\tan^{-1}\left(\frac{f_u}{p_2}\right) \leq 9.347$$

$$p_2 \geq \frac{f_u}{0.1646}$$

$$\frac{g_{m6}}{C_L} \geq \frac{g_{m2}}{C_c(0.1646)} \quad (1) \quad \left(f_u = \frac{g_m}{C_c}\right)$$

$$\therefore Q_c \quad z_1 > 10 f_u$$

$$\boxed{g_{m6} > 10 g_{m2}}$$

now from (1)

$$\frac{10}{C_L} \geq \frac{1}{C_c(0.1646)}$$

$$C_c \geq \frac{C_L}{1.646}$$

$$\boxed{C_c \geq 60.7 fF}$$

$$\boxed{C_c = 120 fF}$$

$$S.R = 12\ V/\mu s$$

$$SR = \frac{I_5}{C_c} \Rightarrow \boxed{I_5 = 1.44 mA}$$

$$GB = \frac{g_{m1}}{C_c}$$

$$g_{m1} = GB \times 2\pi \times C_c$$

$$= 10 \times 10^6 \times 2\pi \times 120 \times 10^{-15}$$

$$\boxed{g_m = 7.54\ \mu S}$$

$$\boxed{g_{m1} = 16 \mu S}$$

Design of M_1, M_2

$$g_{m_1} = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_1 I_{D_1}}$$

$$g_{m_1} = \sqrt{\mu_n C_{ox}\left(\frac{W}{L}\right)_1 I_S}$$

$(2I_{D_1} = I_S)$

$$\left(\frac{W}{L}\right)_1 = \frac{g_{m_1}^2}{\mu_n C_{ox}\left(\frac{W}{L}\right) I_S}$$

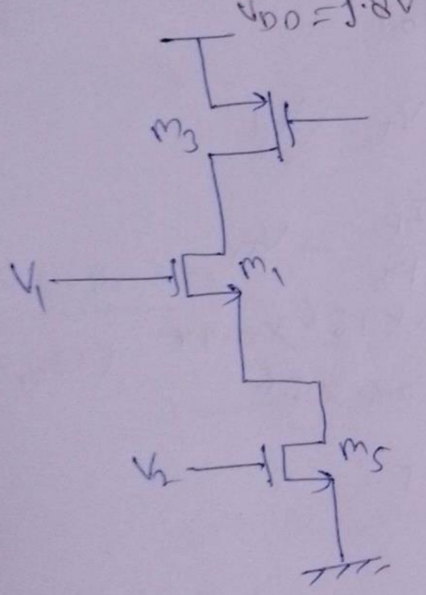
$$\mu_n C_{ox} = 400\times10^{-6}\ A/V^2$$

$$\mu_p C_{ox} = 60\times10^{-6}\ A/V^2$$

$$(W/L)_1 = \frac{16\times16}{400\times1.44} = 0.44$$

$$\boxed{\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = 0.444}$$

Design of M_3, M_4



for M_1 to be in Saturation

$$V_{D_1} \geq V_1 - V_{T_1}$$

$$V_1 \leq V_{D_1} + V_{T_1}$$

$$V_1 = V_{D_1} + V_{T_1}$$

$$V_{D_1} = 1.8 - V_{SG_3} \quad (3)$$

$$I_{D_3} = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_3 (V_{SG_3} - V_{T_3})^2$$

Let $\beta_p = \mu_n C_{ox}\left(\frac{W}{L}\right)_3$

$$\Rightarrow \sqrt{\frac{2I_{D_3}}{\beta_p}} = V_{SG_3} - V_{T_3}$$

$$V_{SG_3} = \sqrt{\frac{2I_{D_3}}{\beta_p}} + V_{T_3}$$

substitute in (3)

$$V_{D_1} = 1.8 - \sqrt{\frac{2I_{D_3}}{\beta_p}} - V_{T_3}$$

Now $$V_1 = 1.8 - \sqrt{\frac{I_S}{\beta_p}} - V_{T_3} + V_{T_1}$$

ICMR (max) = 1.6 V

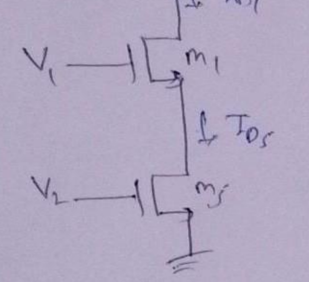
$$\sqrt{\frac{I_8}{\beta_P}} = 1.8 - 1.6 - 0.75 + .75$$

$$\frac{I_5}{\beta_P} = 0.2 \times .2$$

$$\beta_P = \frac{1.44}{4} \times 10^{-4}$$

$$\boxed{\left(\frac{W}{L}\right)_3 = 0.6 = \left(\frac{W}{L}\right)_4}$$

Design of M_5 :-



for M_5 to be in saturation

$$V_{DS} \geq V_2 - V_{T5}$$

$$V_1(\text{min}) \geq V_{GS1} + V_{DS}(\text{min})$$

$$\text{ICMR (min)} \geq V_{GS1} + V_{od}$$

$$\therefore \text{ICMR (min)} \geq \sqrt{\frac{2I_{D1}}{\beta_N}} + V_{T1} + V_{od}$$

$$V_{od} \leq \text{ICMR (min)} - \sqrt{\frac{2I_{D1}}{\beta_n}} - V_{T1}$$

$$\beta_n = \mu_n C_{ox} \left(\frac{W}{L}\right)_1 = 400 \times 10^{-6} \times 0.44 \qquad (2I_{D1} = I_5)$$

$$= 177.6 \times 10^{-6}$$

$$V_{od} \leq 0.8 - \sqrt{\frac{1.44}{177.6}} - 0.5$$

$$V_{od} \leq 0.203\ V$$

take $\boxed{V_{od} \simeq 0.12}$

$$I_5 = \frac{1}{2}\mu_n C_{ox} \left(\frac{W}{L}\right)_5 (V_{od})^2$$

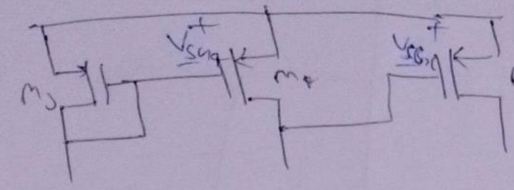
$$\left(\frac{W}{L}\right)_5 = \frac{I_5 \times 2}{\mu_n C_{ox} (V_{od})^2} = \frac{1.44 \times 2}{400 \times (.12)^2} = 0.5$$

$$\boxed{\left(\frac{W}{L}\right)_5 = 0.5}$$

Design of M_6:

$g_{m6} = 10 g_{m2}$

$g_{m6} = 160\,\mu S$



$V_{SG4} = V_{SG6}$ for mirroring

$\frac{I_6}{I_4} = \frac{(W/L)_6}{(W/L)_4} = \frac{g_{m6}}{g_{m4}}$

$g_{m4} = \sqrt{\mu_p C_{ox} (\frac{W}{L}) 2 I_{D4}}$

$= \sqrt{60\times10^{-6}\times0.6\times1.44\times10^{-6}}$

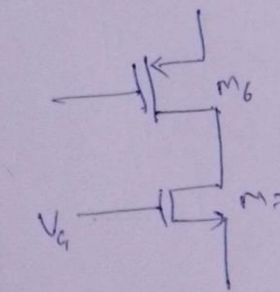
$= 7.2\,\mu S$

$(W/L)_6 = \frac{160}{7.2}\times0.6 = 13.33$

$\boxed{(\frac{W}{L})_6 = 13.33}$

$I_6 = I_4 \times \frac{g_{m6}}{g_{m4}} = 16\,\mu A$

Design M_7



$I_6 = I_7$

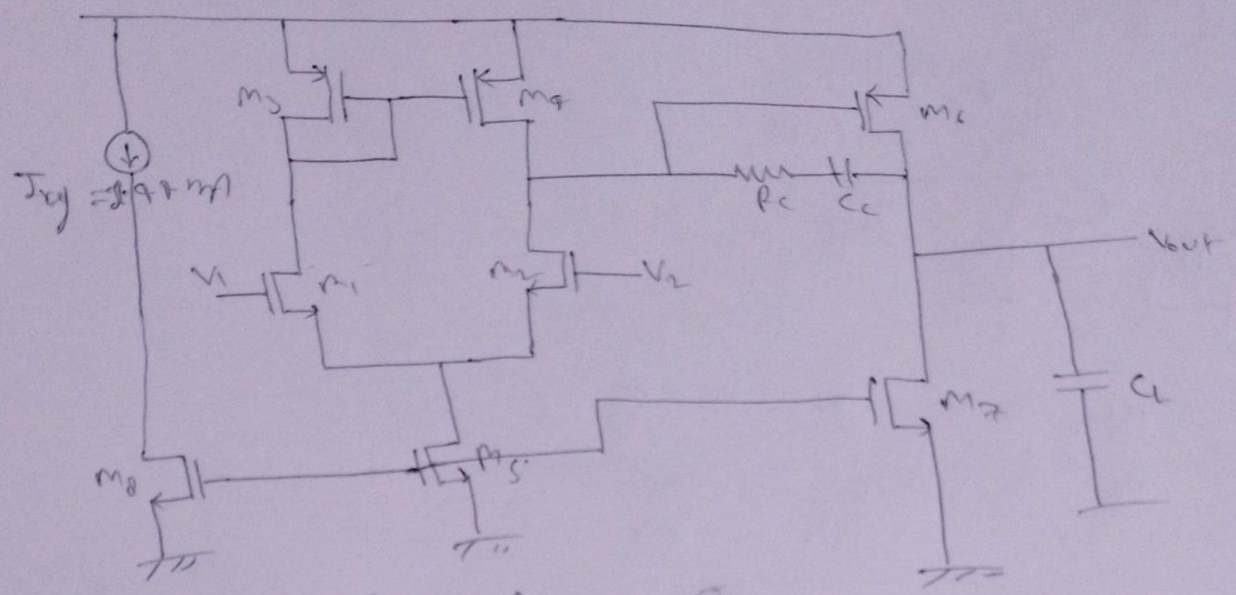
$\frac{I_7}{I_5} = \frac{(W/L)_7}{(W/L)_5}$

$(\frac{W}{L})_7 = \frac{16}{1.44}\times0.5 = 5.55$

Non-Dominant Pole : $p_2 = \frac{g_{m6}}{C_L} = \frac{160}{10^{-13}}\times10^{-6}$

$= 1600\,MHz$

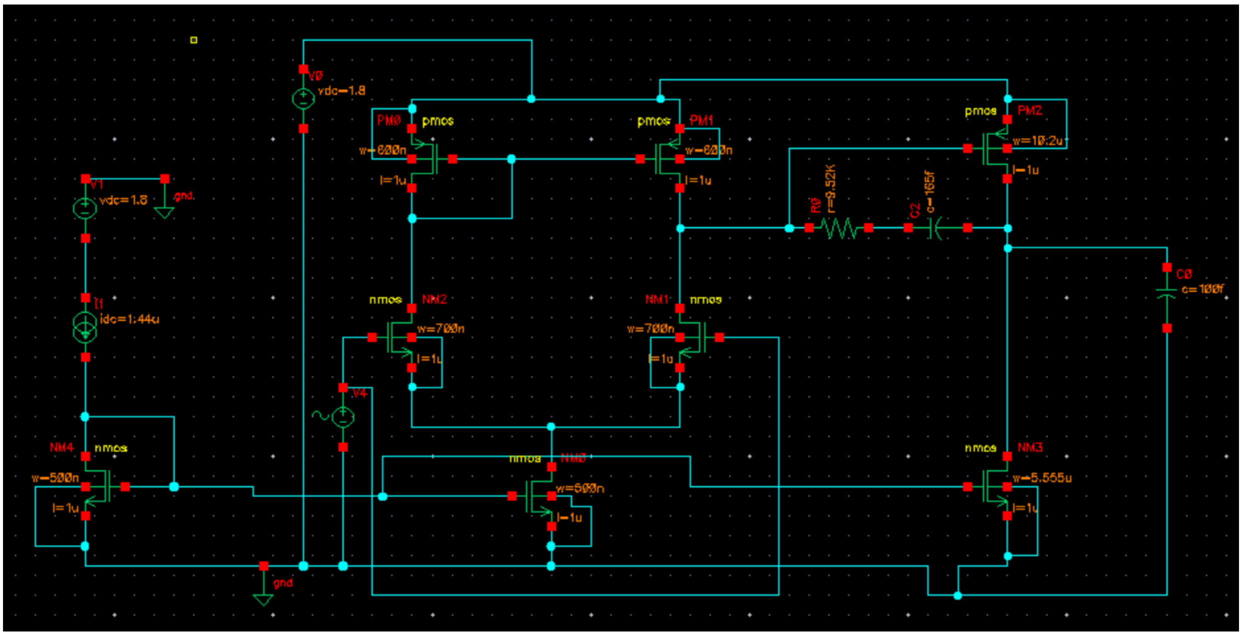
$R_z = \frac{1}{g_{m6}} = 6.25\,K\Omega$



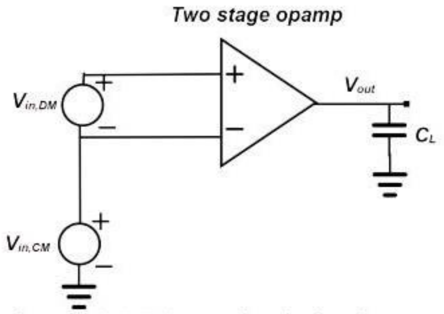
$$\left(\frac{W}{L}\right)_8 = \left(\frac{W}{L}\right)_5 = 0.5$$

Schematic:

After tuning $(W/L)_1 = (W/L)_2 = 0.7$, $(W/L)_6 = 10.2$, $R_z = 9.52K\Omega$



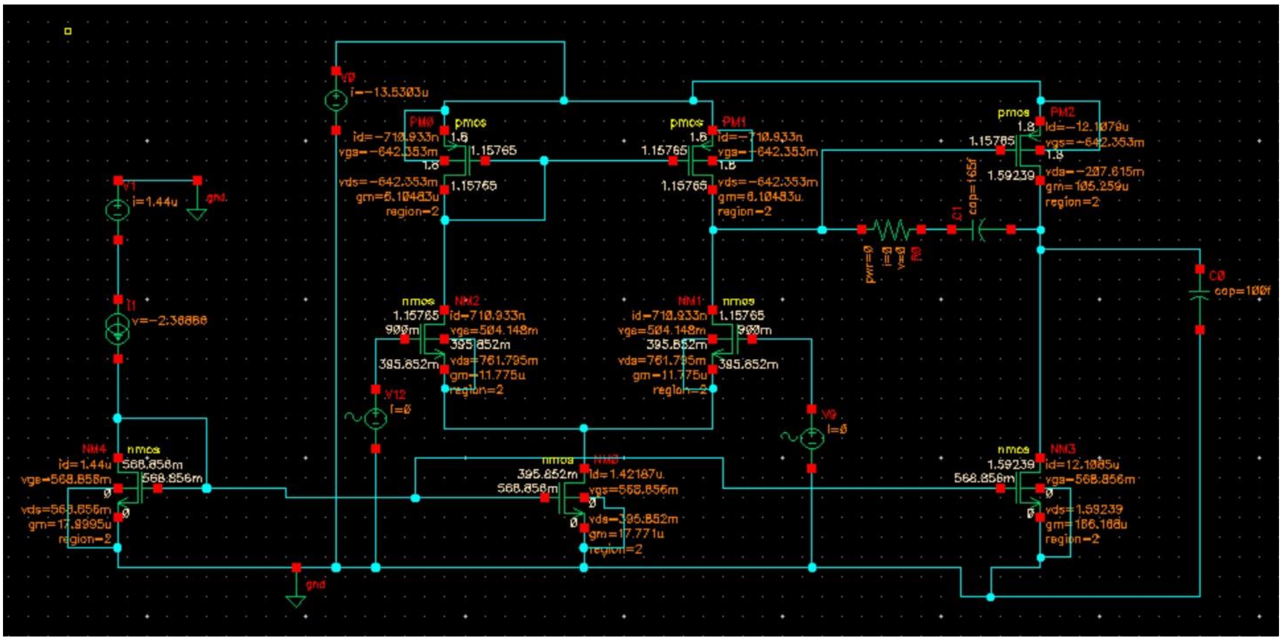
DC analysis



1. Obtain the common-mode range (CMR) curve by plotting the output voltage (V_{out}) with respect tothe common-mode input voltage (V_{ic}). (Sweep V_{ic} rail-to-rail)
2. Obtain the DC voltage transfer characteristic (VTC) curve by sweeping the differential input voltage (V_{id})and plotting the output voltage (V_{out}).
3. Find the input-referred DC offset voltage (V_{offset}) which drives the output voltage to mid-rail voltage.
4. Compute the differential-mode DC voltage gain curve by taking derivative of the VTC with respect to V_{id}.
5. At $V_{ic} = V_{DD}/2$ and $V_{id} = V_{offset}$, obtain the following values:
   a. DC differential-mode voltage gain (A_0)
   b. DC common-mode voltage gain(A_{cm0})
   c. Bias current into both the input terminals ($I_{bias,in1}$ and $I_{bias,in2}$)
   d. Bias current ($I_{bias} = (I_{bias,in1} + I_{bias,in2})/2$)
   e. Offset current ($I_{offset} = | I_{bias,in1} - I_{bias,in2} |$)
   f. Positive and negative output saturation limits (V^- to V^+)
   g. Power dissipation ($P_{diss} = V_{DD} * I_{DD}$)

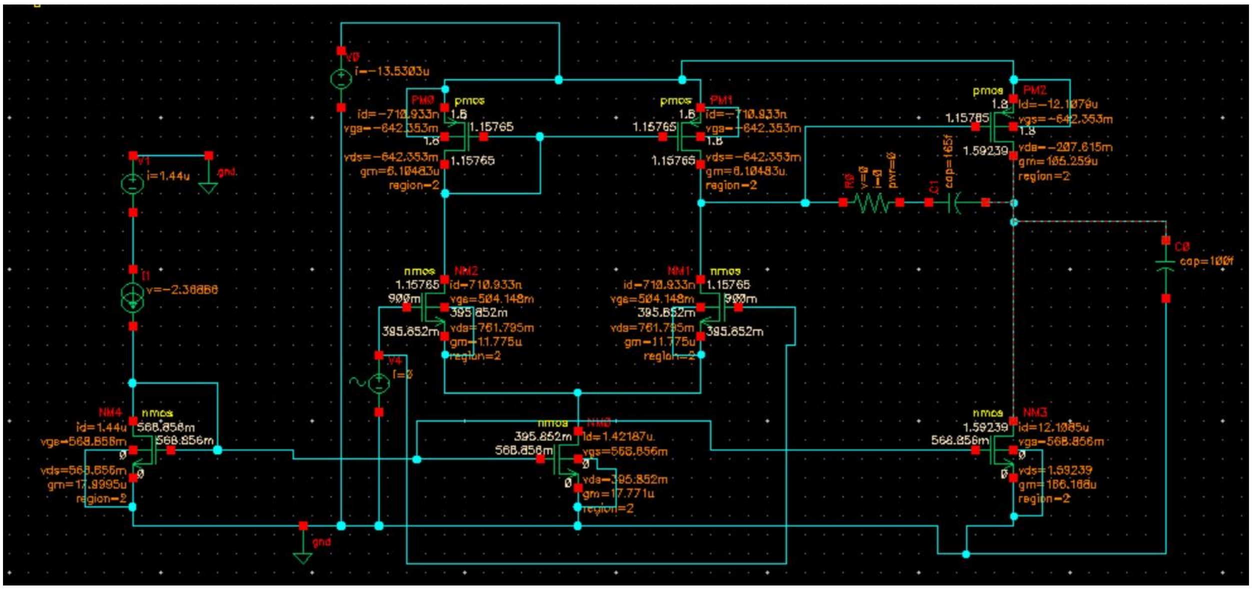
DC Analysis:

DC Operating point:

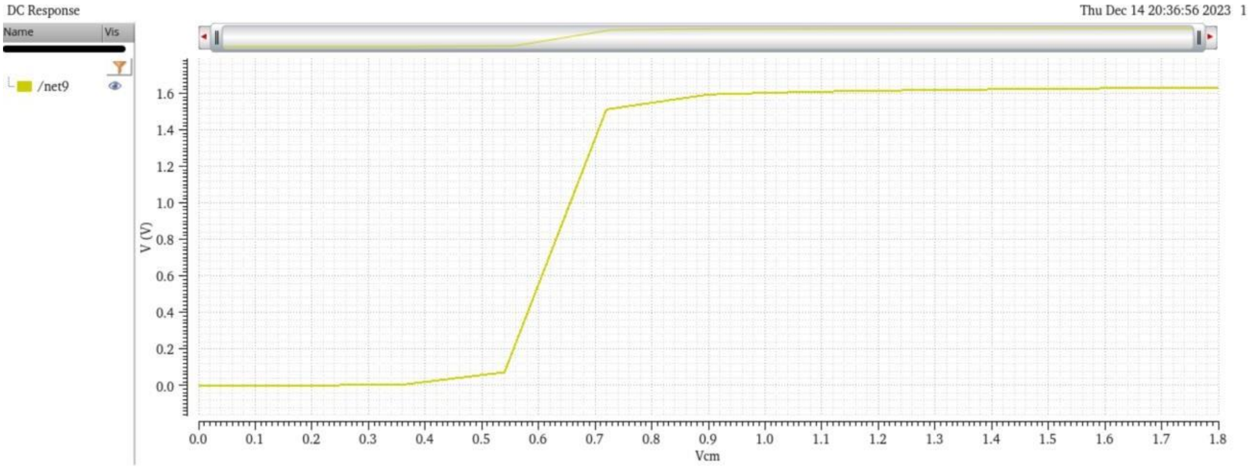


Common mode Range:

Test bench Schematic:

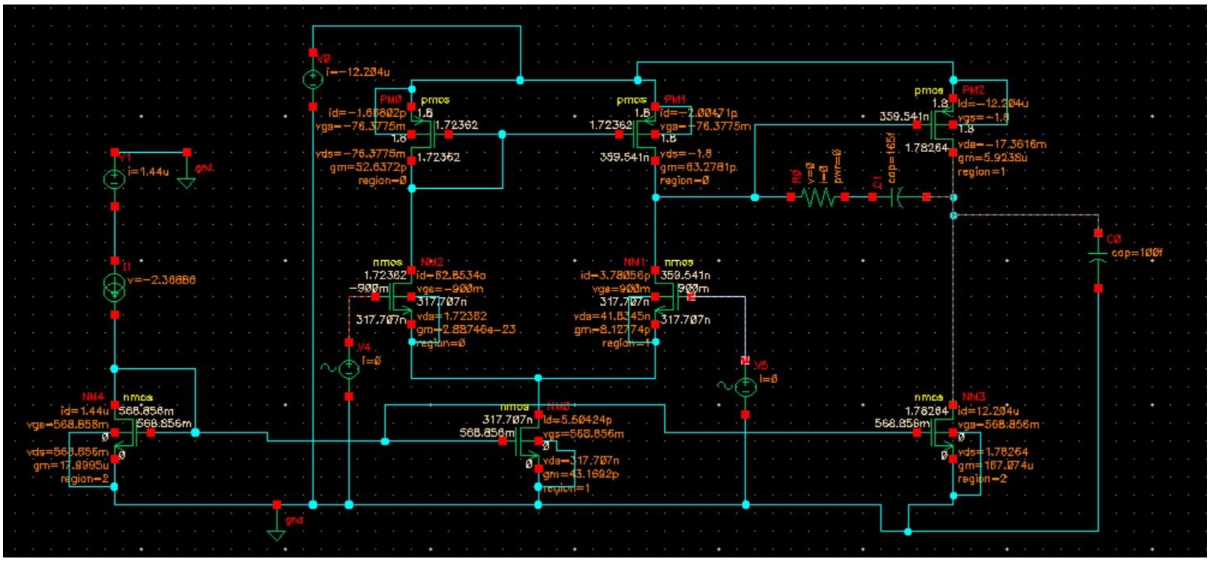


Waveform:

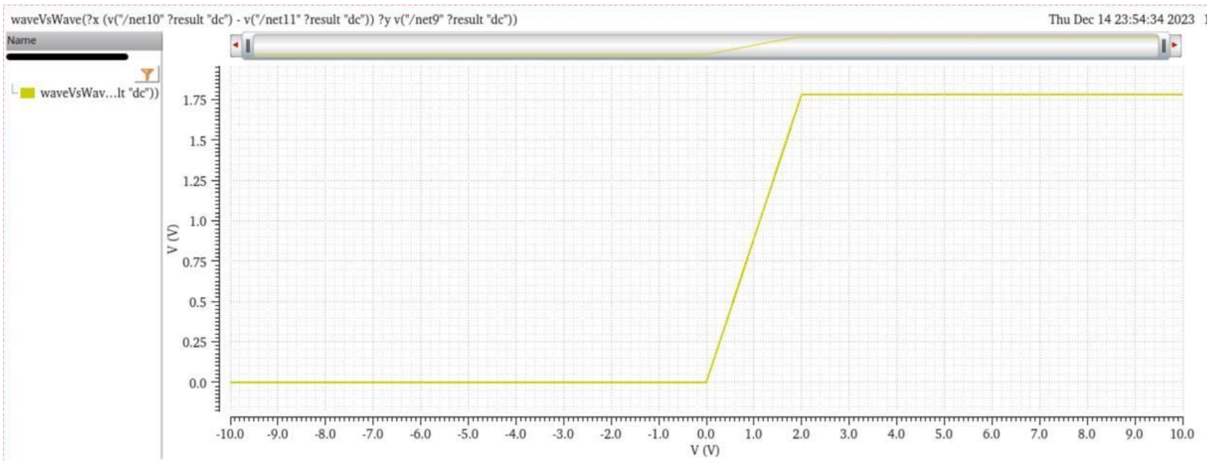


VTC for differential input (large signal):

Test bench schematic:

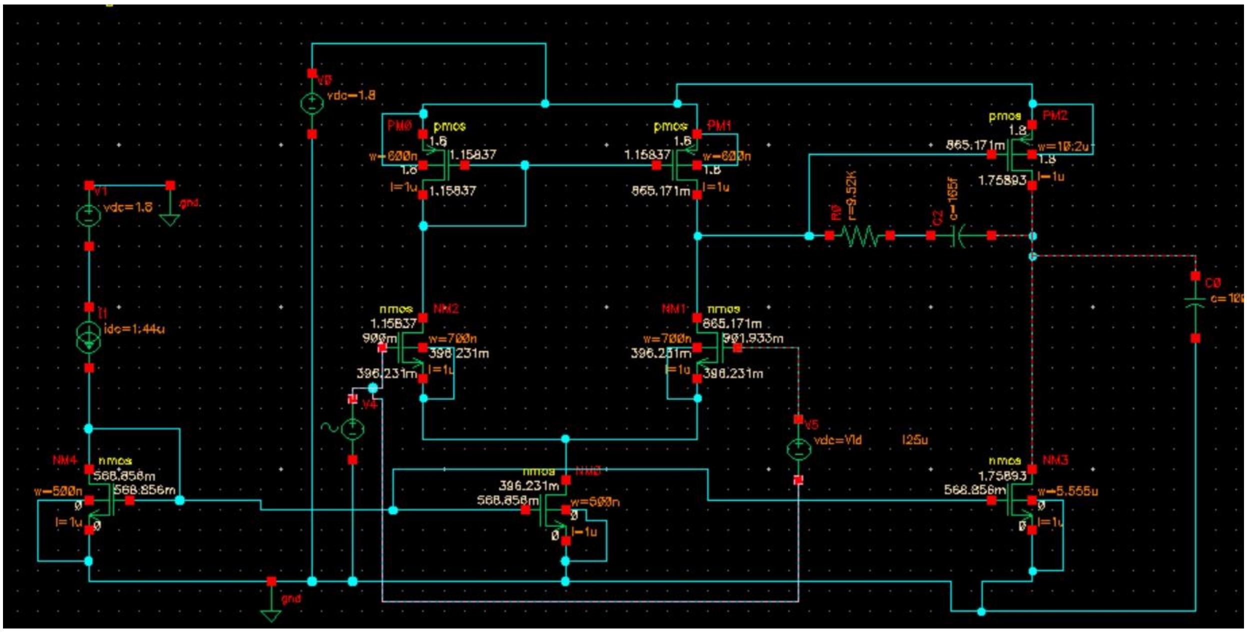


Waveform:

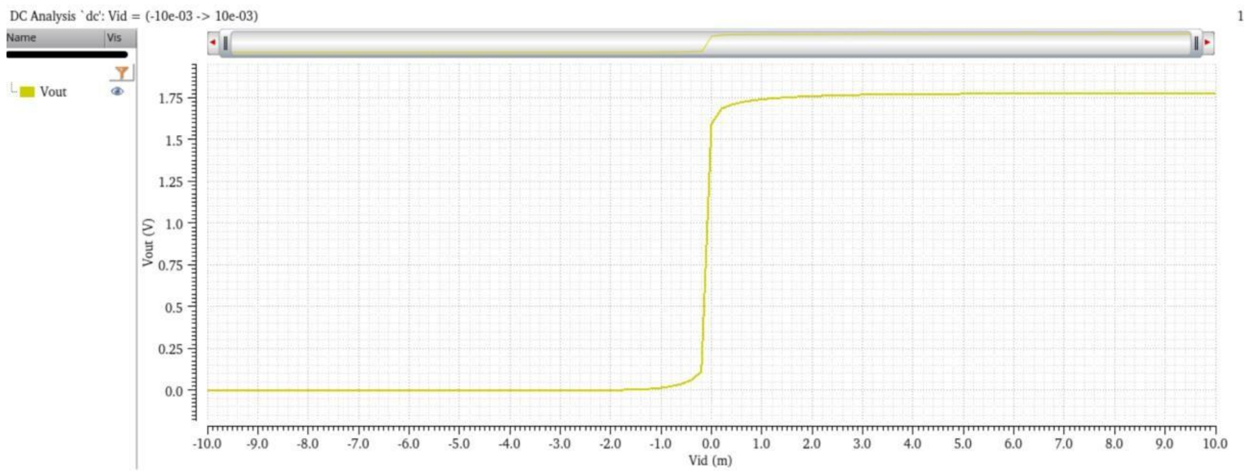


Small signal:

Test bench schematic:

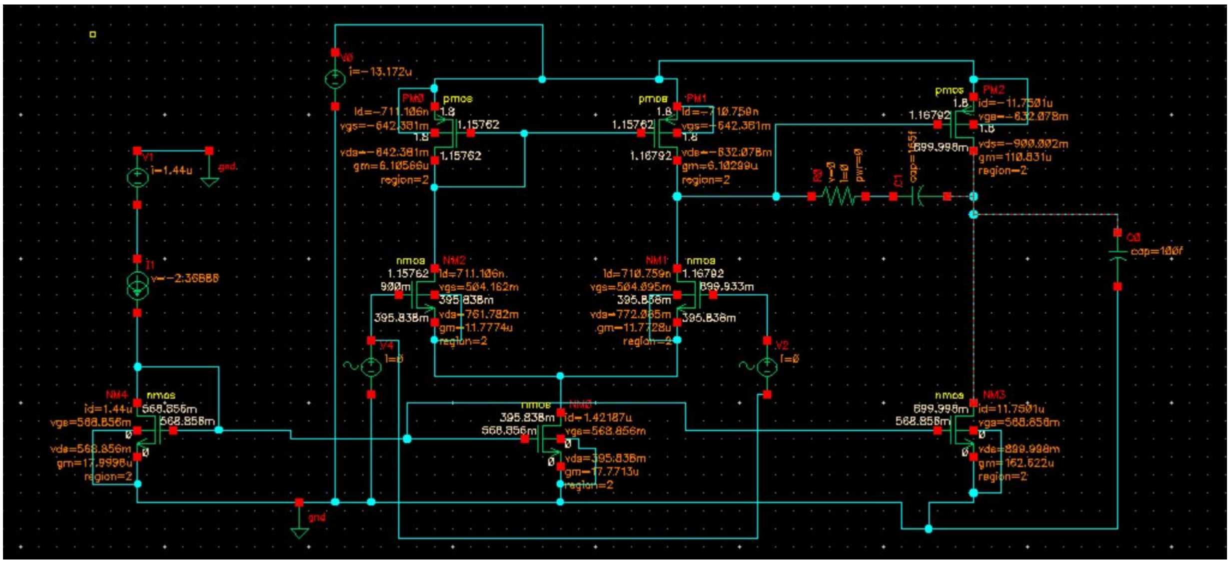


Waveform:

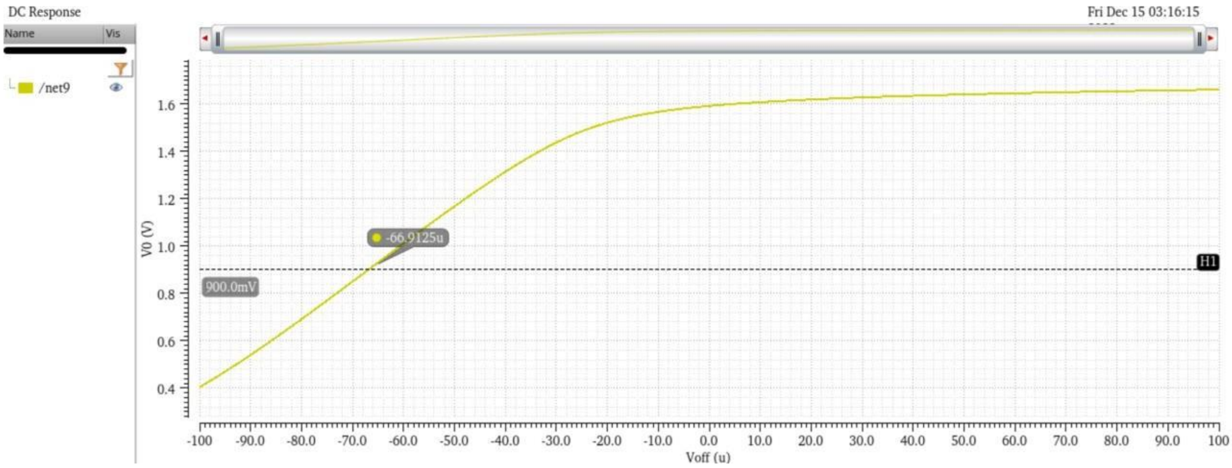


Input referred offset voltage:

Test bench schematic:

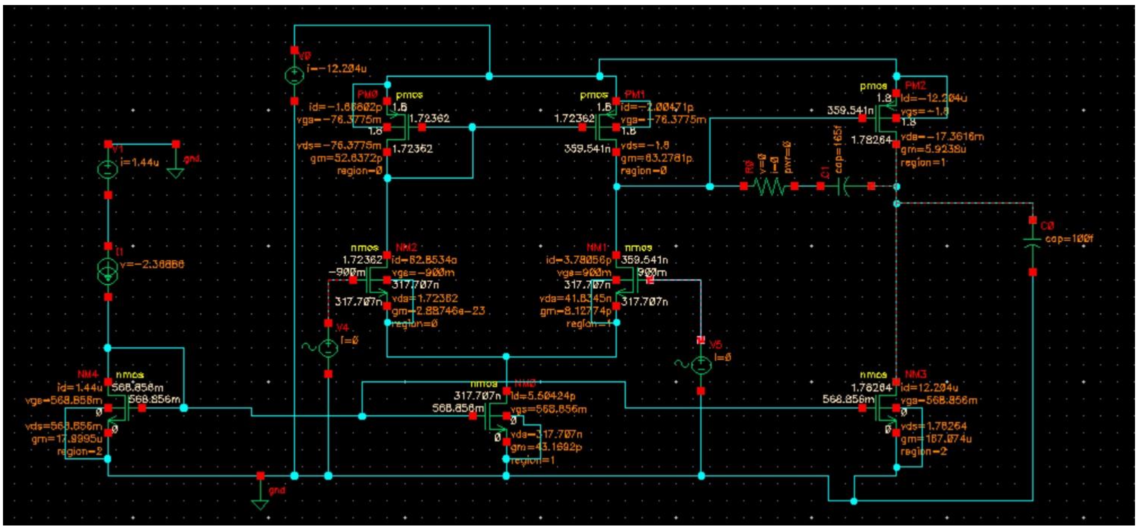


Waveform:

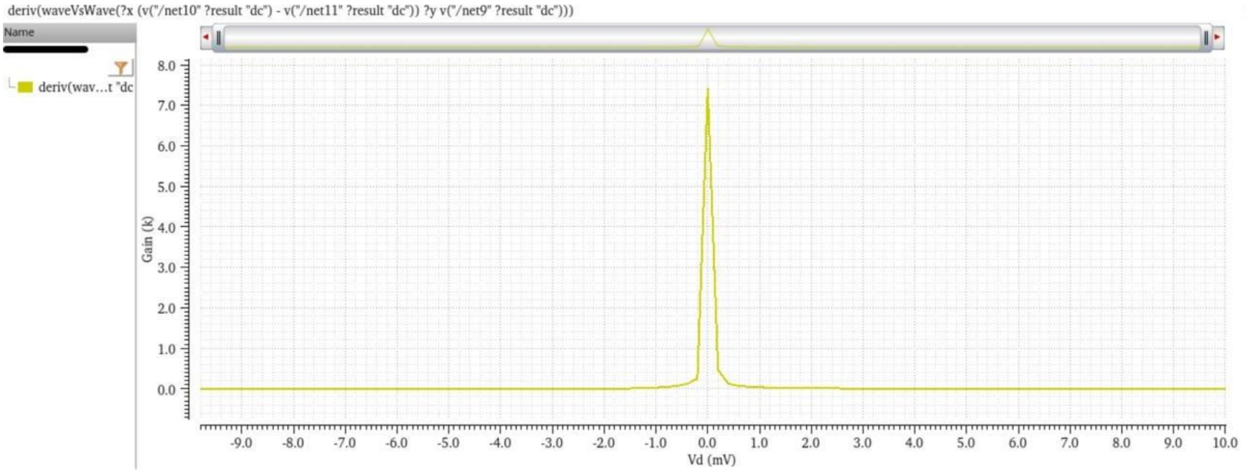


Differential Voltage gain:

Test bench schematic:

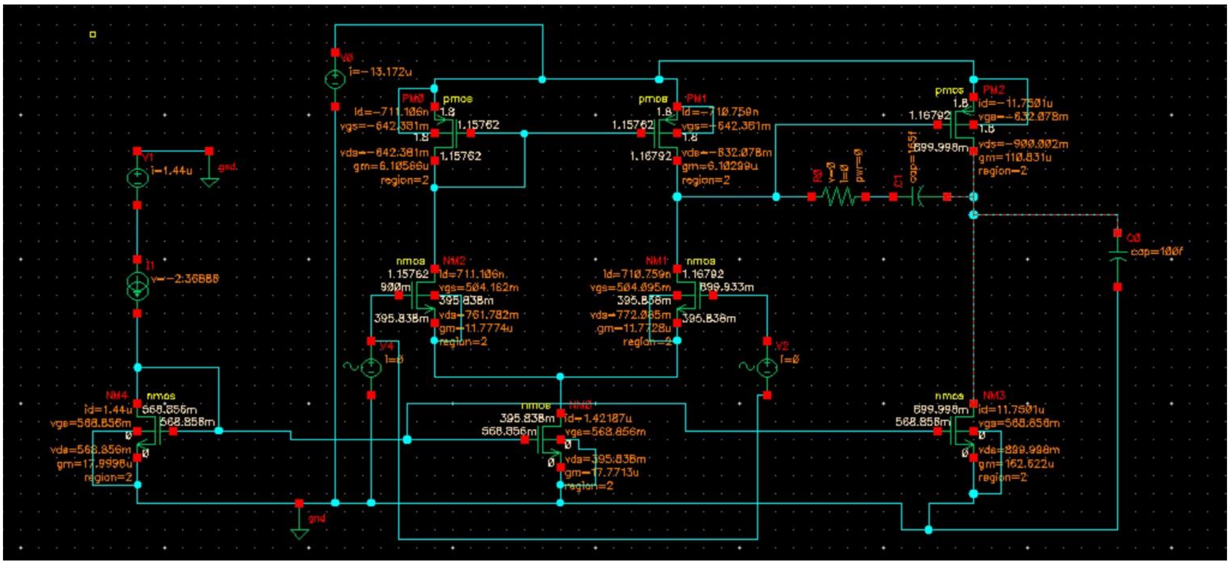


Waveform:



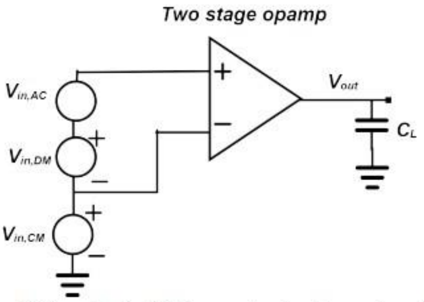
Op-parameters:

Test bench schematic:



DC differential voltage gain (A_o)	80dB
DC common mode gain (A_{cmo})	-10dB
Bias currents (I_{B1}, I_{B2})	0.711uA, 0.7107uA
Bias current ($I_B = (I_{B1} + I_{B2})/2$)	0.7109uA
Offset current ($I_{off} = (I_{B1} - I_{B2})$)	0.4nA
Positive and negative saturation limits	1.6V,250mV
Power dissipation	24.53uW

AC analysis



Set the DC condition for DC analysis (3) i.e. output voltage to mid-rail. Set the $V_{in,CM}$ to mid rail. Add another AC source Vin,AC in series with the differential input $V_{in,DC}$.

1. Obtain the frequency response by plotting magnitude and phase of the differential-mode voltage gain versus frequency from $1 Hz$ to $10\ GHz$ with 100 points/decade step size.

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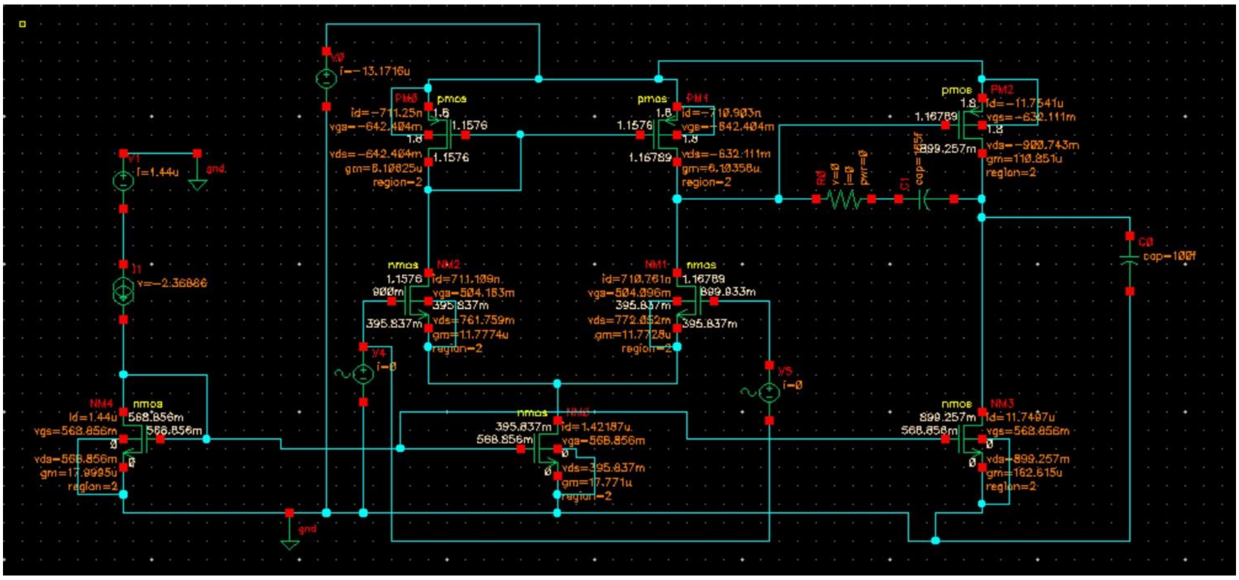
2. Find the $0\,dB$ magnitude crossover frequency (f_{0dB})
3. Find the phase at $f_{0dB}(Phase_{f_{0dB}})$
4. Calculate the phase margin in degree ($PM = 180 + Phase_{f_{0dB}}$)

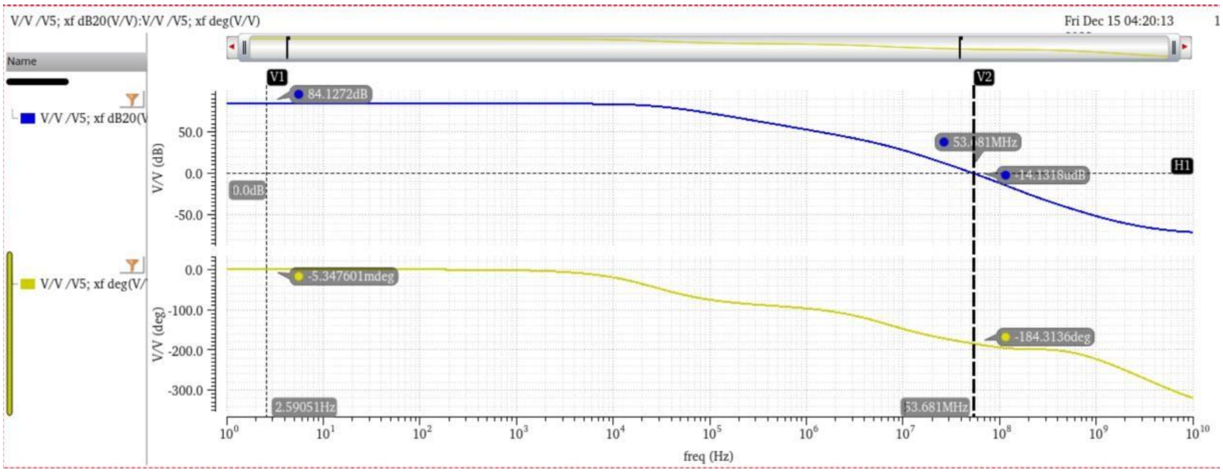
AC Analysis:

Test bench schematic - compensated



Frequency response:

Uncompensated:

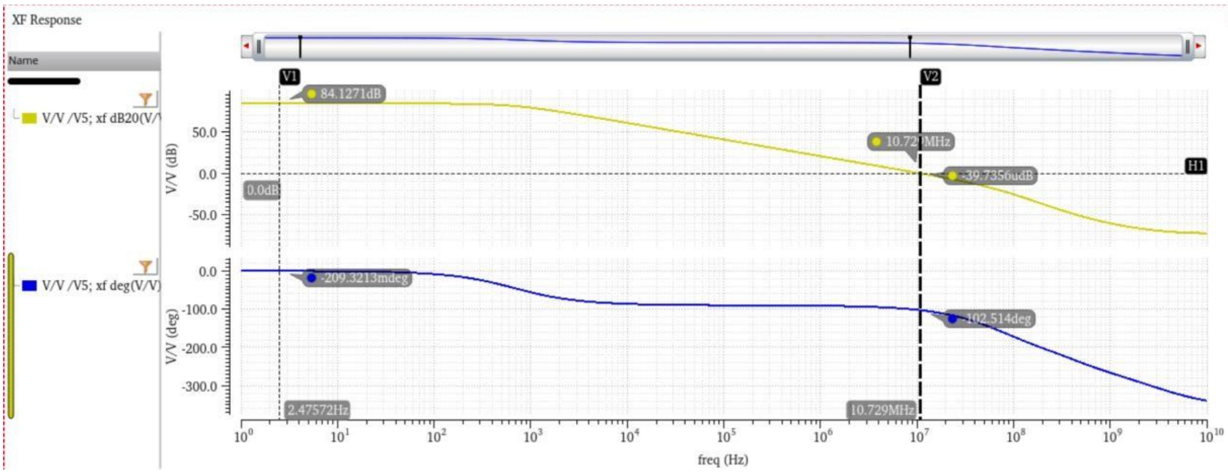


F_u (0dB cross over) = 53.81MHz

Phase (ϕ) = -184.31 deg

PM = 180+ ϕ = - 4.31 deg. Hence unstable.

Compensated:

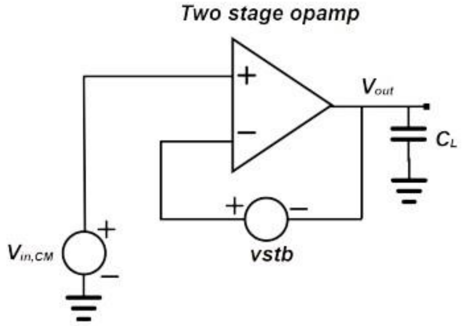


F_u (0dB cross over) = 10.72MHz

Phase (ϕ) = -102.51 deg

PM = 180+ ϕ = 77.49 deg. Hence stable.

Stability analysis

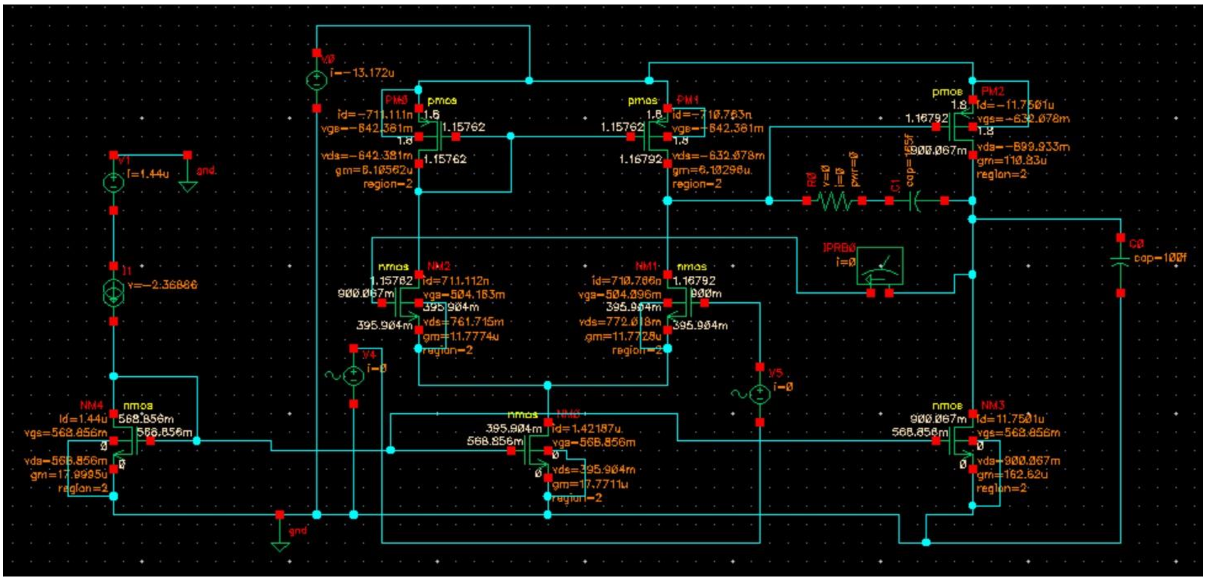


Connect the op-amp in the voltage follower configuration (unity gain feedback) and set the common mode voltage to mid-rail. Use vstb to break the loop in stb analysis as shown in the class.

1. Plot open loop gain and phase
2. Calculate gain and phase margins.

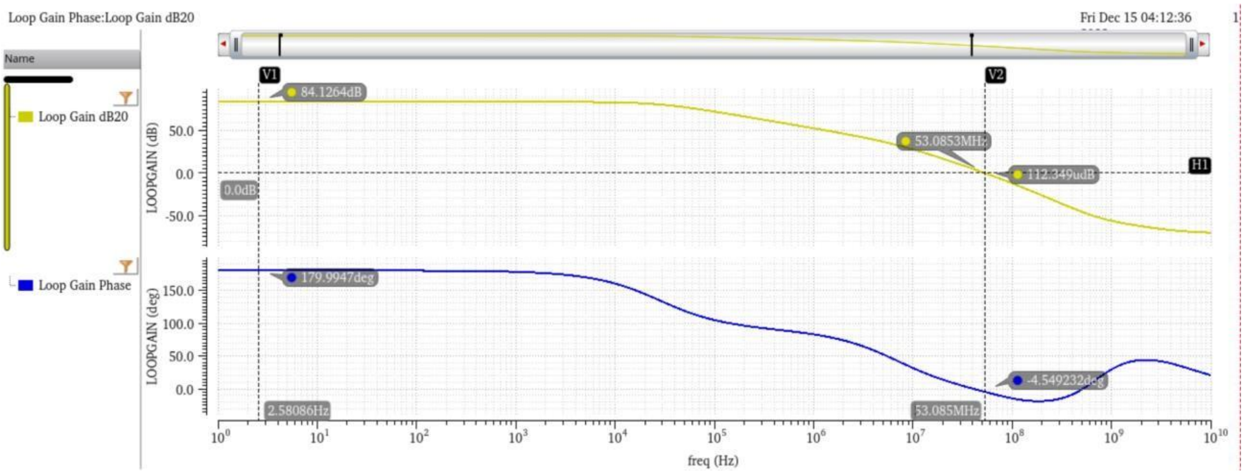
Stability analysis:

Test bench schematic - compensated:



Frequency response:

Uncompensated:



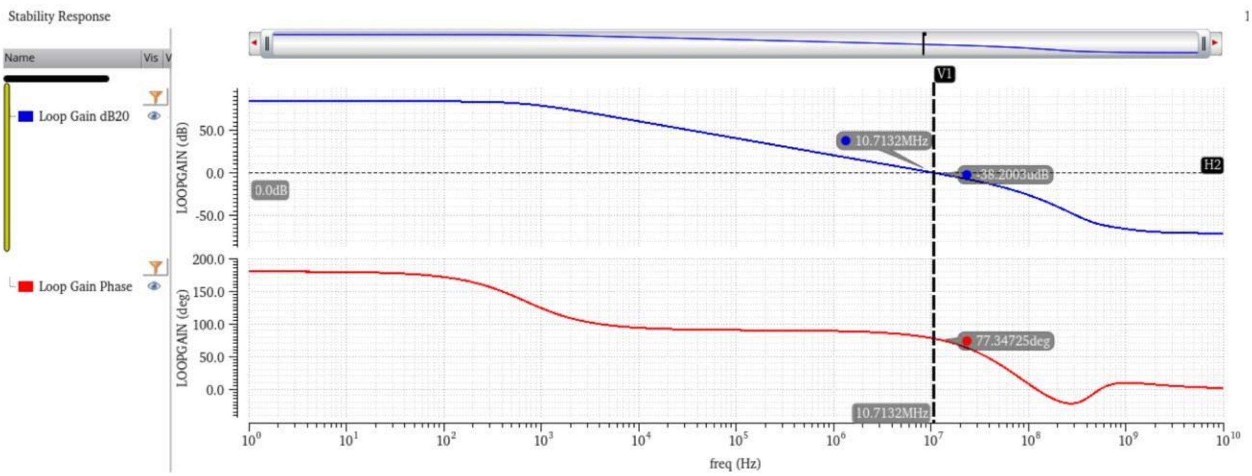
Cannot obtain the PM and GM as the system is unstable (+ve feedback system).

However, from the graph:

Phase of the loop gain at 0db magnitude is -4.5492 deg.

Magnitude of loop gain when its phase is 0 deg is 4.6562dB.

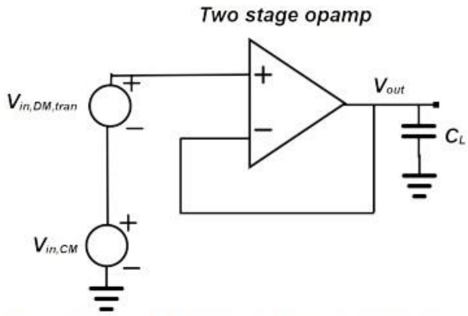
Compensated:



Gain margin: 29.4586dB

Phase margin: 77.343deg

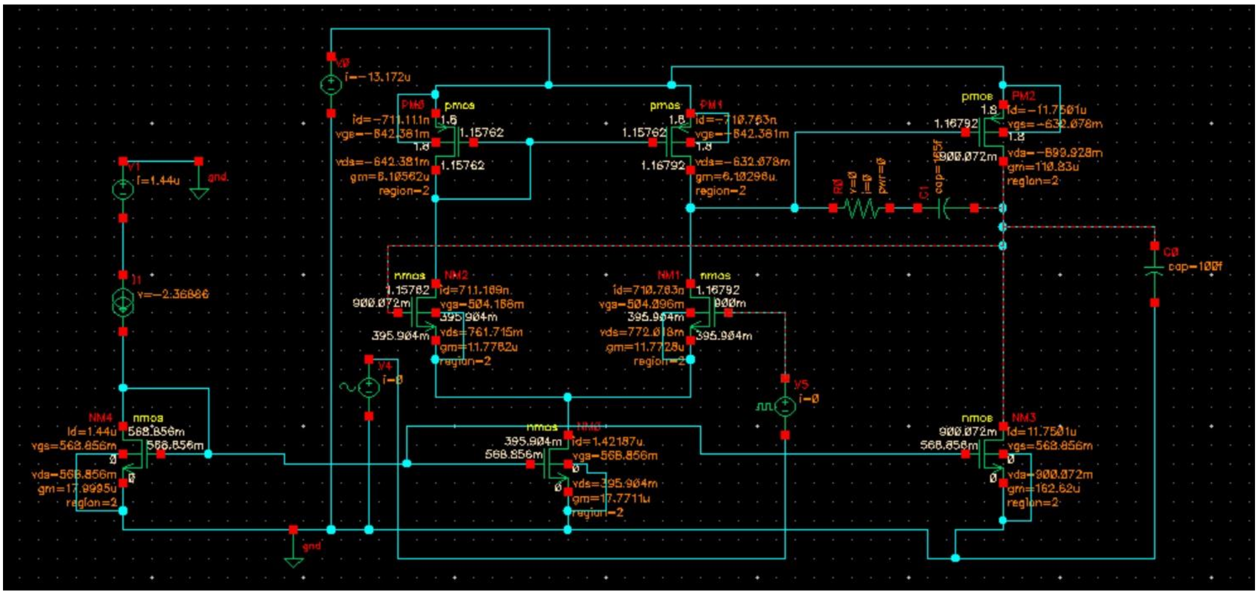
Transient analysis



1. Connect the op-amp in the voltage follower configuration (unity gain feedback) and set the common mode voltage to mid-rail. Excite the input (non-invertingterminal) with a (positive and negative) step signal with large (~ V_{DD}./2) amplitude.
2. Find the positive and negative slew rate (slope of the output V/s) from the transient response.

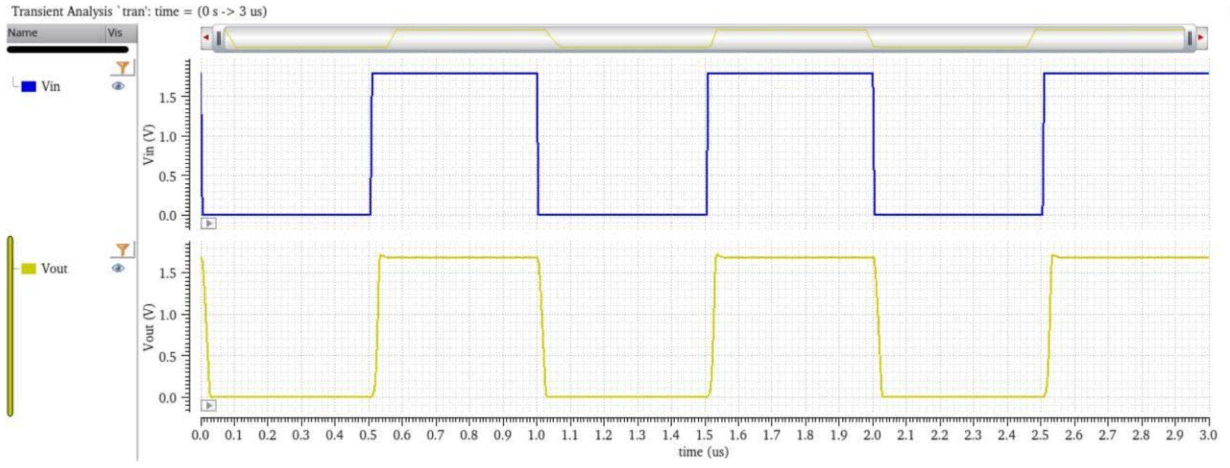
Transient Analysis:

Test bench schematic - compensated:

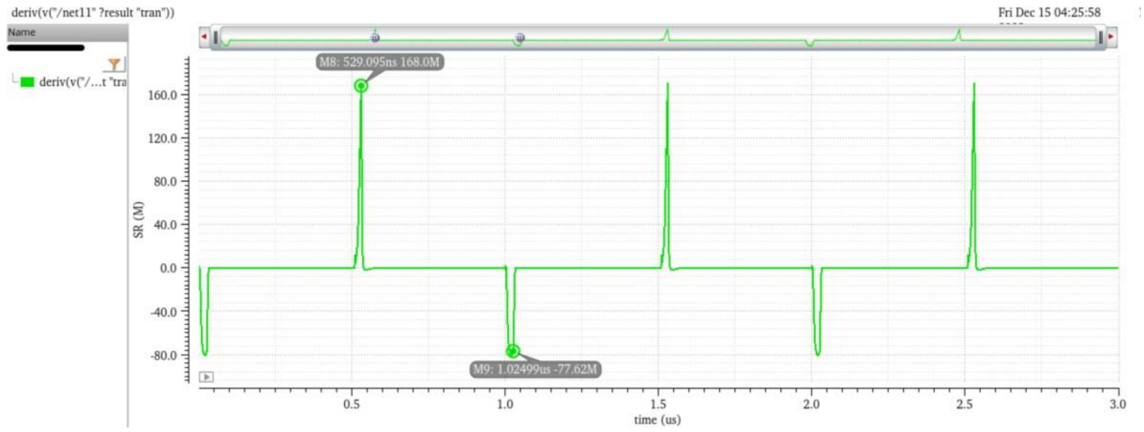


Uncompensated:

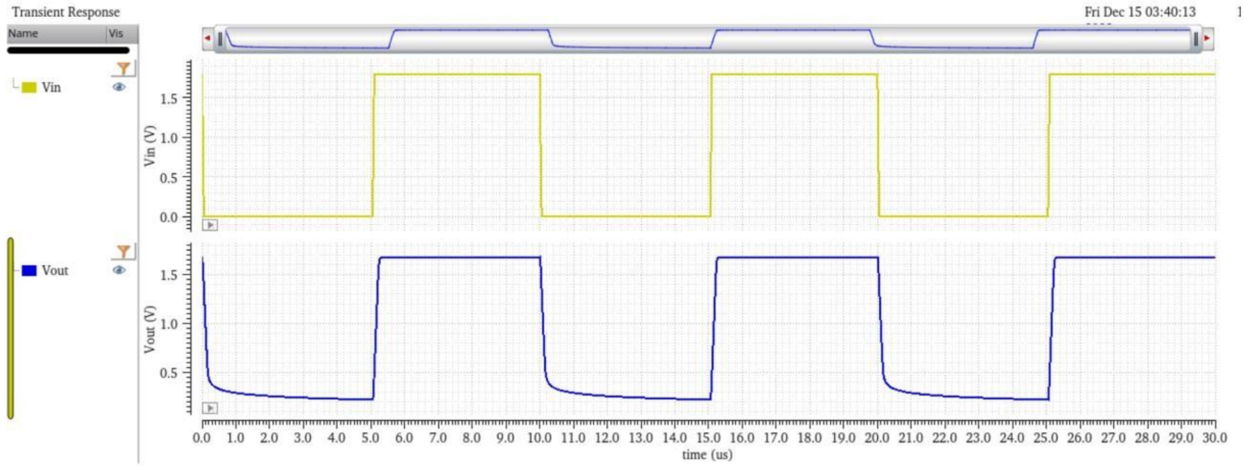
Waveform:



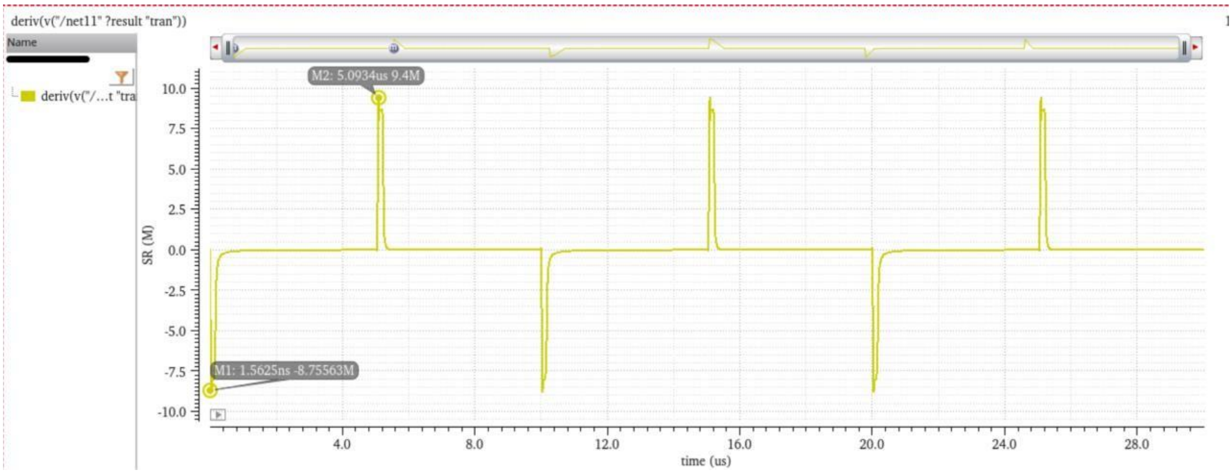
Slew rate:



Compensated:



Slew rate:



Positive slew rate: 9.4M V/s
Negative slew rate: -8.755M V/s

Op-amp parameters:

M1	W1 = 0.7um	L1 = 1um
M2	W2 = 0.7um	L2 = 1um
M3	W3 = 0.6um	L3 = 1um
M4	W4 = 0.8um	L4 = 1um
M5	W5 = 0.5um	L5 = 1um
M6	W6 = 10.2um	L6 = 1um
M7	W7 = 5.55um	L7 = 1um
M8	W8 = 0.5um	L8 = 1um

Gain	80dB
Gain – Bandwidth	10.72MHz
Common mode gain	-10dB
CMRR	70dB
PM	77deg
Bias current	0.7109ua
Offset current	0.4nA
Power dissipation	24.53uW
Slew rate	9.4MV/s, -8.755V/s
Input offset voltage	-66.9125uV