PROCESSOR FUNDAMENTALS

Question 1

(b) The ACC is a general purpose register. The IX is a special purpose register.

Identify **two** other special purpose registers used in the fetch-execute cycle **and** describe their role in the cycle.

Register 1 .....

Role .....

.....

.....

Register 2 .....

Role .....

.....

.....

[4]

Question 2

(iii) The peripheral devices are plugged into USB ports of the computer.

Describe **two** benefits of connecting the peripheral devices using a USB port.

1 .....

.....

.....

.....

2 .....

.....

.....

.....

[4]

Question 3

(c) Billy's computer has several ports.

(i) State the purpose of a port.

.....

..... [1]

(ii) Identify **one** type of port.

.....

..... [1]

Question 4

3 The fetch-execute cycle is shown in register transfer notation.

```
01      MAR ← [PC]
02      PC ← [PC] - 1
03      MDR ← [MAR]
04      CIR ← [MAR]
```

(a) There are **three** errors in the fetch-execute cycle shown.

Identify the line number of each error and give the correction.

Line number .....

Correction .....

Line number .....

Correction .....

Line number .....

Correction .....

[3]

(b) A processor's instruction set can be grouped according to their function. For example, one group is the input and output of data.

Identify **two** other groups of instructions.

1 .....

.....

2 .....

.....

[2]

Question 5

(c) The processor handles interrupts within the fetch-execute cycle.

(i) Give **one** example of a hardware interrupt and **one** example of a software interrupt.

Hardware .....

.....

Software .....

.....

[2]

(ii) Explain how the processor handles an interrupt.

.....

.....

.....

.....

.....

.....

.....

.....

.....

..... [5]

Question 6

1 Von Neumann is an example of a computer architecture.

(a) The diagram has registers used in Von Neumann architecture on the left and descriptions on the right.

Draw **one** line to match each register with its correct description.

Register	Description
Current Instruction Register	Stores the data that has just been read from memory, or is about to be written to memory
Memory Address Register	Stores the instruction that is being decoded and executed
Program Counter	Stores the address of the input device from which the processor accesses the instruction
Memory Data Register	Stores the address of the next instruction to be read
	Stores the address of the memory location about to be written to or read from

[4]

(b) Many components of the computer system transfer data between them using buses. One example of a bus is an address bus.

(i) Name **two** other buses that exist within a computer and give the purpose of each.

Bus 1 .....

Purpose .....

.....

.....

Bus 2 .....

Purpose .....

.....

.....

[4]

(ii) State the benefit of increasing the address bus width from 16 bits to 32 bits.

.....

..... [1]

Question 7

8 The Von Neumann model uses a series of registers.

(a) Explain what is meant by the term **register**.

.....

.....

.....

.....[2]

(b) (i) Explain the purpose of the Memory Data Register (MDR).

.....

.....

.....

.....[2]

(ii) Name **two** registers, other than the MDR, that are used in the fetch-execute cycle.

Register 1 .....

Register 2 .....

[2]

(c) X is a register. The current contents of X are:

1	0	0	0	0	1	1	1

(i) The current contents of register X represent an unsigned binary integer.

Convert the value in X into denary.

.....[1]

(ii) The current contents of register X represent a Binary Coded Decimal.

Convert the value in X into denary.

.....[1]

(iii) The current contents of register X stores a two's complement binary integer.

Convert the value in X into denary.

.....[1]

Question 8

3 A computer is designed using the Von Neumann model.

(a) Describe the role of the Arithmetic and Logic Unit (ALU) and Control Unit (CU) in the Von Neumann model.

ALU .....

.....

.....

.....

CU .....

.....

.....

.....

[4]

(b) Describe the role of the Status Register and Program Counter (PC).

Status Register .....

.....

.....

.....

PC .....

.....

.....

.....

[4]

Question 9

4 A student has written the steps of the fetch stage of the fetch-execute (FE) cycle in register transfer notation. The student has made some errors.

```
Line 1      MDR ← [PC]
Line 2      PC ← PC + 1
Line 3      MDR ← [MAR]
Line 4      CIR ← PC
```

(a) Identify the line numbers of **three** errors that the student has made. Write the correct notation for each error.

Line number of error	Correct notation

[3]

(b) One stage of the FE cycle includes checking for interrupts.

(i) Give **three** different events that can generate an interrupt.

1 .....

2 .....

3 .....

[3]

(ii) Explain how interrupts are handled during the fetch-execute cycle.

.....

.....

.....

.....

.....

.....

.....

.....

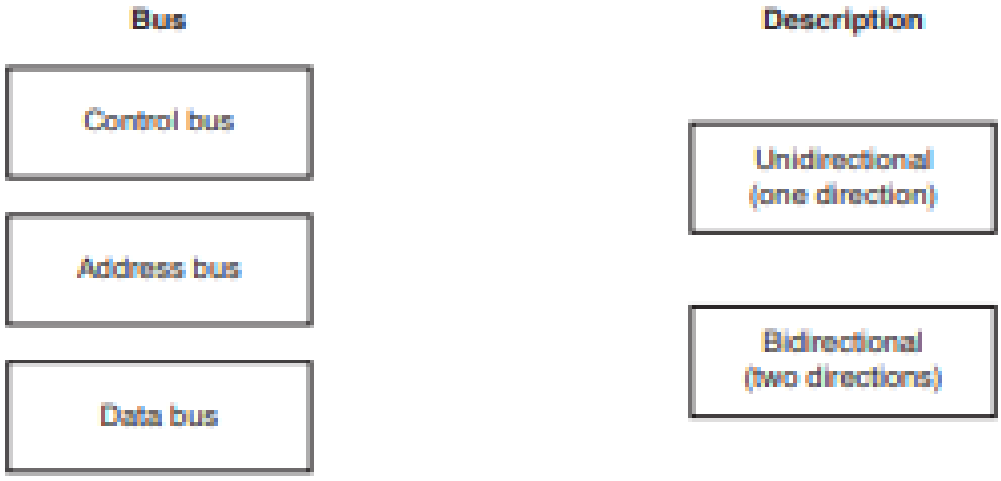
.....

..... [5]

(c) The processor uses buses in the FE cycle.

The diagram shows three buses and two descriptions.

Draw **one** line from each bus to its appropriate description.



[2]

Question 10

6 The fetch-execute (FE) cycle uses special purpose registers.

(a) The stages in the FE cycle are shown in register transfer notation.

```
MAR ← [.....]

PC ← PC + 1

..... ← [ [MAR] ]

..... ← [MDR]
```

(i) The steps shown in **part (a)** are incomplete.

Write the missing register names in the spaces in **part (a)**. [3]

(ii) The third instruction `[ [MAR] ]` has double brackets.

State the purpose of the double brackets.

.....

.....[1]

(b) One stage of the FE cycle includes checking for interrupts.

State what is meant by an **interrupt**.

.....

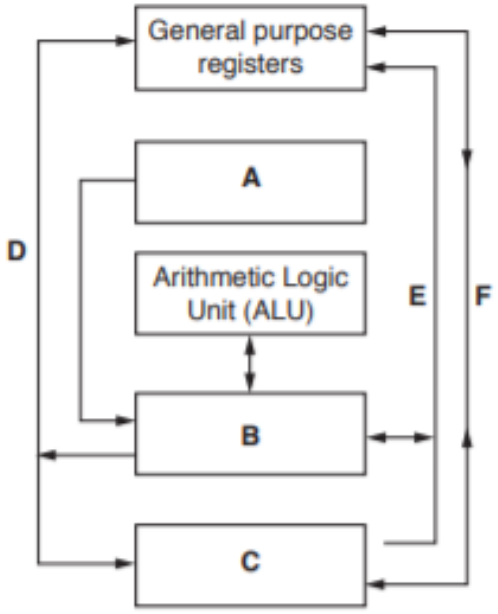
.....

.....

.....[2]

Question 11

4 **(a)** The diagram shows the components and buses found inside a typical Personal Computer (PC).



Some components and buses only have labels **A** to **F** to identify them.

For each label, choose the appropriate title from the following list. The title for label **D** is already given.

- Control bus
- System clock
- Data bus
- Control unit
- Main memory
- Secondary storage

A .....

B .....

C .....

D Address bus

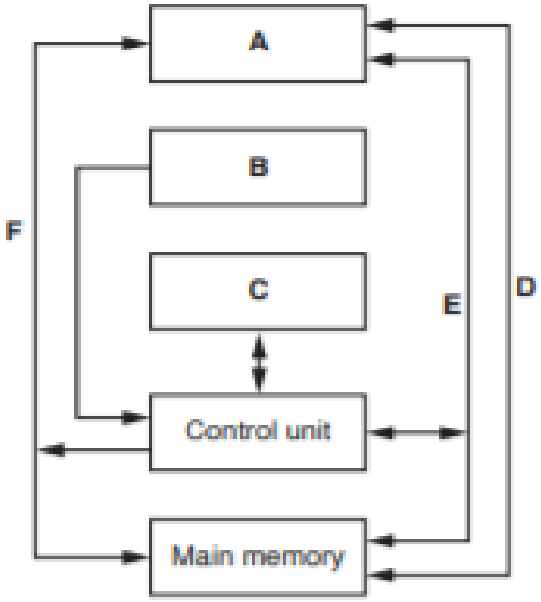
E .....

F .....

[5]

Question 12

4 The following diagram shows the components and buses found inside a typical personal computer (PC).



(a) Some components and buses only have labels **A** to **F** to identify them.

For each label, choose the appropriate title from the following list. The title for label **D** is already given.

- Control bus
- Address bus
- Arithmetic Logic Unit (ALU)
- General purpose registers
- Secondary storage
- System clock

A .....

B .....

C .....

D Data bus

E .....

F .....

[5]

(b) Clock speed is a factor that affects the performance of a PC. Explain this statement.

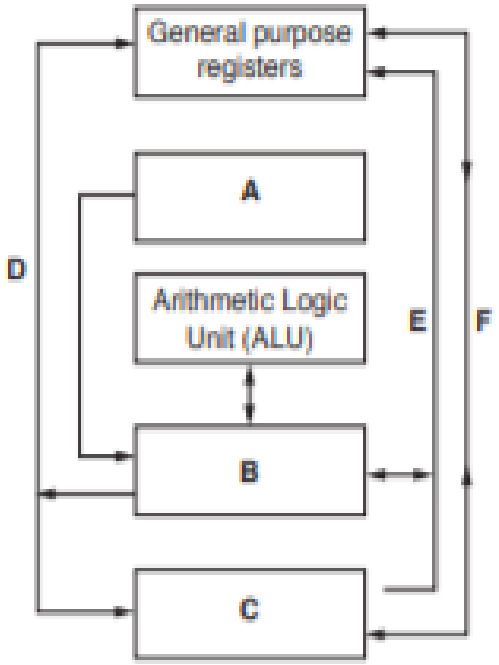
.....

.....

.....[2]

Question 13

4 **(a)** The diagram shows the components and buses found inside a typical Personal Computer (PC).



Some components and buses only have labels **A** to **F** to identify them.

For each label, choose the appropriate title from the following list. The title for label **D** is already given.

- Control bus
- System clock
- Data bus
- Control unit
- Main memory
- Secondary storage

A .....

B .....

C .....

D Address bus

E .....

F .....

[5]

Question 14

3 **(a)** Describe how special purpose registers are used in the fetch stage of the fetch-execute cycle.

.....

.....

.....

.....

.....

.....

.....

.....[4]

(b) Use the statements A, B, C and D to complete the description of how the fetch-execute cycle handles an interrupt.

A	the address of the Interrupt Service Routine (ISR) is loaded to the Program Counter (PC).
B	the processor checks if there is an interrupt.
C	when the ISR completes, the processor restores the register contents.
D	the register contents are saved.

At the end of the cycle for the current instruction ..... .

If the interrupt flag is set, ... , ... and ..... .

The interrupted program continues its execution.

[4]

Question 15

8 (a) Explain how the width of the data bus and system clock speed affect the performance of a computer system.

Width of the data bus .....

.....

.....

.....

Clock speed .....

.....

.....

.....[3]

(c) The table shows six stages in the von Neumann fetch-execute cycle.

Put the stages into the correct sequence by writing the numbers 1 to 6 in the right hand column.

Description of stage	Sequence number
the instruction is copied from the Memory Data Register (MDR) and placed in the Current Instruction Register (CIR)	
the instruction is executed	
the instruction is decoded	
the address contained in the Program Counter (PC) is copied to the Memory Address Register (MAR)	
the value in the Program Counter (PC) is incremented so that it points to the next instruction to be fetched	
the instruction is copied from the memory location contained in the Memory Address Register (MAR) and is placed in the Memory Data Register (MDR)	

[6]

Question 16

5 (a) Name and describe three buses used in the von Neumann model.

Bus 1.....

Description.....

.....

.....

Bus 2.....

Description.....

.....

.....

Bus 3 .....

Description.....

.....

..... [6]

(b) The sequence of operations shows, in register transfer notation, the fetch stage of the fetch-execute cycle.

```
1   MAR ← [PC]
2   PC  ← [PC] + 1
3   MDR ← [[MAR]]
4   CIR ← [MDR]
```

- `[register]` denotes contents of the specified register or memory location
- step 1 above is read as "the contents of the Program Counter are copied to the Memory Address Register"

(i) Describe what is happening at step 2.

.....

..... [1]

(ii) Describe what is happening at step 3.

.....

.....

..... [1]

(iii) Describe what is happening at step 4.

.....

..... [1]

(c) Describe what happens to the registers when the following instruction is executed:

LDD 35

.....

.....

.....

..... [2]

(d) (i) Explain what is meant by an interrupt.

.....

.....

.....

..... [2]

(ii) Explain the actions of the processor when an interrupt is detected.

.....

.....

.....

.....

.....

.....

.....

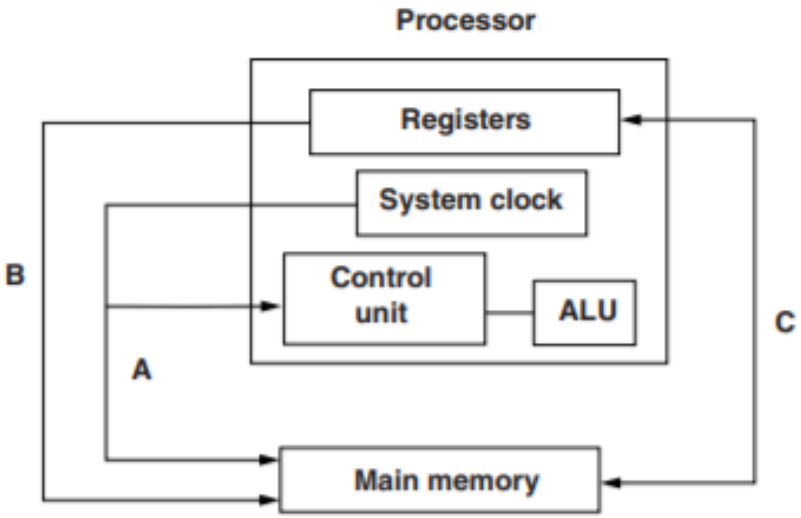
.....

.....

..... [4]

Question 17

2 (a)



The diagram above shows a simplified form of processor architecture.

Name the three buses labelled A, B and C.

A .....

B .....

C .....

[3]

(b) State the role of each of the following special purpose registers used in a typical processor.

Program Counter .....

.....

Memory Data Register .....

.....

Current Instruction Register .....

.....

Memory Address Register .....

.....

[4]

Question 18

2 **(a)** Describe how buffers and interrupts are used when printing a large document stored on a hard drive.

.....

.....

.....

.....

.....

.....

.....

.....

..... [4]

Question 19

1 Describe the function of the following parts of a processor:

(i) control unit

.....

.....[1]

(ii) main memory unit

.....

.....[1]

(iii) arithmetic and logic unit (ALU)

.....

.....[1]

Question 20

1 **(a)** Describe the terms *buffer* and *interrupt*.

buffer .....

.....

.....

interrupt .....

.....

..... [2]

(b) **(i)** Explain the role of the buffer and interrupts when a large document of over 200 pages is sent to a laser printer.

.....

.....

.....

.....

.....

.....

.....

.....

..... [3]

(ii) The use of two buffers would speed up the printing process.

Explain why.

.....

.....

.....

.....

..... [2]

Question 21

5 **(a)** What is meant by an interrupt?

.....

.....

..... [1]

(b) A user starts the printing of a document, and then carries on editing a second document while printing continues.

Explain how interrupts make this possible.

.....

.....

.....

.....

.....

.....

.....

.....

.....

..... [4]