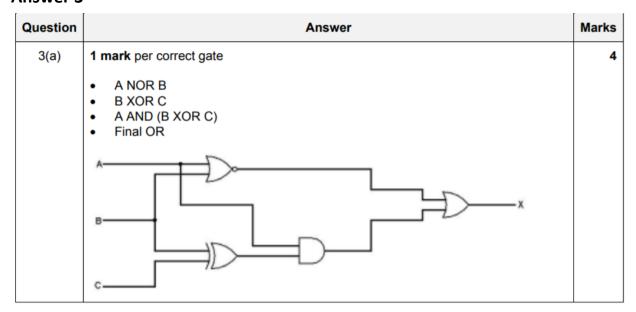
ANSWERS LOGIC GATE

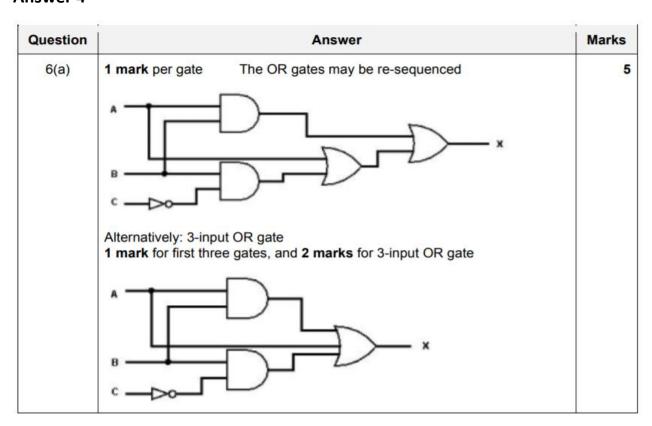
	Answer							
1 mark for each pair of correct answers (shaded)								
A	В	С	Working space	x				
0	0	0		0				
0	0	1		1				
0	1	0		1				
0	1	1		0				
1	0	0		1				
1	0	1		1				
1	1	0		0				
1	1	1		0				
	0 0 0	A B 0 0 0 0 0 1 0 1 1 0	A B C 0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1	A B C Working space 0 0 0 0 0 1 0 1 0 0 1 1 0 1 1 1 0 0 1 0 1	1 mark for each pair of correct answers (shaded) A B C Working space X 0 0 0 0 0 0 1 1 0 1 0 1 0 1 1 0 1 0 0 1 1 0 0 1 1 0 1 1 1 0 1 1 1 0 1 0	1 mark for each pair of correct answers (shaded) A B C Working space X 0 0 0 0 0 0 1 1 0 1 0 1 0 1 1 0 1 0 0 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0 0 0		

Question			Answe	r	Marks				
5(b)		mark for name, 1 mark for symbol, 1 mark for truth table NAND							
	Inp	out	0.1-1						
	Α	В	Output						
	0	0	1						
	0	1	1						
	1	0	1						
	1	1	0						
	NOR	>							
	Ing	out	Output						
	A	В	Output						
	0	0	1						
	0	1	0						
	1	0	0						
	1	1	0						

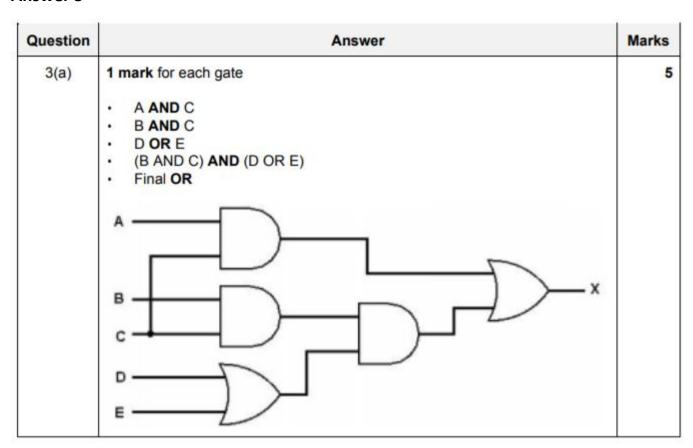
Question	Answer	Marks
3	1 mark for each correct gate	4
	X = NOT (A AND B) OR NOT (NOT B OR C)	
	A S	
4(a)(i)	1 mark only e.g.	1
	 Read about the languages she will be using Visits the office prior to starting Speaks to her manager about concerns 	



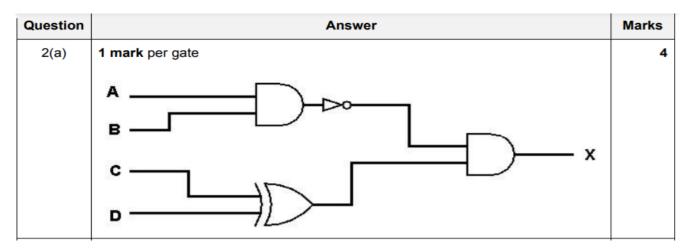
Question		Answer							
3(b)	1 mark f	or each o	correct pa	air of answers (4 shaded sections))		4		
	A	В	С	Working Space	X				
	0	0	0		1				
	0	0	1		1				
	0	1	0		0				
	0	1	1		0				
	1	0	0		0				
	1	0	1		1				
	1	1	0		1				
	1	1	1		0				
3(c)	1 mark f	or name,	1 mark	for symbol matching the name			2		
	NAND	=[) ~						
	NOR	\equiv	> -						



Question	Answer							
6(b)	1 mark for each pair of rows (shaded)							
	A	В	С	Working Space	х			
	0	0	0		0			
	0	0	1		0			
	0	1	0		1			
	0	1	1		0			
	1	0	0		1			
	1	0	1		1			
	1	1	0		1			
	1	1	1		1			

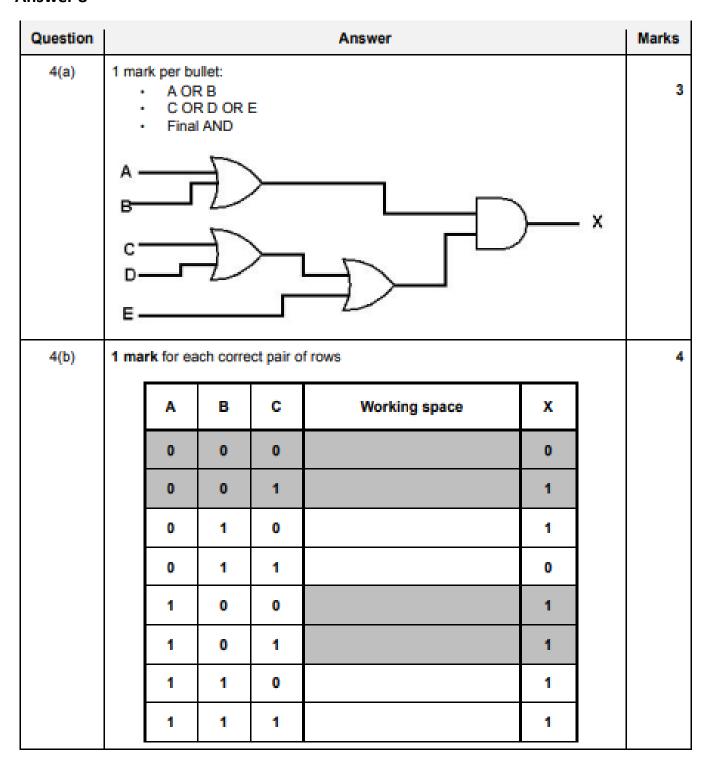


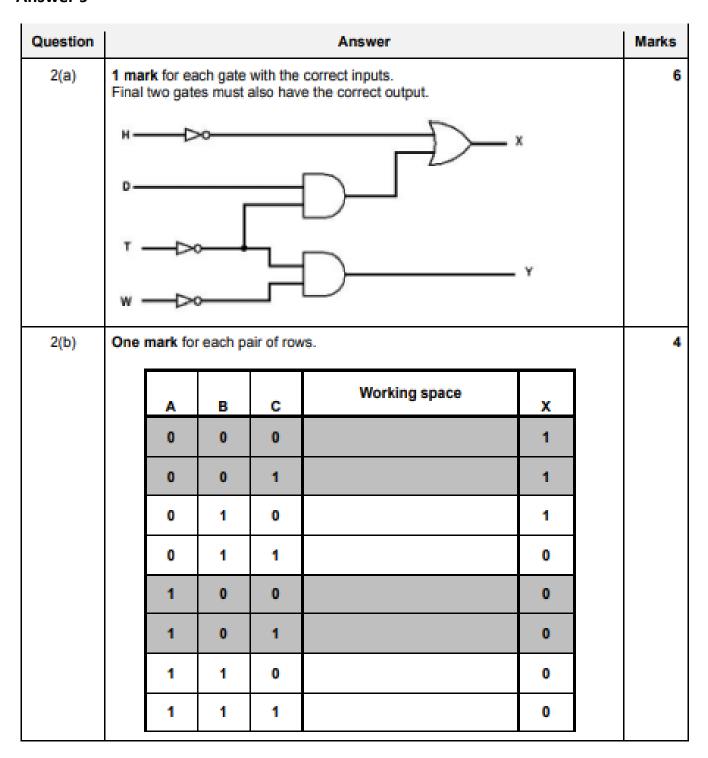
Question		Answer							
3(b)	1 marl	1 mark for each pair of correct rows							
	A	В	С	Working space	x				
	0	0	0		0				
	0	0	1		1				
	0	1	0		1				
	0	1	1		0				
	1	0	0		0				
	1	0	1		1				
	1	1	0		0				
	1	1	1		1				



2(b)	1 mark f	or each p	oair of an	nswers		4
	Α	В	С	Working space	x	
	0	0	0		1	
	0	0	1		1	
	0	1	0		1	
	0	1	1		1	
	1	0	0		1	
	1	0	1		1	
	1	1	0		1	
	1	1	1		0	

Question				Answer		Marks			
5(a)	· A OF	RC (A OR C) B ID NOT B			— х				
5(b)	1 mark fo	or each pa	air of rows	<u> </u>		4			
	A	В	С	Working space	X				
	0	0	0		1				
	0	0	1		0				
	0	1	0		1				
	0	1	1		0				
	1	0	0		1				
	1	1 0 1 1							
	1	1	0		0				
	1	1	1		0				



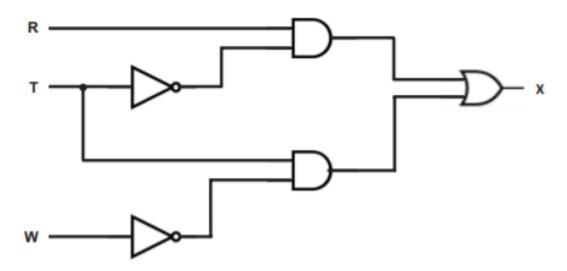


Question		Answer							
5(a)	1 ma	1 mark per correct gate with correct inputs							
	A B C D	_	D 心)— >—	×				
5(b)	1 ma	rk for ea	ich corre	ect pair o	f lines			4	
		Α	В	С	Working space	X			
		0	0	0		0			
		0	0	1		0			
		0	1	0		1			
		0	1	1		0			
		1	0	0		1			
		1	0	1		0			
		1	1	0		0			
		1	1	1		0			

Question	Answer	Marks
8(a)	1 mark for each logic gate with the correct inputs	4

Question		Answer						Marks
8(b)	One	mark fo	r each co	rrect pai	r of lines			4
		4	В	С	Working Space	x		
		0	0	0		1		
		0	0	1		1		
		0	1	0		1		
		0	1	1		1		
		1	0	0		1		
		1	0	1		1		
		1	1	0		1		
		1	1	1		0		

5 (a) (i) One mark for each correct gate.



- (ii) $(R.\overline{T})+(T.\overline{W})$ // (R AND NOTT) OR (T AND NOT W)
- (iii) One mark for each pair of lines as shaded.

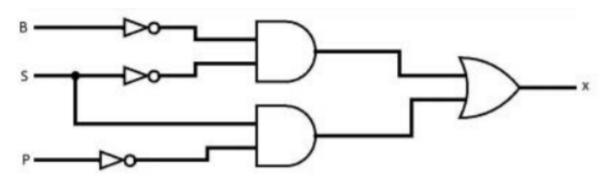
	INPUT		INPUT Working space		ОИТРИТ
R	т	w		x	
0	0	0		0	
0	0	1		0	
0	1	0		1	
0	1	1		0	
1	0	0		1	
1	0	1		1	
1	1	0		1	
1	1	1		0	

[4]

[5]

[2]

1 (a) ONE mark for each correct gate.



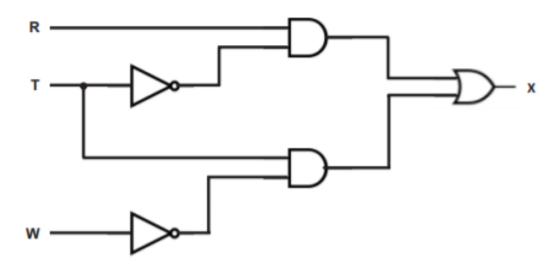
(b) ONE mark for each pair of rows.

			Working space	
В	s	P		X
0	0	0		1
0	0	1		1
0	1	0		1
0	1	1		0
1	0	0		0
1	0	1		0
1	1	0		1
1	1	1		0

[4]

[6]

5 (a) (i) One mark for each correct gate.



(ii) $(R.\overline{T}) + (T.\overline{W})$ // (R AND NOT T) OR (T AND NOT W) [2]

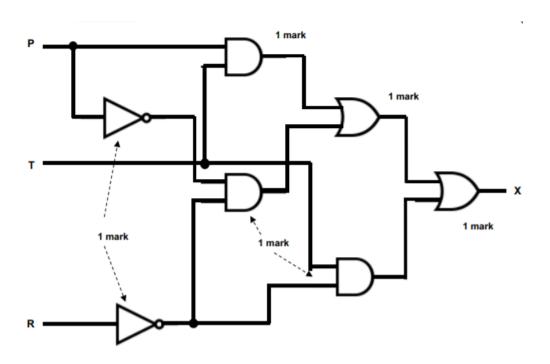
(iii) One mark for each pair of lines as shaded.

	INPUT		INPUT		INPUT Working space		Working space	OUTPUT
R	т	w		X				
0	0	0		0				
0	0	1		0				
0	1	0		1				
0	1	1		0				
1	0	0		1				
1	0	1		1				
1	1	0		1				
1	1	1		0				

[4]

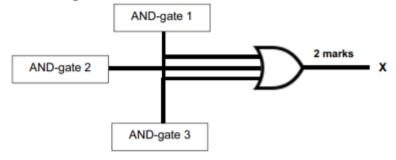
[5]

7 (a) since it is possible to simplify the original conditions, at least 3 possible answers exist for the logic circuit.

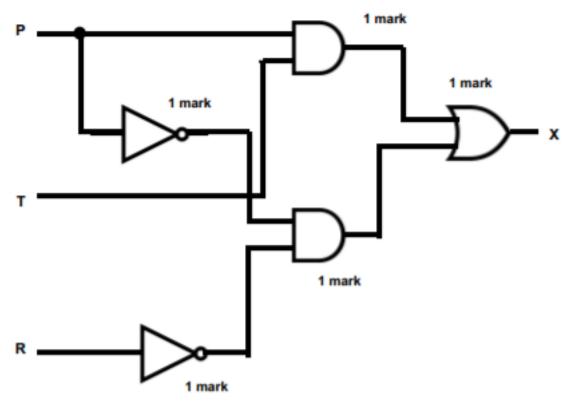


Note: input T has 2 cross overs that should not be connections

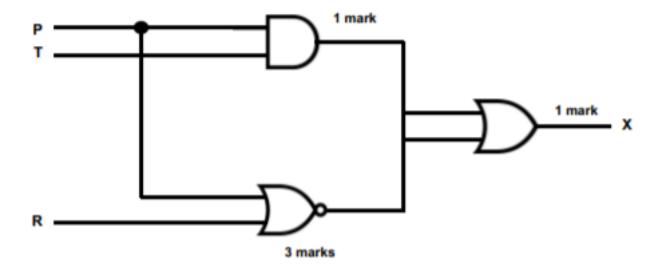
Note: it is possible to use a 3-input OR gate rather than the two 2-input OR gates on the top right:



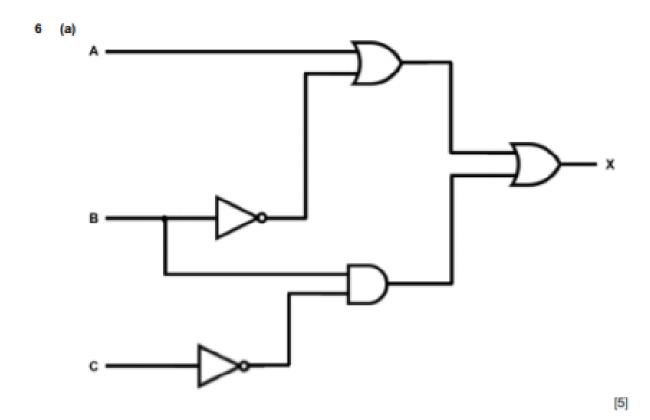
Alternative solution 1:



Alternative solution 2:



(b)						
	Р	т	R	Workspace	X	
	0	0	0		1	
	U	•	·			} 1 mark
	0	0	1		0	
	0	1	0		1	} 1 mark
	0	1	1		0	J I IIIaik
	1	0	0		0	Lamark
	1	0	1		0	} 1 mark
	1	1	0		1	1
	1	1	1		1	} 1 mark
						[4]



[4]

[3]

(b)

Α	В	С	working	x	
0	0	0		1	1
0	0	1		1	} 1 mark
0	1	0		1	1
0	1	1		0	} 1 mark
1	0	0		1	1
1	0	1		1	} 1 mark
1	1	0		1	1
1	1	1		1	1 mark

(c) ((A is NOT 1 AND B is 1) OR (B is NOT 1 OR C is 1)) AND C is NOT 1

<----1 mark---->

NOTE: all brackets may not be shown - but check answer still correct

Alternatives include:

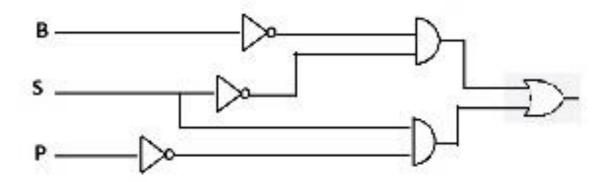
((NOT A AND B) OR (NOT B OR C)) AND NOT C

NOTE: expressions may be reversed but still OK

(e.g. NOT C AND ((NOT A AND B) OR (NOT B OR C))

NOT C AND ((NOT B OR C) OR (NOT A AND B)) and so on)

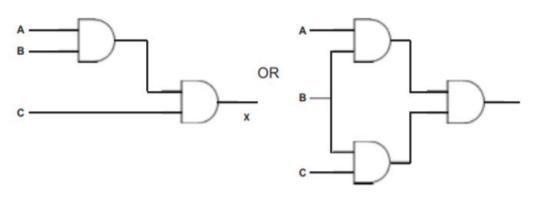
В	S	Р	Х
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0



Answer 18

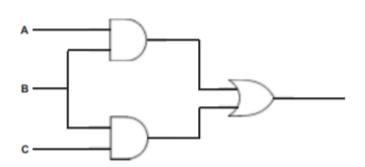
8 (a) 2 marks per part IF candidate uses 2 gates mark from 2 gate diagram if draws 3 gates mark from 3 gate diagram for all 3 parts

(i) (allow correct alternatives)

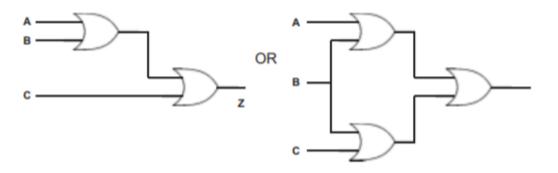


[2]





(iii) (allow correct alternatives)



(b)

Α	В	С	X	Y	Z
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	0	1
0	1	1	0	1	1
1	0	0	0	0	1
1	0	1	0	0	1
1	1	0	0	1	1
1	1	1	1	1	1
	0 0 0	0 0 0 0 0 0 0 1 0 1 1 0 0	0 0 0 0 1 0 0 1 1 0 1 0 1 0	0 0 0 0 0 0 1 0 0 1 0 0 0 1 1 0 1 0 0 0 1 0 1 0	0 0 0 0 0 0 0 1 0 0 0 1 0 0 0 0 1 1 0 1 1 0 0 0 0 1 0 1 0 0

2 marks 2 marks 2 marks

(-1 mark for each error in each column)

[6]

[2]

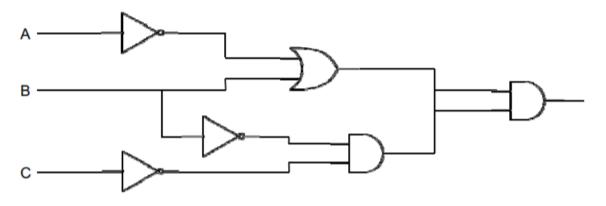
[2]

Answer 19

8 (a)

Α	В	С	x	
0	0	0	1	1 mark
0	0	1	1	1 mark
0	1	0	0	1 morte
0	1	1	0	1 mark
1	0	0	0	1 morte
1	0	1	1	1 mark
1	1	0	0	4 mark
1	1	1	0	1 mark

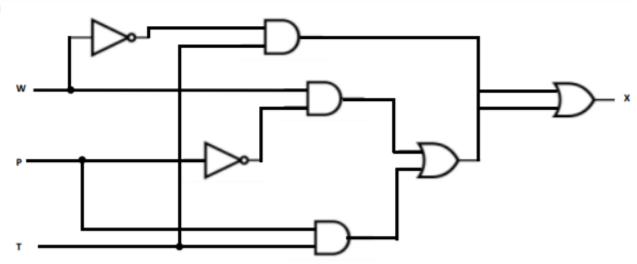
(b) 1 mark per correct logic gate in correct position



[4]

[6]

6 (a)



(corresponds to: [W = 1 AND P = NOT 1] OR [T = 1 AND P = 1] OR [W = NOT 1 AND T = 1])

1 mark for each correct logic gate in correct position -

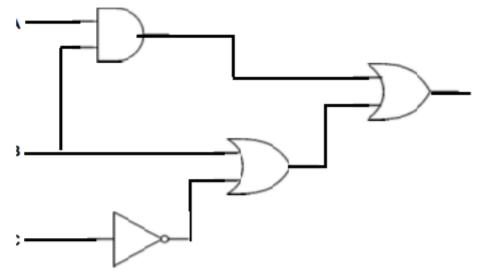
[7]

(b)

_				
	output X	input T	input P	input W
1 mark	0	0	0	0
	1	1	0	0
1 mark	0	0	1	0
	1	1	1	0
1 mark	1	0	0	1
	1	1	0	1
1 mark	0	0	1	1
	1	1	1	1

[4]

9 (a) 1 mark for each correct logic gate (accept other logic gate nomenclature)



If a candidate has only one input to AND gate or an OR gate they lose the mark for that gate

(b)

A	В	С	X
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

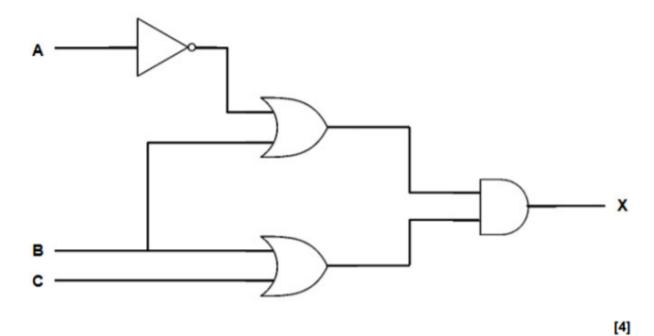
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[4]

4 (a) 1 mark for each correct logic gate



(b) В С 1 mark 1 mark 1 mark

1 mark

[4]

[2]

[4]

Answer 23

(1 mark for the 1,0 and 1 mark for 0, 0)

(b) A B C D Y
0 0 0 1 0
0 1 1 0 0
1 0 1 1 1
1 1 1 0 0

(1 mark for each row).