# Week-1
# Presentation
# Analog Design Internship

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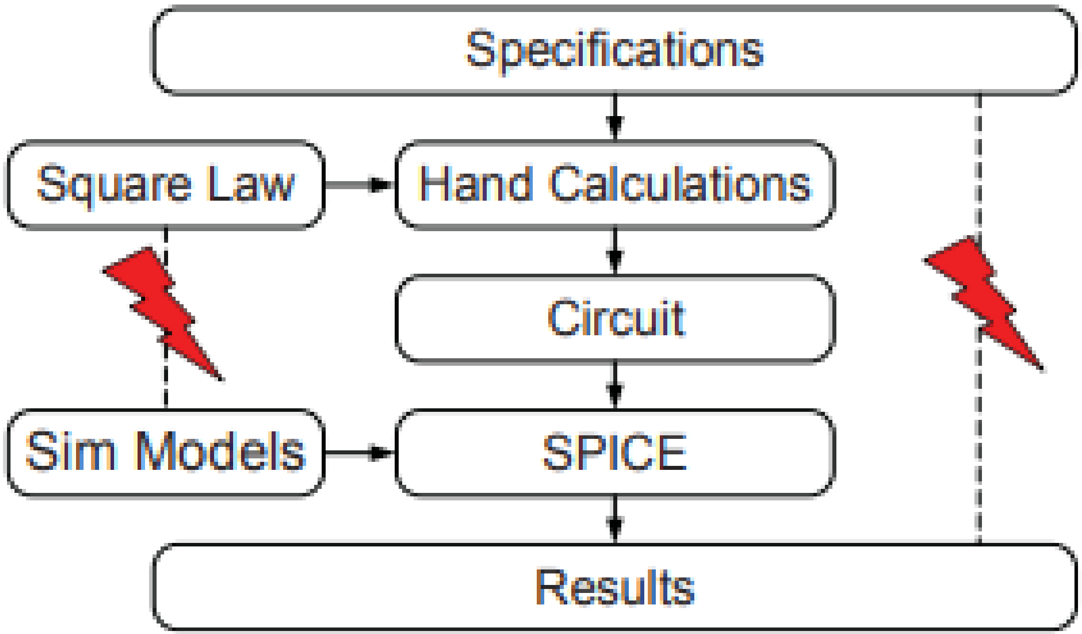
# Outline

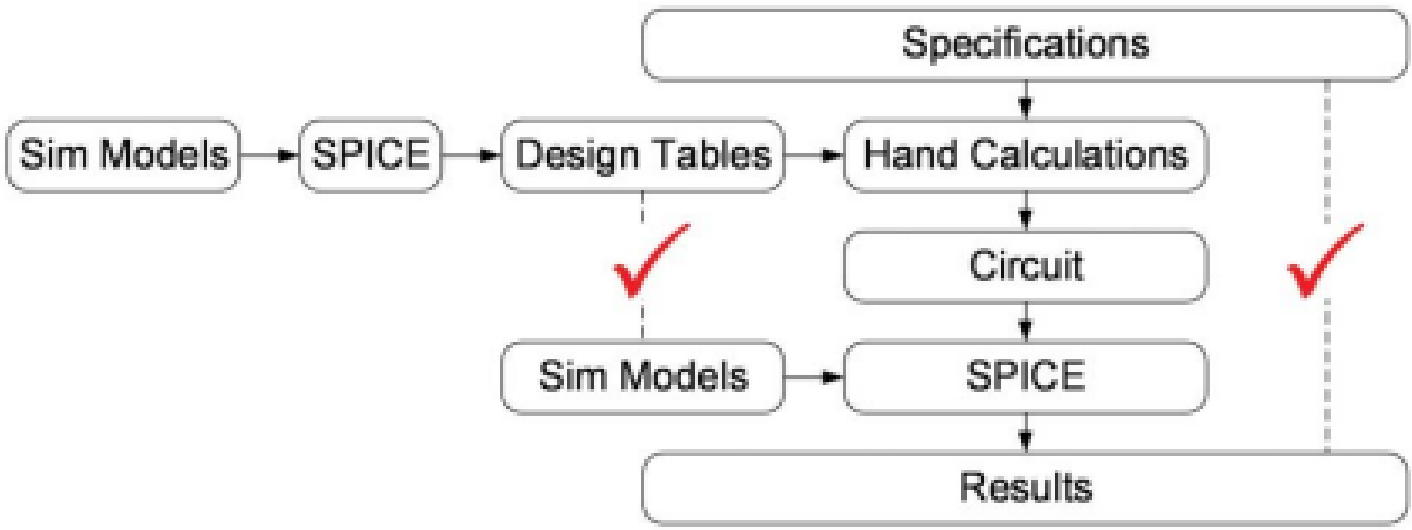
- Designing Problems
- Solution
- Brief: gm/id methology
- How to build charts
- Charts for NMOS
- Charts for PMOS
- Common Source Amplifier
- Common Drain Amplifier
- Reference

# Designing Problems




- Since there is a disconnect between actual transistor behavior and the simple square law model, any square-law driven design optimization will be far off from SPICE results

# Solution




- Use pre-computed SPICE data in hand calculations

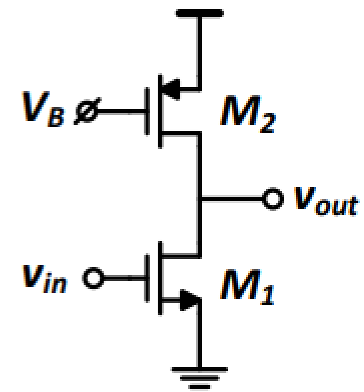
# The gm/ID Design Methodology

- ## Why gm/id Design?
- The hand calculation method requires the µncox, µpcox, and vth values of the transistor. However, since these values differ in the model file, the hand-calculated value does not align with the simulated value
- Square law model is not efficient.
- The gm/id method is a valuable tool in amplifier design as it allows designers to quickly estimate and compare performance parameters, facilitating efficient and effective amplifier design.
- The gm/ID is directly related to circuit specification.
- It defines gain, speed, and noise
- The search-range of gm/ID is typically: 5 to 25
- The range of gm/ID values doesn't differ much
  - From one device to another
  - And from one technology to another

# Some tips

| Use small gm/ID if you want | Use large gm/ID if you want |
|---|---|
| ➢ Strong-inversion (SI) biasing<br>➢ Small gm (for a given ID)<br>▪ Devices whose gm do NOT contribute to gain (Ex: active loads)<br>➢ Small area<br>➢ Small capacitance<br>➢ High speed<br>➢ Large $V_A$ (large ro)<br>▪ The gate has better control on channel (VDS effect is less) | ➢ Moderate inversion (MI) or weak-inversion (WI) biasing<br>➢ Large gm (for a given ID)<br>▪ Devices whose gm do contribute to gain (Ex: input stage and cascode devices)<br>➢ High efficiency<br>▪ Low power consumption (low ID) for a given speed or noise spec (gm spec)<br>➢ Less random mismatch<br>▪ Large gm/ID implies larger W (larger area) (beware of exceptions due to non-uniform doping profile)<br>➢ Low flicker noise<br>▪ Large gm/ID implies larger W (larger area)<br>➢ Large input range and/or output swing<br>▪ Large gm/ID implies small V* |

The best compromise is usually in MI
Gm/id range = 10 to 20

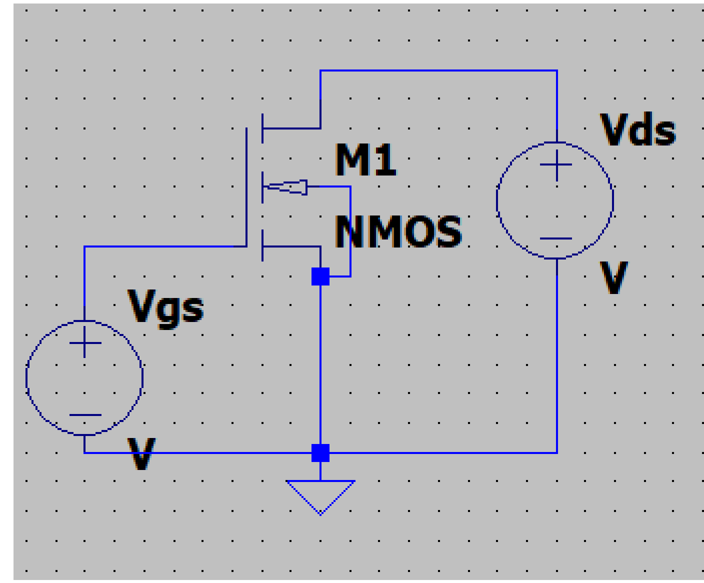



- From gain perspective
  - A large gm/ID may be good for M1
  - But a small gm/ID is better for M2
- Generally, from gain perspective
  - Use large gm/ID for transistors whose $gm$ contribute to the gain
    - Ex: input stage and cascode devices
  - Use small gm/ID for transistors whose $gm$ do not contribute to gain
    - Ex: active loads

- Ratios of these parameters are width independent!

$$\frac{gm}{\text{id}}, fT = \frac{gm}{2\pi Cgg}, \frac{gm}{w}, gmro = \frac{gm}{gds}, VA = \frac{id}{gds}$$

# Building The Design Charts




MOSFET is a function of five variables

Three voltages

- VGS: Sweep (primary variable)
- VDS: Set to fixed value (e.g vdd/2)
- VSB: Set to fixed value (neglected )

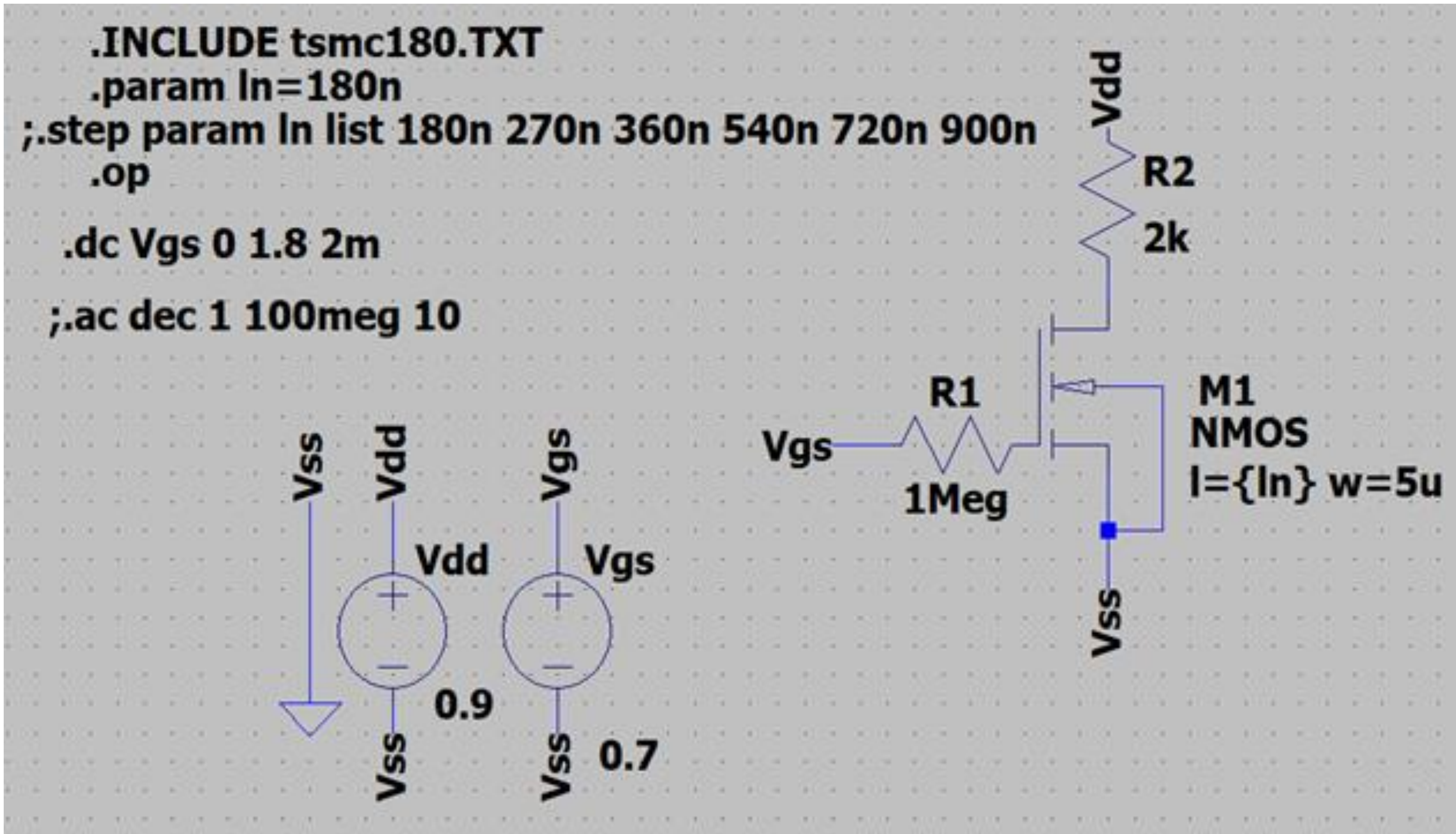
Two sizing parameters

- L: Step (secondary variable)
- W: Set to a reference value (e.g., 5um)

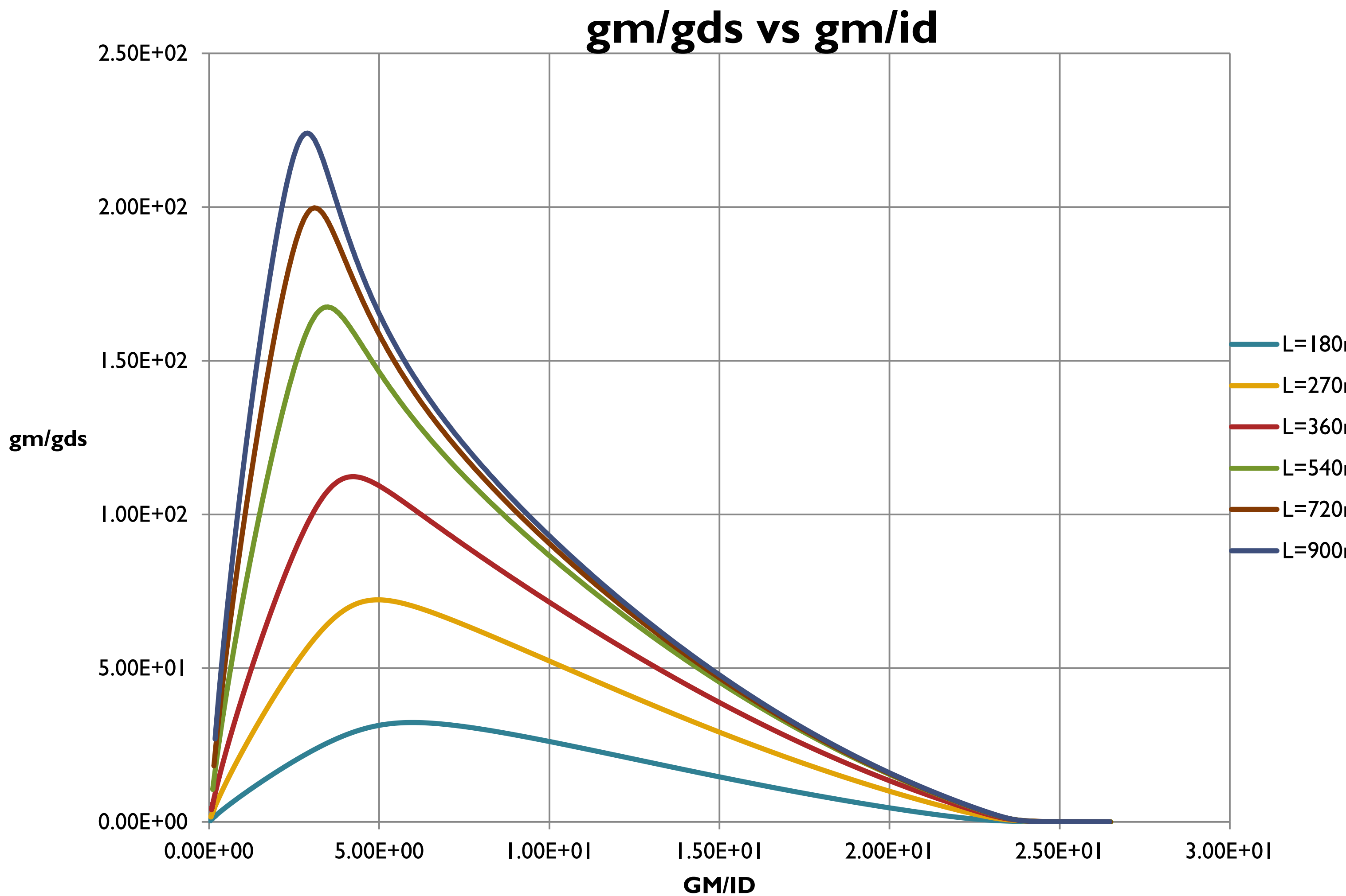
Ploted charts for

- gm/gds vs gm/id
- Id/w vs gm/id
- gm/id vs vgs

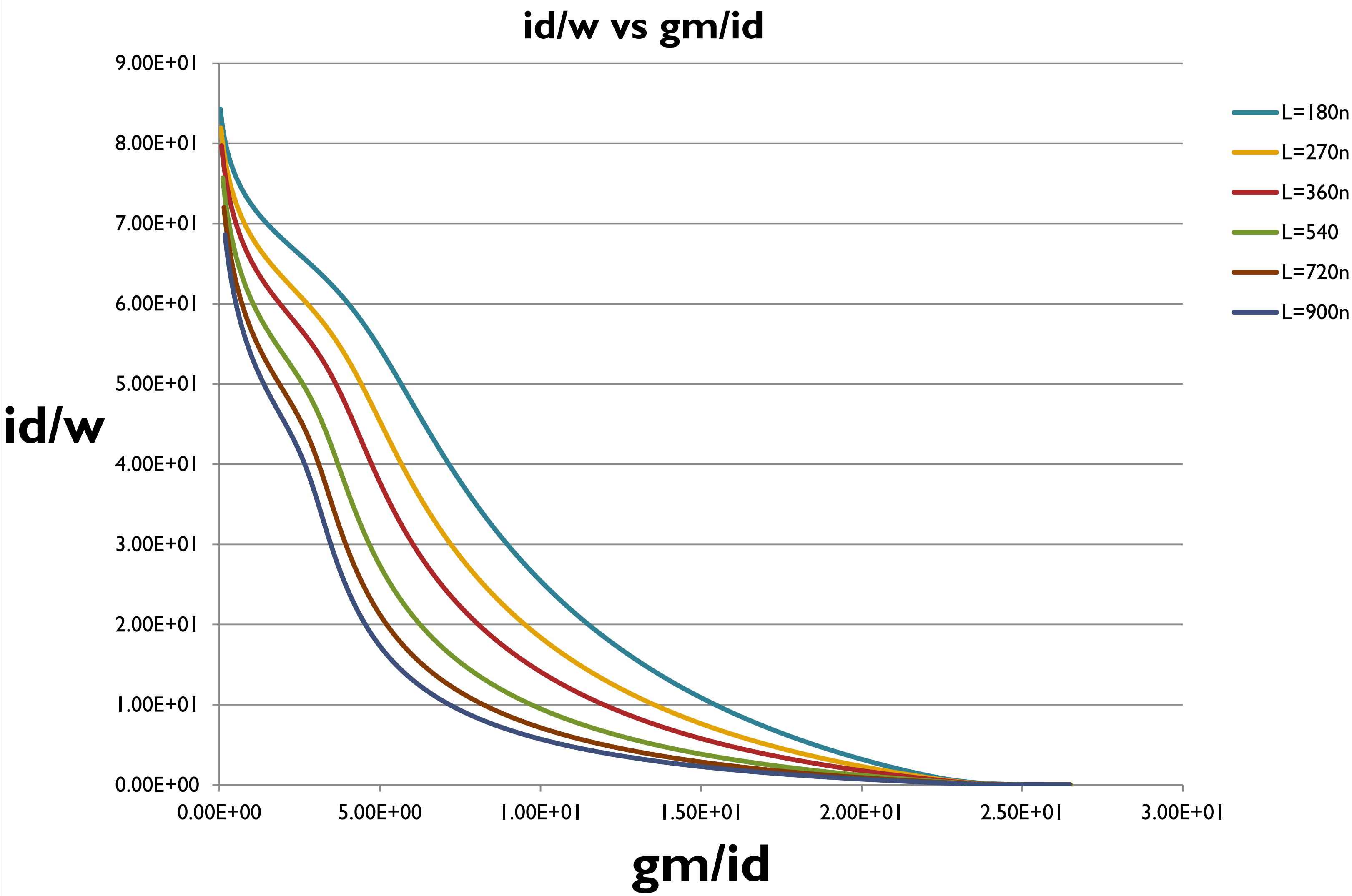
# Schematic for chart (NMOS)



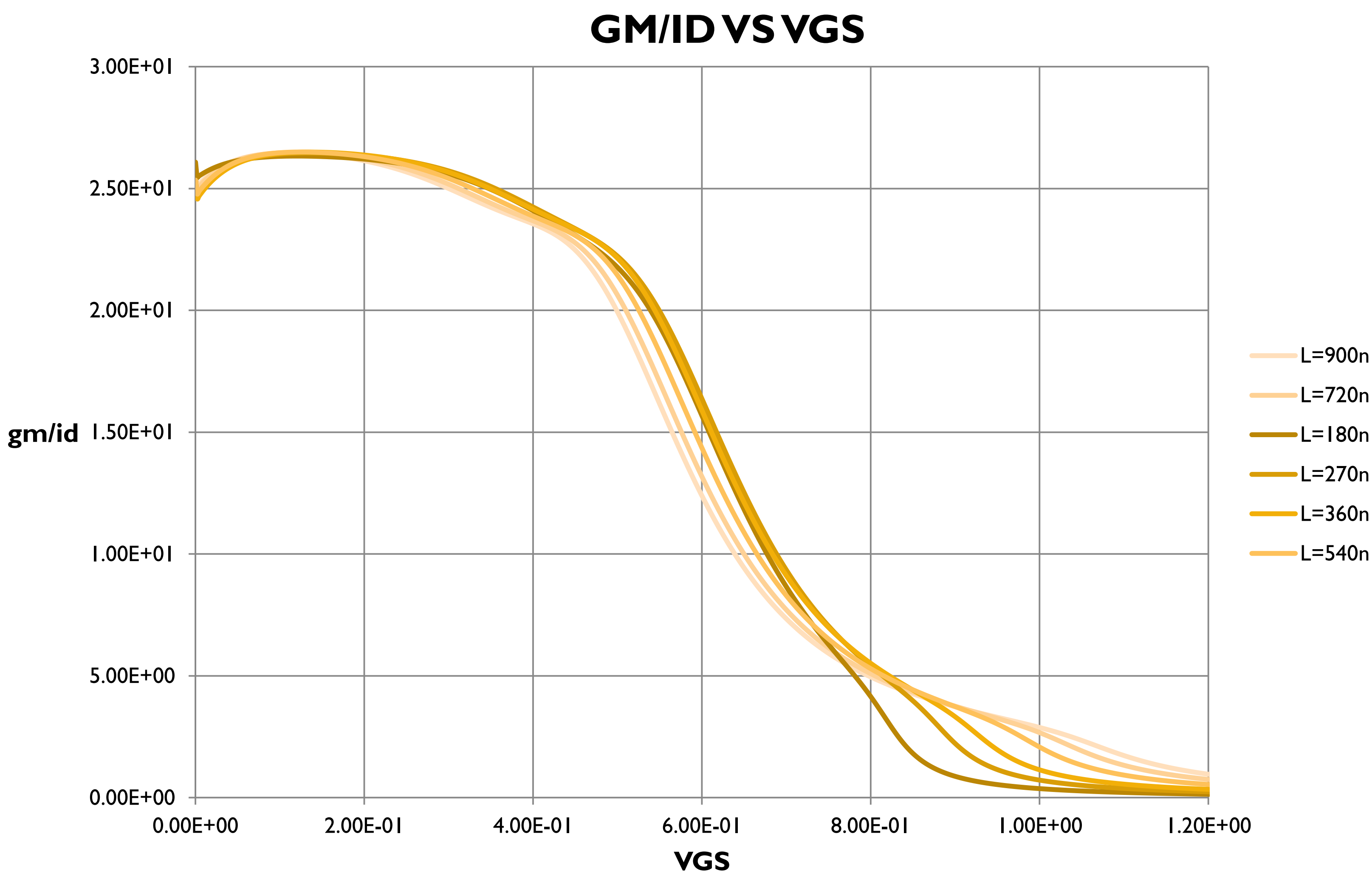
# Charts for NMOS MOSFET



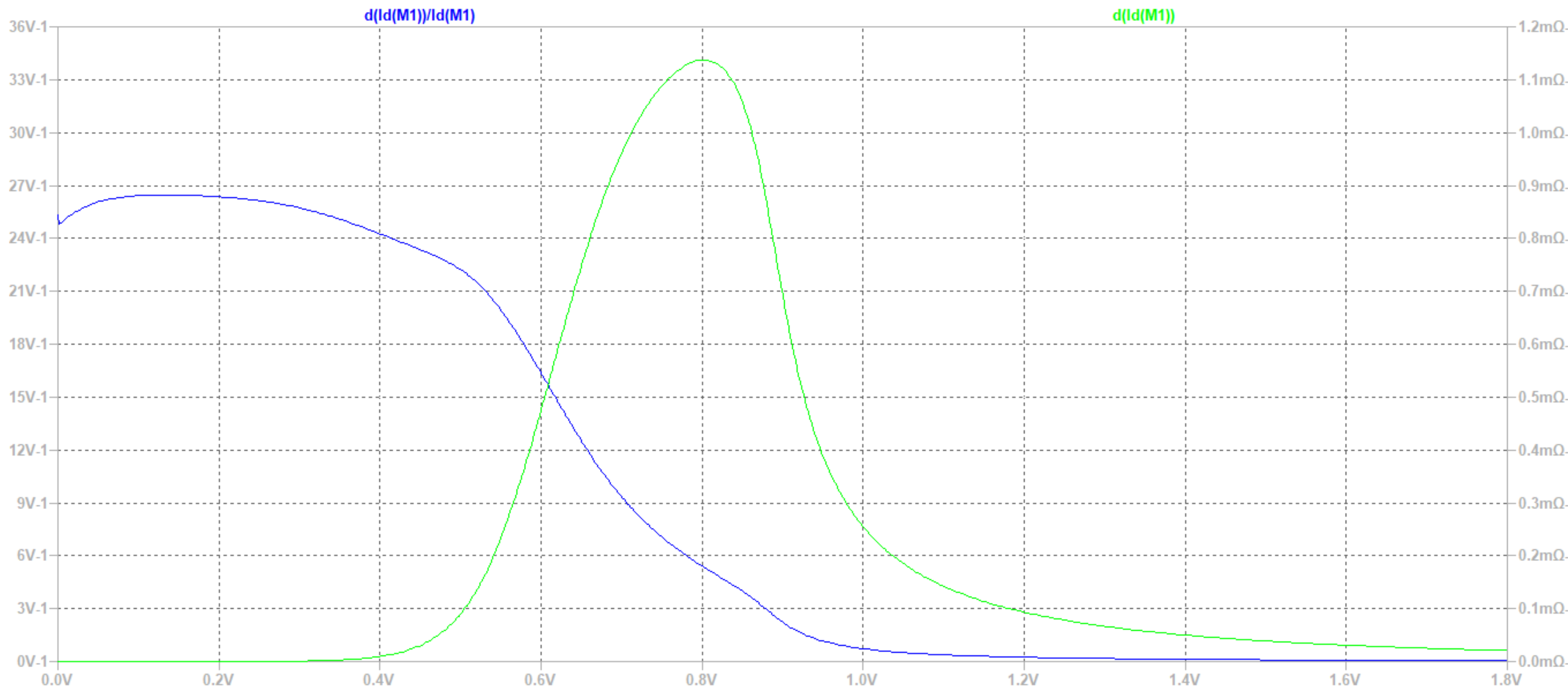
# Charts for NMOS MOSFET



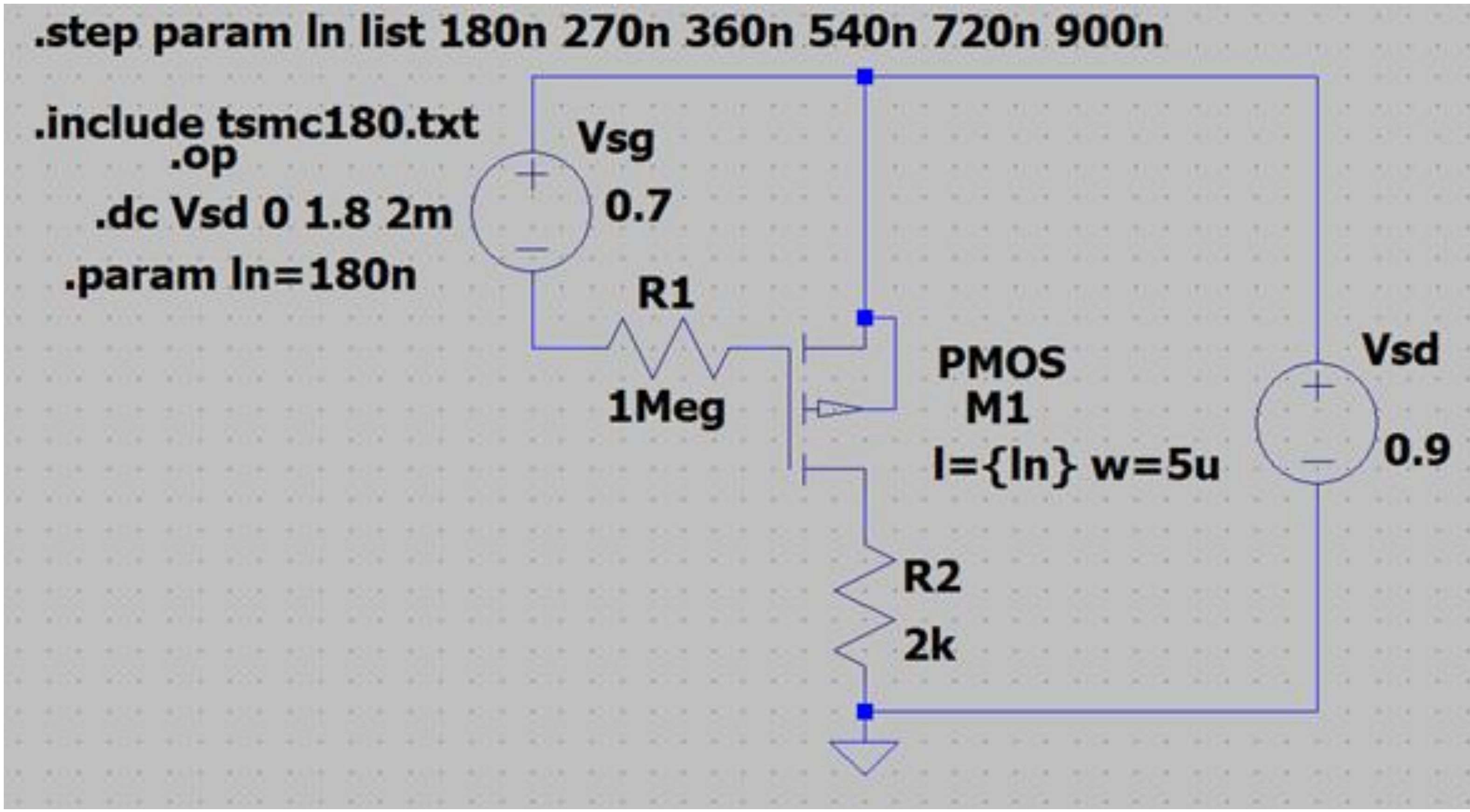
# Charts for NMOS MOSFET



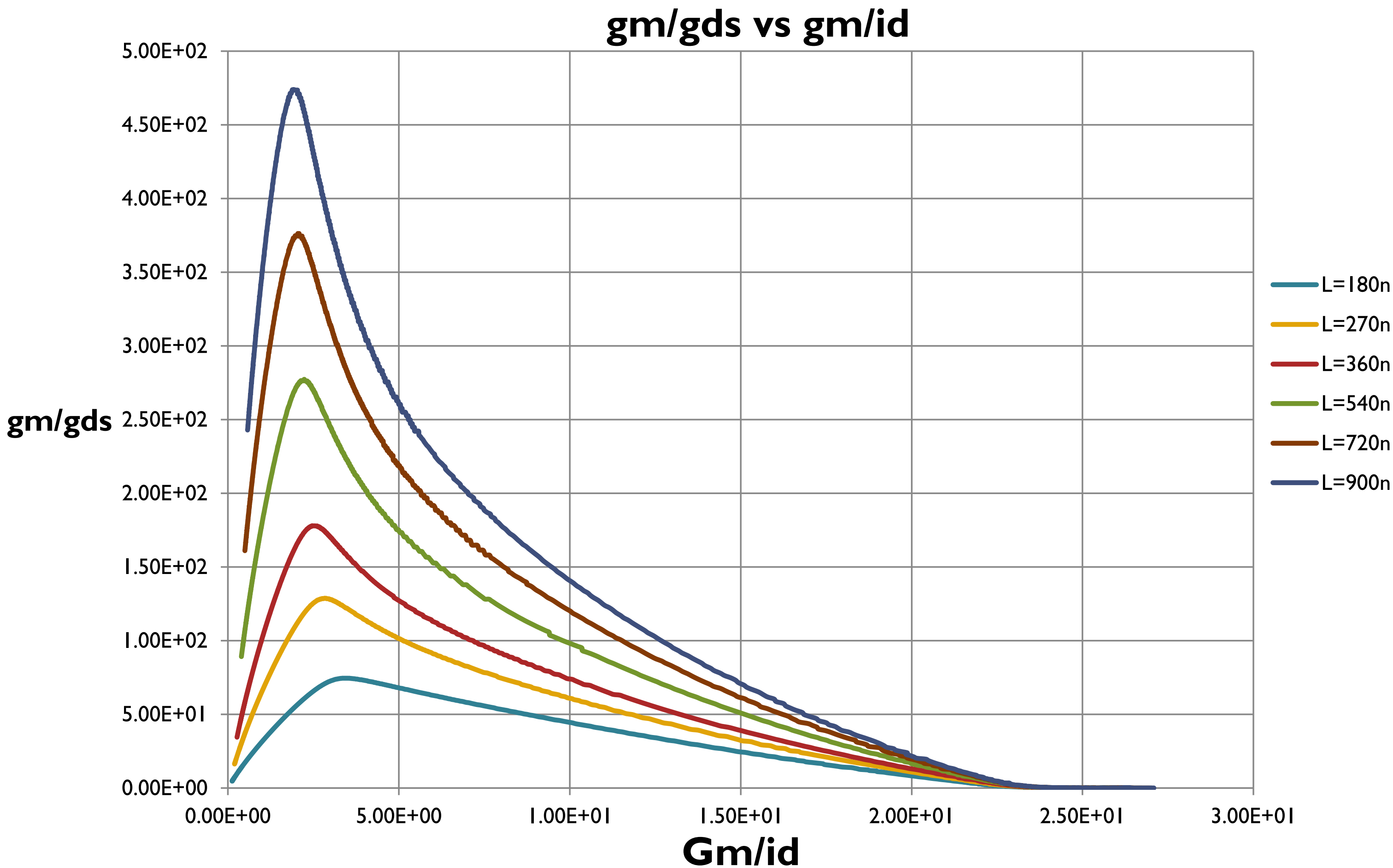
# Gm/id vs vgs for 270nm



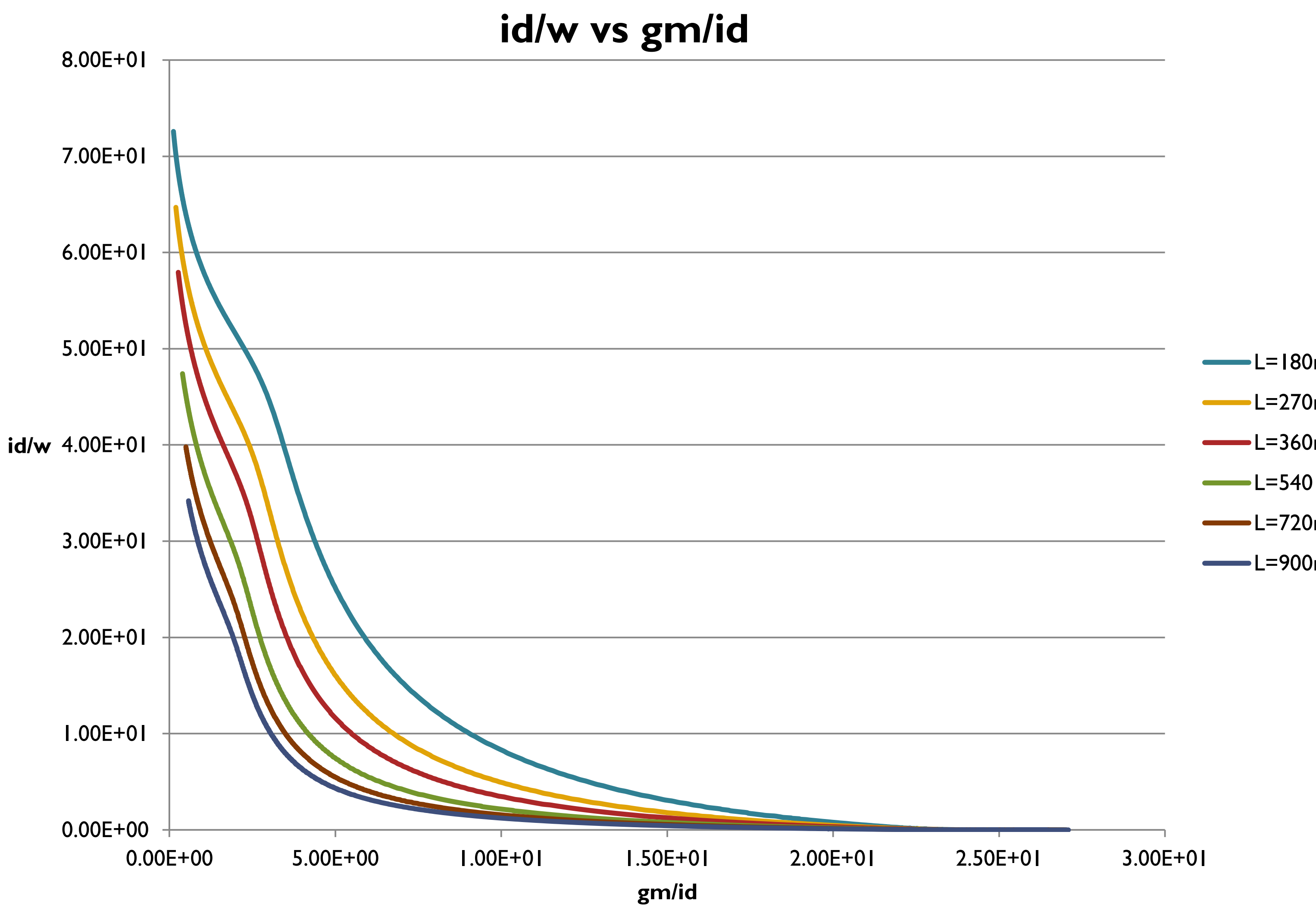
# Schematic for chart (PMOS)



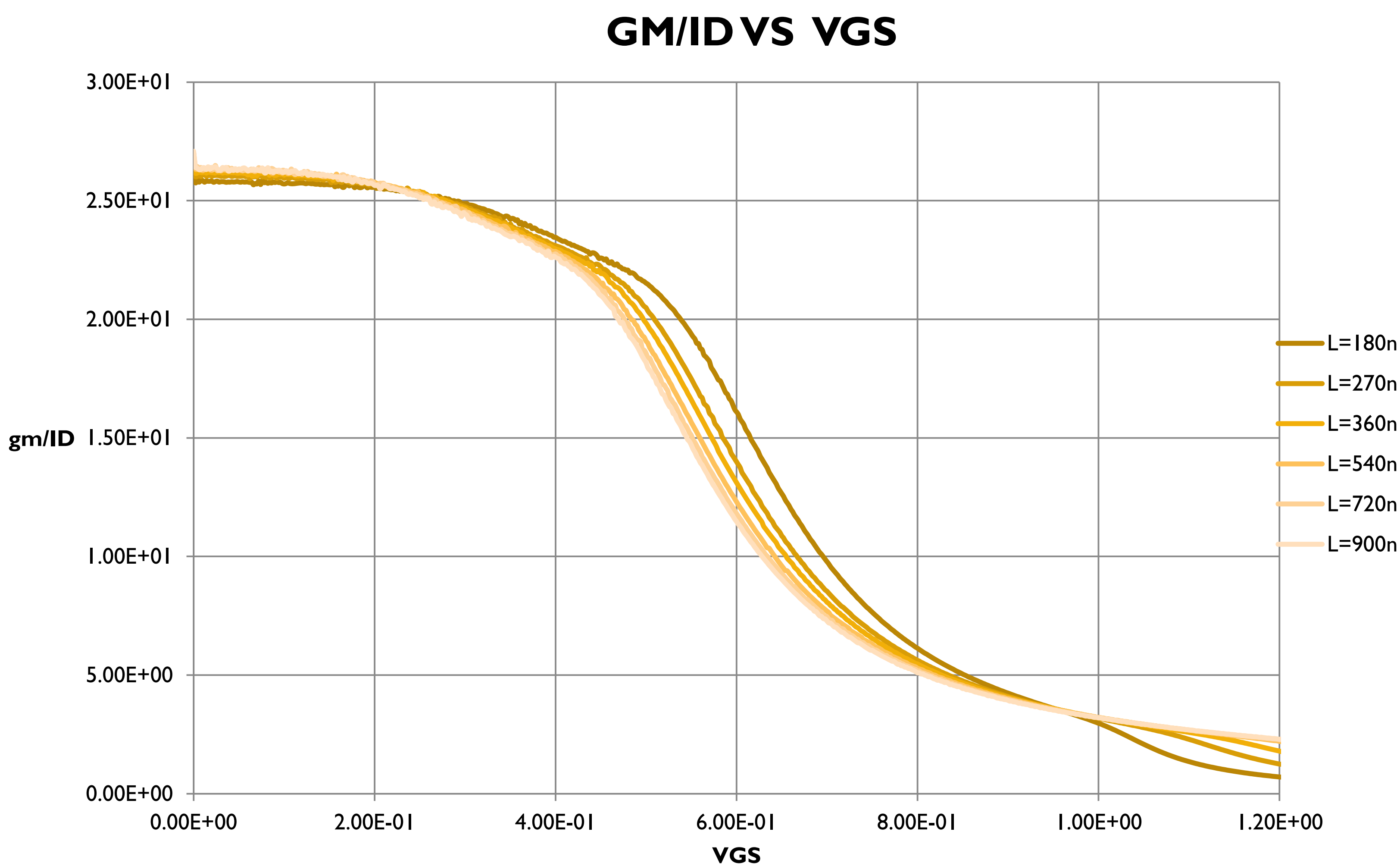
# Charts for PMOS MOSFET



# Charts for PMOS MOSFET

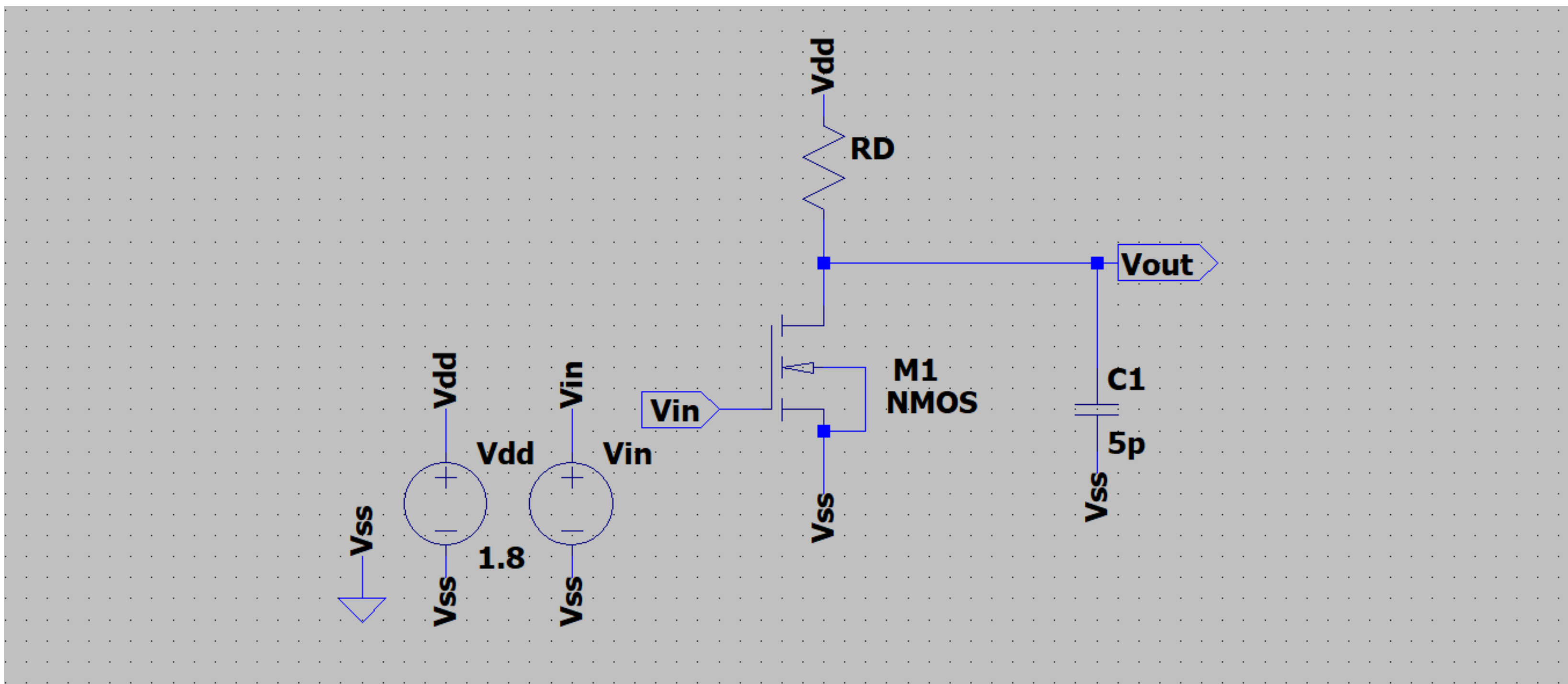


# Charts for PMOS MOSFET



# 1. Common Source with Passive Load

Specification
Av= -7 v/v
BW= 90MHz
CL= 5pF



# Calculation

BW= $\frac{1}{2\pi\ .Rout.CL}$ ---(i) Av= gm.Rout ----(ii)

Rout= Rd || ro ----(iii) ro= $\frac{1}{gds}$ ----(iv)

W= $\frac{\text{id}}{\text{(id/w)}}$ ----(v)

Rout= 353.6 Ω gm=19.8 mS

**Choose gm/id=12**

Id= 1.65mA

Gm/gds = 43 v/v ----from chart id/w=13.2 ----from chart

Gds= 460.4μS

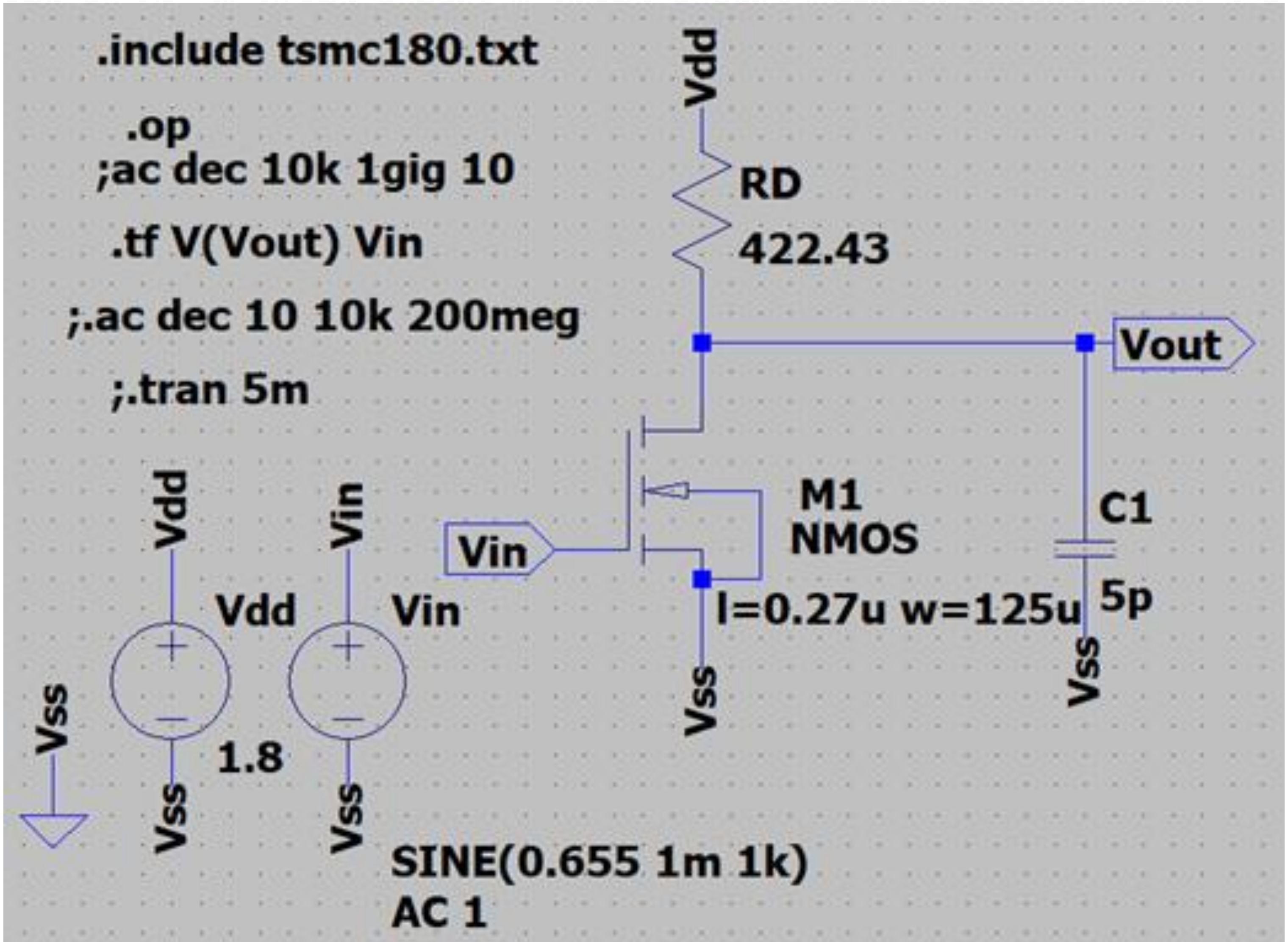
ro= 2.17 KΩ

Rd= 422.43 Ω

Vgs=0.655 V

$\frac{W}{L}$= $\frac{125\mu m}{0.27\mu m}$

# Simulation



.include tsmc180.txt
.op
;ac dec 10k 1gig 10
.tf V(Vout) Vin
;.ac dec 10 10k 200meg
;.tran 5m
Vdd
RD
422.43
Vout
M1
NMOS
C1
5p
l=0.27u w=125u
Vin
Vdd
Vin
Vdd
Vin
Vss
Vss
Vss
Vss
Vss
1.8
SINE(0.655 1m 1k)
AC 1

# Result and Conclusion

Simulation output

Av= -7.8

gm = 20.5mS

Gds=257 μS

BW= 81MHz

Id =1.7 mA

Vds= 1v

Pd =3mW

GBW= 631.8MHz

Design parameter

Av= -7

gm = 19.8mS

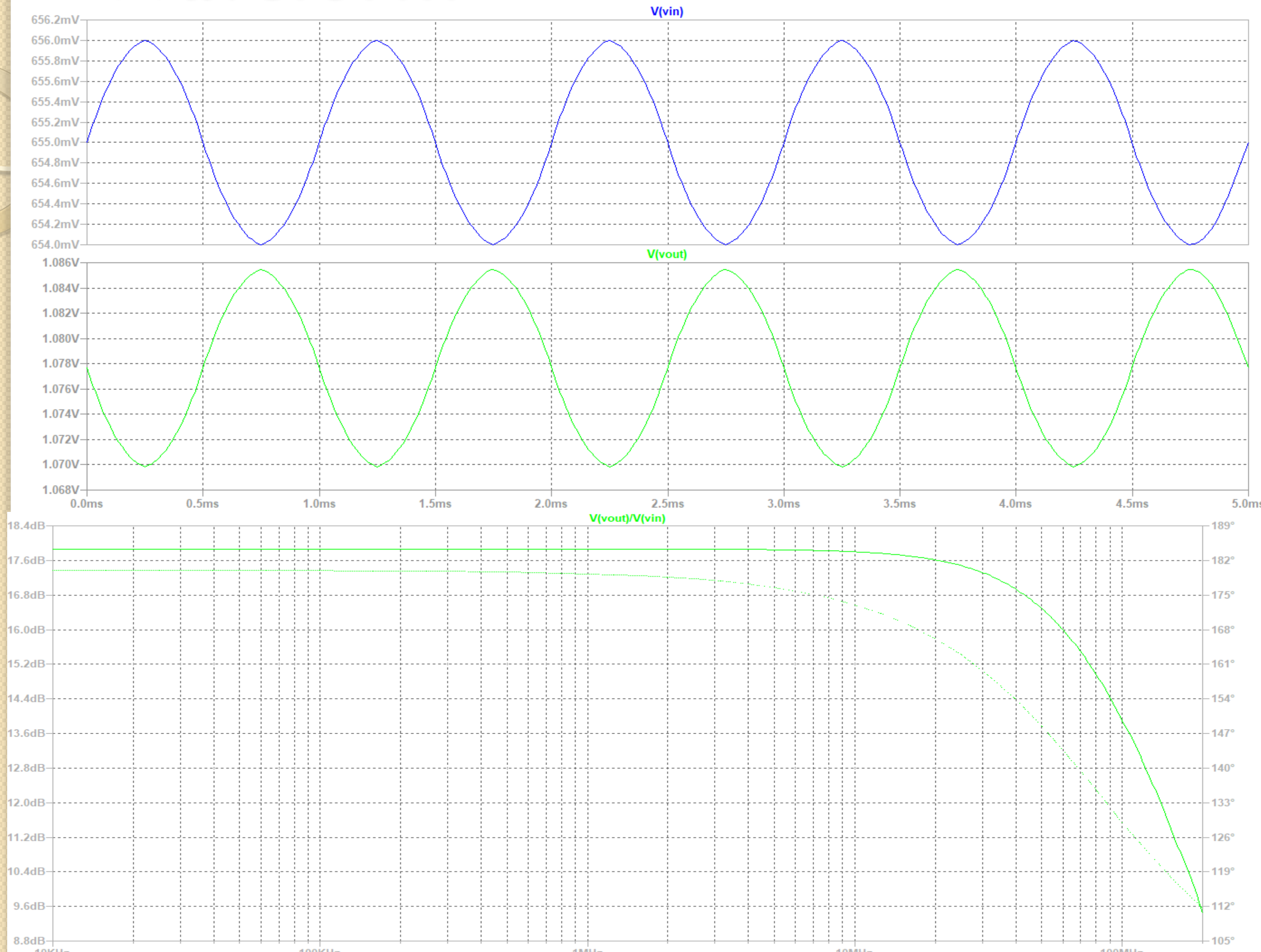
Gds=460.4 μS

BW= 90MHz

Id =1.65 mA

GBW= 630MHz

# Waveform



V(vin)
656.2mV
656.0mV
655.8mV
655.6mV
655.4mV
655.2mV
655.0mV
654.8mV
654.6mV
654.4mV
654.2mV
654.0mV
V(vout)
1.086V
1.084V
1.082V
1.080V
1.078V
1.076V
1.074V
1.072V
1.070V
1.068V
0.0ms
0.5ms
1.0ms
1.5ms
2.0ms
2.5ms
3.0ms
3.5ms
4.0ms
4.5ms
5.0ms
V(vout)/V(vin)
18.4dB
17.6dB
16.8dB
16.0dB
15.2dB
14.4dB
13.6dB
12.8dB
12.0dB
11.2dB
10.4dB
9.6dB
8.8dB
189°
182°
175°
168°
161°
154°
147°
140°
133°
126°
119°
112°
105°
10KHz
100KHz
1MHz
10MHz
100MHz

# 2. Common Source with Passive Load

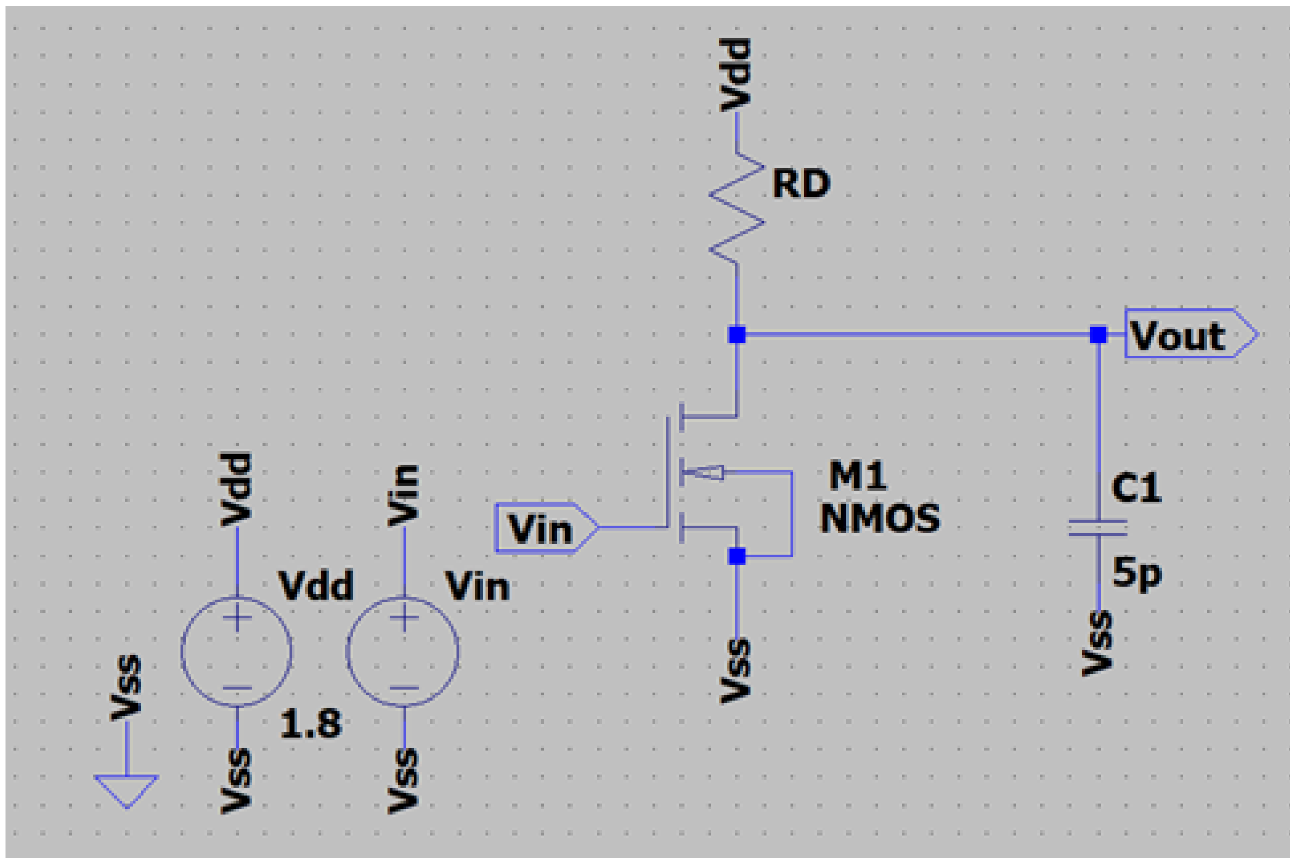
Specification

**GBW= 560MHz**

Av= -10 v/v

CL= 5pF

BW= 56MHz



# Calculation

BW= $\frac{1}{2\pi .Rout.CL}$ ---(i)

Av= gm.Rout ----(ii)

Rout= Rd || ro ----(iii)

ro= $\frac{1}{gds}$ ----(iv)

W= id/(id/w) ----(v)

Rout= 568.4 Ω

gm=17.6 mS

**Choose gm/id=15**

Id= 1.17 mA

gm/gds = 25.5 v/v ----from chart

id/w= 8 ----from chart

gds= 690 µS

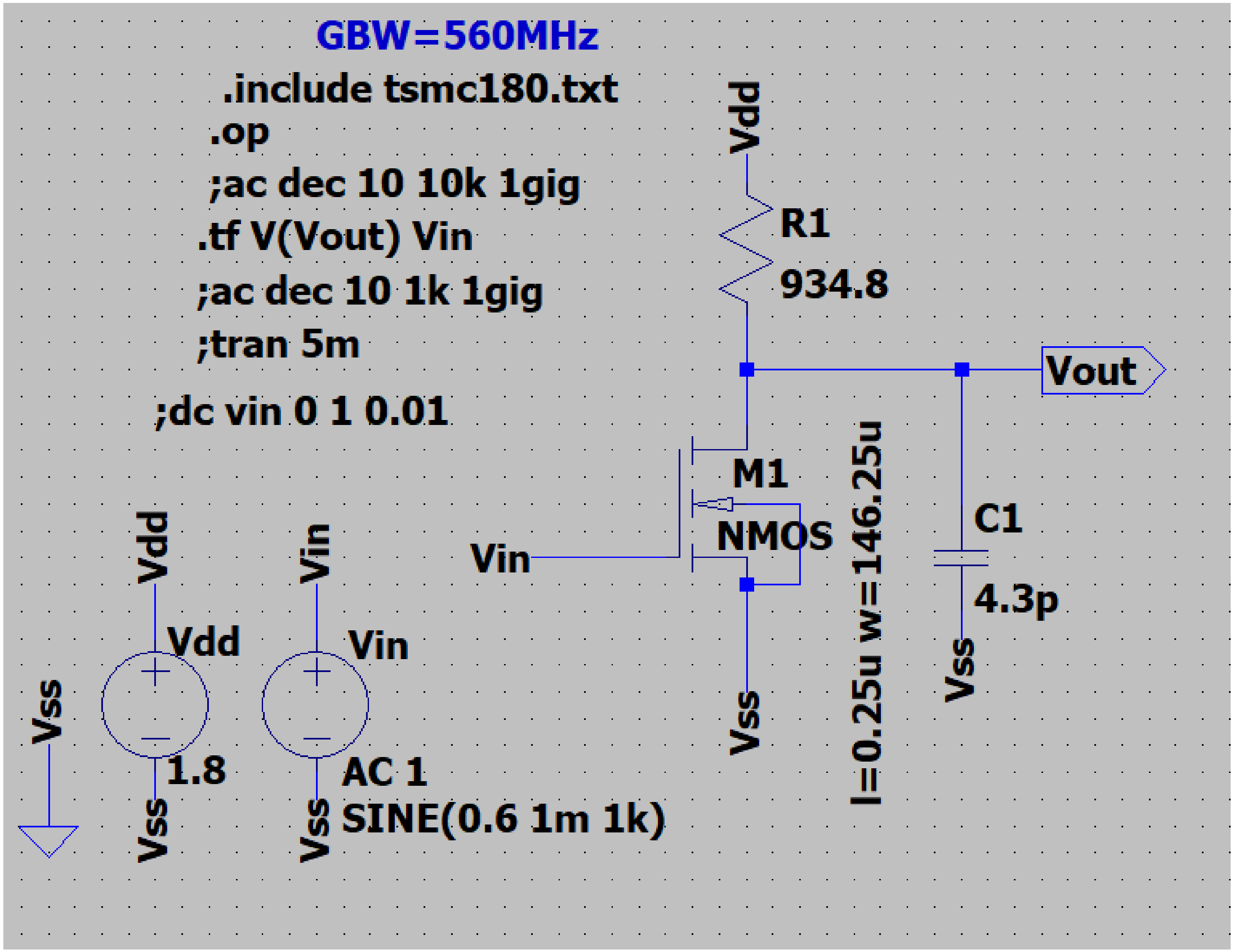
ro= 1.45 KΩ

Rd= 934.8 Ω

Vgs=0.655 V

$\frac{W}{L}$= $\frac{146.25\mu m}{0.25\mu m}$

# Simulation



GBW=560MHz
.include tsmc180.txt
.op
;ac dec 10 10k 1gig
.tf V(Vout) Vin
;ac dec 10 1k 1gig
;tran 5m
;dc vin 0 1 0.01
Vdd
R1
934.8
Vout
M1
NMOS
l=0.25u w=146.25u
C1
4.3p
Vin
Vss
Vdd
Vdd
1.8
Vss
Vin
Vin
AC 1
SINE(0.6 1m 1k)
Vss
Vss
Vss

# Result and Conclusion

Simulation output

- Av= -12.25
- gm = 15.7mS
- Gds=209 μS
- BW= 45.75MHz
- Id =1 mA
- Vds= 0.9v
- Pd =1.73 mW
- GBW= 560.4MHz

Design parameter
Av= -10
gm = 17.6 mS
Gds=690μS
Id =1.17 mA

GBW= 560MHz

# 3. Common Source with current source Load

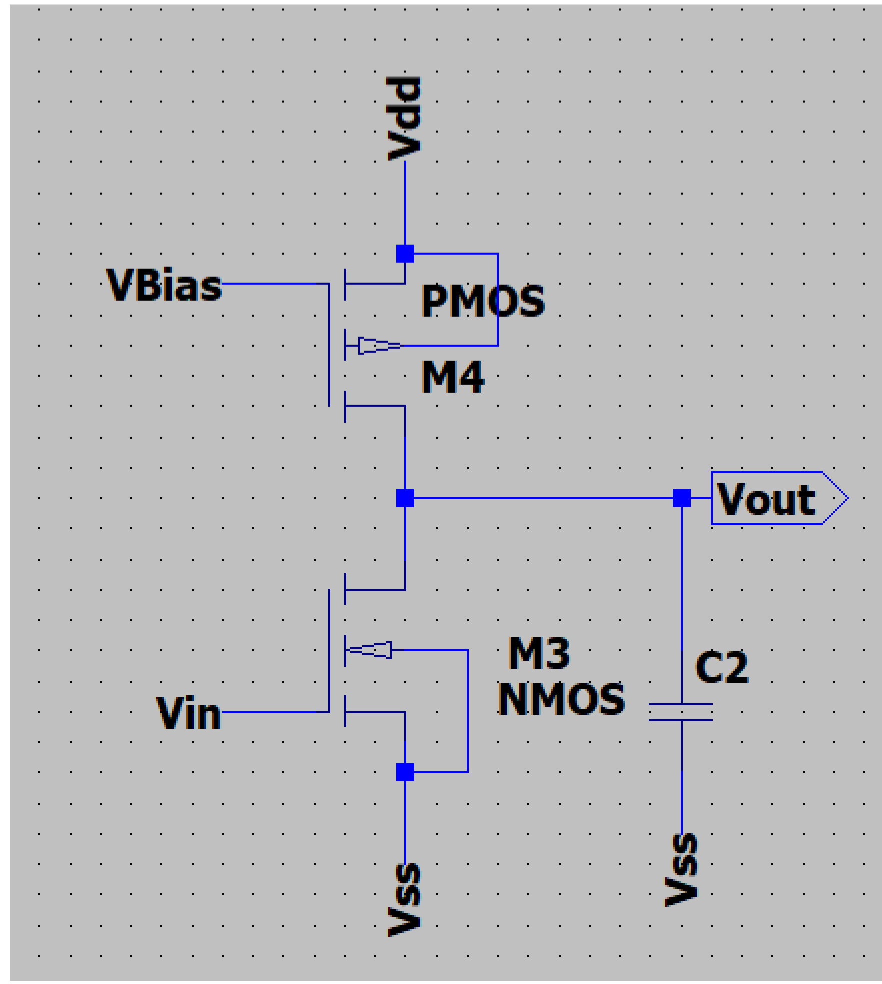
Specification

Av= -30 v/v

BW= 100 MHz

CL= 1pF

GBW= 3 GHz

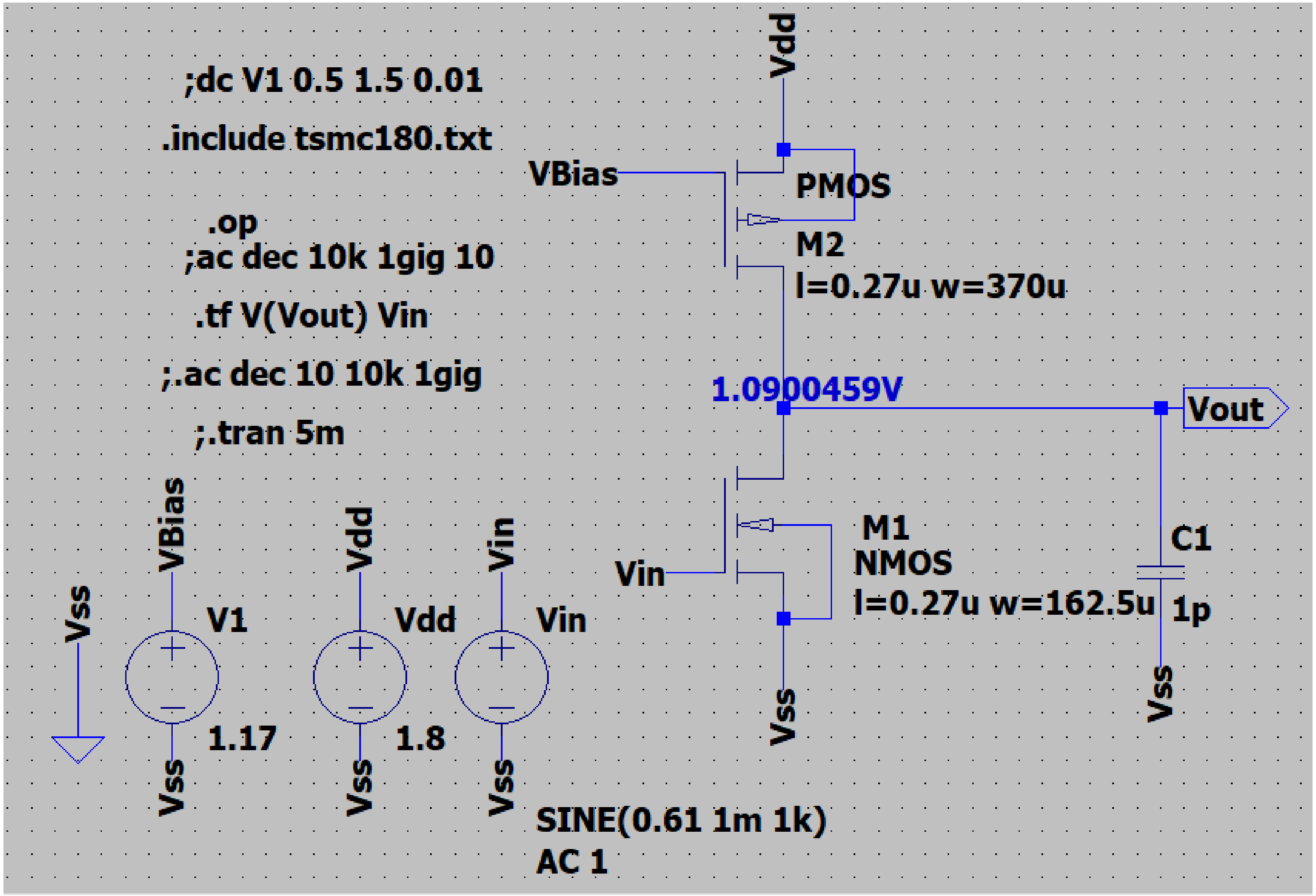


# Calculation

- BW= $\frac{1}{2\pi\ .Rout.CL}$ ---(i) Av= gm.Rout ----(ii)
- Rout= ro1 || ro2 ----(iii) ro= $\frac{1}{gds}$ ----(iv)
- W= id/(id/w) ----(v)
- Rout= 1.6 kΩ gm=18.75 mS
- **Choose gm/id=15**
- Id= 1.25 mA
- **For M1(NMOS)**
- gm/gds = 24.4 v/v ----from chart id/w= 7.69 ----from chart
- gds= 768.4 μS
- ro1= 1.3 KΩ
- Vgs=0.61 V
- $\frac{W}{L}$= $\frac{162.5\mu m}{0.27\ \mu m}$

- **For M2(PMOS)**
- Id= 1.25 Ma
- Gm/gds = 10.2  ----(Choose)
- Gm= 12.75mA
- gm/gds = 72.8 v/v ----from chart
- id/w= 3.37 ----from chart
- gds= 175.1 µS
- ro2= 5.71  KΩ
- Vbias= 1.15 V  -----from chart
- $\frac{W}{L} = \frac{370 \mu m}{0.27\ \mu m}$

# Simulation



;dc V1 0.5 1.5 0.01
.include tsmc180.txt
.op
;ac dec 10k 1gig 10
.tf V(Vout) Vin
;.ac dec 10 10k 1gig
;.tran 5m
Vdd
VBias
PMOS
M2
l=0.27u w=370u
1.0900459V
Vout
M1
NMOS
l=0.27u w=162.5u
C1
1p
Vin
Vss
VBias
V1
1.17
Vdd
1.8
Vin
SINE(0.61 1m 1k)
AC 1

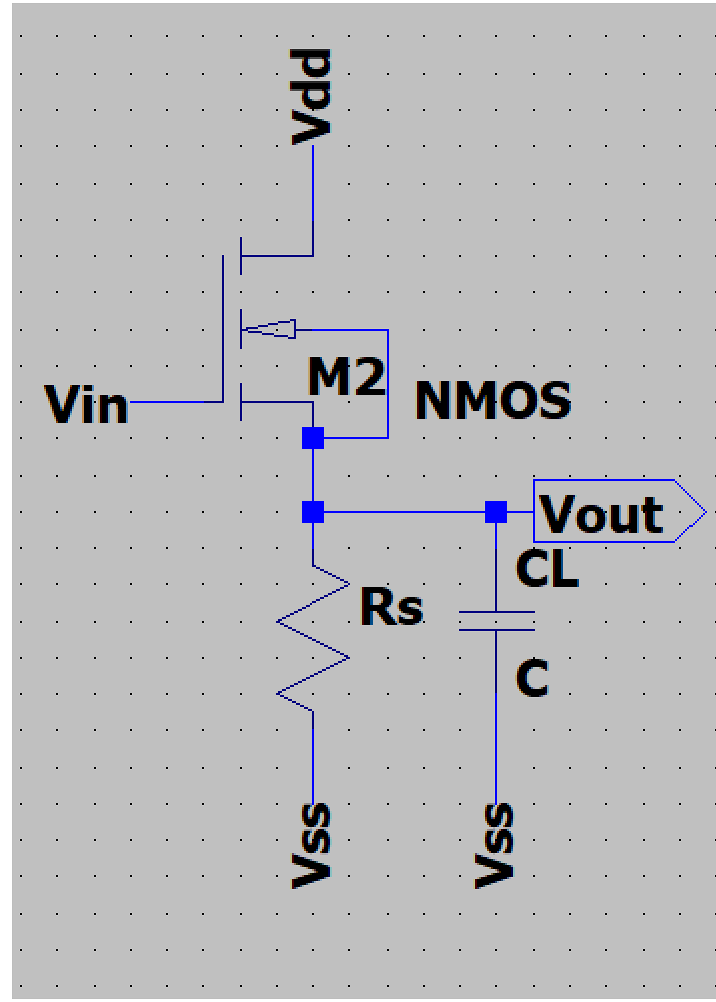
# Result and Conclusion

- Simulation output
- Av= -50.31
- gmn = 18.5 mS
- Gmp=14.8 mS
- Gdsn=216 µS
- Gdsp=152 µS
- BW= 41.9 MHz
- Id =1.2 mA
- Vds= 0.9v
- Pd =2.17 mW
- GBW= 2.1 GHz

Design parameter
Av= -30
gmn = 18.75 mS
Gmp= 12.75 mS
Gdsn =768.4 µS
Gdsp = 175.1 µS
BW= 100 MHz
Id =1.25 mA
GBW= 3 GHz

# Common Drain Amplifier

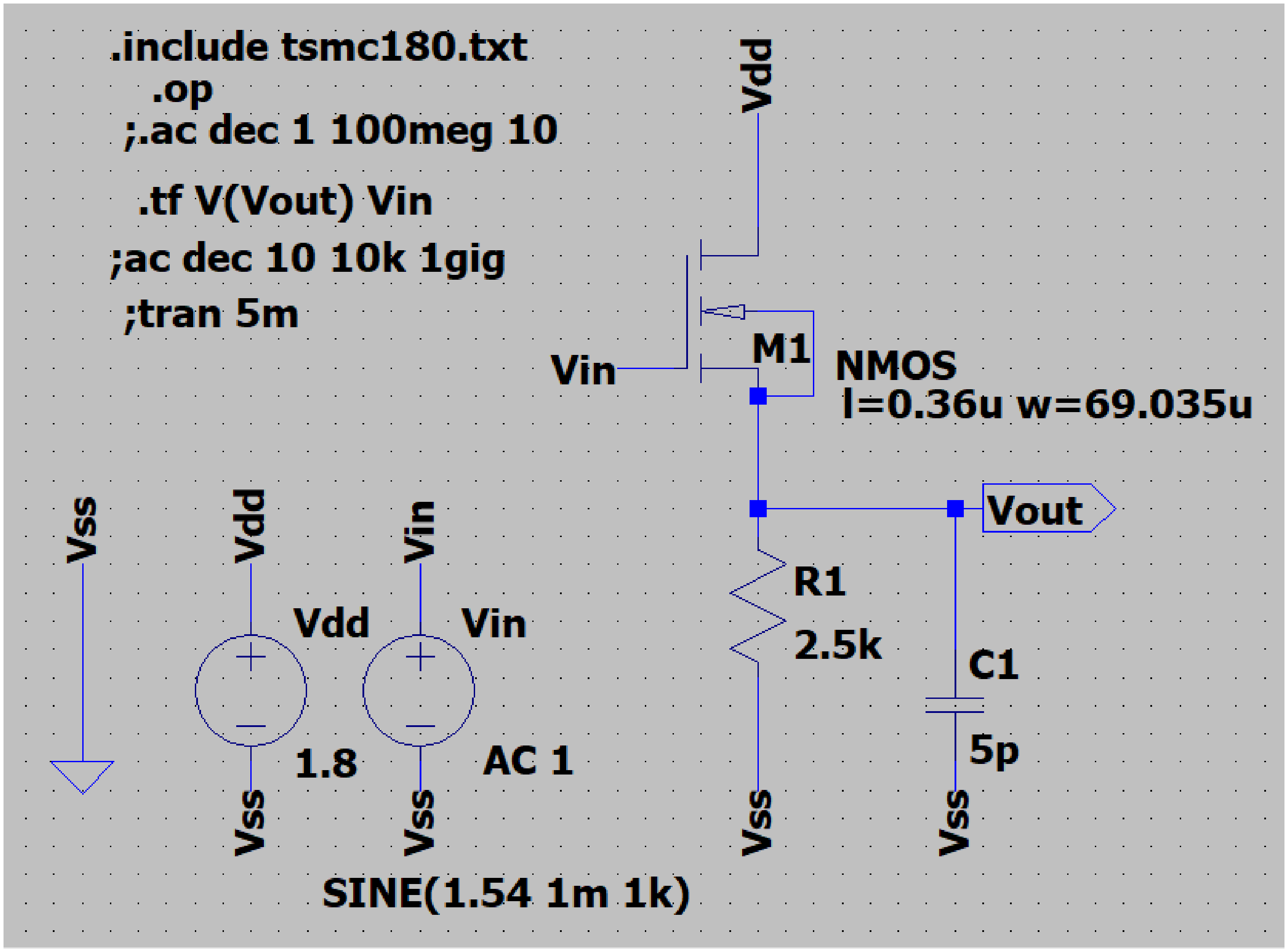
Specification
Av= 0.95 v/v
BW= 200 MHz
CL= 5pF
Vdd= 1.8V



# Calculation

- Av= $\frac{(Rs||ro)}{\frac{1}{gm}+(Rs||ro)}$ Rout=$\frac{1}{gm}$ || ro || Rs
- BW= $\frac{1}{2\pi\ .Rout.CL}$
- Rout = 159 Ω
- Gm=5.9 mS
- Choose gm/id= 15.1
- Id= 390 μA
- Gm/gds= 44.5 ---- from chart
- Gds=132.5 μS ro=7.54 k Ω
- Rs=5.62k Ω
- **Note: Rs= 2.5KΩ (iteration value)**
- $\frac{id}{w} = 5.65$ --from chart
- W=69.03μm

# Simulation



.include tsmc180.txt
.op
;.ac dec 1 100meg 10
.tf V(Vout) Vin
;ac dec 10 10k 1gig
;tran 5m
Vdd
Vin
M1
NMOS
l=0.36u w=69.035u
Vout
R1
2.5k
C1
5p
Vss
Vdd
Vin
Vdd
Vin
1.8
AC 1
Vss
Vss
Vss
Vss
SINE(1.54 1m 1k)

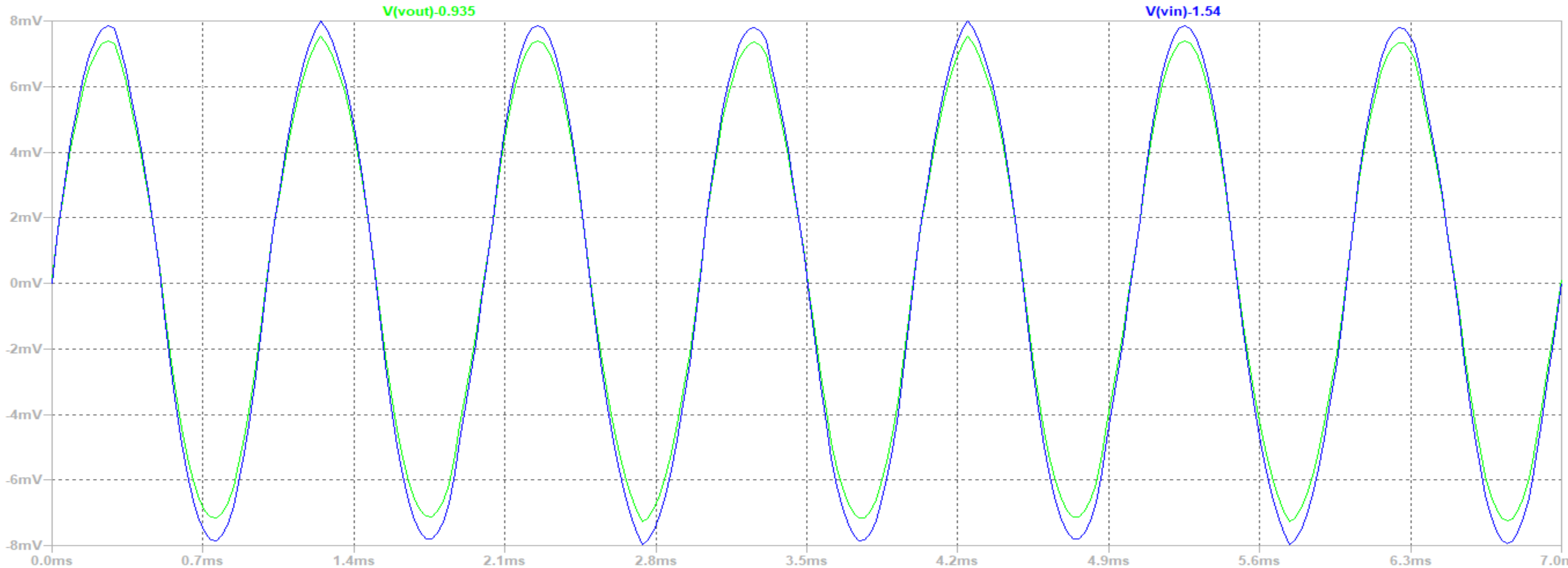
# Result and conclusion

- Simulation output
- Av= 0.927
- Rout = 161.3Ω
- gm = 5.75 mS
- **Gds=49.2 µS**
- BW= 205.3 MHz
- Id =374 µA
- Vds= 0.935 V
- Pd =673.2 µw

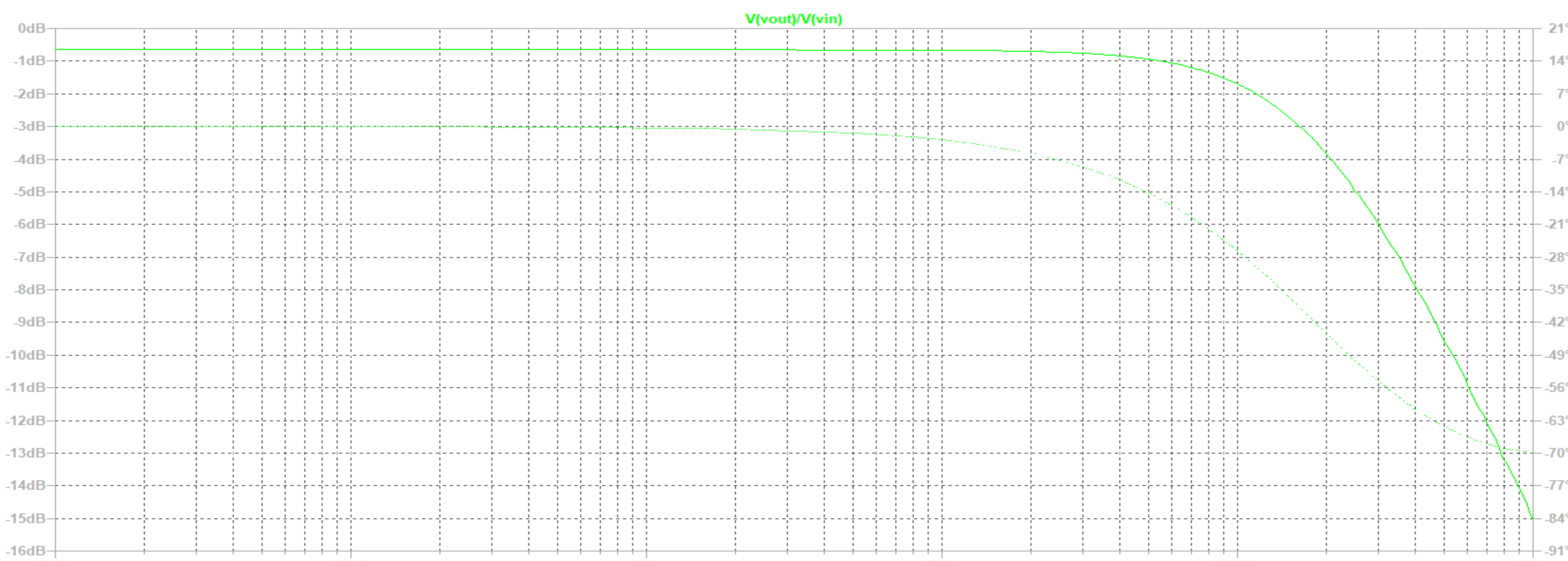
Design parameter
Av= 0.95
BW= 200 MHz

gm = 5.9 mS
**Gds=132.5 µS**
Id =390 µA

# Waveform



V(vout)-0.935
V(vin)-1.54
8mV
6mV
4mV
2mV
0mV
-2mV
-4mV
-6mV
-8mV
0.0ms
0.7ms
1.4ms
2.1ms
2.8ms
3.5ms
4.2ms
4.9ms
5.6ms
6.3ms
7.0ms

V(vout)/V(vin)
0dB
-1dB
-2dB
-3dB
-4dB
-5dB
-6dB
-7dB
-8dB
-9dB
-10dB
-11dB
-12dB
-13dB
-14dB
-15dB
-16dB
21°
14°
7°
0°
-7°
-14°
-21°
-28°
-35°
-42°
-49°
-56°
-63°
-70°
-77°
-84°
-91°
10KHz
100KHz
1MHz
10MHz
100MHz
1GHz

# Reference

- The gm/ID Design Methodology Demystified
  - Dr. Hesham A. Omran
- Youtube link: https://youtu.be/2FdDI2qpL5Q
- Ross Walker, ECE/CS 5720/6720 Fall 2017 University of Utah

Thank You