



WEEK-5 PRESENTATION ANALOG DESIGN INTERNSHIP

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SESSION OUTLINE

- Previous Preview
- ADT Toolbox
- Source Follower Amplifier design
- Common Source Amplifier design
- Differential Pair design
- Operational Amplifier design
- Project: Two stage op-amp design



WEEK-1

- Extract Charts for NMOS & PMOS
- g_m/g_{ds} vs g_m/i_d
- V_{gs} vs g_m/i_d
- I_d/w vs g_m/i_d
- Design Common Source and Source Follower Amplifier from charts.
- Observe large (W/L) ratios.



Week-2

- Design Current Mirror
- Design Delay Cell
- Design Common Source amplifier, Differential Pair and op-amp with Small (W/L) ratios.

Week-3

- Design Cascode CS amplifier & op-amp.



ADT TOOLBOX

- Official link: <https://at.master-micro.com>

The screenshot shows the homepage of the ADT Toolbox website. The header features the ADT logo (Analog Designer's Toolbox) and navigation links: 'What is ADT?', 'ADT Features', 'Pricing Plans', 'Contact Us', 'Downloads', 'Request Demo' (a grey button), and 'Dashboard' (a blue button). The main content area has the title 'Analog Designer's Toolbox' in large white text, followed by the tagline 'From Designers...To Designers'. Below this are two buttons: a red 'Watch ADT Demo' button and a blue 'Download Windows Version v1.8' button. A link 'Not your OS?' is positioned below the blue button. To the right, there is a stack of three overlapping screenshots of the software interface, showing various plots and data tables. On the far right edge, there is a vertical social media sidebar with icons for LinkedIn, Facebook, and YouTube.

DESIGN BY USING ADT TOOLBOX

- The Analog Designer's Toolbox (ADT): Towards a new paradigm for analog IC design.
- ADT provides a turnkey solution that enables everyone to reap the benefits of the GM/ID design methodology powered by pre-computed lookup tables (LUTs).
- At the device level, ADT Device Xplore gives an easy interface to plot arbitrary design charts involving complex expressions.
- The designer can explore devices from different technologies at different corners and temperatures, and extract simulator-accurate design points while taking second-order effects into consideration.

CONTINUE.....

- At the block level, ADT Design Xplore gives the designer the power of design space exploration, constraints management, live tuning, and optimization, all in a single cockpit without invoking the simulator.
- Moreover, with a single click, ADT can build the testbenches in the background and report the results from your favorite simulator. The aim of ADT is to boost productivity, restore designer's intuition, and make the design process systematic, optimized, and fun!



ADT TOOLBOX INTERFACE

LUT GENERATION

Analog Designer's Toolbox (Non-commercial use only)

File View Tabs Tools Help

Work Directory: C:\Users\ASUS\Desktop\ADT_Windows_Release_v1.1.8\ADT_Windows_Release_v1.1.8\ADT

LUT Generation

Simulator Settings

Simulator: LTspice
Simulation Command: C:\Program Files\TC\LTspiceXVII\XVIIx64.exe
Netlist Path: Release_v1.1.8\ADT\ltspice_example\ex_ltspice_netlist.cir

LUT Save Settings

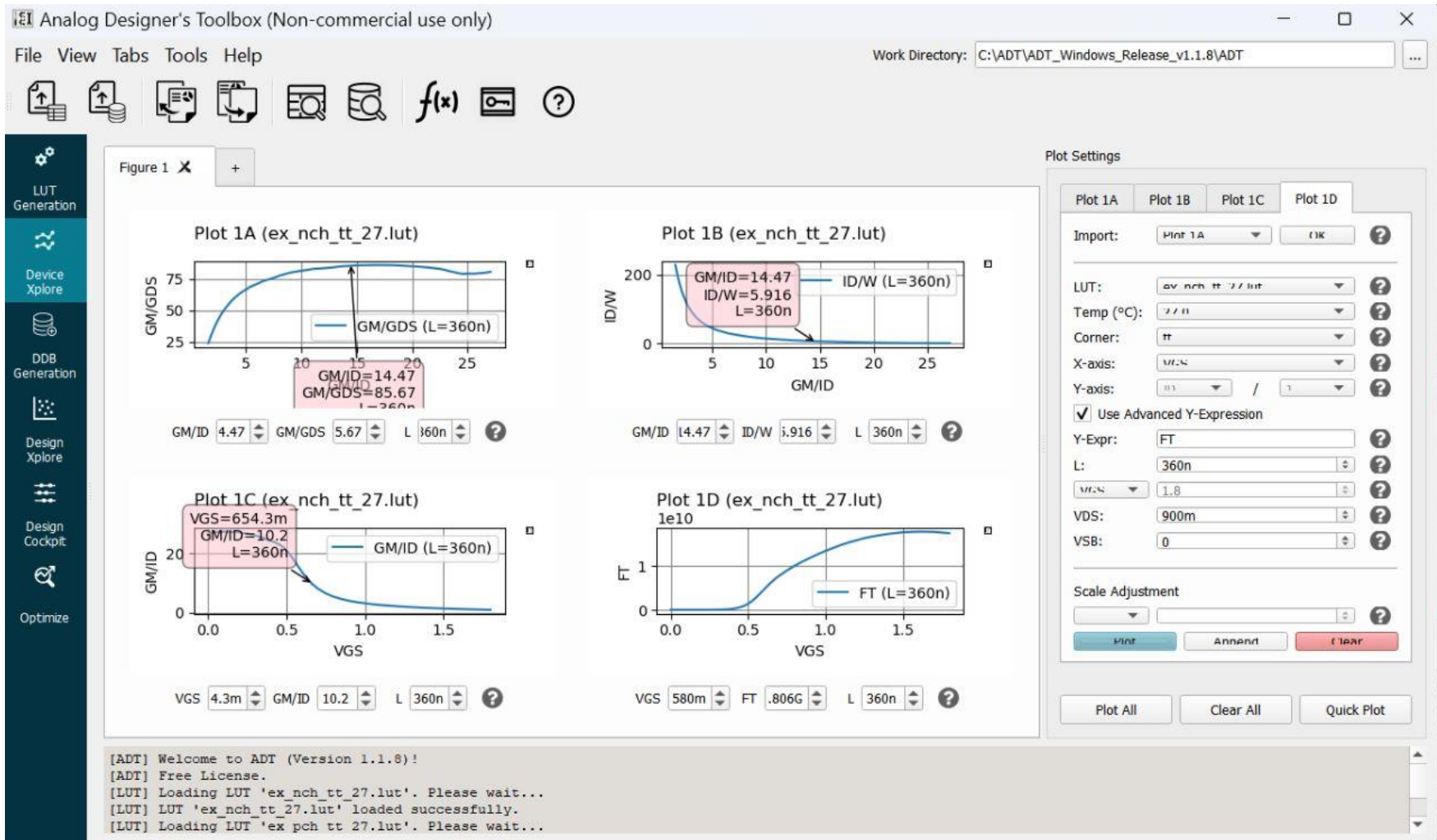
Save Path: If left empty, the LUTs will be saved in the work directory.
LUT Prefix Name: ex
☐ Save every device corner in a separate LUT file.

Device Characterization Parameters

MOSFET BJT

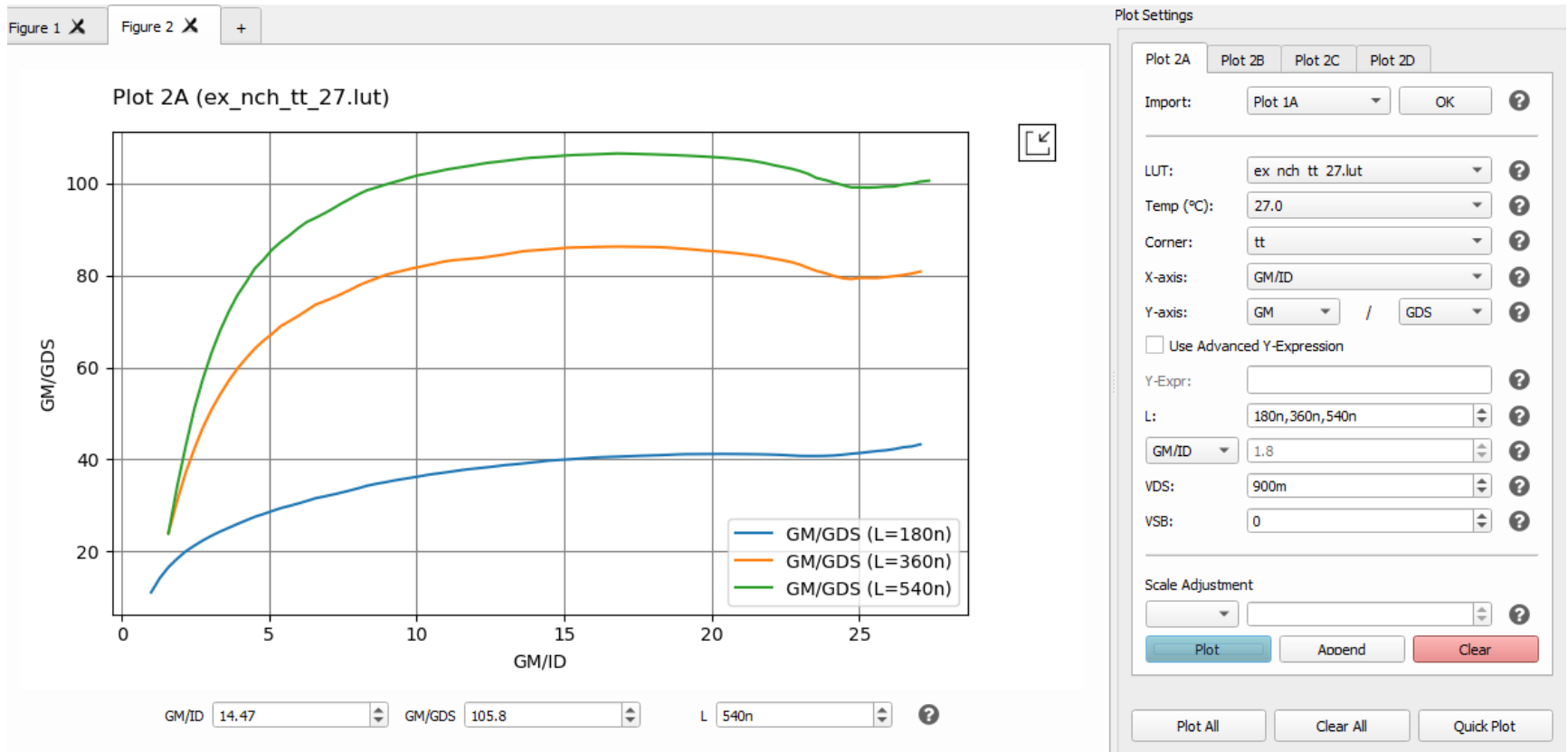
Ref. Width per Finger: 10u
Ref. No. of Fingers: 1
Length: 0.18u:0.02u:0.5u, 0.6u:0.1u:1u, 1.2u:0.2u:2u
VGS: 0:20m:1.2, 1.25:50m:1.8
VDS: 25m:25m:1.2, 1.3:0.1:1.8
VSB: 0:50m:1.2, 1.3:0.1:1.8
Output Variables: 0:1 0:2 0:3 0:4 0:5 0:6 0:7 0:8 0:9 0:10 0:11 0:12 0:13 0:14 0:15 0:16 0:17 0:18 0:19 0:20 0:21 0:22 0:23 0:24 0:25 0:26 0:27 0:28 0:29 0:30 0:31 0:32 0:33 0:34 0:35 0:36 0:37 0:38 0:39 0:40 0:41 0:42 0:43 0:44 0:45 0:46 0:47 0:48 0:49 0:50 0:51 0:52 0:53 0:54 0:55 0:56 0:57 0:58 0:59 0:60 0:61 0:62 0:63 0:64 0:65 0:66 0:67 0:68 0:69 0:70 0:71 0:72 0:73 0:74 0:75 0:76 0:77 0:78 0:79 0:80 0:81 0:82 0:83 0:84 0:85 0:86 0:87 0:88 0:89 0:90 0:91 0:92 0:93 0:94 0:95 0:96 0:97 0:98 0:99 0:100 0:101 0:102 0:103 0:104 0:105 0:106 0:107 0:108 0:109 0:110 0:111 0:112 0:113 0:114 0:115 0:116 0:117 0:118 0:119 0:120 0:121 0:122 0:123 0:124 0:125 0:126 0:127 0:128 0:129 0:130 0:131 0:132 0:133 0:134 0:135 0:136 0:137 0:138 0:139 0:140 0:141 0:142 0:143 0:144 0:145 0:146 0:147 0:148 0:149 0:150 0:151 0:152 0:153 0:154 0:155 0:156 0:157 0:158 0:159 0:160 0:161 0:162 0:163 0:164 0:165 0:166 0:167 0:168 0:169 0:170 0:171 0:172 0:173 0:174 0:175 0:176 0:177 0:178 0:179 0:180 0:181 0:182 0:183 0:184 0:185 0:186 0:187 0:188 0:189 0:190 0:191 0:192 0:193 0:194 0:195 0:196 0:197 0:198 0:199 0:200 0:201 0:202 0:203 0:204 0:205 0:206 0:207 0:208 0:209 0:210 0:211 0:212 0:213 0:214 0:215 0:216 0:217 0:218 0:219 0:220 0:221 0:222 0:223 0:224 0:225 0:226 0:227 0:228 0:229 0:230 0:231 0:232 0:233 0:234 0:235 0:236 0:237 0:238 0:239 0:240 0:241 0:242 0:243 0:244 0:245 0:246 0:247 0:248 0:249 0:250 0:251 0:252 0:253 0:254 0:255 0:256 0:257 0:258 0:259 0:260 0:261 0:262 0:263 0:264 0:265 0:266 0:267 0:268 0:269 0:270 0:271 0:272 0:273 0:274 0:275 0:276 0:277 0:278 0:279 0:280 0:281 0:282 0:283 0:284 0:285 0:286 0:287 0:288 0:289 0:290 0:291 0:292 0:293 0:294 0:295 0:296 0:297 0:298 0:299 0:300 0:301 0:302 0:303 0:304 0:305 0:306 0:307 0:308 0:309 0:310 0:311 0:312 0:313 0:314 0:315 0:316 0:317 0:318 0:319 0:320 0:321 0:322 0:323 0:324 0:325 0:326 0:327 0:328 0:329 0:330 0:331 0:332 0:333 0:334 0:335 0:336 0:337 0:338 0:339 0:340 0:341 0:342 0:343 0:344 0:345 0:346 0:347 0:348 0:349 0:350 0:351 0:352 0:353 0:354 0:355 0:356 0:357 0:358 0:359 0:360 0:361 0:362 0:363 0:364 0:365 0:366 0:367 0:368 0:369 0:370 0:371 0:372 0:373 0:374 0:375 0:376 0:377 0:378 0:379 0:380 0:381 0:382 0:383 0:384 0:385 0:386 0:387 0:388 0:389 0:390 0:391 0:392 0:393 0:394 0:395 0:396 0:397 0:398 0:399 0:400 0:401 0:402 0:403 0:404 0:405 0:406 0:407 0:408 0:409 0:410 0:411 0:412 0:413 0:414 0:415 0:416 0:417 0:418 0:419 0:420 0:421 0:422 0:423 0:424 0:425 0:426 0:427 0:428 0:429 0:430 0:431 0:432 0:433 0:434 0:435 0:436 0:437 0:438 0:439 0:440 0:441 0:442 0:443 0:444 0:445 0:446 0:447 0:448 0:449 0:450 0:451 0:452 0:453 0:454 0:455 0:456 0:457 0:458 0:459 0:460 0:461 0:462 0:463 0:464 0:465 0:466 0:467 0:468 0:469 0:470 0:471 0:472 0:473 0:474 0:475 0:476 0:477 0:478 0:479 0:480 0:481 0:482 0:483 0:484 0:485 0:486 0:487 0:488 0:489 0:490 0:491 0:492 0:493 0:494 0:495 0:496 0:497 0:498 0:499 0:500 0:501 0:502 0:503 0:504 0:505 0:506 0:507 0:508 0:509 0:510 0:511 0:512 0:513 0:514 0:515 0:516 0:517 0:518 0:519 0:520 0:521 0:522 0:523 0:524 0:525 0:526 0:527 0:528 0:529 0:530 0:531 0:532 0:533 0:534 0:535 0:536 0:537 0:538 0:539 0:540 0:541 0:542 0:543 0:544 0:545 0:546 0:547 0:548 0:549 0:550 0:551 0:552 0:553 0:554 0:555 0:556 0:557 0:558 0:559 0:560 0:561 0:562 0:563 0:564 0:565 0:566 0:567 0:568 0:569 0:570 0:571 0:572 0:573 0:574 0:575 0:576 0:577 0:578 0:579 0:580 0:581 0:582 0:583 0:584 0:585 0:586 0:587 0:588 0:589 0:590 0:591 0:592 0:593 0:594 0:595 0:596 0:597 0:598 0:599 0:600 0:601 0:602 0:603 0:604 0:605 0:606 0:607 0:608 0:609 0:610 0:611 0:612 0:613 0:614 0:615 0:616 0:617 0:618 0:619 0:620 0:621 0:622 0:623 0:624 0:625 0:626 0:627 0:628 0:629 0:630 0:631 0:632 0:633 0:634 0:635 0:636 0:637 0:638 0:639 0:640 0:641 0:642 0:643 0:644 0:645 0:646 0:647 0:648 0:649 0:650 0:651 0:652 0:653 0:654 0:655 0:656 0:657 0:658 0:659 0:660 0:661 0:662 0:663 0:664 0:665 0:666 0:667 0:668 0:669 0:670 0:671 0:672 0:673 0:674 0:675 0:676 0:677 0:678 0:679 0:680 0:681 0:682 0:683 0:684 0:685 0:686 0:687 0:688 0:689 0:690 0:691 0:692 0:693 0:694 0:695 0:696 0:697 0:698 0:699 0:700 0:701 0:702 0:703 0:704 0:705 0:706 0:707 0:708 0:709 0:710 0:711 0:712 0:713 0:714 0:715 0:716 0:717 0:718 0:719 0:720 0:721 0:722 0:723 0:724 0:725 0:726 0:727 0:728 0:729 0:730 0:731 0:732 0:733 0:734 0:735 0:736 0:737 0:738 0:739 0:740 0:741 0:742 0:743 0:744 0:745 0:746 0:747 0:748 0:749 0:750 0:751 0:752 0:753 0:754 0:755 0:756 0:757 0:758 0:759 0:760 0:761 0:762 0:763 0:764 0:765 0:766 0:767 0:768 0:769 0:770 0:771 0:772 0:773 0:774 0:775 0:776 0:777 0:778 0:779 0:780 0:781 0:782 0:783 0:784 0:785 0:786 0:787 0:788 0:789 0:790 0:791 0:792 0:793 0:794 0:795 0:796 0:797 0:798 0:799 0:800 0:801 0:802 0:803 0:804 0:805 0:806 0:807 0:808 0:809 0:810 0:811 0:812 0:813 0:814 0:815 0:816 0:817 0:818 0:819 0:820 0:821 0:822 0:823 0:824 0:825 0:826 0:827 0:828 0:829 0:830 0:831 0:832 0:833 0:834 0:835 0:836 0:837 0:838 0:839 0:840 0:841 0:842 0:843 0:844 0:845 0:846 0:847 0:848 0:849 0:850 0:851 0:852 0:853 0:854 0:855 0:856 0:857 0:858 0:859 0:860 0:861 0:862 0:863 0:864 0:865 0:866 0:867 0:868 0:869 0:870 0:871 0:872 0:873 0:874 0:875 0:876 0:877 0:878 0:879 0:880 0:881 0:882 0:883 0:884 0:885 0:886 0:887 0:888 0:889 0:890 0:891 0:892 0:893 0:894 0:895 0:896 0:897 0:898 0:899 0:900 0:901 0:902 0:903 0:904 0:905 0:906 0:907 0:908 0:909 0:910 0:911 0:912 0:913 0:914 0:915 0:916 0:917 0:918 0:919 0:920 0:921 0:922 0:923 0:924 0:925 0:926 0:927 0:928 0:929 0:930 0:931 0:932 0:933 0:934 0:935 0:936 0:937 0:938 0:939 0:940 0:941 0:942 0:943 0:944 0:945 0:946 0:947 0:948 0:949 0:950 0:951 0:952 0:953 0:954 0:955 0:956 0:957 0:958 0:959 0:960 0:961 0:962 0:963 0:964 0:965 0:966 0:967 0:968 0:969 0:970 0:971 0:972 0:973 0:974 0:975 0:976 0:977 0:978 0:979 0:980 0:981 0:982 0:983 0:984 0:985 0:986 0:987 0:988 0:989 0:990 0:991 0:992 0:993 0:994 0:995 0:996 0:997 0:998 0:999 1000 1001 1002 1003 1004 1005 1006 1007 1008 1009 1010 1011 1012 1013 1014 1015 1016 1017 1018 1019 1020 1021 1022 1023 1024 1025 1026 1027 1028 1029 1030 1031 1032 1033 1034 1035 1036 1037 1038 1039 1040 1041 1042 1043 1044 1045 1046 1047 1048 1049 1050 1051 1052 1053 1054 1055 1056 1057 1058 1059 1060 1061 1062 1063 1064 1065 1066 1067 1068 1069 1070 1071 1072 1073 1074 1075 1076 1077 1078 1079 1080 1081 1082 1083 1084 1085 1086 1087 1088 1089 1090 1091 1092 1093 1094 1095 1096 1097 1098 1099 1100 1101 1102 1103 1104 1105 1106 1107 1108 1109 1110 1111 1112 1113 1114 1115 1116 1117 1118 1119 1120 1121 1122 1123 1124 1125 1126 1127 1128 1129 1130 1131 1132 1133 1134 1135 1136 1137 1138 1139 1140 1141 1142 1143 1144 1145 1146 1147 1148 1149 1150 1151 1152 1153 1154 1155 1156 1157 1158 1159 1160 1161 1162 1163 1164 1165 1166 1167 1168 1169 1170 1171 1172 1173 1174 1175 1176 1177 1178 1179 1180 1181 1182 1183 1184 1185 1186 1187 1188 1189 1190 1191 1192 1193 1194 1195 1196 1197 1198 1199 1200 1201 1202 1203 1204 1205 1206 1207 1208 1209 1210 1211 1212 1213 1214 1215 1216 1217 1218 1219 1220 1221 1222 1223 1224 1225 1226 1227 1228 1229 1230 1231 1232 1233 1234 1235 1236 1237 1238 1239 1240 1241 1242 1243 1244 1245 1246 1247 1248 1249 1250 1251 1252 1253 1254 1255 1256 1257 1258 1259 1260 1261 1262 1263 1264 1265 1266 1267 1268 1269 1270 1271 1272 1273 1274 1275 1276 1277 1278 1279 1280 1281 1282 1283 1284 1285 1286 1287 1288 1289 1290 1291 1292 1293 1294 1295 1296 1297 1298 1299 1300 1301 1302 1303 1304 1305 1306 1307 1308 1309 1310 1311 1312 1313 1314 1315 1316 1317 1318 1319 1320 1321 1322 1323 1324 1325 1326 1327 1328 1329 1330 1331 1332 1333 1334 1335 1336 1337 1338 1339 1340 1341 1342 1343 1344 1345 1346 1347 1348 1349 1350 1351 1352 1353 1354 1355 1356 1357 1358 1359 1360 1361 1362 1363 1364 1365 1366 1367 1368 1369 1370 1371 1372 1373 1374 1375 1376 1377 1378 1379 1380 1381 1382 1383 1384 1385 1386 1387 1388 1389 1390 1391 1392 1393 1394 1395 1396 1397 1398 1399 1400 1401 1402 1403 1404 1405 1406 1407 1408 1409 1410 1411 1412 1413 1414 1415 1416 1417 1418 1419 1420 1421 1422 1423 1424 1425 1426 1427 1428 1429 1430 1431 1432 1433 1434 1435 1436 1437 1438 1439 1440 1441 1442 1443 1444 1445 1446 1447 1448 1449 1450 1451 1452 1453 1454 1455 1456 1457 1458 1459 1460 1461 1462 1463 1464 1465 1466 1467 1468 1469 1470 1471 1472 1473 1474 1475 1476 1477 1478 1479 1480 1481 1482 1483 1484 1485 1486 1487 1488 1489 1490 1491 1492 1493 1494 1495 1496 1497 1498 1499 1500 1501 1502 1503 1504 1505 1506 1507 1508 1509 1510 1511 1512 1513 1514 1515 1516 1517 1518 1519 1520 1521 1522 1523 1524 1525 1526 1527 1528 1529 1530 1531 1532 1533 1534 1535 1536 1537 1538 1539 1540 1541 1542 1543 1544 1545 1546 1547 1548 1549 1550 1551 1552 1553 1554 1555 1556 1557 1558 1559 1560 1561 1562 1563 1564 1565 1566 1567 1568 1569 1570 1571 1572 1573 1574 1575 1576 1577 1578 1579 1580 1581 1582 1583 1584 1585 1586 1587 1588 1589 1590 1591 1592 1593 1594 1595 1596 1597 1598 1599 1600 1601 1602 1603 1604 1605 1606 1607 1608 1609 1610 1611 1612 1613 1614 1615 1616 1617 1618 1619 1620 1621 1622 1623 1624 1625 1626 1627 1628 1629 1630 1631 1632 1633 1634 1635 1636 1637 1638 1639 1640 1641 1642 1643 1644 1645 1646 1647 1648 1649 1650 1651 1652 1653 1654 1655 1656 1657 1658 1659 1660 1661 1662 1663 1664 1665 1666 1667 1668 1669 1670 1671 1672 1673 1674 1675 1676 1677 1678 1679 1680 1681 1682 1683 1684 1685 1686 1687 1688 1689 1690 1691 1692 1693 1694 1695 1696 1697 1698 1699 1700 1701 1702 1703 1704 1705 1706 1707 1708 1709 1710 1711 1712 1713 1714 1715 1716 1717 1718 1719 1720 1721 1722 1723 1724 1725 1726 1727 1728 1729 1730 1731 1732 1733 1734 1735 1736 1737 1738 1739 1740 1741 1742 1743 1744 1745 1746 1747 1748 1749 1750 1751 1752 1753 1754 1755 1756 1757 1758 1759 1760 1761 1762 1763 1764 1765 1766 1767 1768 1769 1770 1771 1772 1773 1774 1775 1776 1777 1778 1779 1780 1781 1782 1783 1784 1785 1786 1787 1788 1789 1790 1791 1792 1793 1794 1795 1796 1797 1798 1799 1800 1801 1802 1803 1804 1805 1806 1807 1808 1809 1810 1811 1812 1813 1814 1815 1816 1817 1818 1819 1820 1821 1822 1823 1824 1825 1826 1827 1828 1829 1830 1831 1832 1833 1834 1835 1836 1837 1838 1839 1840 1841 1842 1843 1844 1845 1846 1847 1848 1849 1850 1851 1852 1853 1854 1855 1856 1857 1858 1859 1860 1861 1862 1863 1864 1865 1866 1867 1868 1869 1870 1871 1872 1873 1874 1875 1876 1877 1878 1879 1880 1881 1882 1883 1884 1885 1886 1887 1888 1889 1890 1891 1892 1893 1894 1895 1896 1897 1898 1899 1900 1901 1902 1903 1904 1905 1906 1907 1908 1909 1910 1911 1912 1913 1914 1915 1916 1917 1918 1919 1920 1921 1922 1923 1924 1925 1926 1927 1928 1929 1930 1931 1932 1933 1934 1935 1936 1937 1938 1939 1940 1941 1942 1943 1944 1945 1946 1947 1948 1949 1950 1951 1952 1953 1954 1955 1956 1957 1958 1959 1960 1961 1962 1963 1964 1965 1966 1967 1968 1969 1970 1971 1972 1973 1974 1975 1976 1977 1978 1979 1980 1981 1982 1983 1984 1985 1986 1987 1988 1989 1990 1991 1992 1993 1994 1995 1996 1997 1998 1999 2000 2001 2002 2003 2004 2005 2006 2007 2008 2009 2010 2011 2012 2013 2014 2015 2016 2017 2018 2019 2020 2021 2022 2023 2024 2025 2026 2027 2028 2029 2030 2031 2032 2033 2034 2035 2036 2037 2038 2039 2040 2041 2042 2043 2044 2045 2046 2047 2048 2049 2050 2051 2052 2053 2054 2055 2056 2057 2058 2059 2060 2061 2062 2063 2064 2065 2066 2067 2068 2069 2070 2071 2072 2073 2074 2075 2076 2077 2078 2079 2080 2081 2082 2083 2084 2085 2086 2087 2088 2089 2090 2091 2092 2093 2094 2095 2096 2097 2098 2099 2100 2101 2102 2103 2104 2105 2106 2107 2108 2109 2110 2111 2112 2113 2114 2115 2116 2117 2118 2119 2120 2121 2122 2123 2124 2125 2126 2127 2128 2129 2130 2131 2132 2133 2134 2135 2136 2137 2138 2139 2140 2141 2142 2143 2144 2145 2146 2147 2148 2149 2150 2151 2152 2153 2154 2155 2156 2157 2158 2159 2160 2161 2162 2163 2164 2165 2166 2167 2168 2169 2170 2171 2172 2173 2174 2175 2176 2177 2178 2179 2180 2181 2182 2183 2184 2185 2186 2187 2188 2189 2190 2191 2192 2193 2194 2195 2196 2

ADT: DEVICE XPLORE

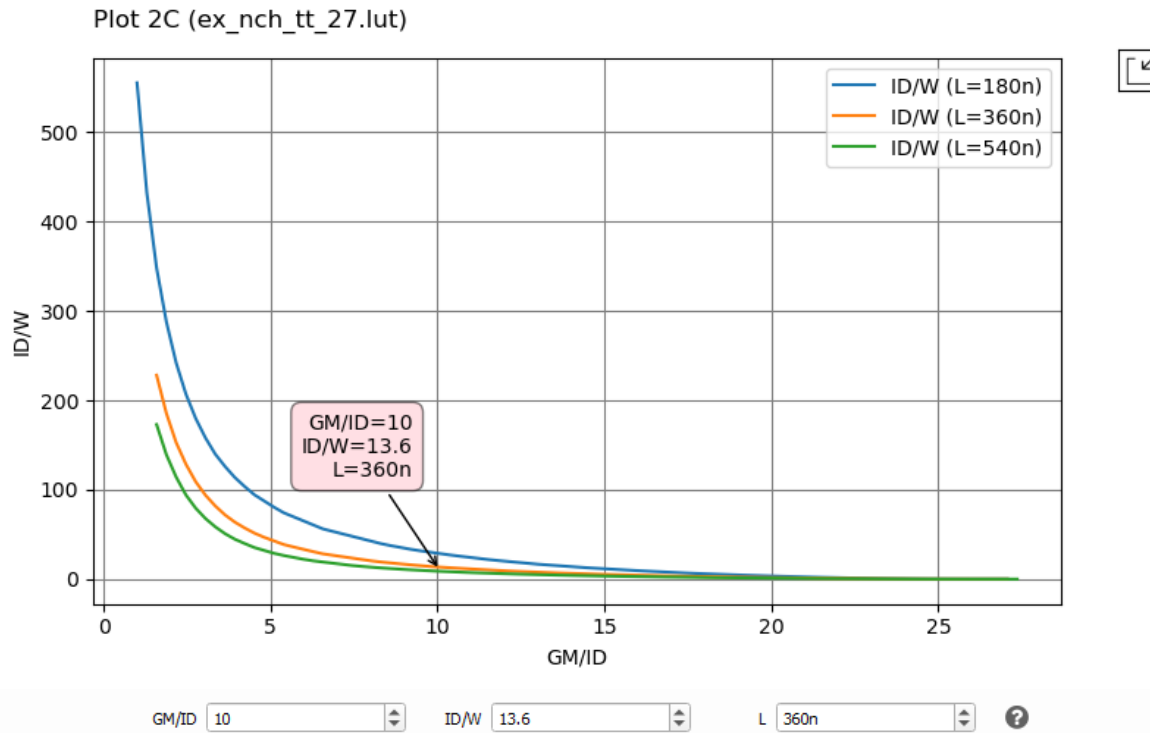


LUT INTERFACE

GM/GDS VS GM/ID CHART



ID/W VS GM/ID CHART



Plot 2A Plot 2B Plot 2C Plot 2D

Import: Plot 1A OK ?

LUT: ex_nch_tt_27.lut ?

Temp (°C): 27.0 ?

Corner: tt ?

X-axis: GM/ID ?

Y-axis: ID / W ?

☐ Use Advanced Y-Expression

Y-Expr: ?

L: 180n,360n,540n ?

GM/ID: 10 ?

VDS: 900m ?

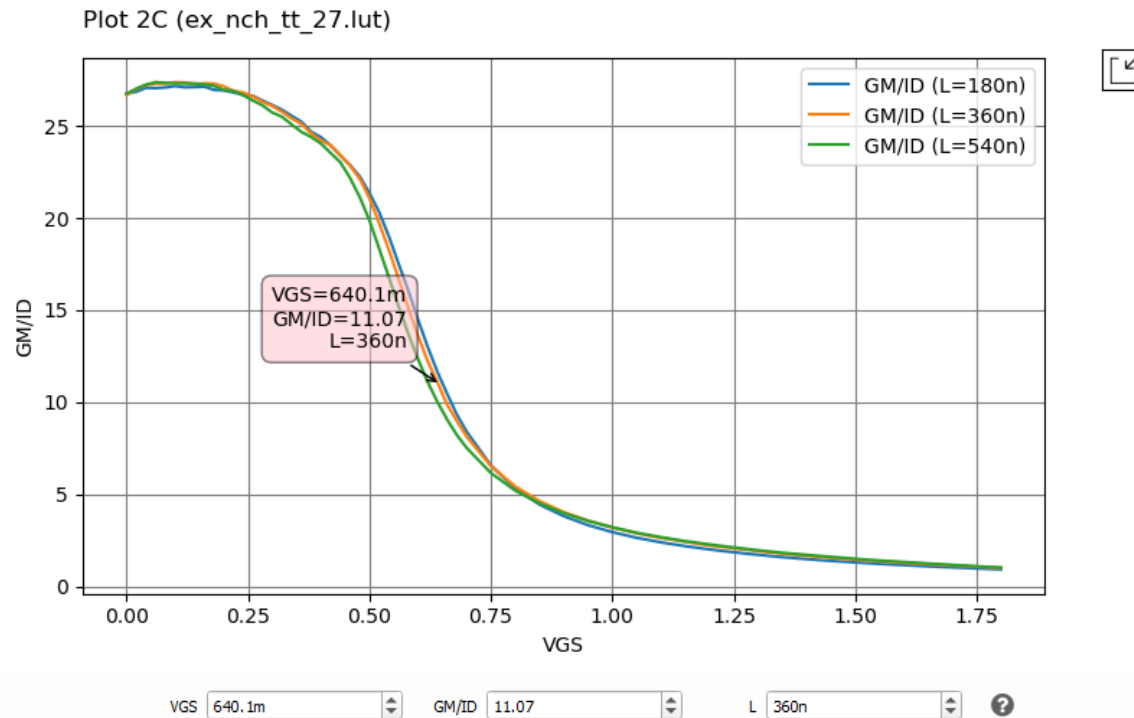
VSB: 0 ?

Scale Adjustment

Plot Append Clear

Plot All Clear All Quick Plot

VGS VS GM/ID CHARTS



Plot 2A Plot 2B Plot 2C Plot 2D

Import: Plot 1A OK ?

LUT: ex_nch_tt_27.lut ?

Temp (°C): 27.0 ?

Corner: tt ?

X-axis: VGS ?

Y-axis: GM / ID ?

☐ Use Advanced Y-Expression

Y-Expr: ?

L: 180n,360n,540n ?

VGS: 1.8 ?

VDS: 900m ?

VSB: 0 ?

Scale Adjustment

Plot Append Clear

Plot All Clear All Quick Plot

Note: We can draw many charts from ADT Device Xplore
e.g: ID/GDS, GBW, FT vs GM/ID



MODEL FILE USED

- File: CMOS180.txt
- Supply Voltage: 1.8 V
- <https://web.stanford.edu/~murmnn/gmid>
- 0.18 μ m CMOS models



SOURCE FOLLOWER AMPLIFIER

- **Specs:**

- $A_v=1$ $CL= 1\text{pF}$

- $R_{out}=75\ \Omega$

- $g_m/i_d= 10 \dots(\text{Choose})$

- $g_m/g_{ds}=76.93$

$I_d/w=14.58$

$V_{gs}=870\text{mV}$

- $g_m=13.33\ \text{mS}$

$W1=91.22\ \mu\text{m}$

$V_{in}=1.77\text{V}$

- $I_d=1.33\ \text{mA}$

$W1=66.6\ \mu\text{m}$ (tuning to get R_{out})

- $g_{ds}=172.2\ \mu\text{S}$

- $R_{o1}=5.77\ \text{K}\Omega$

- Let $R_{o2}=10\ \text{K}\Omega$

$g_{ds}=100\ \mu\text{S}$

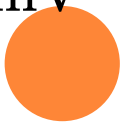
- $I_d/g_{ds}=13.3$

- $g_m/i_d=5.112$

$g_m/g_{ds}=67.36$

$V_{gs}=819.2\text{mV}$

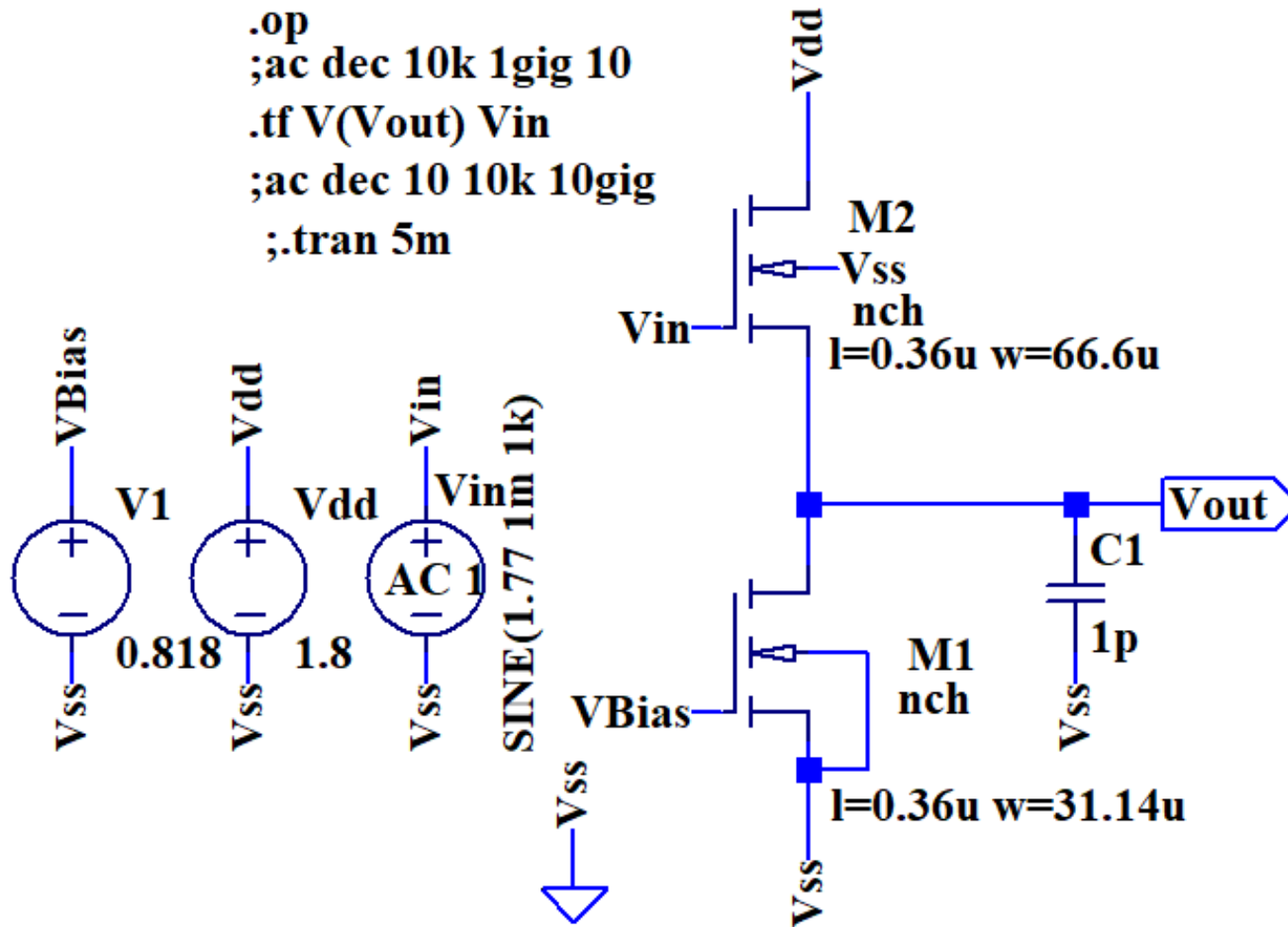
- $W2=31\ \mu\text{m}$



SIMULATION

```
.include "C:\Users\ASUS\Desktop\CMOS180.txt"
```

```
.op  
;ac dec 10k 1gig 10  
.tf V(Vout) Vin  
;ac dec 10 10k 10gig  
;.tran 5m
```

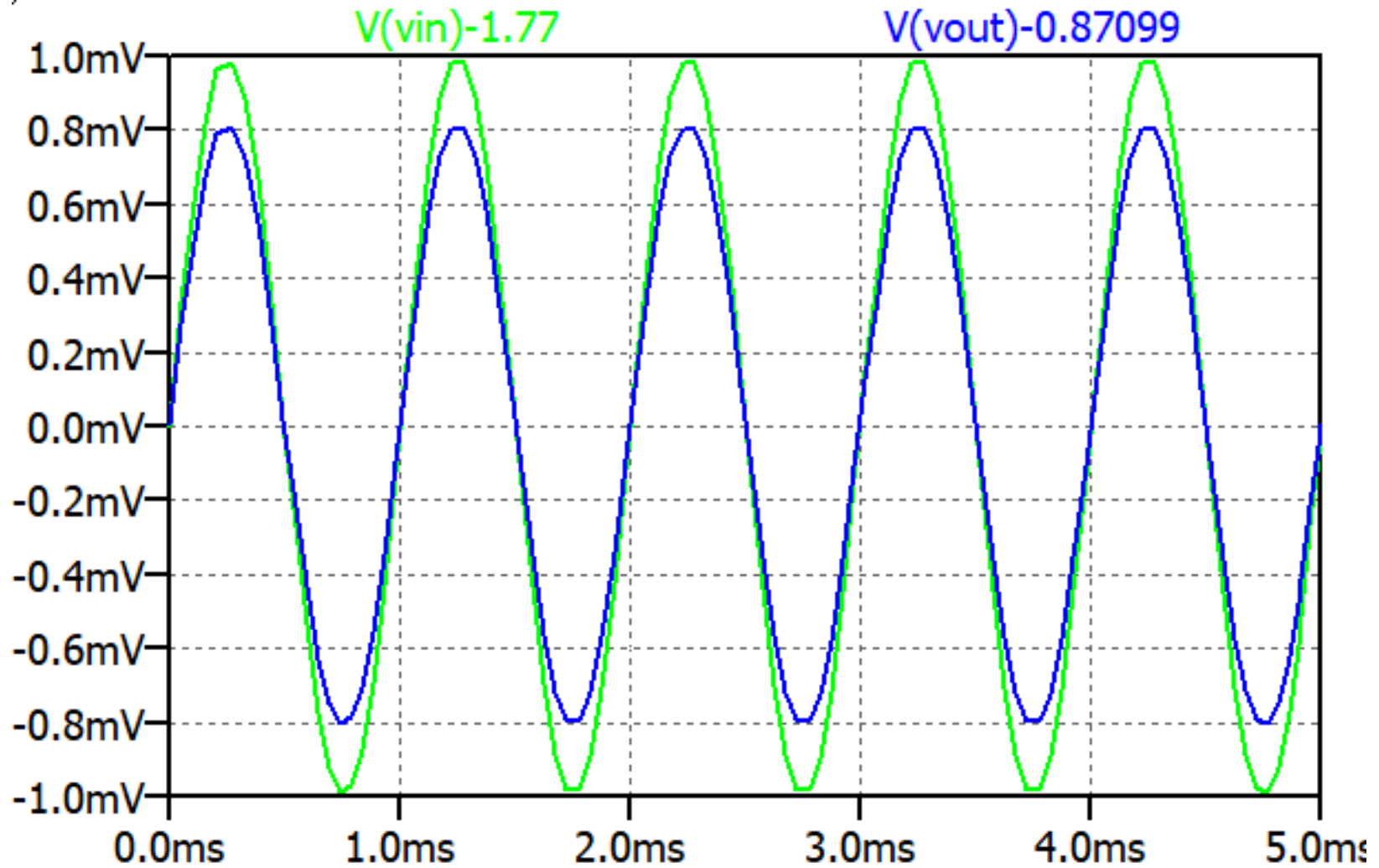


RESULT

Simulated Value	Specifications
$A_v = 0.814 \text{ v/v}$	$A_v = 1 \text{ v/v}$
$BW = 1.82 \text{ GHz}$	$BW = 2.12 \text{ GHz}$
$R_{out} = 75.1 \text{ } \Omega$	$R_{out} = 75 \text{ } \Omega$
$I_d = 1.3 \text{ mA}$	$I_d = 1.33 \text{ mA}$
$V_{out(dc)} = 0.87 \text{ V}$	$V_{out(dc)} = 0.9 \text{ V}$



TRANSIENT ANALYSIS



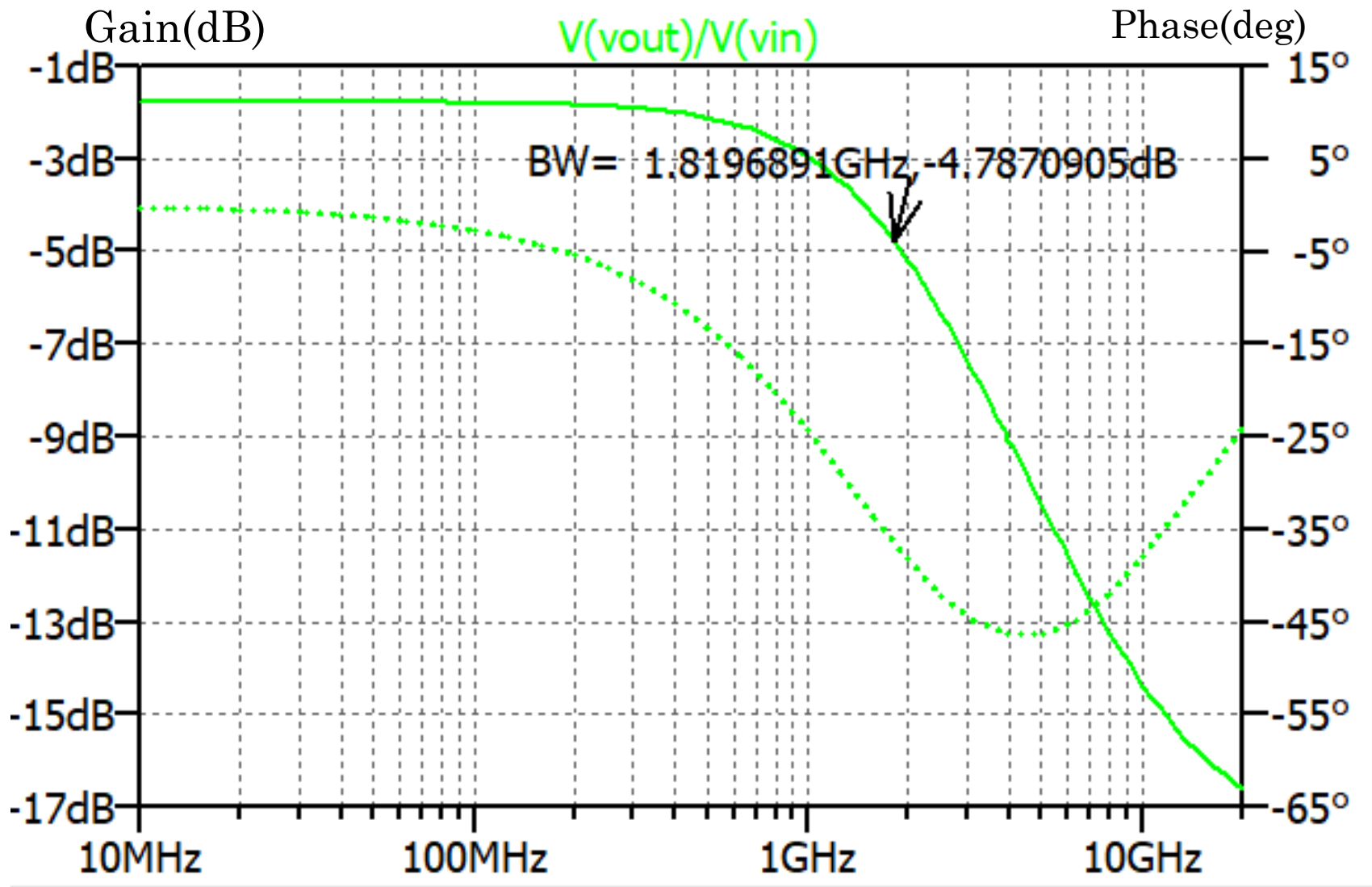
$V_{in}(p-p)=2 \text{ mV}$

$V_{out}=1.6 \text{ mV}$

Gain=0.8



FREQUENCY RESPONSE



Frequency

COMMON SOURCE AMPLIFIER

Specification:

Gain(A_v)=40

R_{out} =150 K Ω

BW=25 MHz

Calculation:

Formula Used

- $BW(3dB \text{ freq}) = \frac{1}{2\pi \cdot R_{out} \cdot C_L}$ $A_v = g_m \cdot R_{out}$
- $R_{out} = r_{o1} // r_{o2}$
- $C_L = 42.44 \text{ fF}$
- $g_m / I_D = 10$ (Choose)
- $g_m = 0.266 \text{ mS}$
- $I_D = 26.6 \mu A$
- $g_m / g_{ds} = 81.72$ from chart $I_D / W = 13.6$
- $g_{ds} = 3.25 \mu S$ $W_1 = 1.95 \mu m$
- $R_{o1} = 307.21 \text{ K}\Omega$ $V_{gs1} = 657.8 \text{ mV}$



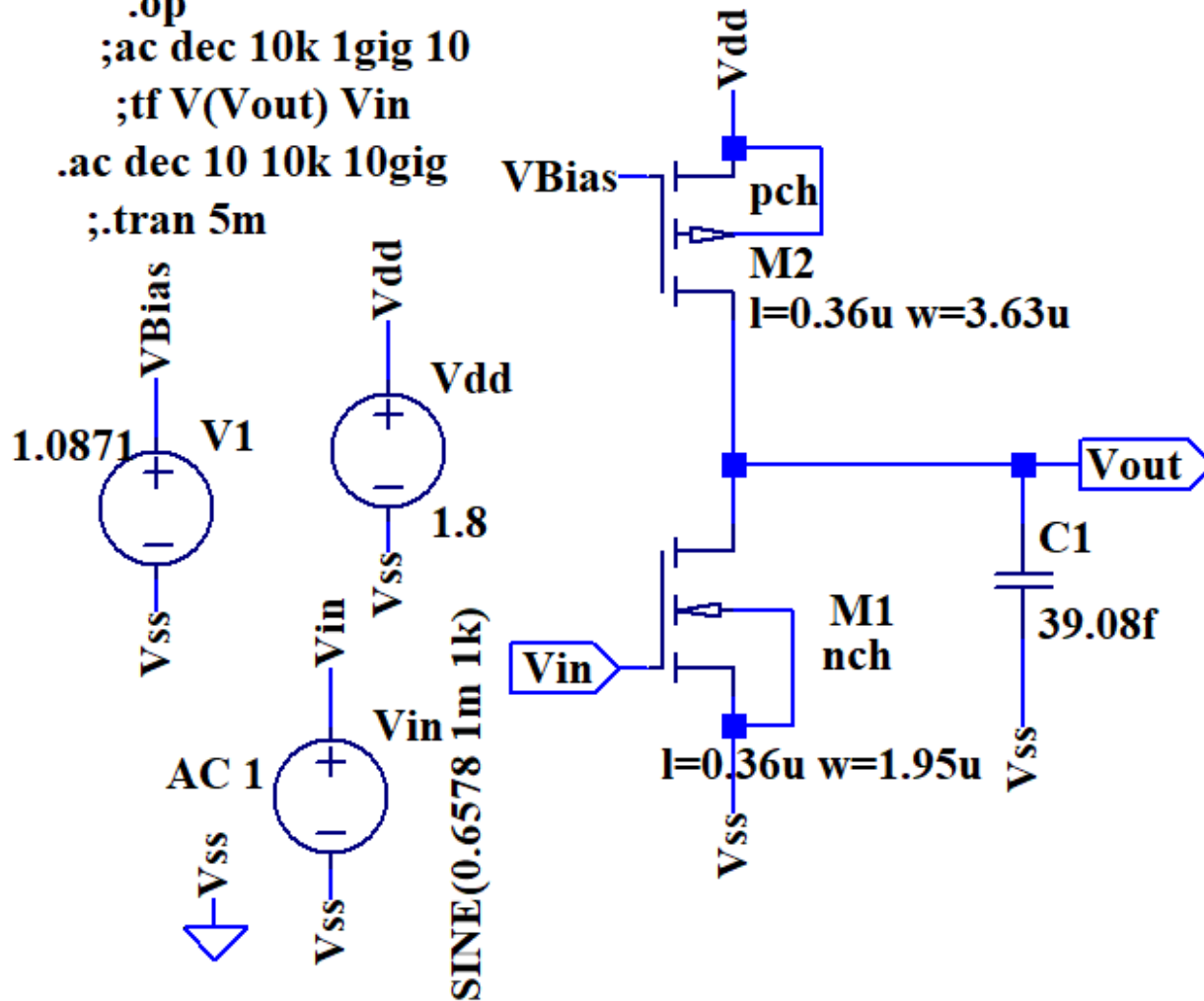
Continue....

- $R_{o2}=293.12 \text{ K } \Omega$
- $g_{ds2}=3.41 \text{ } \mu\text{S}$
- $(I_d/g_{ds})_2=7.8$
- $(g_m/i_d)_2= 7.106 \text{ from chart}$
- $(I_d/w)_2=7.312 \text{ from chart}$
- $V_{gs2}=712.9 \text{ mV}$
- $W_2= 3.63 \text{ } \mu\text{m}$



SIMULATION

```
.include C:\Users\ASUS\Desktop\CMOS180.txt
.op
;ac dec 10k 1gig 10
;tf V(Vout) Vin
.ac dec 10 10k 10gig
;.tran 5m
```



SOME CHANGES

Internal capacitance at node $V_{out} = c_{gd2} + c_{gd1}(1+A_v)$

$$C(V_{out}) = 3.36 \text{ fF}$$

$$\text{So } C_L = 42.44 \text{ f} - 3.36 \text{ f} = \mathbf{39.08 \text{ fF}}$$



RESULT AND CONCLUSION

Simulated Value	Specifications
$A_v = 40.01 \text{ v/v}$	$A_v = 40 \text{ v/v}$
$BW = 25.06 \text{ MHz}$	$BW = 25 \text{ MHz}$
$GBW = 1.002 \text{ GHz}$	$GBW = 1 \text{ GHz}$
$R_{out} = 149.327 \text{ K}\Omega$	$R_{out} = 150 \text{ K}\Omega$
$I_d = 26.73 \text{ }\mu\text{A}$	$I_d = 26.6 \text{ }\mu\text{A}$
$V_{out(dc)} = 0.773 \text{ V}$	$V_{out(dc)} = 0.9 \text{ V}$

SPICE ERROR LOG FILE

--- Transfer Function ---

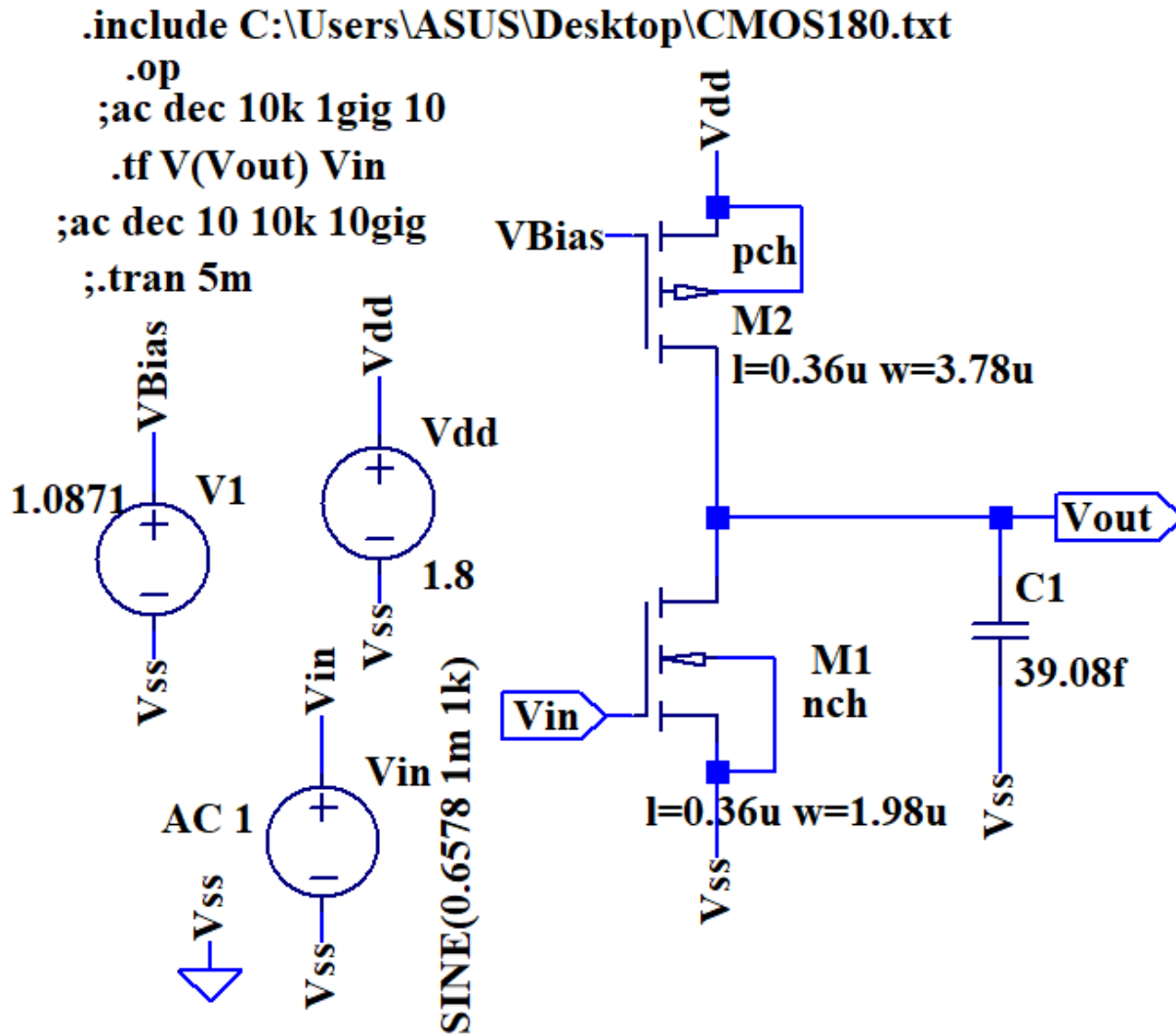
Transfer_function:	-40.0109	transfer
vin#Input_impedance:	1e+020	impedance
output_impedance_at_V(vout):	149327	impedance

Semiconductor Device Operating Points:

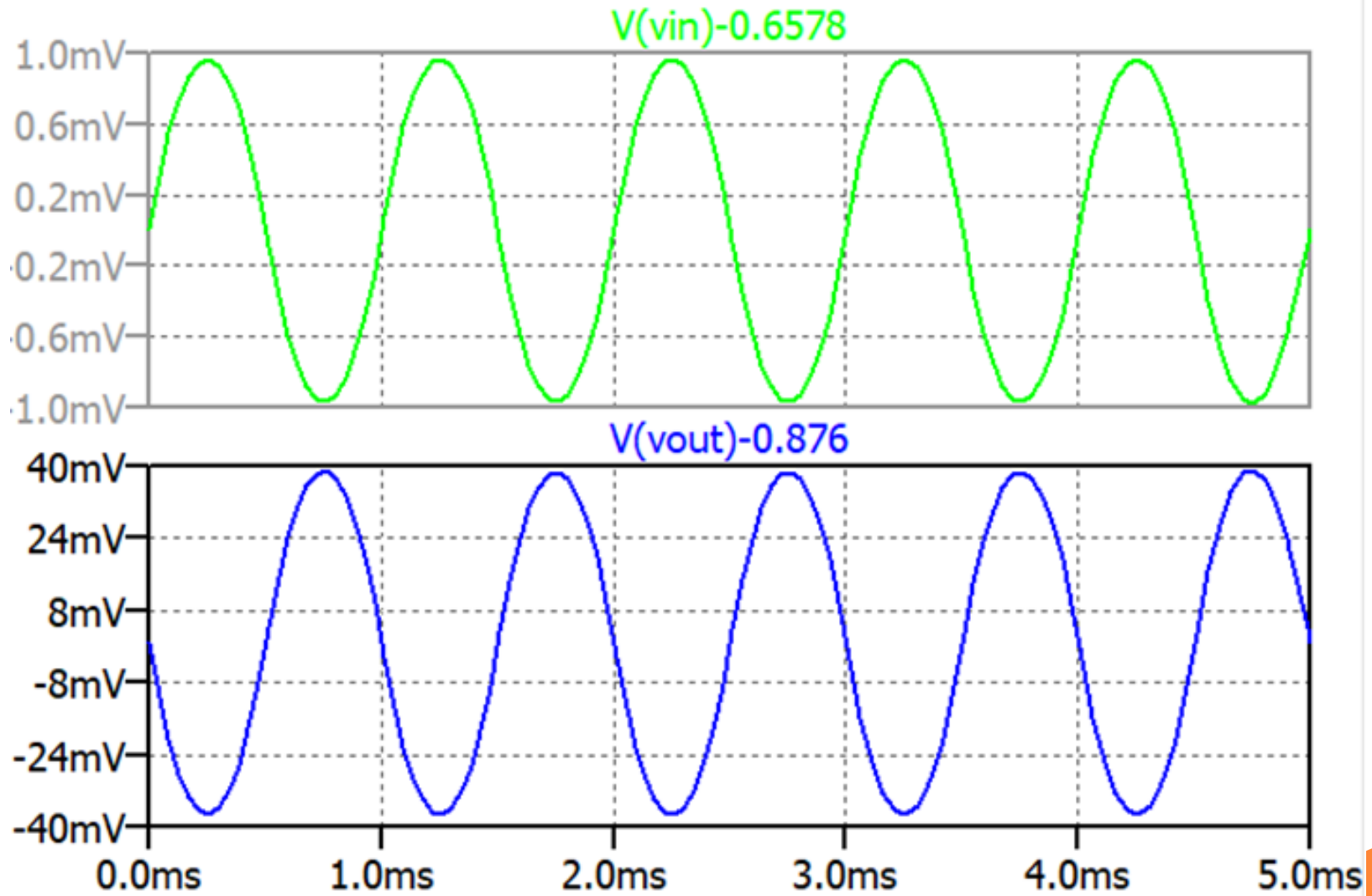
--- BSIM3 MOSFETS ---

Name:	m2	m1
Model:	pch	nch
Id:	-2.67e-05	2.67e-05
Vgs:	-7.13e-01	6.58e-01
Vds:	-1.03e+00	7.74e-01
Vbs:	0.00e+00	0.00e+00
Vth:	-4.48e-01	4.59e-01
Vdsat:	-2.19e-01	1.52e-01
Gm:	1.87e-04	2.68e-04
Gds:	3.21e-06	3.49e-06
Gmb	5.86e-05	7.00e-05
Cbd:	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00
Cgsov:	2.38e-15	9.57e-16
Cgdov:	2.38e-15	9.57e-16
Cgbov:	2.98e-19	3.28e-19
dQgdVgb:	1.24e-14	6.48e-15
dQgdVdb:	-2.38e-15	-9.32e-16
dQgdVsb:	-9.67e-15	-5.23e-15
dQddVgb:	-2.39e-15	-9.63e-16
dQddVdb:	2.39e-15	9.60e-16
dQddVsb:	4.60e-18	4.49e-18
dQbdVgb:	-1.61e-15	-9.88e-16
dQbdVdb:	-5.20e-19	1.92e-18
dQbdVsb:	-7.20e-16	-4.05e-16

UNIT DEVICES



TRANSIENT ANALYSIS

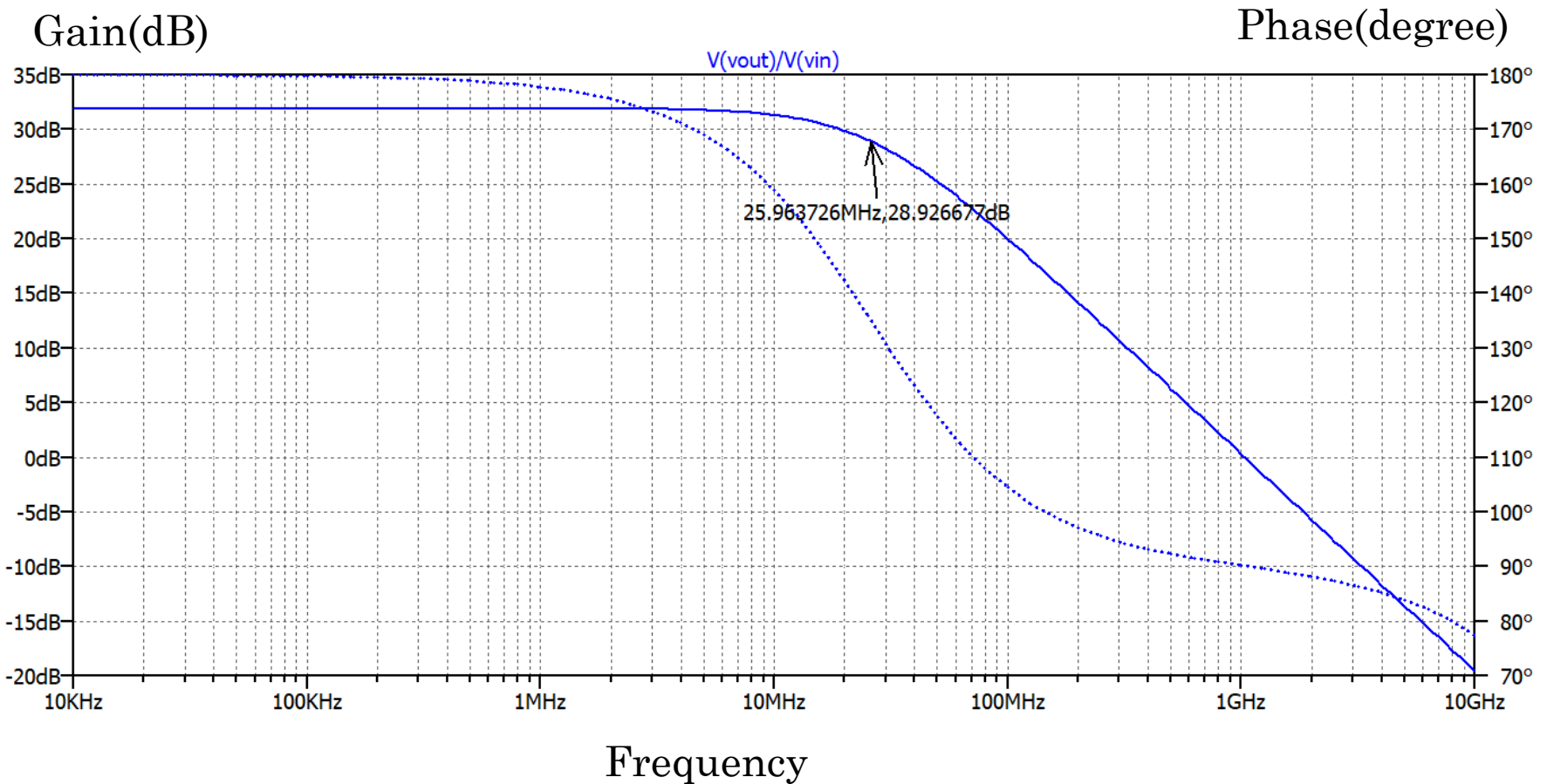


$V_{in}(p-p)=2 \text{ mV}$

$V_{out}=78.88 \text{ mV}$

Gain=39.44

FREQUENCY



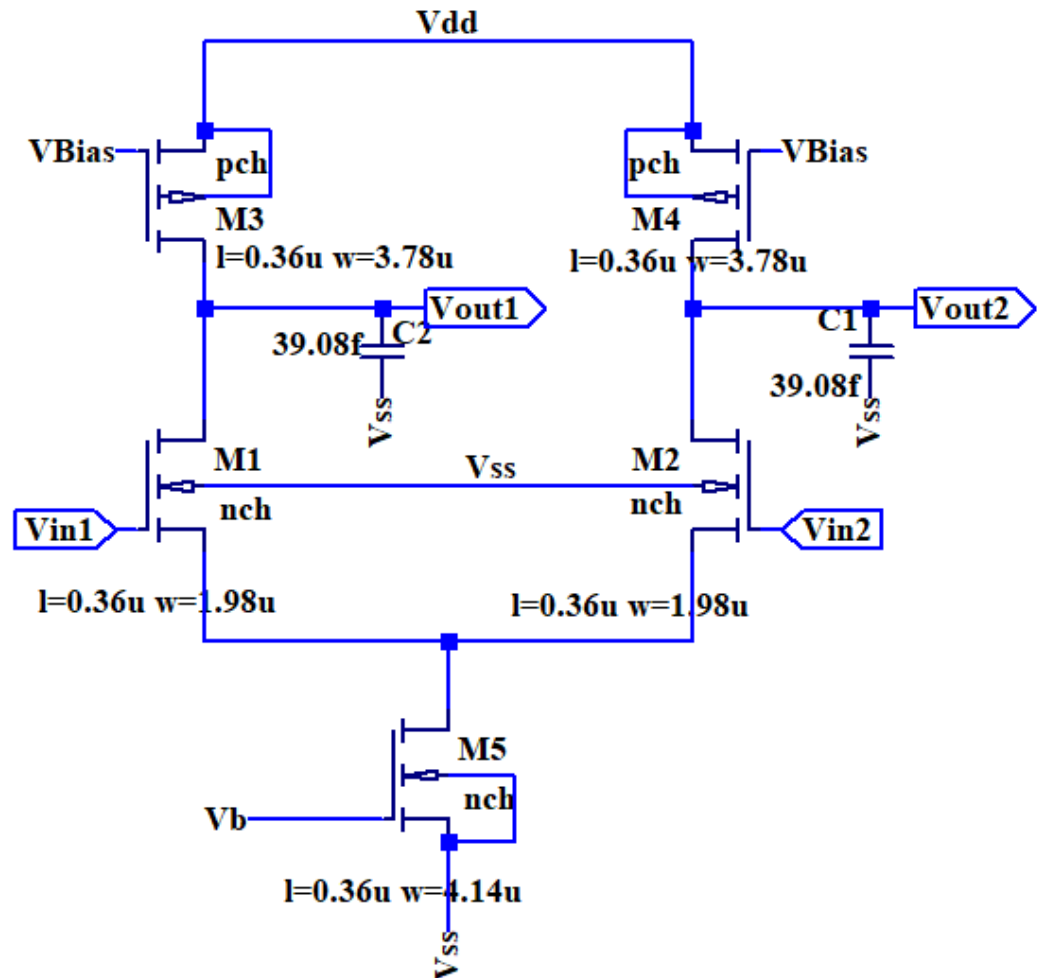
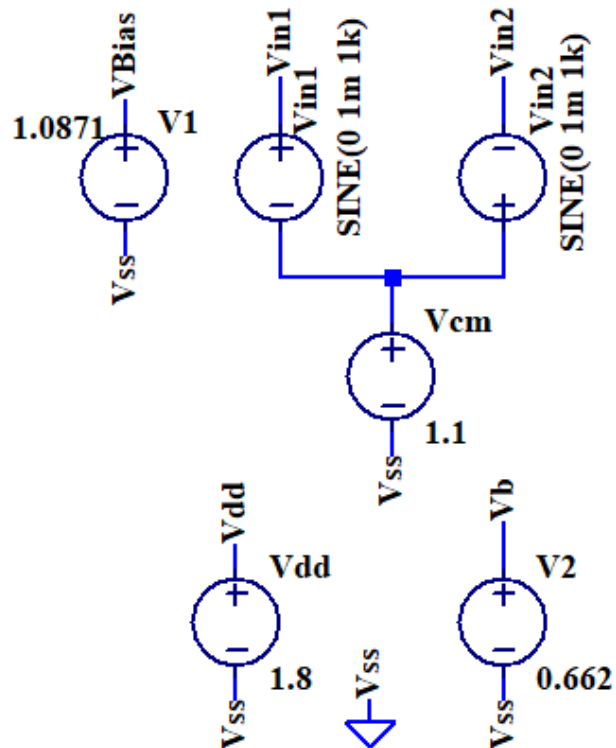
BW=25.96 MHz



DIFFERENTIAL PAIR

Using two Common Source Amplifier

```
.include C:\Users\ASUS\Desktop\CMOS180.txt
.op
;ac dec 10k 1gig 10
.tf V(Vout1,Vout2) (Vin1,Vin2)
;ac dec 10 10k 10gig
;tran 5m
```



CALCULATION FOR CURRENT SOURCE

$$I_d = 54.96 \mu A$$

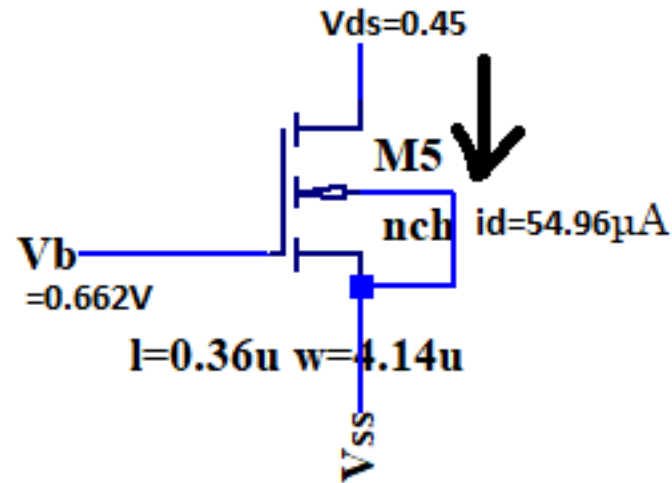
$$g_m/I_d = 10 \dots (\text{Choose})$$

$$V_{gs} = V_b = 0.662$$

$$I_d/w = 13.41$$

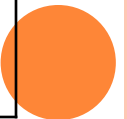
$$W_5 = 4.09 \mu m$$

$$W_5 = 4.14 \mu m \dots \text{for unit device}$$

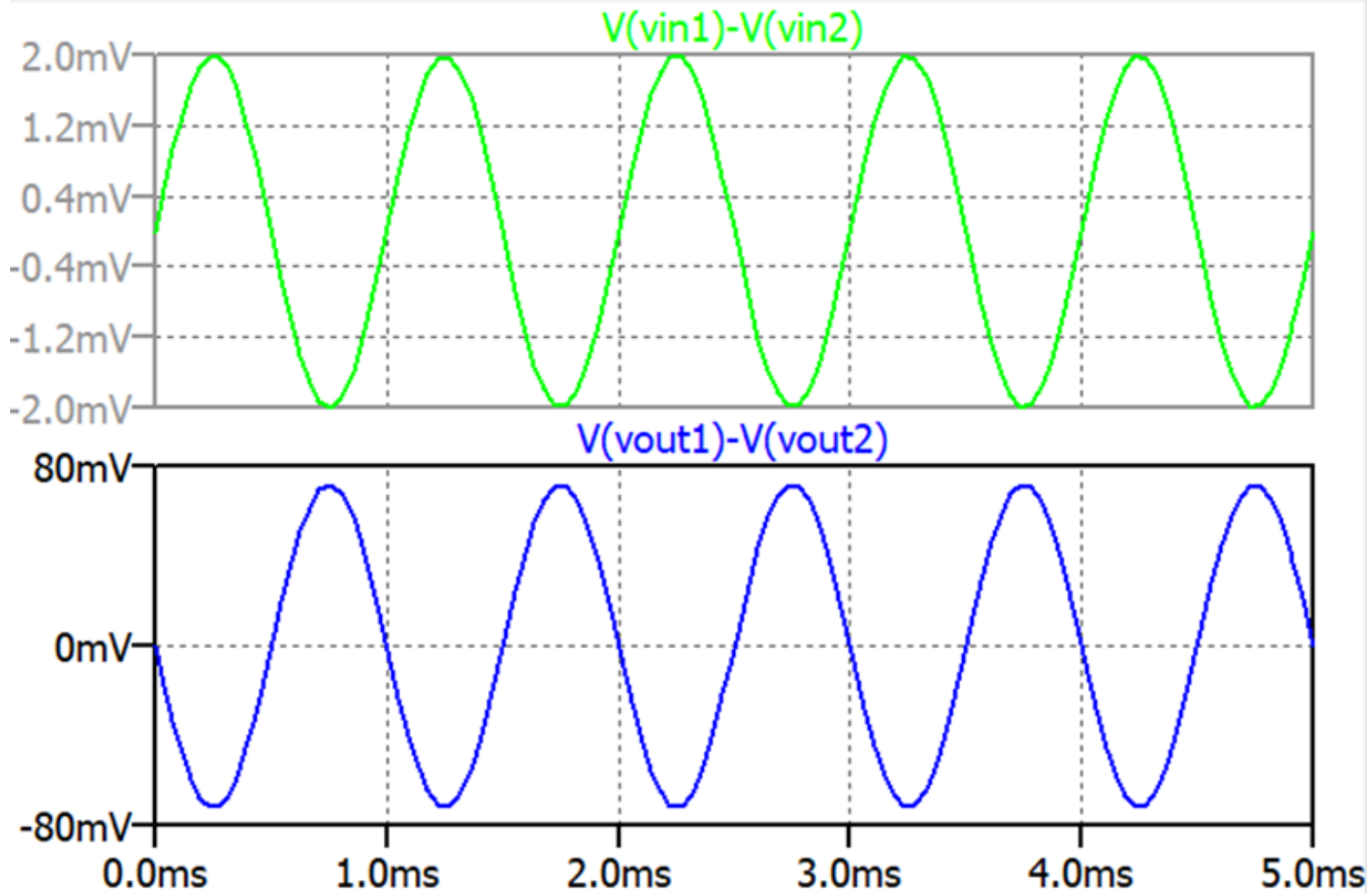


RESULT AND CONCLUSION

Simulated Value	Specifications
$A_v = 36.18 \text{ v/v}$	$A_v = 40 \text{ v/v}$
$BW = 28.66 \text{ MHz}$	$BW = 25 \text{ MHz}$
$GBW = 1.03 \text{ GHz}$	$GBW = 1 \text{ GHz}$
$R_{out} = 263.492 \text{ K}\Omega$	
$I_{ss} = 54.46 \text{ }\mu\text{A}$	$I_{ss} = 54.96 \text{ }\mu\text{A}$
$V_{out(dc)} = 0.949 \text{ V}$	$V_{out(dc)} = 0.9 \text{ V}$



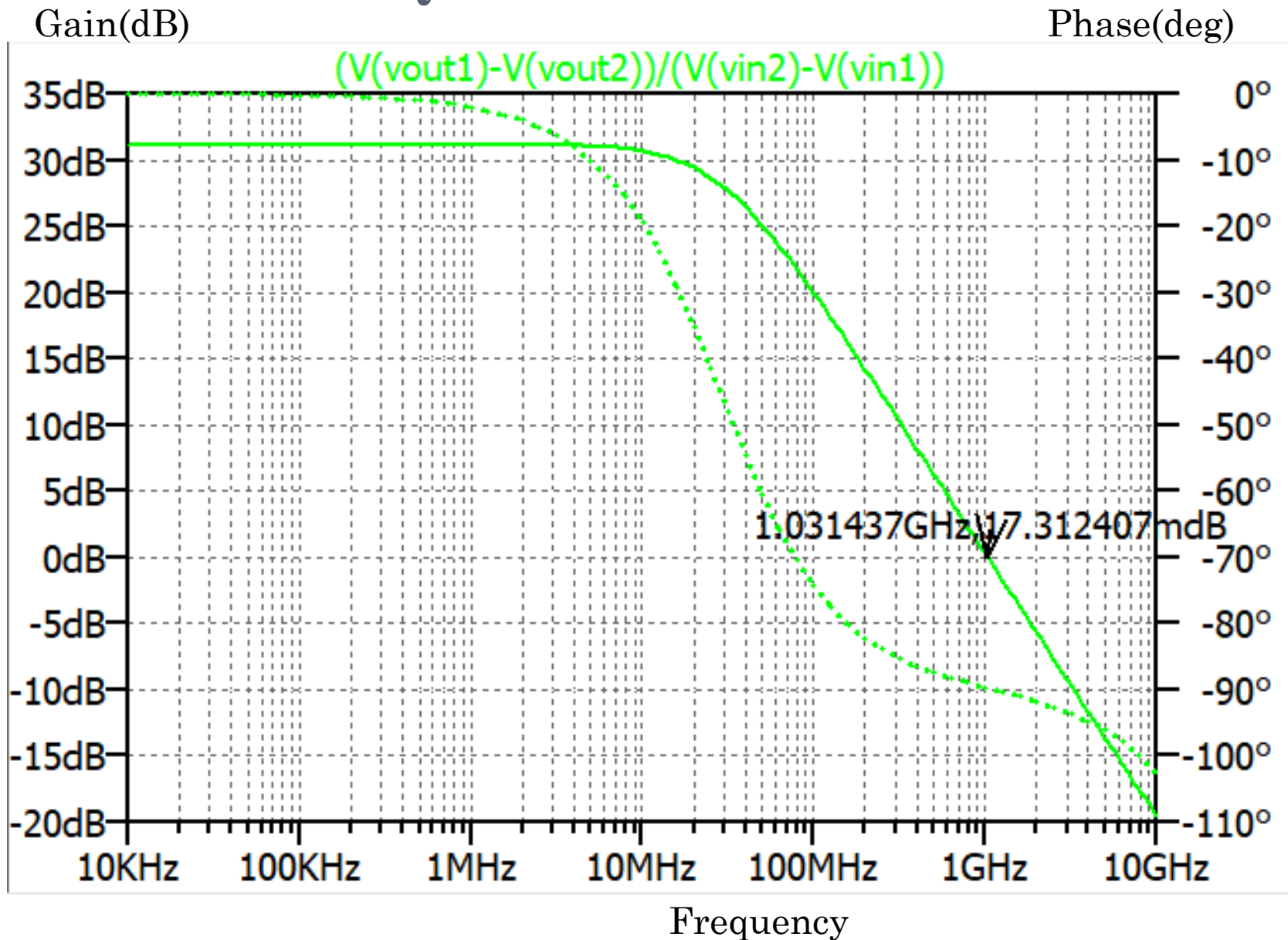
TRANSIENT ANALYSIS



$V_{\text{in1}} - V_{\text{in2}}(\text{pp}) = 4 \text{ mV}$ $V_{\text{out1}} - V_{\text{out2}}(\text{pp}) = 144.56 \text{ mV}$ Gain = 36.14



FREQUENCY RESPONSE



COMMON SOURCE AMPLIFIER

Specs:

$A_v=40$

$R_{out}=93\text{ K}\Omega$

Formula Used

$$A_v = g_m \cdot R_{out}$$

$$W = \frac{I_D}{I_D/W}$$

$$R_{out} = R_{o1} \parallel R_{o3}$$

$$g_{ds} = \frac{1}{r_o}$$

○ $g_m = 0.43\text{ mS}$

○ $g_m/I_D = 12$

○ $I_D = 35.8\text{ }\mu\text{A}$

○ $R_{o1} = 165\text{ K}\Omega$

○ $g_{ds3} = 4.69\text{ }\mu\text{S}$

○ $(I_D/g_{ds})_3 = 7.63$

○ $g_m/I_D = 6.315$

○ $W_3 = 3.91\text{ }\mu\text{m}$

$$g_m/g_{ds} = 70.92$$

$$g_{ds} = 6.06\text{ }\mu\text{S}$$

$$R_{o3} = 213.125\text{ K}\Omega$$

$$I_D/W = 9.896$$

$$W_1 = 3.61\text{ }\mu\text{m}$$

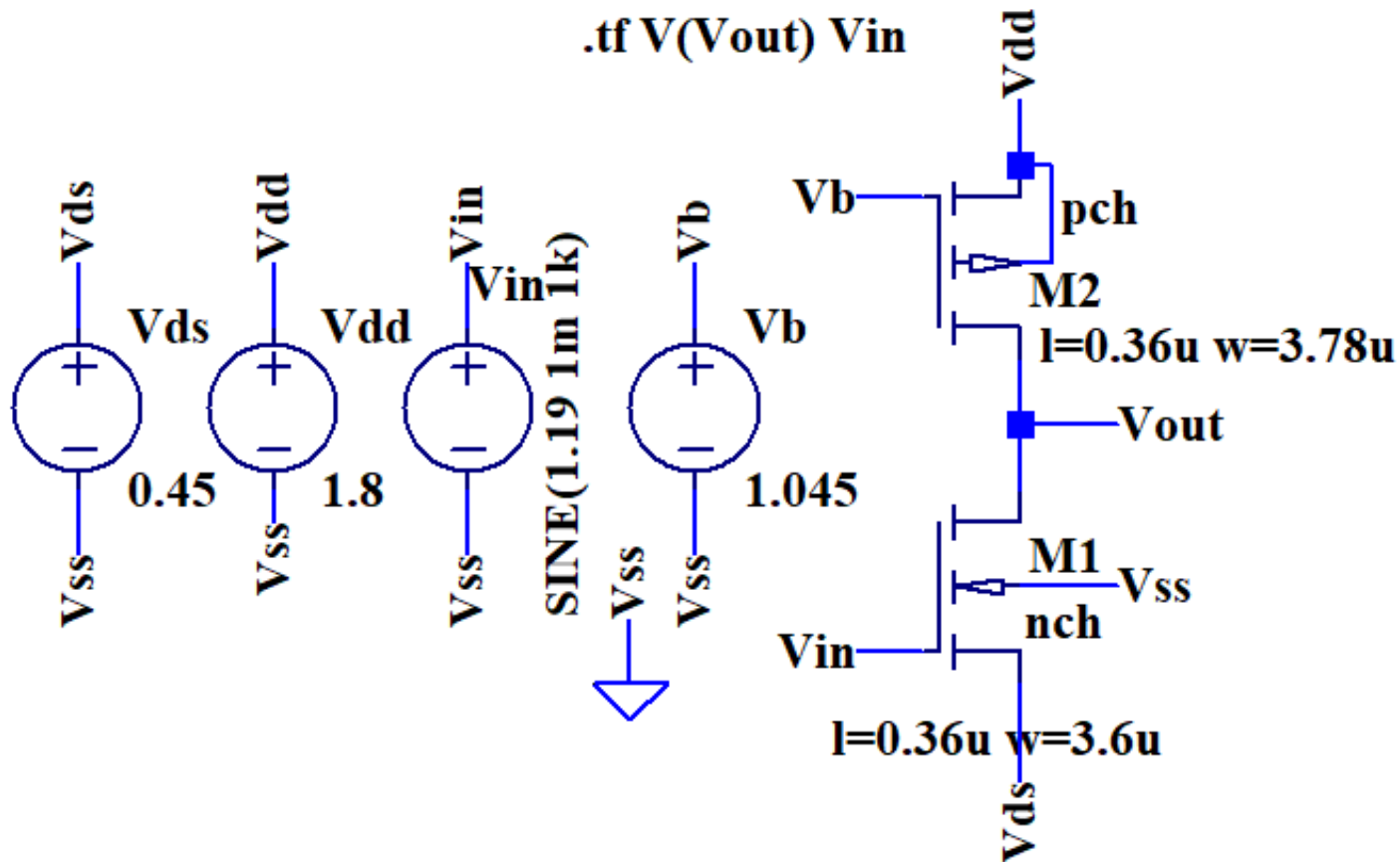
$$I_D/W = 9.133$$



SIMULATION

.include C:\Users\ASUS\Desktop\CMOS180.txt

.tf V(Vout) Vin



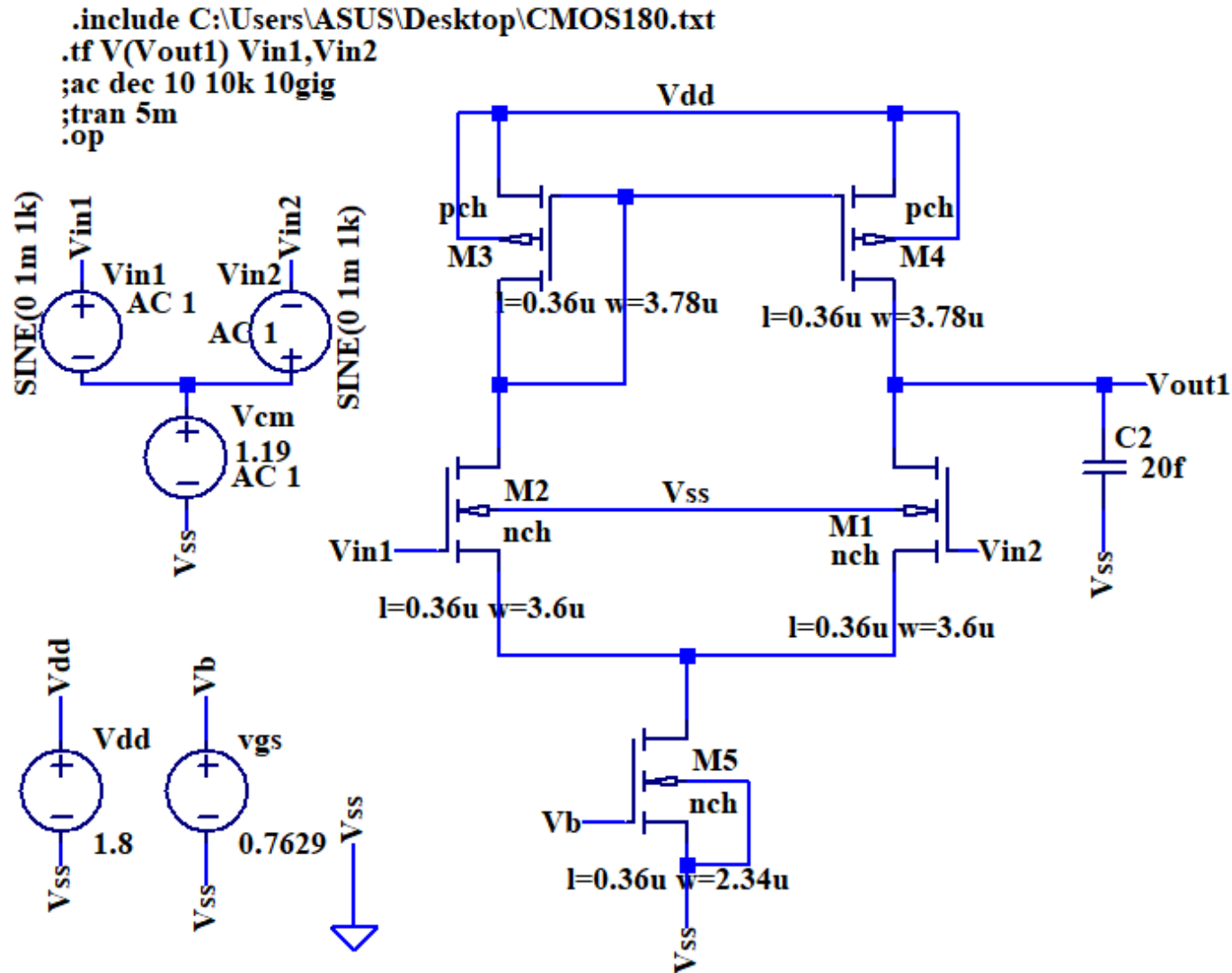
RESULTS

Simulated Value	Specifications
$A_v = 40.15 \text{ v/v}$	$A_v = 40 \text{ v/v}$
$R_{out} = 95.632 \text{ K}\Omega$	$R_{out} = 93 \text{ K}\Omega$
$I_d = 35.18 \text{ }\mu\text{A}$	$I_d = 35.8 \text{ }\mu\text{A}$
$V_{out(dc)} = 1.07 \text{ V}$	$V_{out(dc)} = 0.9 \text{ V}$




OP-AMP (STAGE-1)

Using Common Source Amplifier

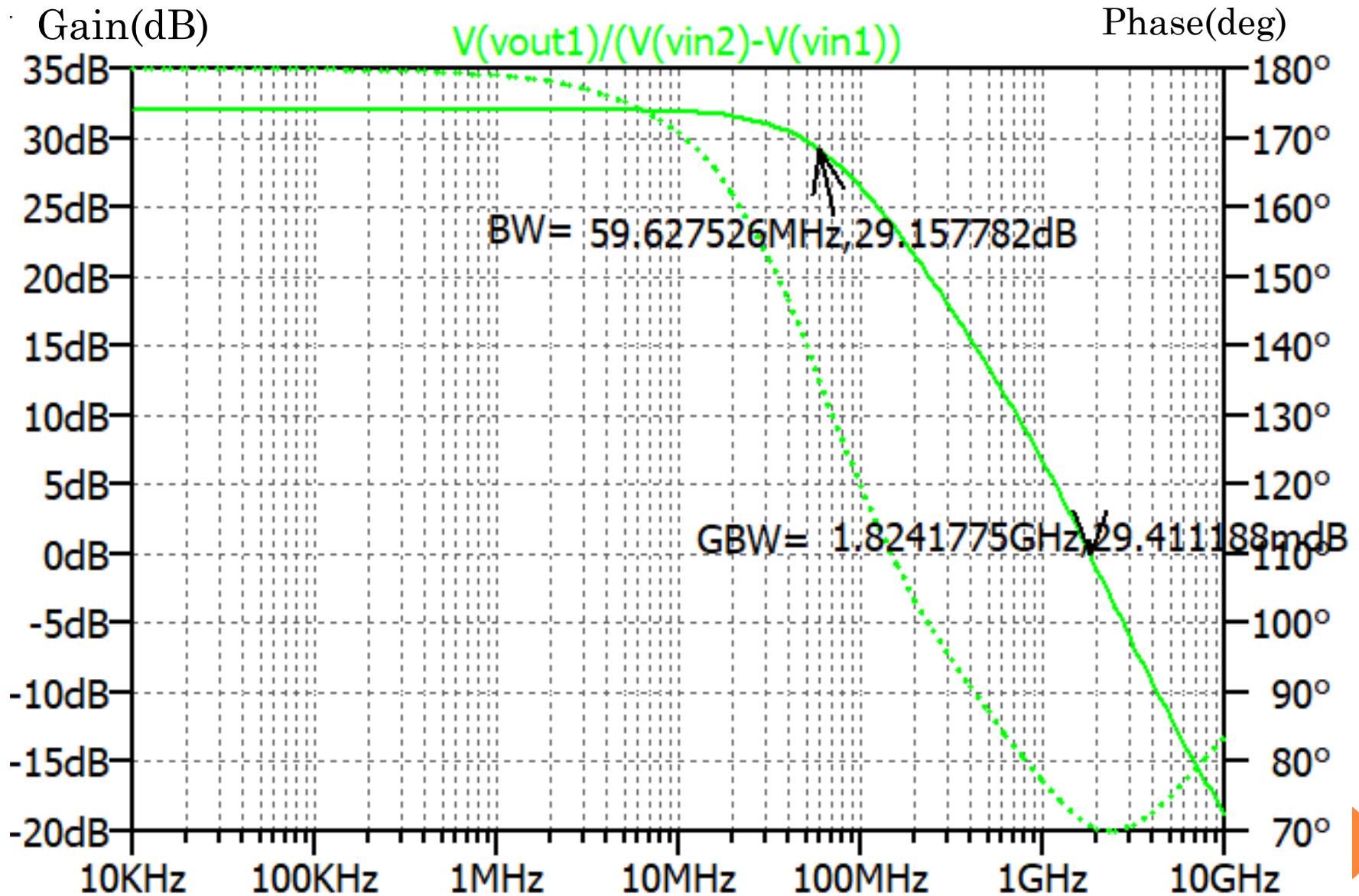


RESULT

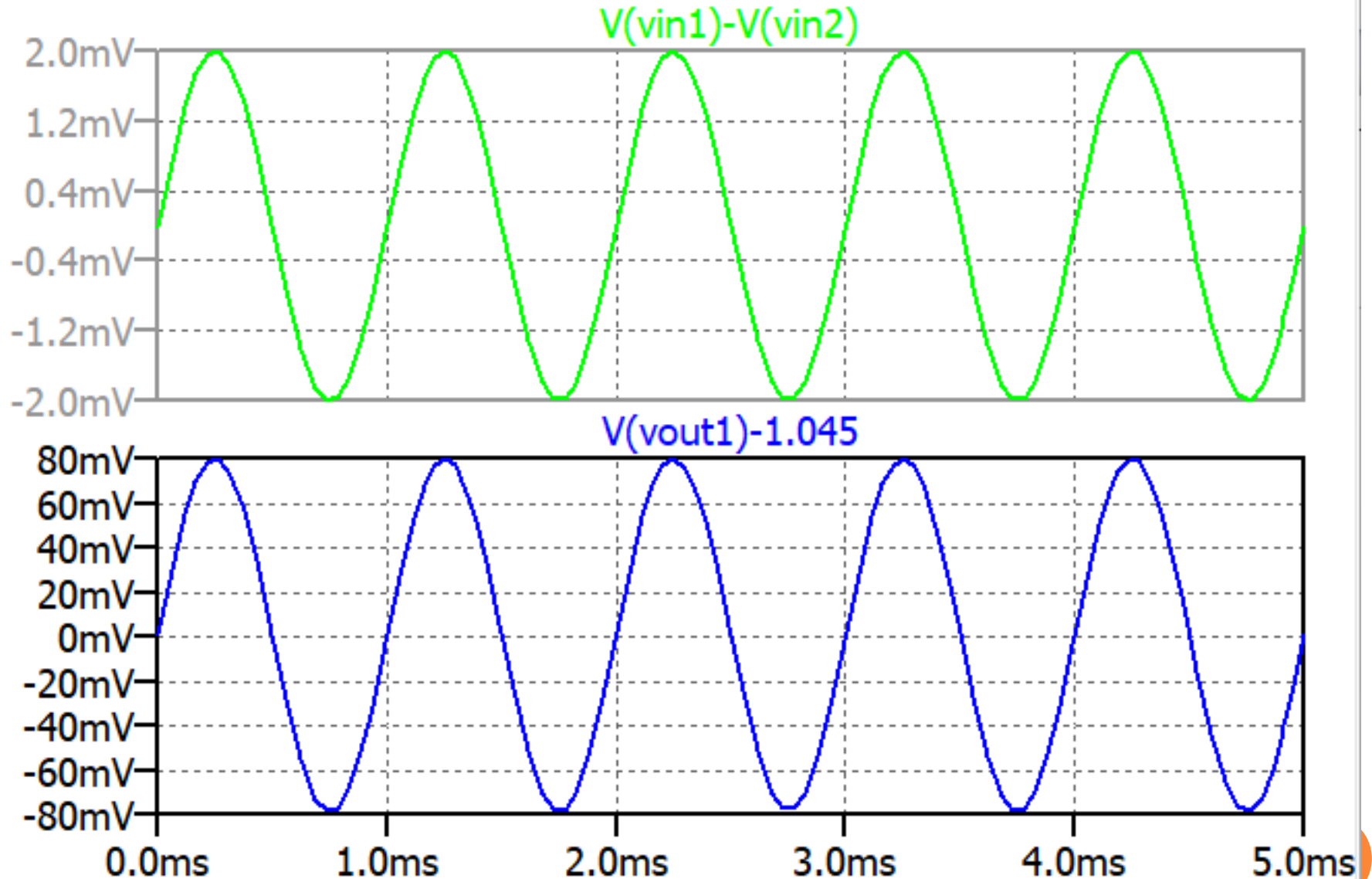
Simulated Value	Specifications
$A_v = 39.8092 \text{ v/v}$	$A_v = 40 \text{ v/v}$
$BW = 28.66 \text{ MHz}$	$BW = 25 \text{ MHz}$
$GBW = 1.03 \text{ GHz}$	$GBW = 1 \text{ GHz}$
$R_{out} = 97.259 \text{ K}\Omega$	$R_{out} = 93 \text{ K}\Omega$
$I_{ss} = 70.3 \text{ }\mu\text{A}$	$I_{ss} = 71.6 \text{ }\mu\text{A}$
$V_{out(dc)} = 1.04 \text{ V}$	$V_{out(dc)} = 1.15 \text{ V}$



FREQUENCY ANALYSIS



TRANSIENT ANALYSIS



$V_{\text{in1}}-V_{\text{in2}}(\text{pp})=4 \text{ mV}$ $V_{\text{out1}}(\text{pp})=158.68 \text{ mV}$ $\text{Gain}=39.67$

COMMON SOURCE AMPLIFIER

For Second Stage op-amp

Specs:

$$A_v = 28$$

$$g_{m2} = 8 \times 0.432 \text{ mS} = 3.384 \text{ mS}$$

$$R_{out2} = 8 \text{ K}\Omega$$

- $V_{gs1} = 780 \text{ mV}$

- $g_m/i_d = 5.466$ $i_d/w = 11.9$ from chart

- $g_m/g_{ds} = 46.96$ from chart

- $I_d = 619 \text{ }\mu\text{A}$

- $W_6 = 52 \text{ }\mu\text{m}$

- $g_{ds6} = 72.06 \text{ }\mu\text{S}$ $R_{o6} = 13.87 \text{ K}\Omega$

- $R_{o7} = 18.9 \text{ K}\Omega$ $g_{ds7} = 52.9 \text{ }\mu\text{S}$



- $(I_d/g_{ds})_7 = 11.7$
- $g_m/i_d = 6.24$ $i_d/w = 31.05$
- $W_7 = 19.9 \mu\text{m}$ **$W_7 = 15.84 \mu\text{m}$ in Simulation**
- $V_{gs7} = 0.7629 \text{ V}$



SIMULATION

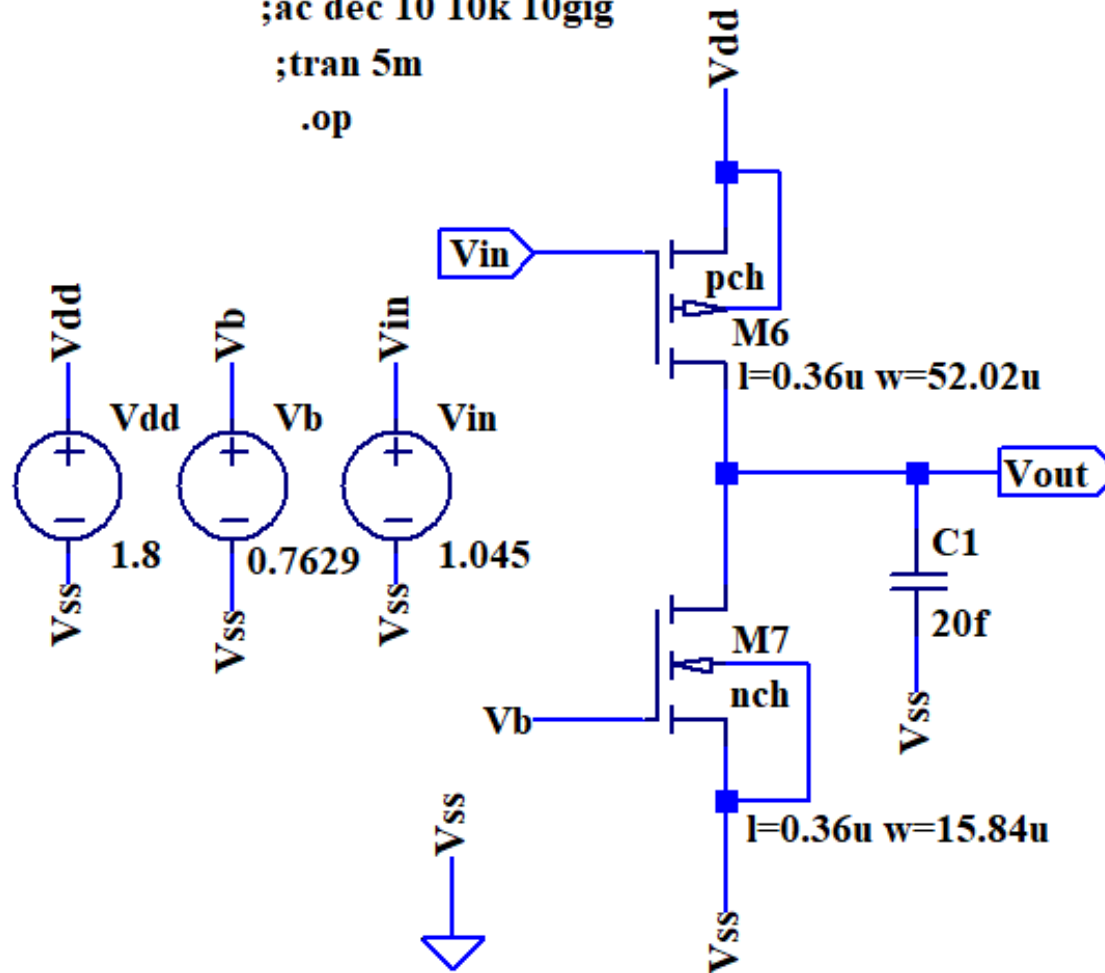
```
.include C:\Users\ASUS\Desktop\CMOS180.txt
```

```
.tf V(Vout) Vin
```

```
;ac dec 10 10k 10gig
```

```
;tran 5m
```

```
.op
```

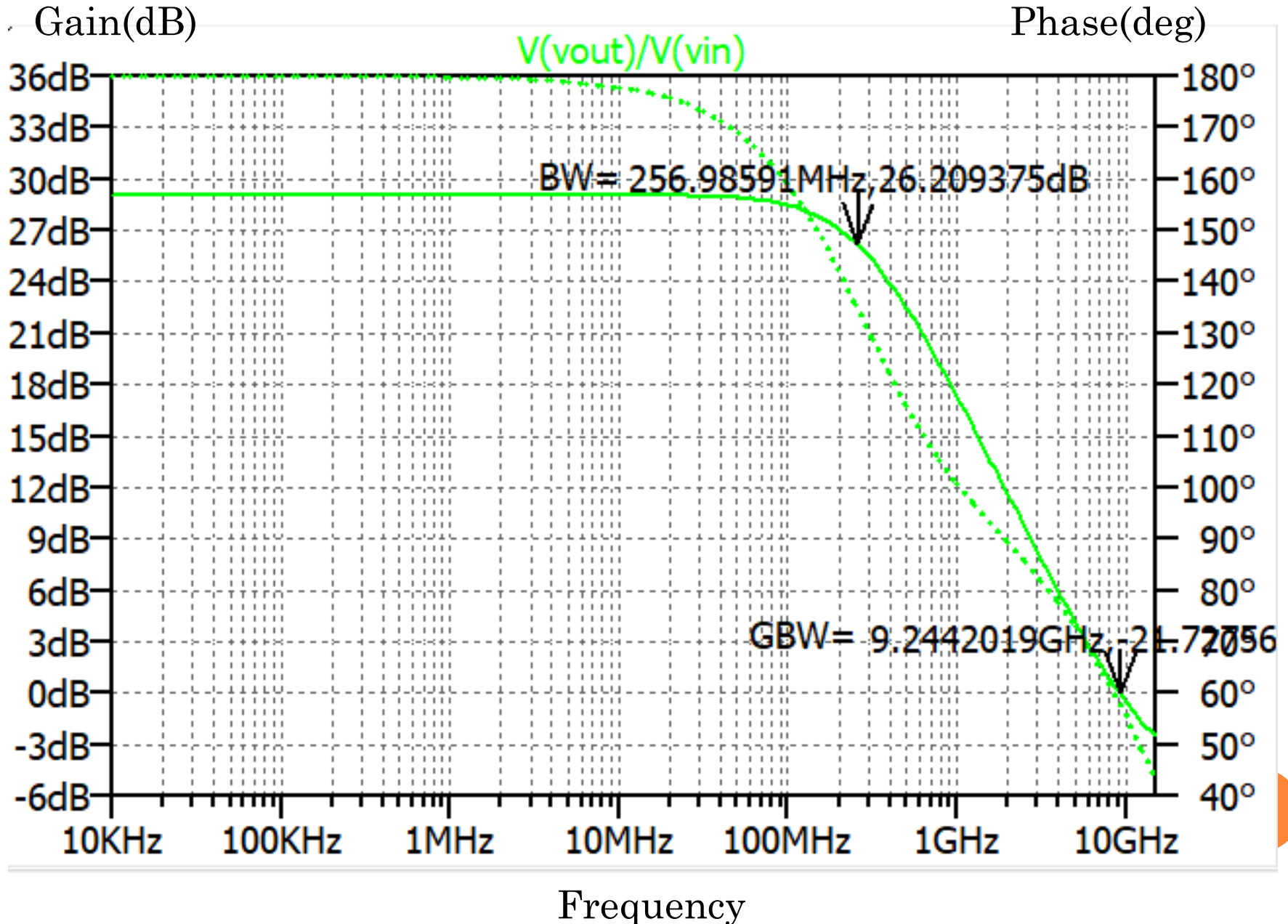


RESULT

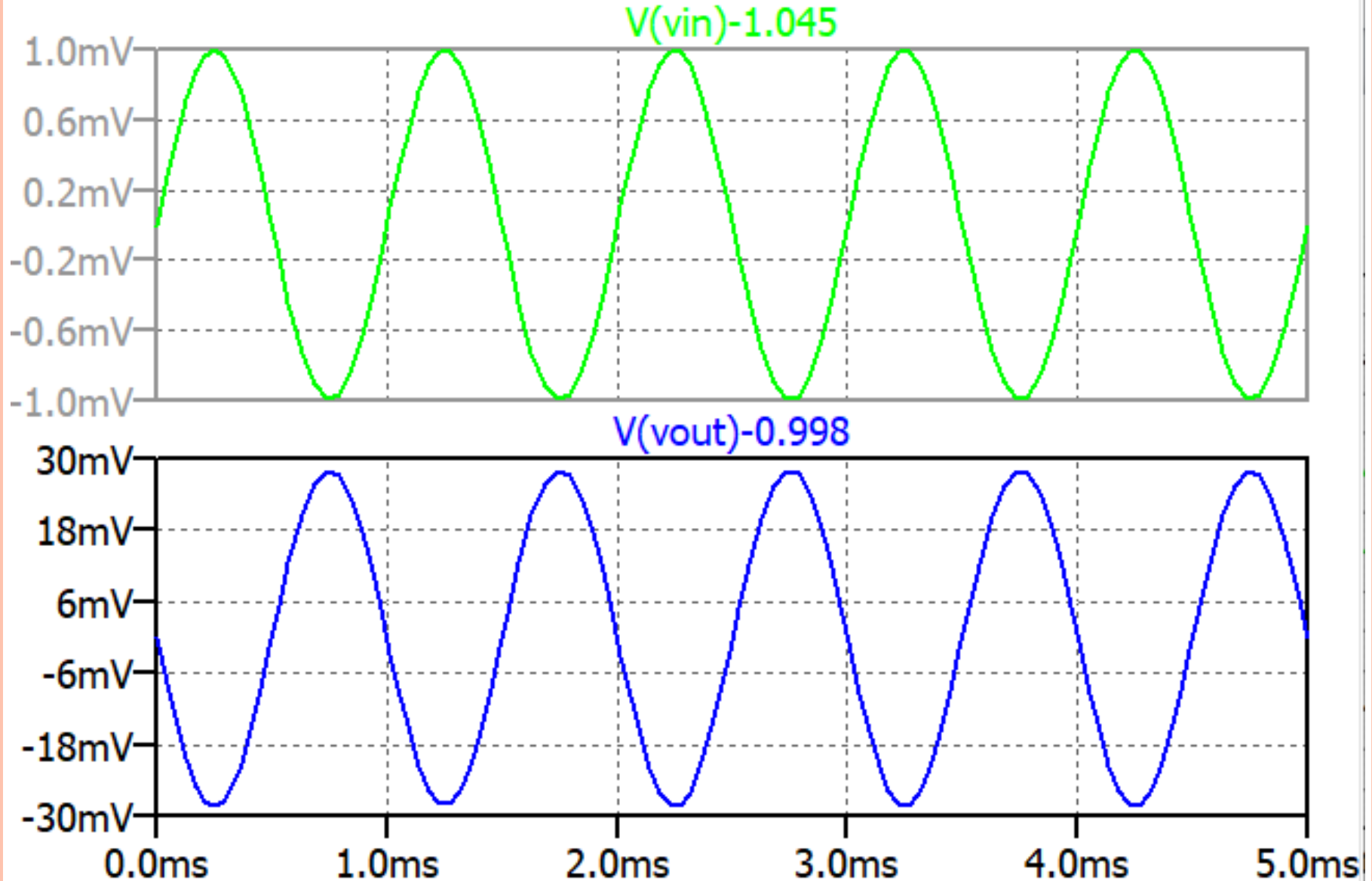
Simulated Value	Specifications
$A_v = 28.34 \text{ v/v}$	$A_v = 28 \text{ v/v}$
$BW = 256.9 \text{ MHz}$	
$GBW = 9.24 \text{ GHz}$	
$R_{out} = 9.6 \text{ K}\Omega$	$R_{out} = 8 \text{ K}\Omega$
$I_{B2} = 494 \text{ }\mu\text{A}$	$I_{B2} = 619 \text{ }\mu\text{A}$
$V_{out(dc)} = 0.998 \text{ V}$	$V_{out(dc)} = 0.9 \text{ V}$



FREQUENCY RESPONSE



TRANSIENT ANALYSIS



$V_{in(pp)}=2 \text{ mV}$ $V_{out(pp)}=56.63 \text{ mV}$ Gain=28.315

PROJECT: DESIGNING OF TWO STAGE OPERATIONAL AMPLIFIER

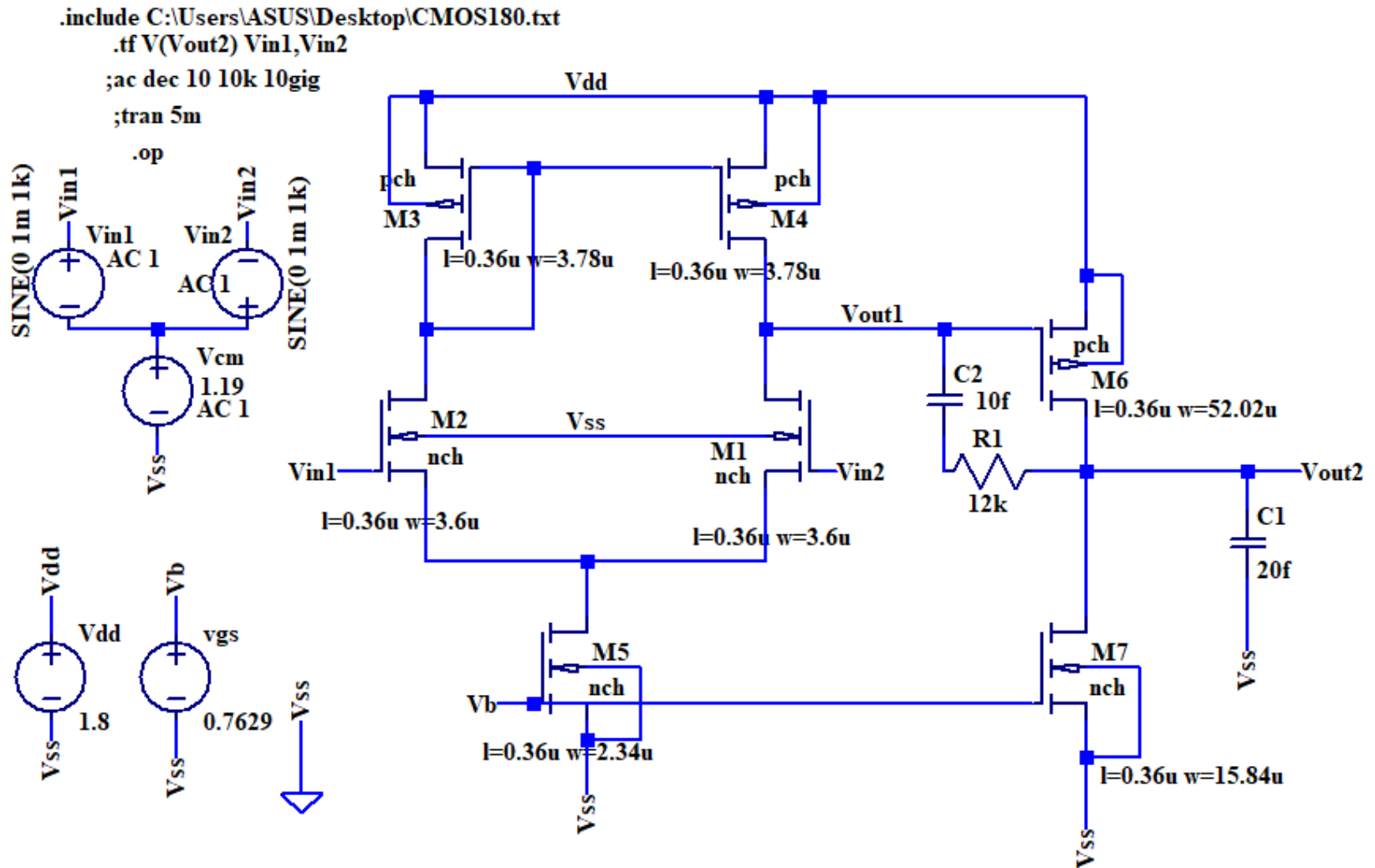
Specification

Gain(A_v)	≥ 1000 (60dB)
GBW	1GHz
Phase Margin	≥ 50
Load Capacitance	20 fF

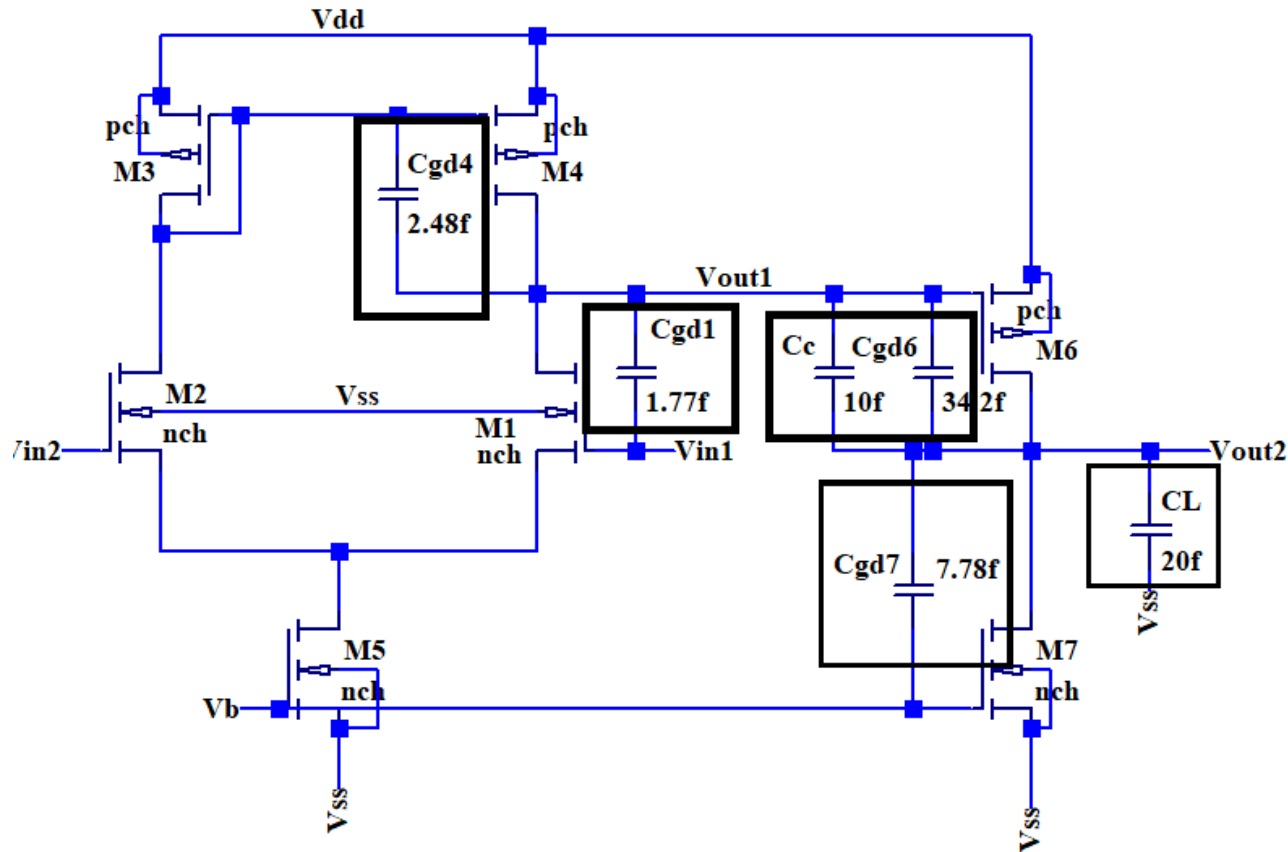


PROJECT: TWO STAGE OP-AMP

Combining Stage-1 and Stage-2



CAPACITOR



$C1 = \text{Capacitance at Node}(V_{out1}) = C_{gd4} + C_{gd1} + \{ (C_{gd6} + C_c) * (1 + A_{v2}) \}$

$C1 = 1.3 \text{ pF}$

$C2 = \text{Capacitance at Node}(V_{out2}) = C_L + C_{gd7} + \{ (C_{gd6} + C_c) * (1 + \frac{1}{A_{v2}}) \}$

$C2 = 73.52 \text{ fF}$



POLE AND ZERO

- Dominant Pole

- $F_{p1} = \frac{1}{2\pi \cdot R_{out1} \cdot C1}$

- $F_{p1} = 1.2 \text{ MHz}$ where $R_{out1} = 97.25 \text{ K}\Omega$

- $F_{p2} = \text{Beyond } 1\text{GHz}$

- $S_z = \frac{1}{C_c \left(\frac{1}{G_{m6}} - R_z \right)}$

- $F_z = -1.36\text{GHz}$ where $R_z = 12\text{k}$, $G_{m2} = 2.95\text{mS}$



FREQUENCY COMPENSATION

- $C_c = 10 \text{ fF}$ (generally $C_c = (0.3 - 0.5) * C_L$)
- $R_z = 12 \text{ K}\Omega$ (generally $R_z = 1 / G_{m2}$)
- But we have taken $12 \text{ K}\Omega$ for achieving Phase Margin of 45° .



RESULT

Simulated Value	Specifications
$A_v = 1139 \text{ v/v}$	$A_v \geq 1000 \text{ v/v}$
$BW = 1.12 \text{ MHz}$	$BW = 1 \text{ MHz}$
$GBW = 1.02 \text{ GHz}$	$GBW = 1 \text{ GHz}$
$R_{out} = 9.68 \text{ K}\Omega$	$R_{out} = 8 \text{ K}\Omega$
$V_{out(dc)} = 0.97 \text{ V}$	$V_{out(dc)} = 0.9 \text{ V}$
$I_{B1} = 70.3 \text{ }\mu\text{A}$, $I_{B2} = 493.24 \text{ }\mu\text{A}$ Total Current = $563.54 \text{ }\mu\text{A}$ $V_{dd} = 1.8$ Power Dissipation = 1.01 mW	- - - -
Phase Margin = 45°	Phase Margin = 50°
Gain Margin = 16.5 dB	-
$C_L = 20 \text{ fF}$	$C_L = 20 \text{ fF}$

TABLE

Stage 1	Stage 2
$L=0.36\mu\text{m}$	$L=0.36\mu\text{m}$
$W_{1,2} = 3.6\mu\text{m}$ $\frac{W}{L} = 10$	$W_6=52.02\mu\text{m}$ $\frac{W}{L} = 144.5$
$gm_{1,2} = 0.419 \text{ mS}$	$gm_6 = 2.59 \text{ mS}$
$W_{3,4} = 3.78\mu\text{m}$ $\frac{W}{L} = 10.5$	$W_7= 15.84 \mu\text{m}$ $\frac{W}{L} = 44$
$gm_{3,4} = 0.21 \text{ mS}$	$gm_7 = 3.05 \text{ mS}$



SPICE ERROR LOG FILE

Semiconductor Device Operating Points:

--- BSIM3 MOSFETS ---

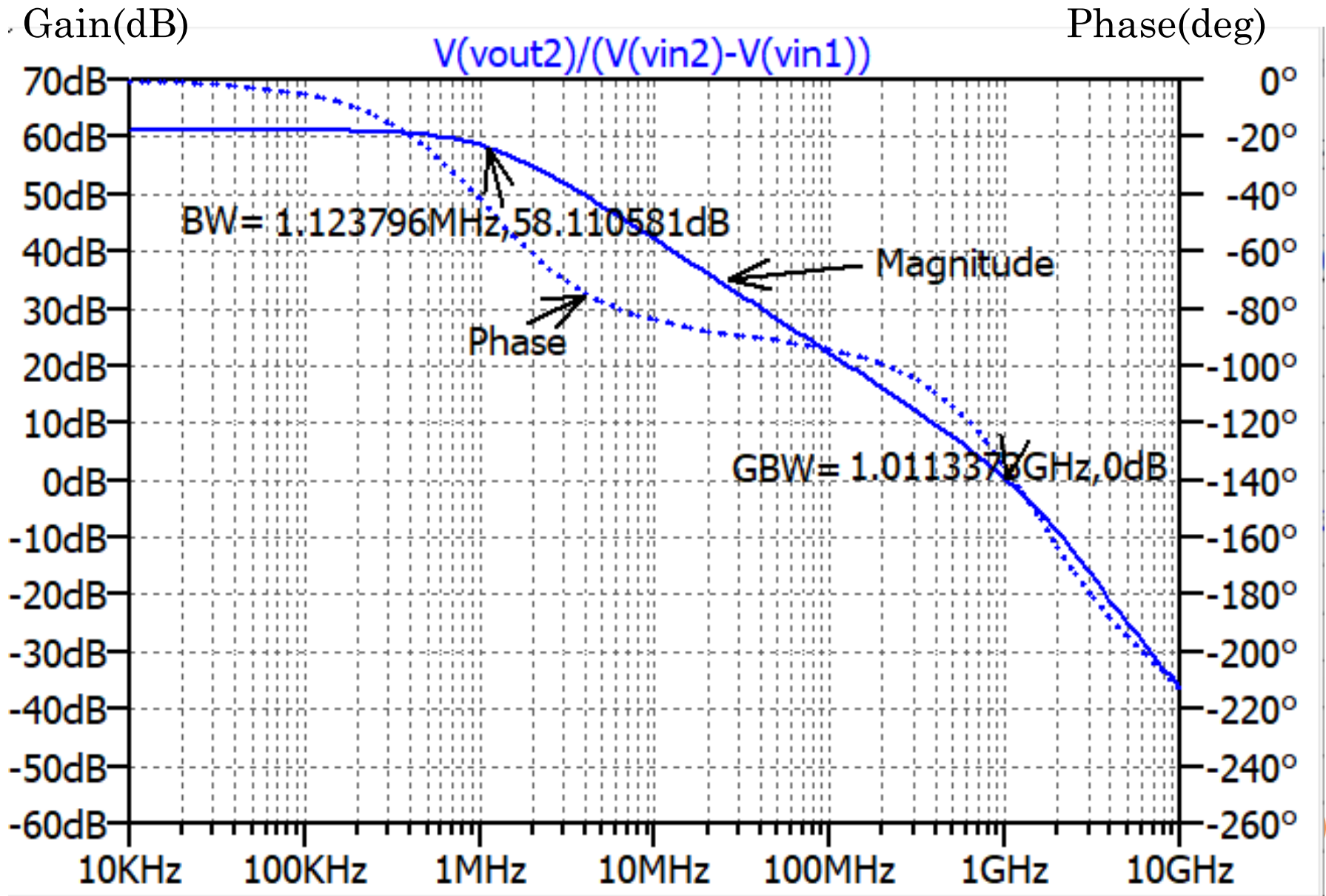
Name:	m6	m3	m4	m7	m5	m2	m1
Model:	pch	pch	pch	nch	nch	nch	nch
Id:	-4.93e-04	-3.52e-05	-3.52e-05	4.93e-04	7.03e-05	3.52e-05	3.52e-05
Vgs:	-7.54e-01	-7.54e-01	-7.54e-01	7.63e-01	7.63e-01	7.40e-01	7.40e-01
Vds:	-8.26e-01	-7.54e-01	-7.54e-01	9.74e-01	4.50e-01	5.96e-01	5.96e-01
Vbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	-4.50e-01	-4.50e-01
Vth:	-4.50e-01	-4.48e-01	-4.48e-01	4.58e-01	4.62e-01	5.82e-01	5.82e-01
Vdsat:	-2.55e-01	-2.50e-01	-2.50e-01	2.19e-01	2.15e-01	1.38e-01	1.38e-01
Gm:	2.95e-03	2.11e-04	2.11e-04	3.05e-03	4.40e-04	4.19e-04	4.19e-04
Gds:	6.24e-05	4.69e-06	4.69e-06	4.09e-05	1.09e-05	5.73e-06	5.73e-06
Gmb:	9.53e-04	6.66e-05	6.66e-05	7.91e-04	1.13e-04	9.52e-05	9.52e-05
Cbd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgsov:	3.42e-14	2.48e-15	2.48e-15	7.78e-15	1.15e-15	1.77e-15	1.77e-15
Cgdov:	3.42e-14	2.48e-15	2.48e-15	7.78e-15	1.15e-15	1.77e-15	1.77e-15
Cgbov:	2.98e-19	2.98e-19	2.98e-19	3.28e-19	3.28e-19	3.28e-19	3.28e-19
dQgdVgb:	1.78e-13	1.30e-14	1.30e-14	5.26e-14	7.80e-15	1.18e-14	1.18e-14
dQgdVdb:	-3.42e-14	-2.48e-15	-2.48e-15	-7.58e-15	-1.13e-15	-1.72e-15	-1.72e-15
dQgdVsb:	-1.38e-13	-1.01e-14	-1.01e-14	-4.27e-14	-6.32e-15	-9.53e-15	-9.53e-15
dQddVgb:	-3.43e-14	-2.50e-15	-2.50e-15	-7.81e-15	-1.19e-15	-1.78e-15	-1.78e-15
dQddVdb:	3.43e-14	2.49e-15	2.49e-15	7.79e-15	1.18e-15	1.78e-15	1.78e-15
dQddVsb:	1.04e-16	8.68e-18	8.68e-18	2.36e-17	1.14e-17	1.33e-17	1.33e-17
dQbdVgb:	-2.25e-14	-1.67e-15	-1.67e-15	-7.92e-15	-1.17e-15	-1.67e-15	-1.67e-15
dQbdVdb:	-2.52e-17	-2.70e-18	-2.70e-18	1.63e-17	-9.51e-18	7.38e-19	7.38e-19
dQbdVsb:	-1.10e-14	-7.45e-16	-7.45e-16	-3.25e-15	-4.67e-16	-4.71e-16	-4.71e-16

--- Transfer Function ---

Transfer_function:	-1139.14	transfer	
vin1#Input_impedance:	1e+020	impedance	
output_impedance_at_V(vout2):		9688.45	impedance

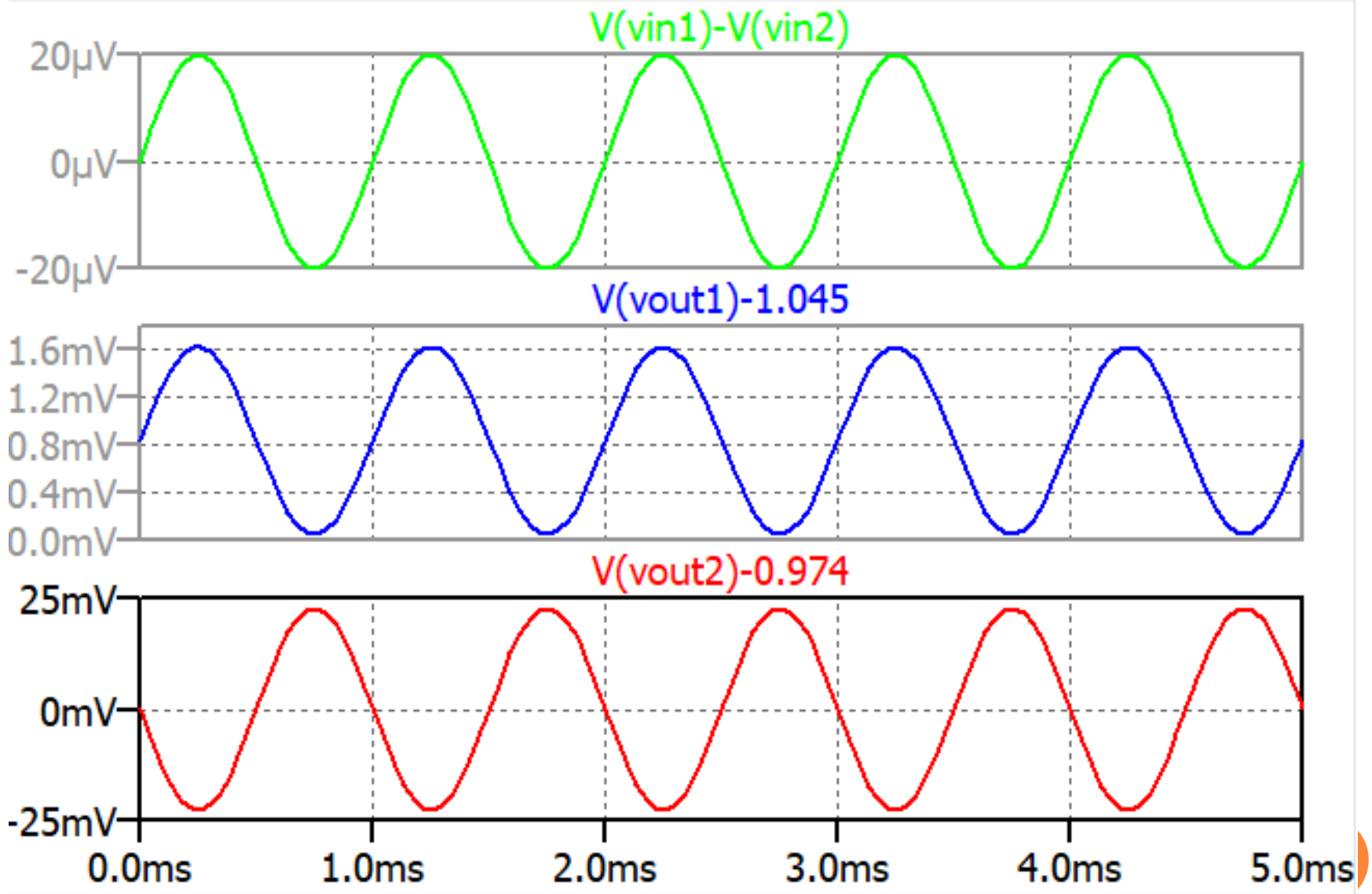


FREQUENCY RESPONSE



Frequency

TRANSIENT ANALYSIS



$V_{\text{in1}}-V_{\text{in2}}(\text{pp})=40\mu\text{V}$ $V_{\text{out2}}(\text{pp})=45.54\text{mV}$ $\text{Gain}=1138.5$

LEARN IN THIS INTERNSHIP

- Learn gmid methodology for designing Amplifier.
- How to Extract different charts used in gmid method
- Designed using ADT Toolbox
- Able to Design Amplifier with given Specification
- Completed project: Design of two Stage op-amp with gain bandwidth product of 1Ghz.



REFERENCES

- IEEE.ORG
- The Design of Two-Stage Miller Op-Amp: The Final Verdict! | Dr. Hesham Omran, Youtube Link: https://youtu.be/PT31xAEd_v4



Special Thanks to:

- Prof Syed Atiqur Rahman Sir
- Prof Mohammad Jawaid Siddiqui Sir
 - Dr Saif Abrar Sir
 - Mudassir Sir
 - Shamsul Haque Sir
 - Mohd Kashif Sir
 - Ayush Sharma
 - Afzal Malik
 - Mohsin Hussain
- &
- My Parents



Thank you

