Week-5 Presentation
Analog Design Internship

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Session Outline

- Previous Preview
- ADT Toolbox
- Source Follower Amplifier design
- Common Source Amplifier design
- Differential Pair design
- Operational Amplifier design
- Project: Two stage op-amp design

WEEK-1

- Extract Charts for NMOS & PMOS
- gm/gds vs gm/id
- Vgs vs gm/id
- Id/w vs gm/id

- Design Common Source and Source Follower Amplifier from charts.
- Observe large (W/L) ratios.

Week-2

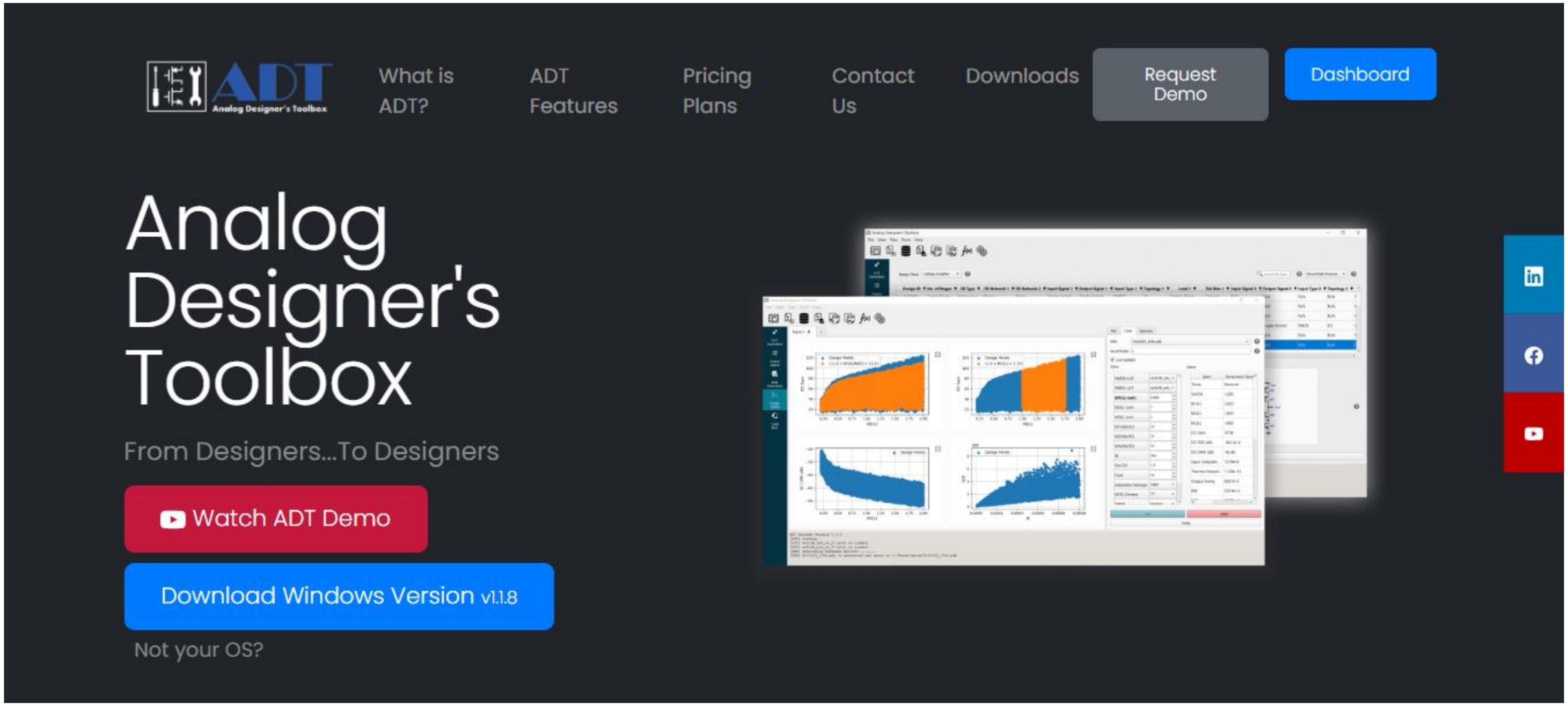
- Design Current Mirror
- Design Delay Cell
- Design Common Source amplifier, Differential Pair and op-amp with Small (W/L) ratios.

Week-3

- Design Cascode CS amplifier & op-amp.

ADT TOOLBOX

- Official link: https://at.master-micro.com



DESIGN BY USING ADT TOOLBOX

- The Analog Designer's Toolbox (ADT): Towards a new paradigm for analog IC design.
- ADT provides a turnkey solution that enables everyone to reap the benefits of the GM/ID design methodology powered by pre-computed lookup tables (LUTs).
- At the device level, ADT Device Xplore gives an easy interface to plot arbitrary design charts involving complex expressions.
- The designer can explore devices from different technologies at different corners and temperatures, and extract simulator-accurate design points while taking second-order effects into consideration.

Source: ieee.org

Continue…..

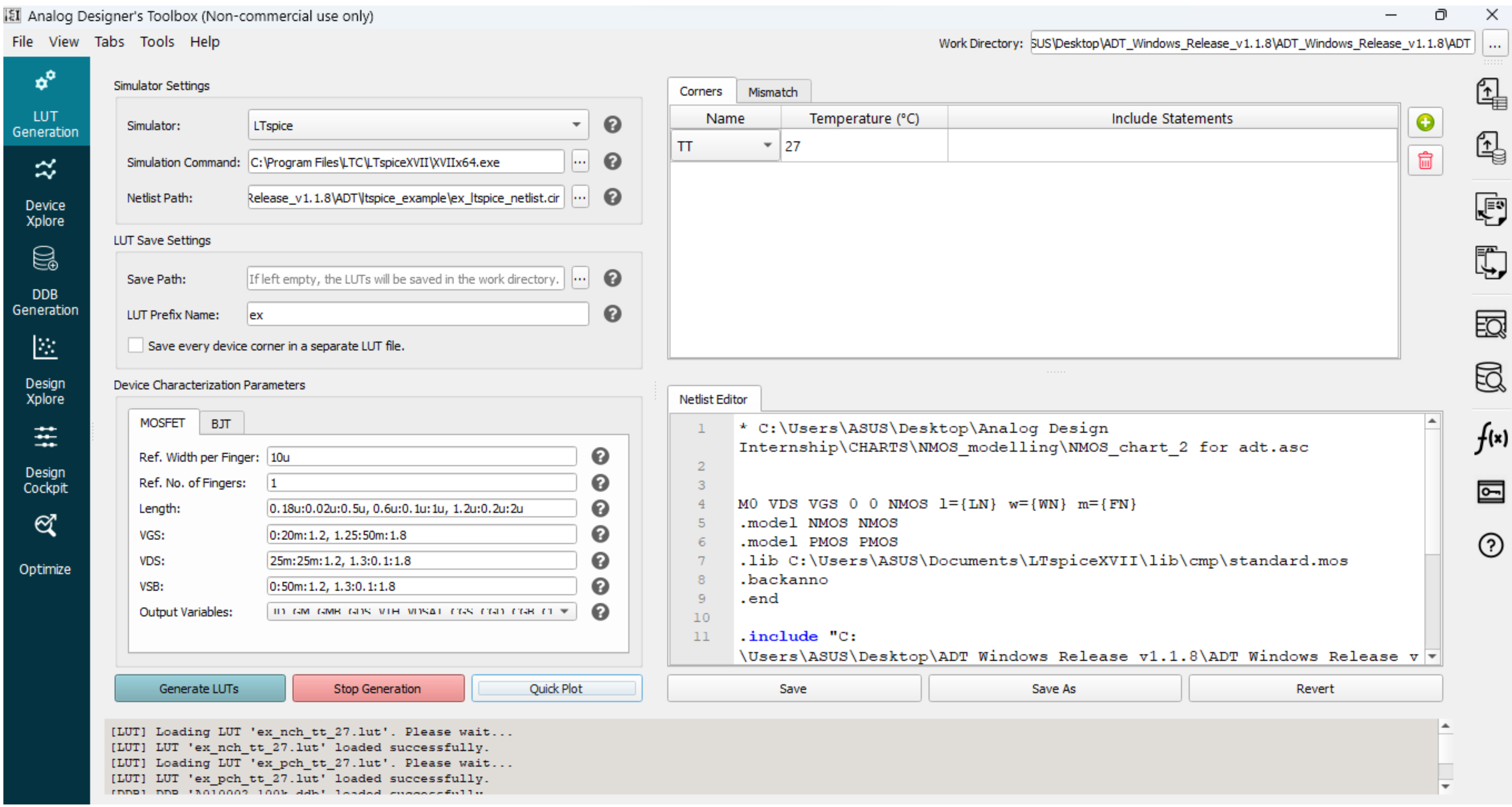
- At the block level, ADT Design Xplore gives the designer the power of design space exploration, constraints management, live tuning, and optimization, all in a single cockpit without invoking the simulator.

- Moreover, with a single click, ADT can build the testbenches in the background and report the results from your favorite simulator. The aim of ADT is to boost productivity, restore designer's intuition, and make the design process systematic, optimized, and fun!

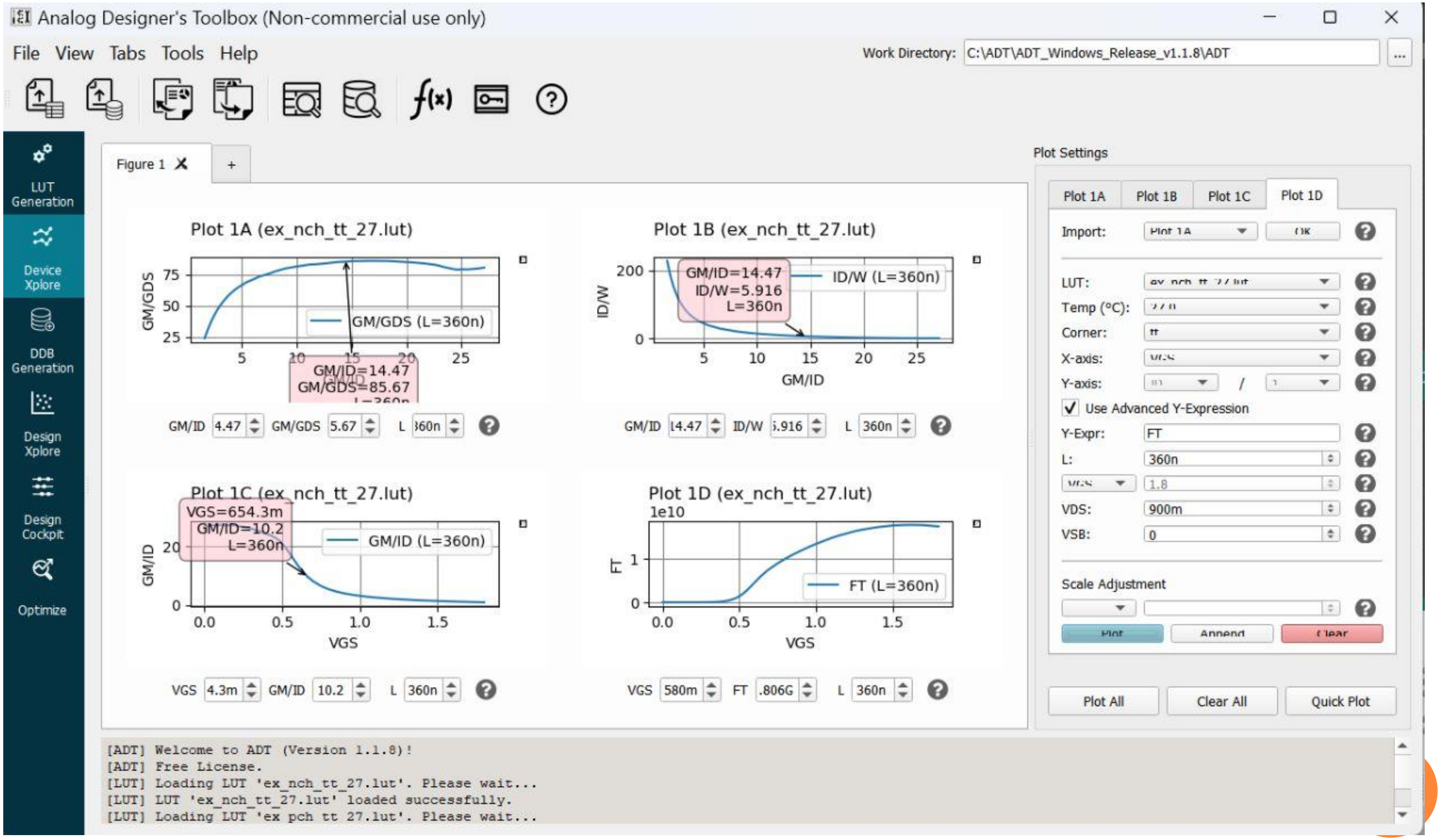
Source: ieee.org

ADT TOOLBOX INTERFACE

LUT GENERATION

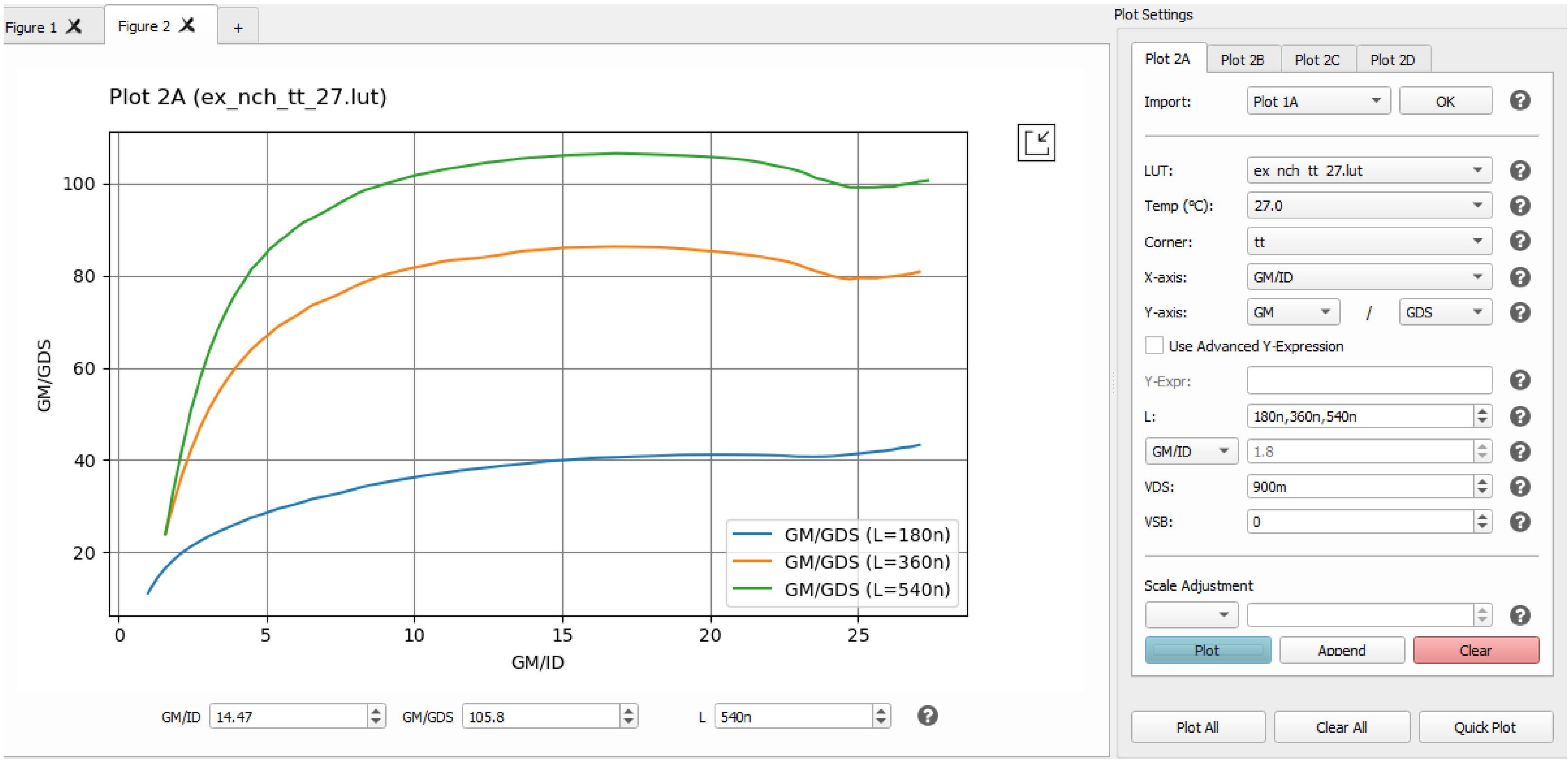


ADT: DEVICE XPLORE

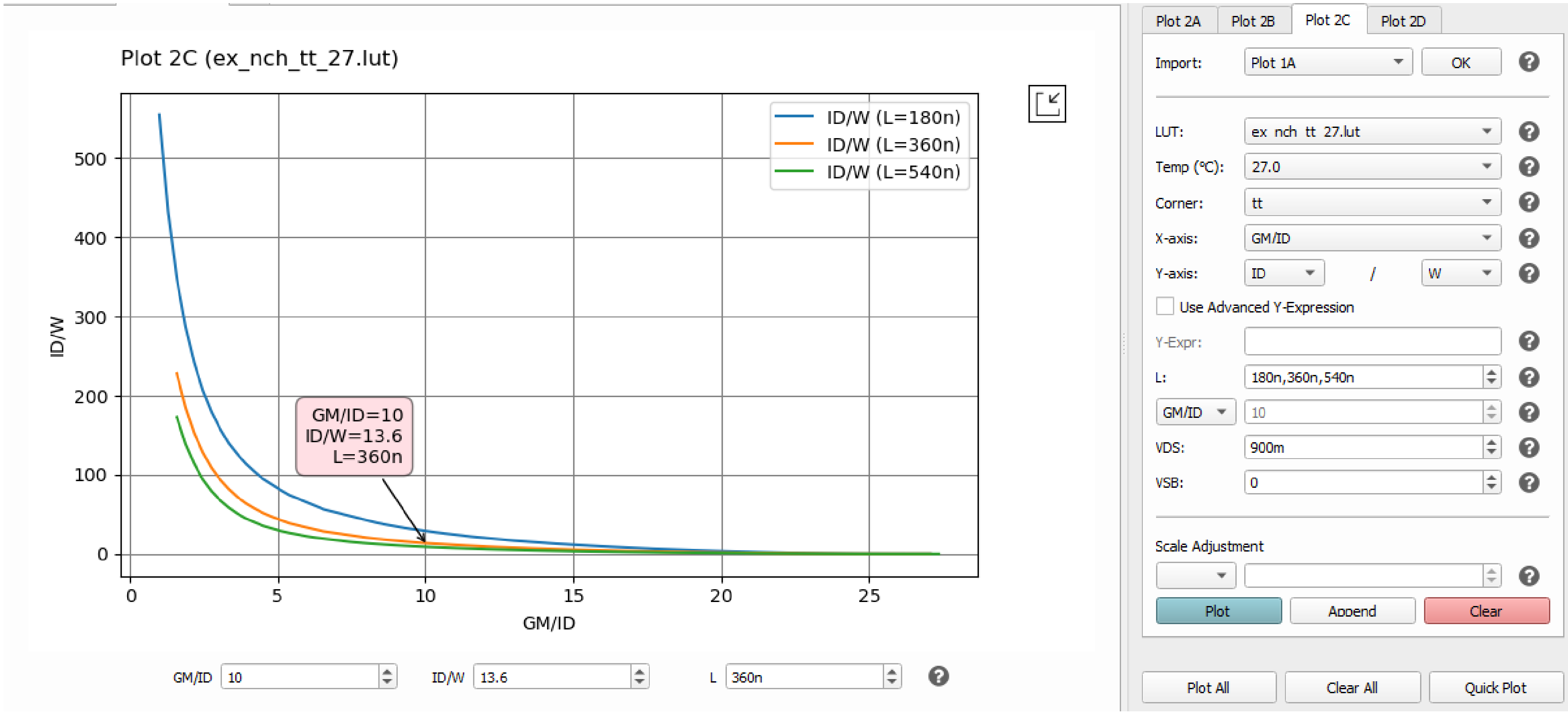


LUT Interface

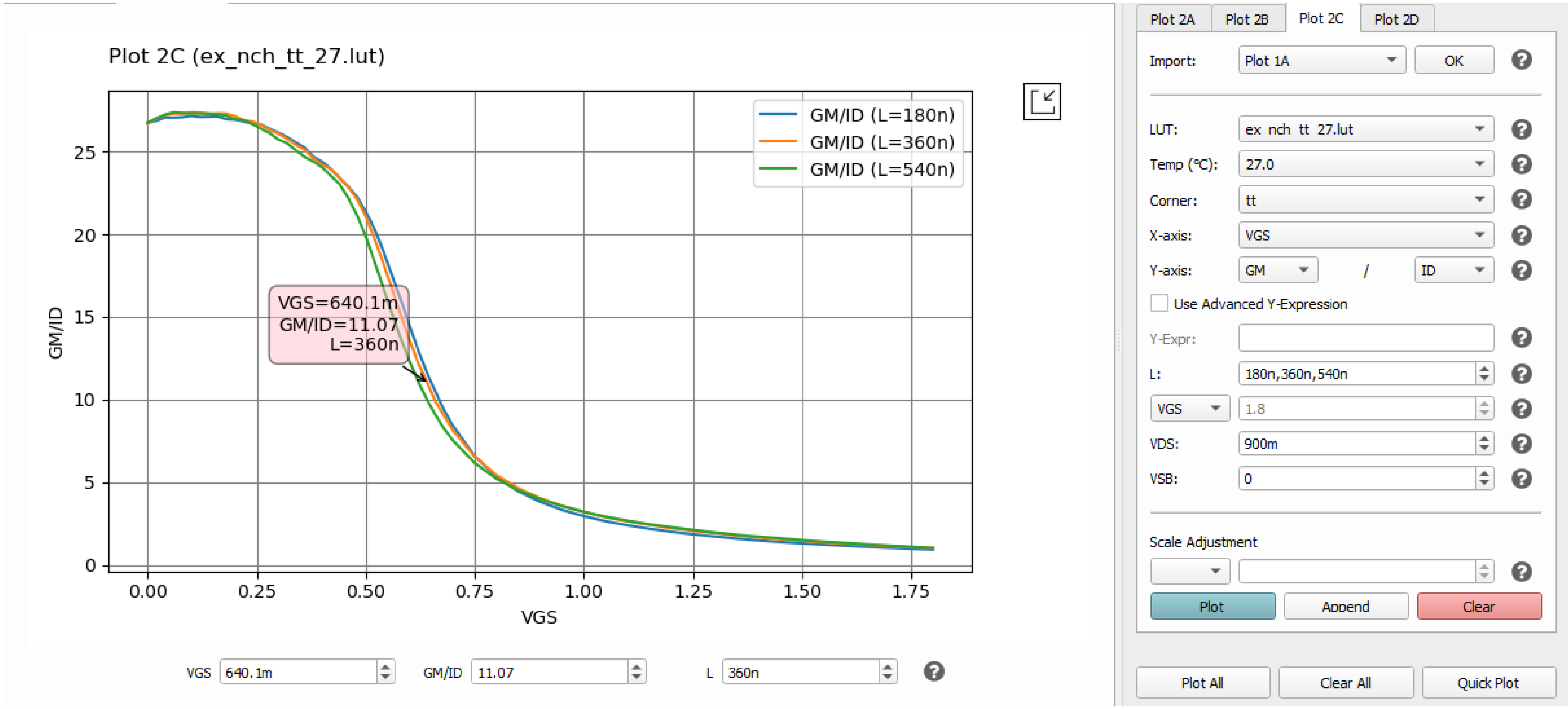
GM/GDS VS GM/ID CHART



ID/W VS GM/ID CHART



VGS VS GM/ID CHARTS



Note: We can draw many charts from ADT Device Xplore
e.g: ID/GDS, GBW, FT vs GM/ID

Model File Used

- File: CMOS180.txt
- Supply Voltage: 1.8 V

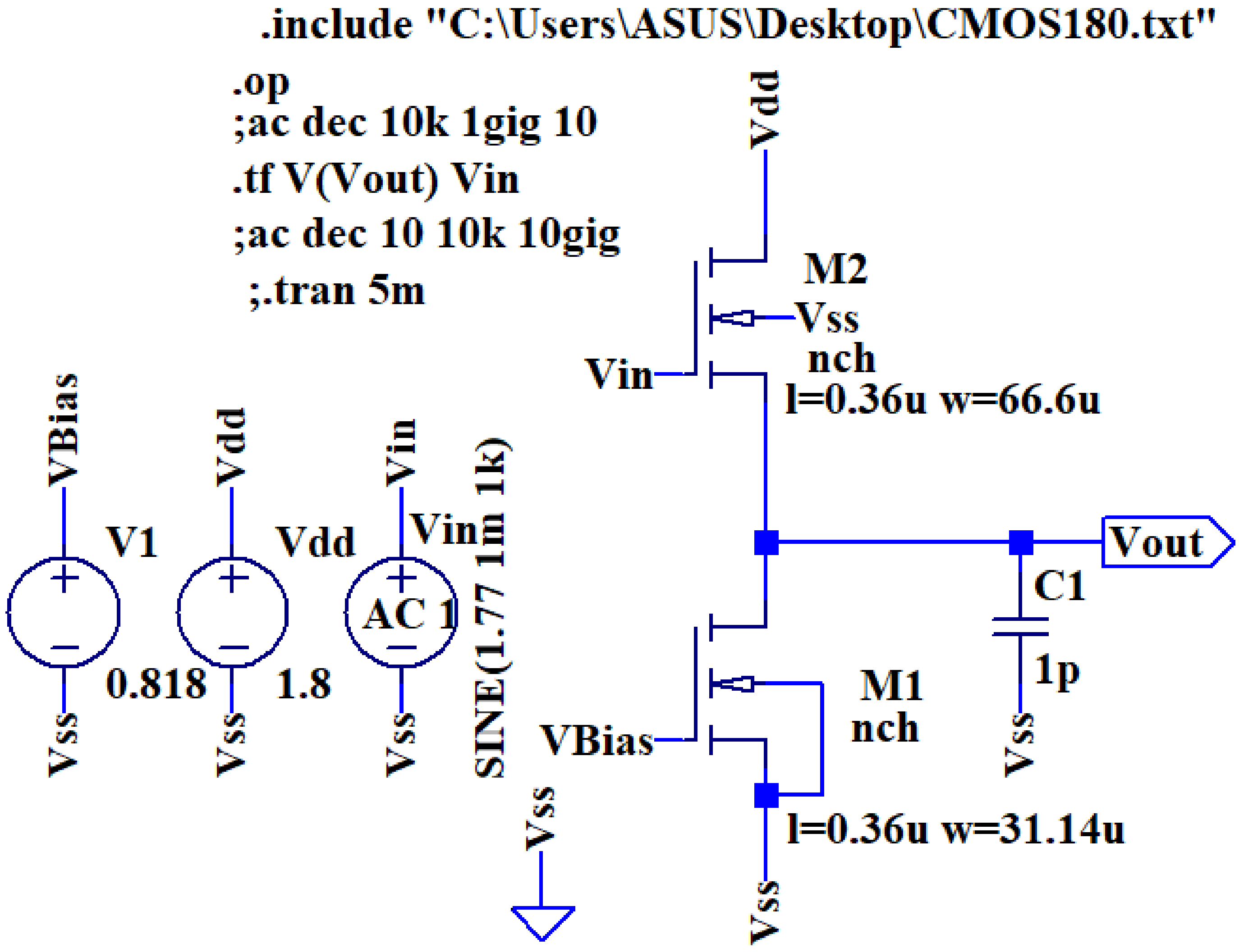
- https://web.stanford.edu/~murmann/gmid
- 0.18µm CMOS models

Source Follower Amplifier

- **Specs:**
- Av=1 CL= 1pF
- Rout=75 Ω

- gm/id= 10 ….(Choose)
- gm/gds=76.93 Id/w=14.58 Vgs=870mV
- gm=13.33 mS W1=91.22 µm Vin=1.77V
- Id=1.33 mA **W1=66.6 µm (tuning to get Rout)**
- gds=172.2 µS
- Ro1=5.77 KΩ
- Let Ro2=10 KΩ gds=100 µS
- Id/gds=13.3
- gm/id=5.112 gm/gds=67.36 Vgs=819.2mV
- W2=31 µm

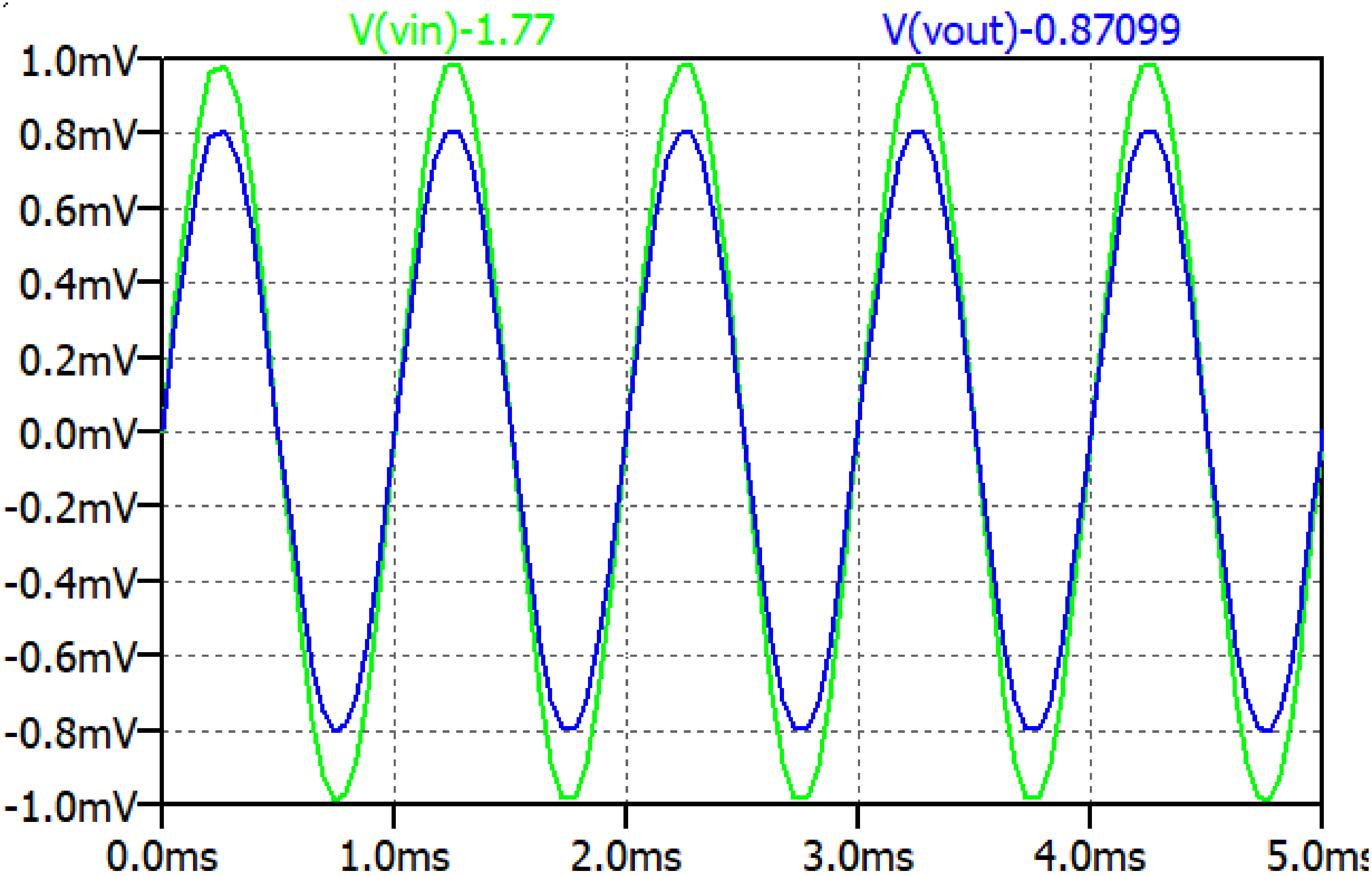
Simulation


.include "C:\Users\ASUS\Desktop\CMOS180.txt"
.op
;ac dec 10k 1gig 10
.tf V(Vout) Vin
;ac dec 10 10k 10gig
;.tran 5m
Vdd
M2
Vss
nch
l=0.36u w=66.6u
Vin
VBias
V1
0.818
Vss
Vdd
Vdd
1.8
Vss
Vin
Vin
AC 1
SINE(1.77 1m 1k)
Vss
Vout
C1
1p
Vss
M1
nch
VBias
l=0.36u w=31.14u
Vss
Vss

Result

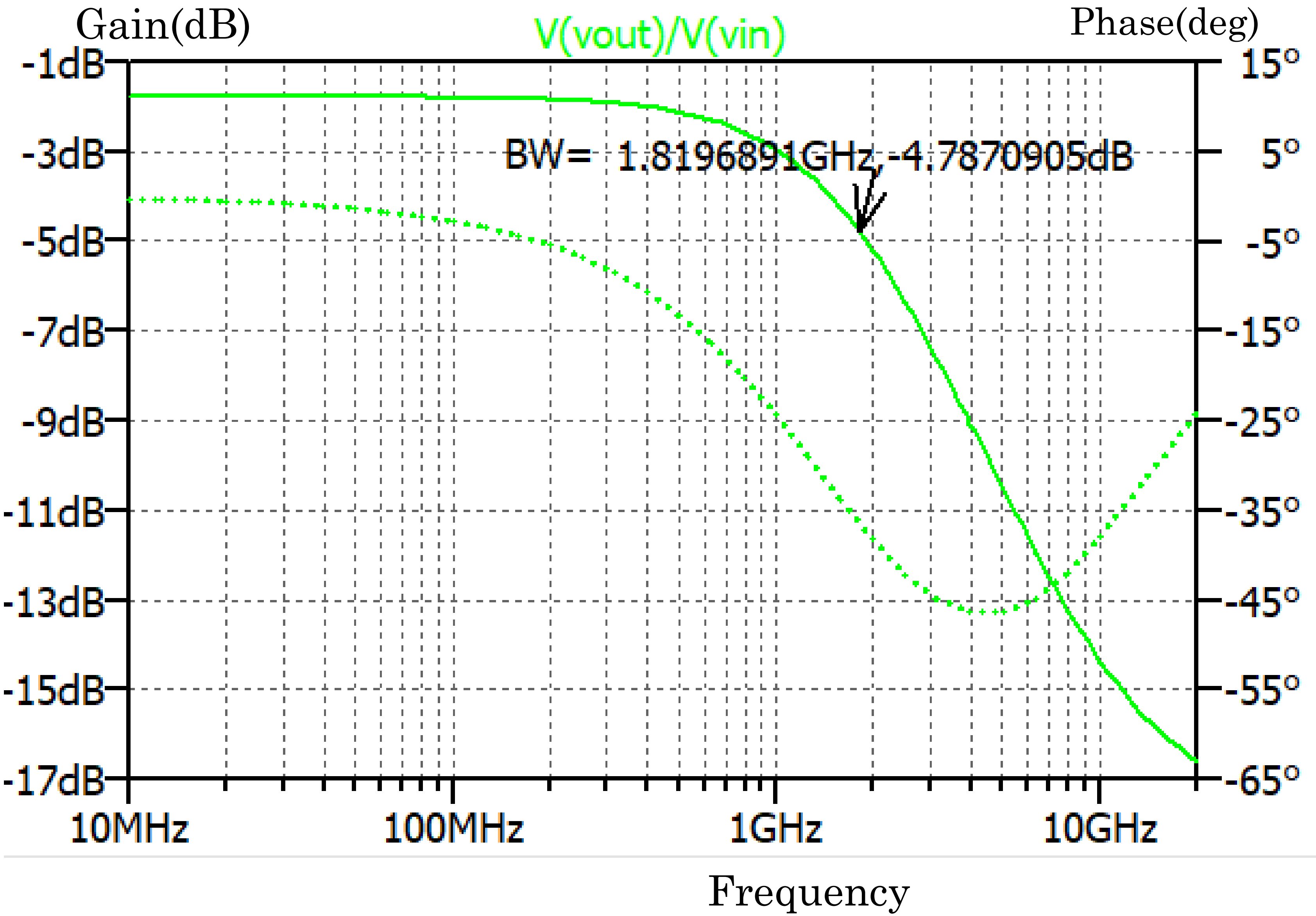
Simulated Value	Specifications
Av= 0.814 v/v	Av=1 v/v
BW=1.82 GHz	BW=2.12 GHz
Rout=75.1 Ω	Rout=75 Ω
Id=1.3 mA	Id=1.33 mA
Vout(dc)=0.87 V	Vout(dc)=0.9 V

Transient Analysis



Vin(p-p)=2 mV Vout=1.6 mV Gain=0.8

FREQUENCY RESPONSE



Common Source Amplifier

Specification:
Gain(Av)=40
Rout=150 KΩ
BW=25 MHz

Calculation:

- **Formula Used**

- BW(3dB freq) $= \frac{1}{2\pi.Rout.CL}$
- Rout= ro1 // ro2

Av=gm.Rout

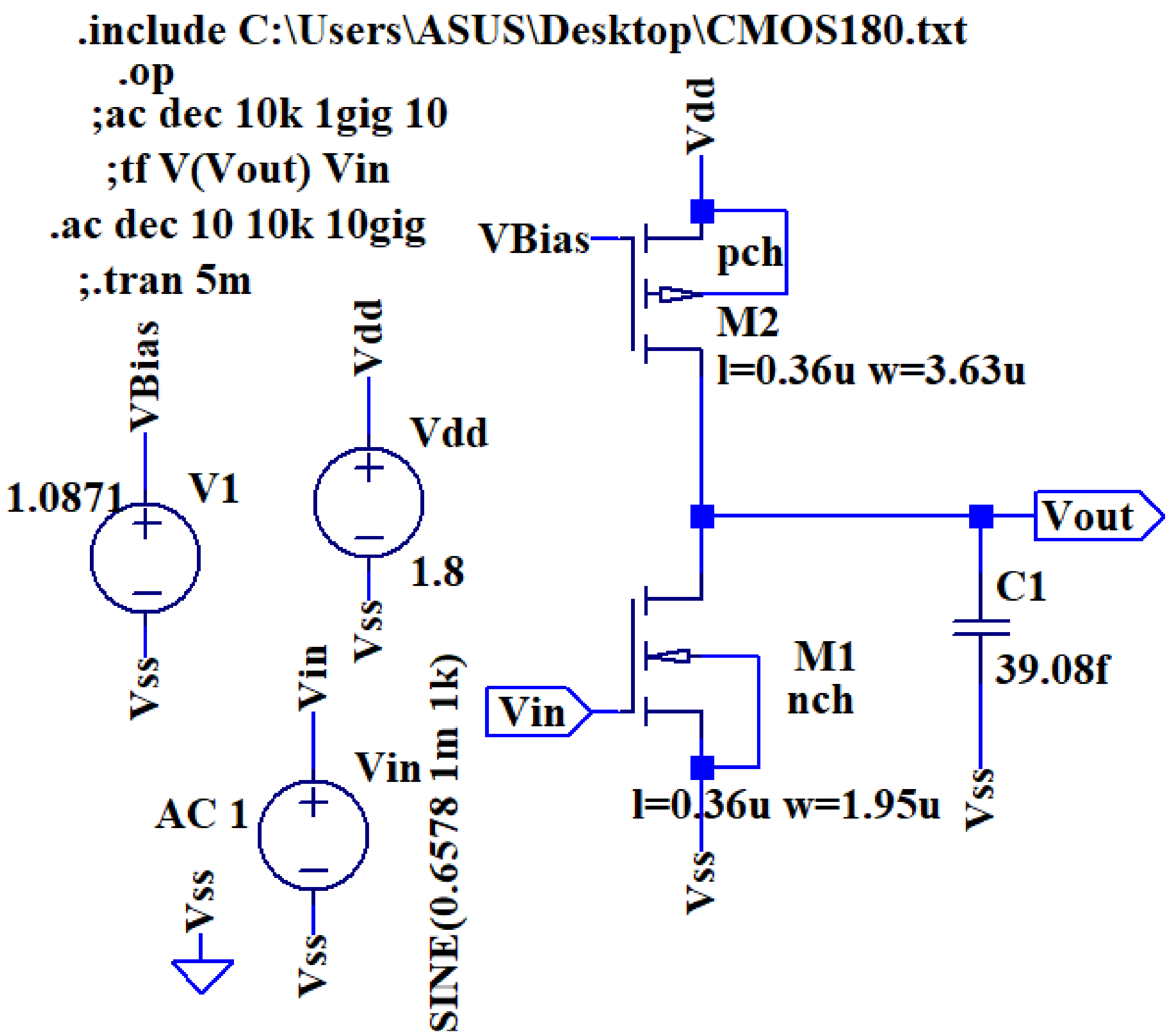
- CL=42.44 fF
- gm/id=10 (Choose)
- gm=0.266 mS
- Id=26.6 µA
- gm/gds= 81.72 ……from chart
- gds=3.25 µS
- Ro1=307.21 KΩ

id/w=13.6
W1=1.95 µm
Vgs1=657.8mV

Continue….

- $Ro2=293.12\ K\Omega$
- $gds2=3.41\ \mu S$
- $(Id/gds)_2=7.8$
- $(gm/id)_2= 7.106$ …… from chart
- $(Id/w)_2=7.312$ …… from chart
- $Vgs2=712.9\ mV$
- $W2= 3.63\ \mu m$

Simulation



.include C:\Users\ASUS\Desktop\CMOS180.txt
.op
;ac dec 10k 1gig 10
;tf V(Vout) Vin
.ac dec 10 10k 10gig
;.tran 5m
VBias
1.0871
V1
Vss
Vdd
Vdd
1.8
Vss
Vin
Vin
AC 1
Vss
Vss
SINE(0.6578 1m 1k)
Vdd
VBias
pch
M2
l=0.36u w=3.63u
Vout
C1
39.08f
Vss
Vin
M1
nch
l=0.36u w=1.95u
Vss

Some Changes

Internal capacitance at node Vout = cgd2 +cgd1(1+Av)

C(Vout) = 3.36 fF

So CL=42.44 f -3.36f = **39.08 fF**

Result And Conclusion

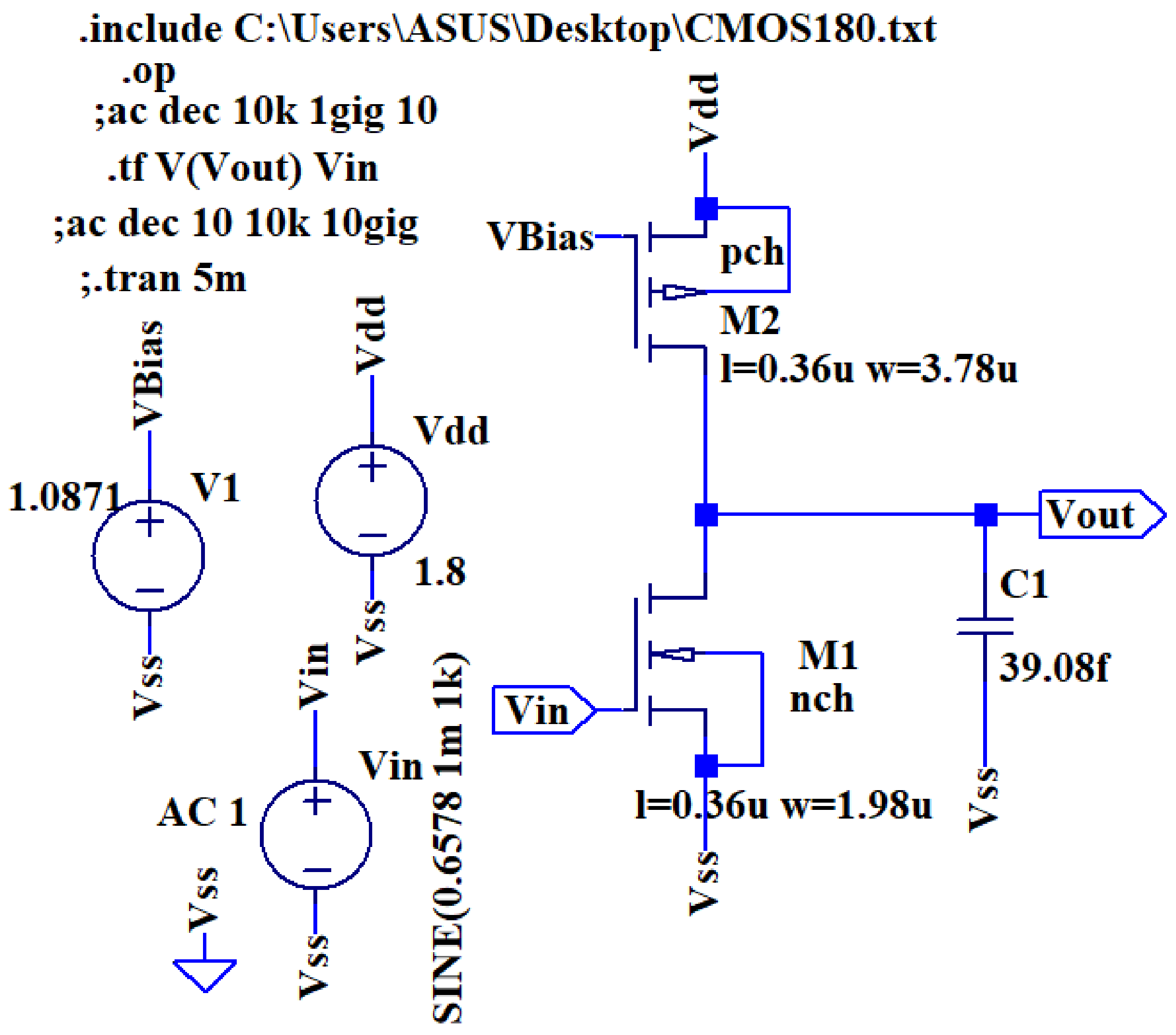
Simulated Value	Specifications
Av= 40.01 v/v	Av=40 v/v
BW=25.06 MHz	BW=25MHz
GBW=1.002 GHz	GBW=1 GHz
Rout=149.327 KΩ	Rout=150 KΩ
Id=26.73 µA	Id=26.6 µA
Vout(dc)=0.773 V	Vout(dc)=0.9 V

Spice Error Log File

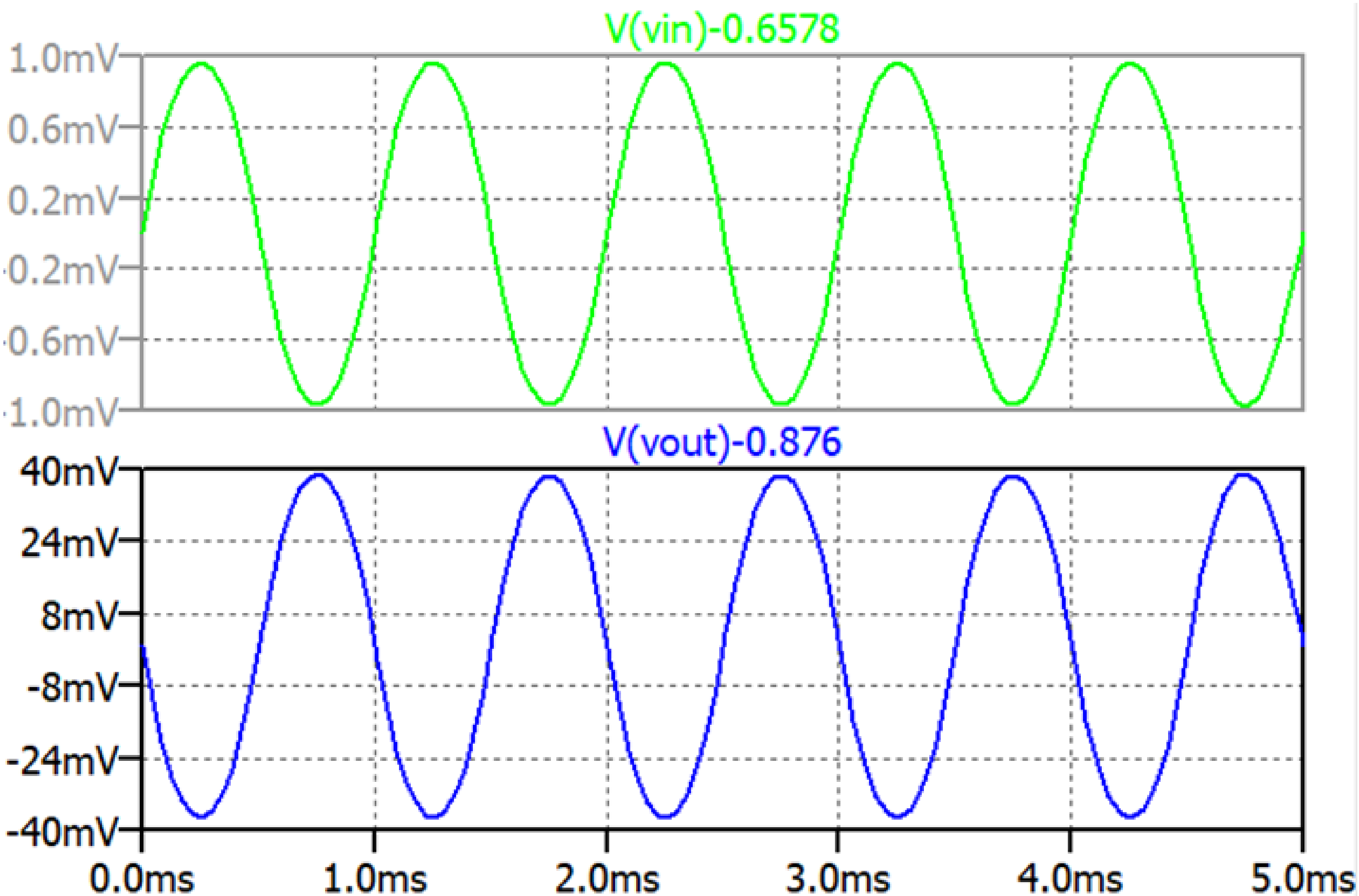
```
        --- Transfer Function ---

Transfer_function:              -40.0109        transfer
vin#Input_impedance:            1e+020          impedance
output_impedance_at_V(vout):    149327          impedance
```

```
Semiconductor Device Operating Points:
                        --- BSIM3 MOSFETS ---
Name:          m2          m1
Model:         pch         nch
Id:         -2.67e-05    2.67e-05
Vgs:        -7.13e-01    6.58e-01
Vds:        -1.03e+00    7.74e-01
Vbs:         0.00e+00    0.00e+00
Vth:        -4.48e-01    4.59e-01
Vdsat:      -2.19e-01    1.52e-01
Gm:          1.87e-04    2.68e-04
Gds:         3.21e-06    3.49e-06
Gmb          5.86e-05    7.00e-05
Cbd:         0.00e+00    0.00e+00
Cbs:         0.00e+00    0.00e+00
Cgsov:       2.38e-15    9.57e-16
Cgdov:       2.38e-15    9.57e-16
Cgbov:       2.98e-19    3.28e-19
dQgdVgb:     1.24e-14    6.48e-15
dQgdVdb:    -2.38e-15   -9.32e-16
dQgdVsb:    -9.67e-15   -5.23e-15
dQddVgb:    -2.39e-15   -9.63e-16
dQddVdb:     2.39e-15    9.60e-16
dQddVsb:     4.60e-18    4.49e-18
dQbdVgb:    -1.61e-15   -9.88e-16
dQbdVdb:    -5.20e-19    1.92e-18
dQbdVsb:    -7.20e-16   -4.05e-16
```

Unit Devices

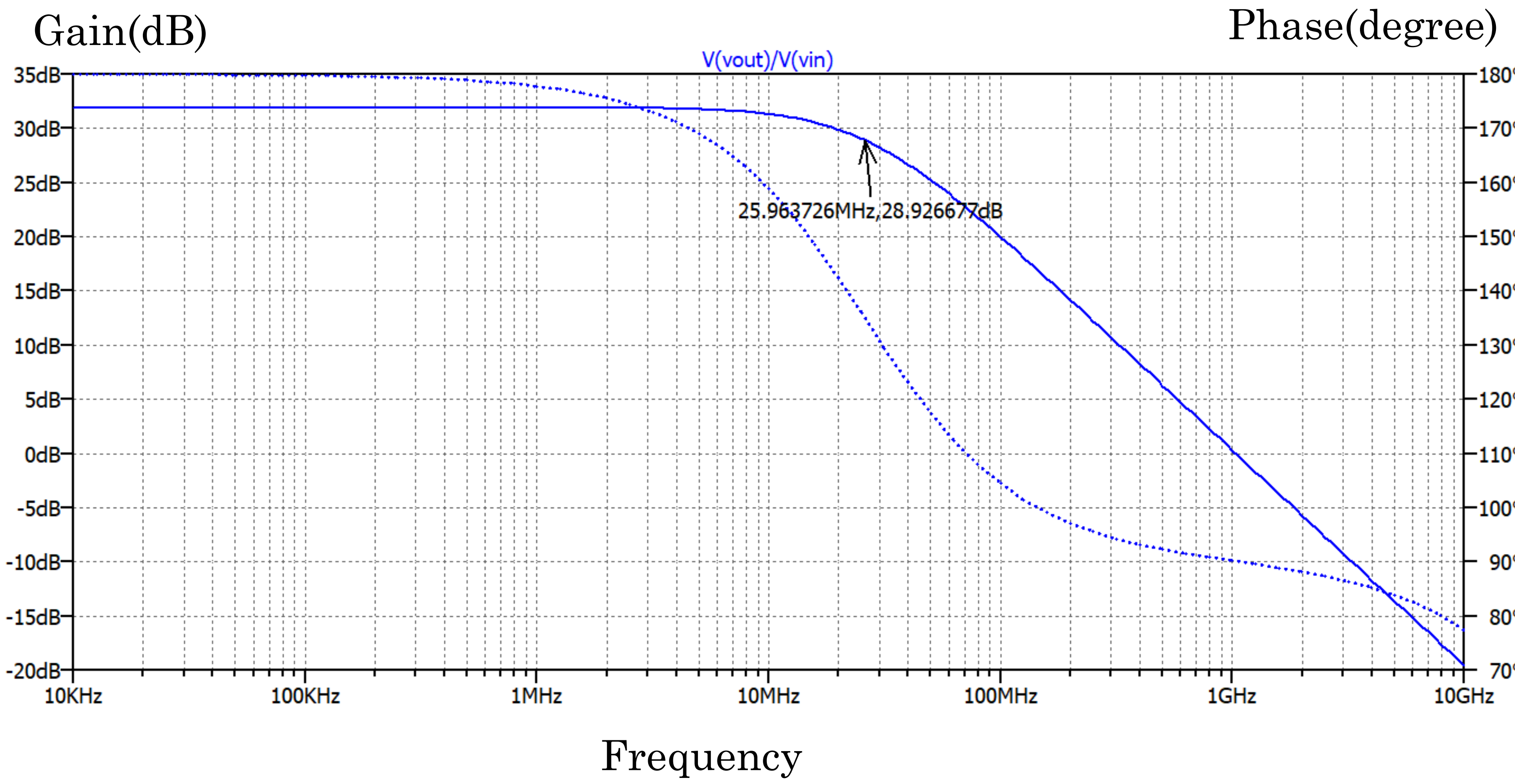


Transient Analysis



Vin(p-p)=2 mV Vout=78.88 mV Gain=39.44

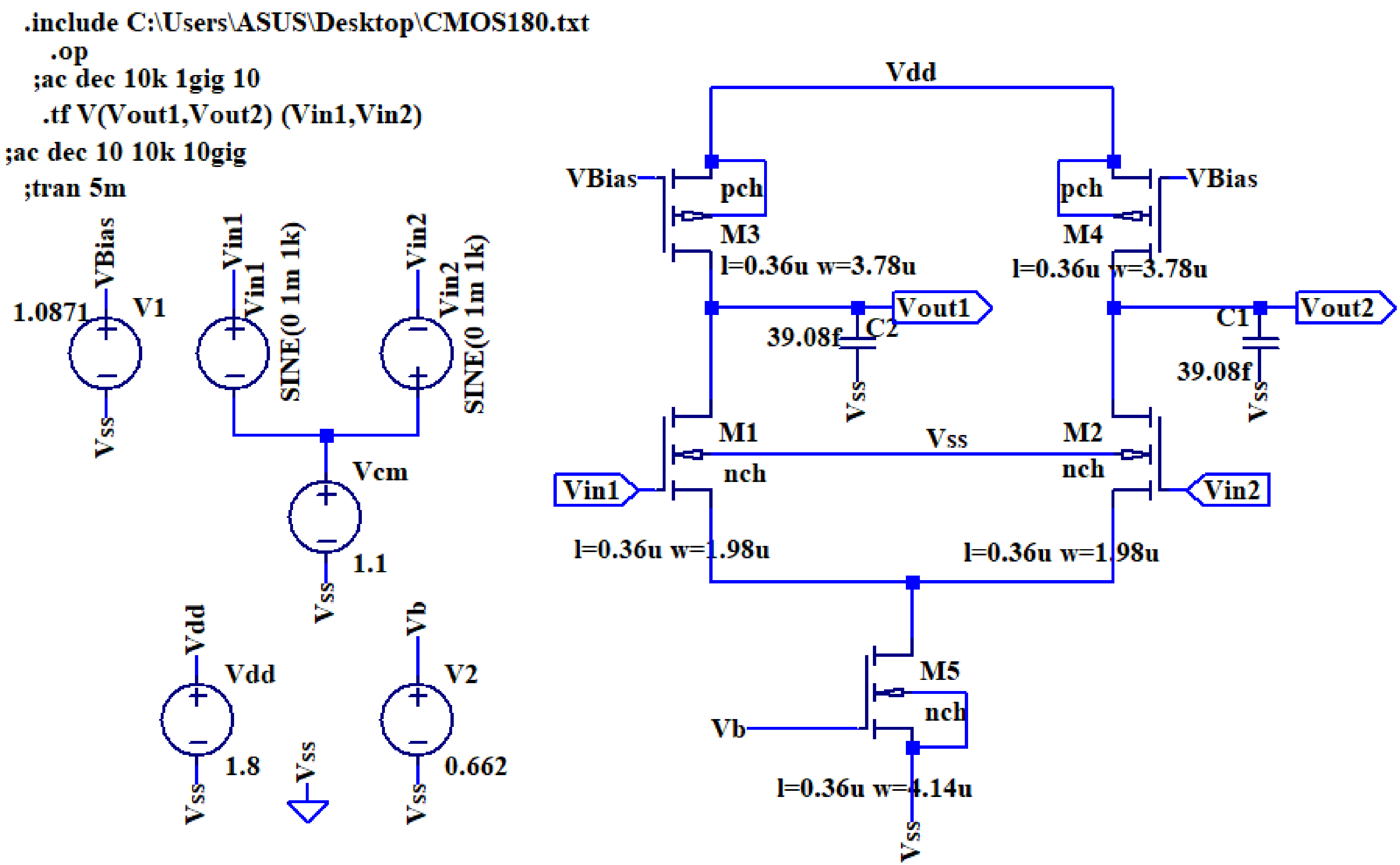
Frequency



BW=25.96 MHz

Differential Pair

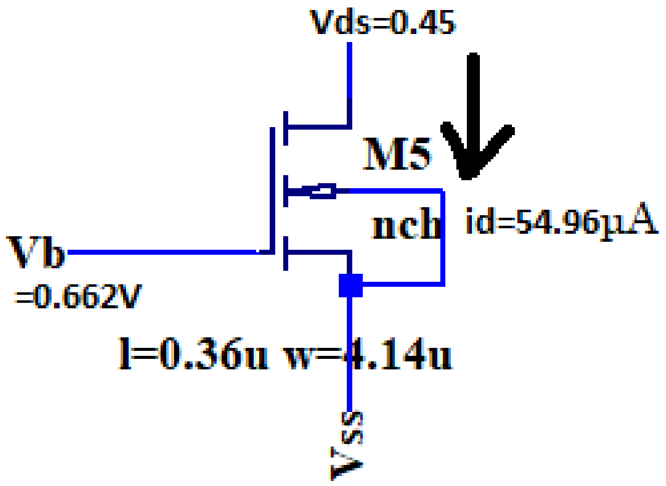
Using two Common Source Amplifier



Calculation for Current Source

Id=54.96 µA
gm/id= 10 …(Choose)
Vgs=Vb=0.662
Id/w=13.41

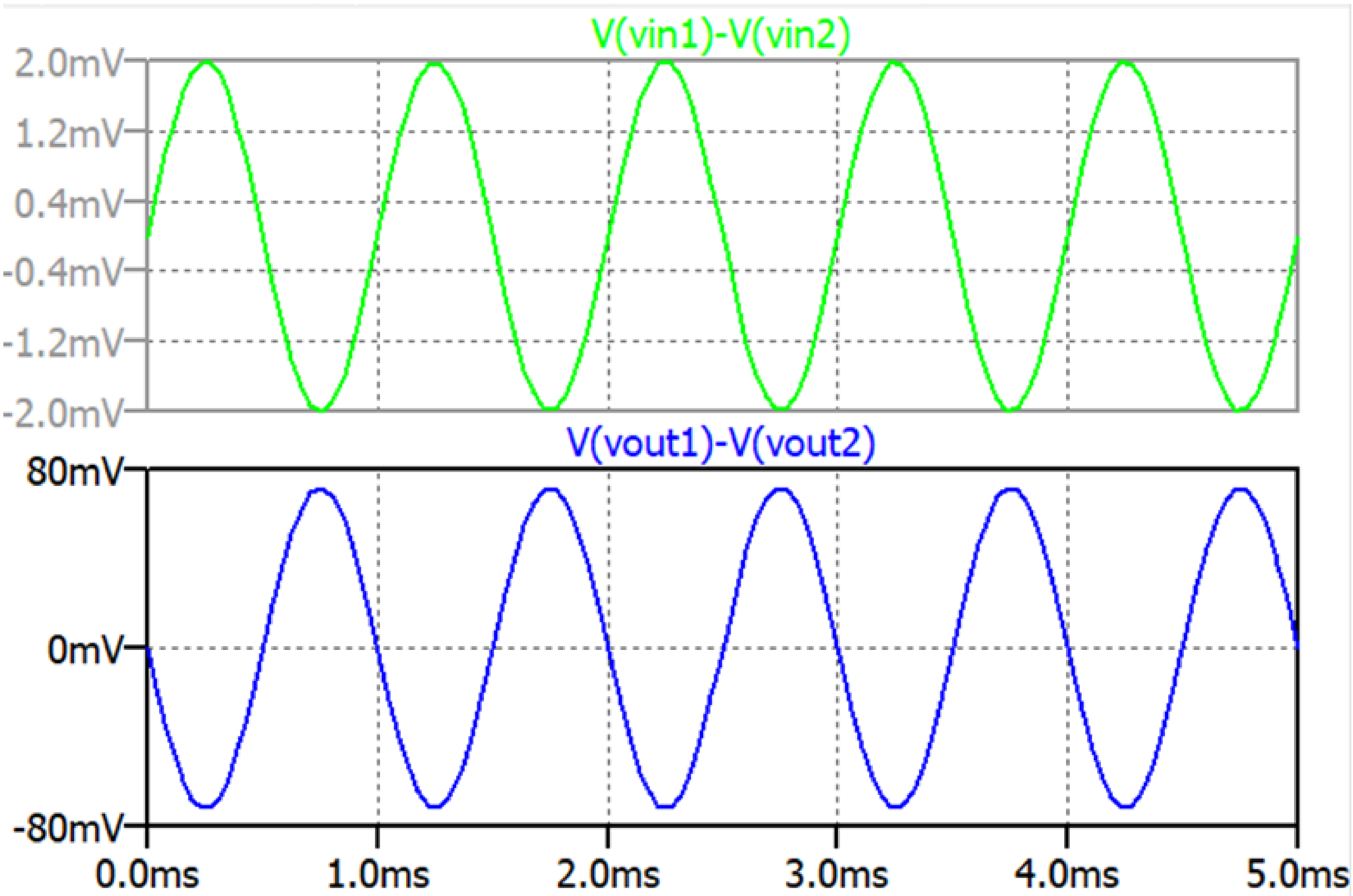
W5=4.09 µm
W5=4.14 µm …..for unit device



Result and Conclusion

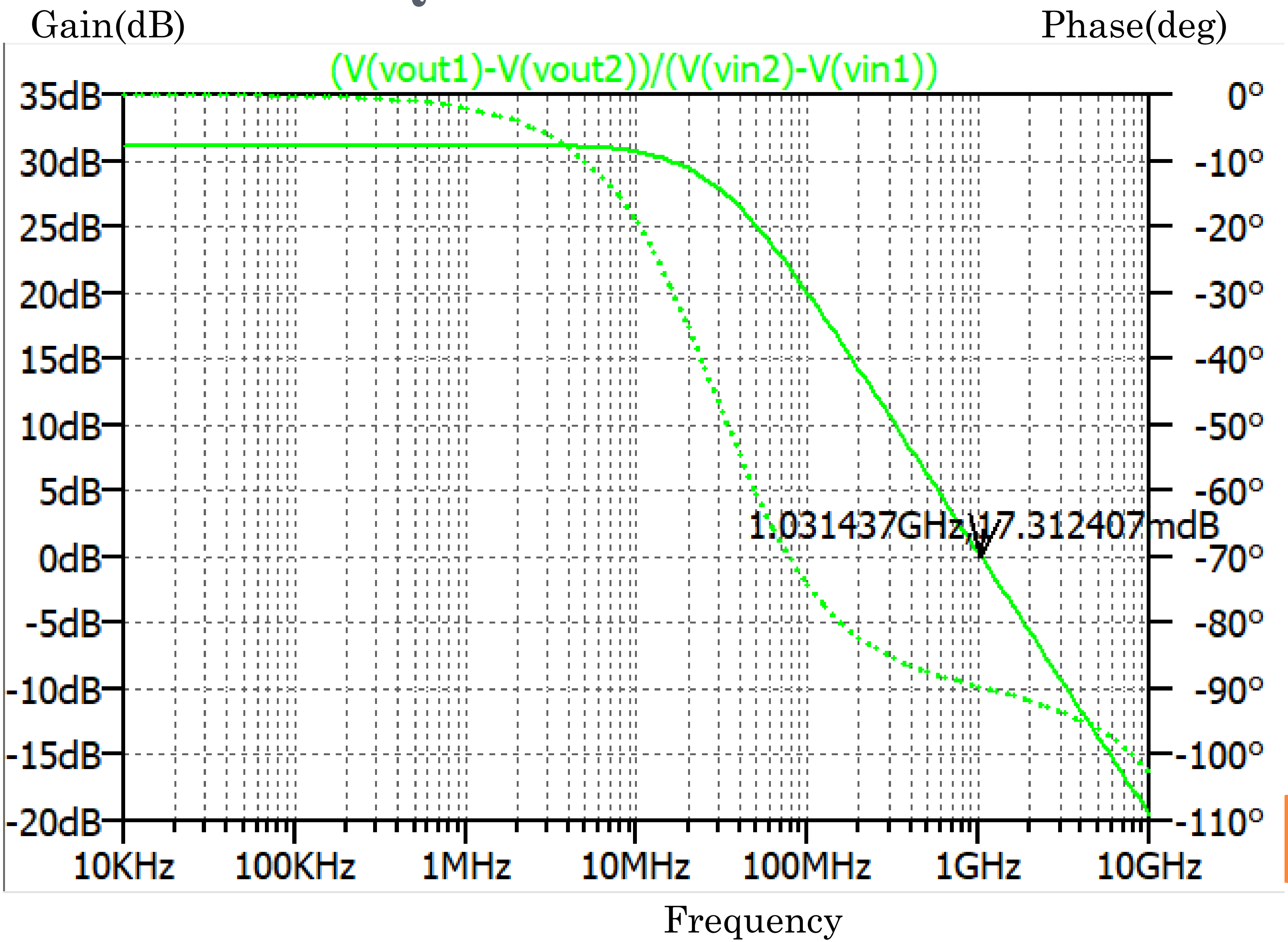
Simulated Value	**Specifications**
Av= 36.18 v/v	Av=40 v/v
BW=28.66 MHz	BW=25MHz
GBW=1.03 GHz	GBW=1 GHz
Rout=263.492 KΩ	
Iss= 54.46 µA	Iss= 54.96µA
Vout(dc)=0.949 V	Vout(dc)=0.9 V

Transient Analysis



Vin1-Vin2(pp)=4 mV Vout1-Vout2(pp)=144.56mV Gain=36.14

Frequency Response



Common Source Amplifier

Specs:
Av=40
Rout=93 KΩ

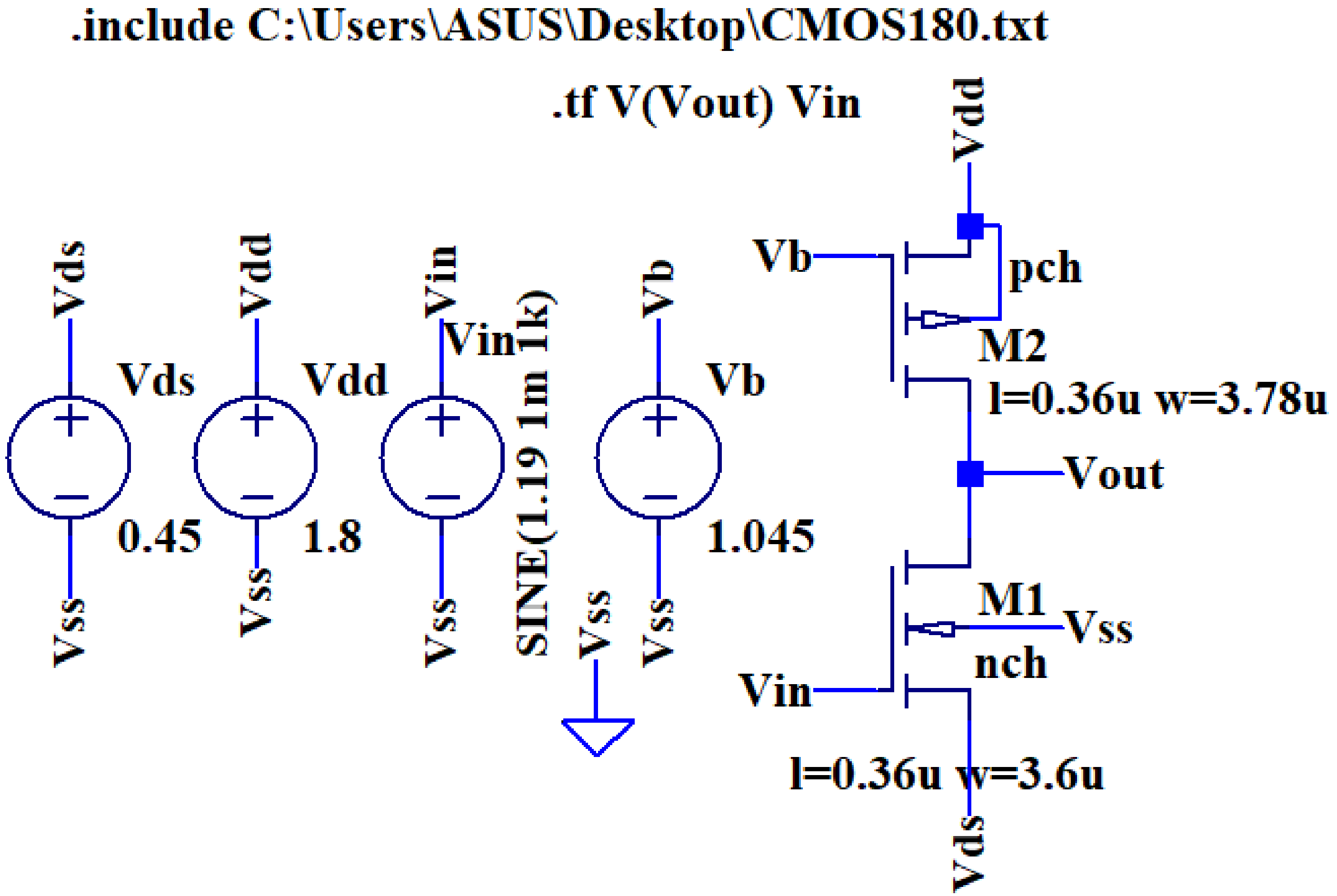
Formula Used

Av=gm.Rout   Rout=Ro1 // Ro3   gds=$\frac{1}{ro}$

W=$\frac{id}{id/w}$

- gm=0.43 mS
- gm/id=12   gm/gds=70.92   Id/W=9.896
- Id=35.8 µA   gds=6.06 µS   W1=3.61 µm
- Ro1=165 KΩ   Ro3= 213.125 KΩ
- gds3= 4.69 µS
- $(Id/gds)_3$=7.63
- gm/id=6.315   Id/W=9.133
- W3=3.91 µm

Simulation



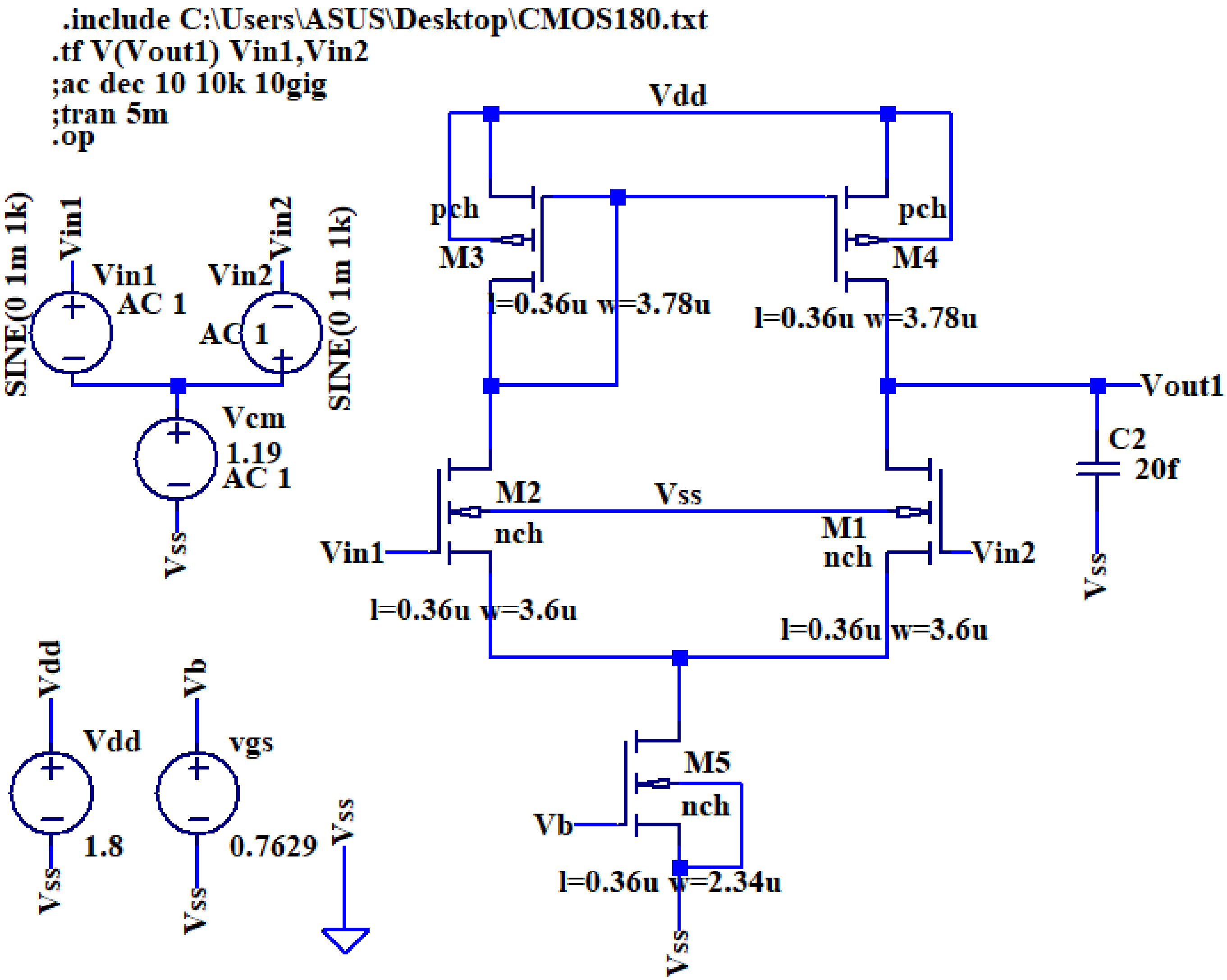
.include C:\Users\ASUS\Desktop\CMOS180.txt
.tf V(Vout) Vin
Vds
Vds
0.45
Vss
Vdd
Vdd
1.8
Vss
Vin
Vin
SINE(1.19 1m 1k)
Vss
Vss
Vb
Vb
1.045
Vss
Vdd
Vb
pch
M2
l=0.36u w=3.78u
Vout
M1
Vss
nch
Vin
l=0.36u w=3.6u
Vds

Results

Simulated Value	Specifications
Av= 40.15 v/v	Av=40 v/v
Rout=95.632 KΩ	Rout=93 KΩ
Id= 35.18 µA	Id= 35.8 µA
Vout(dc)=1.07 V	Vout(dc)=0.9 V

OP-AMP (STAGE-1)

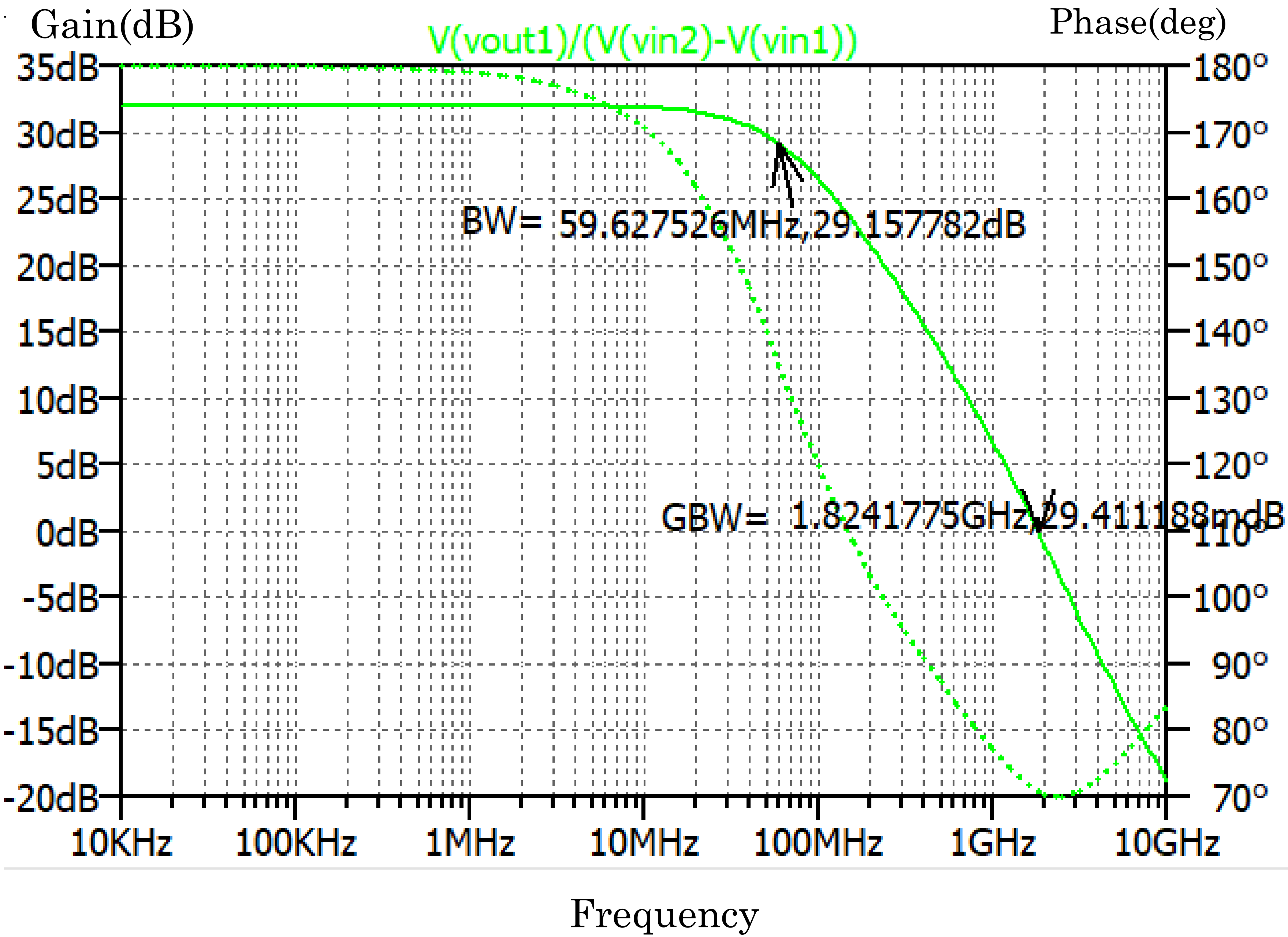
Using Common Source Amplifier



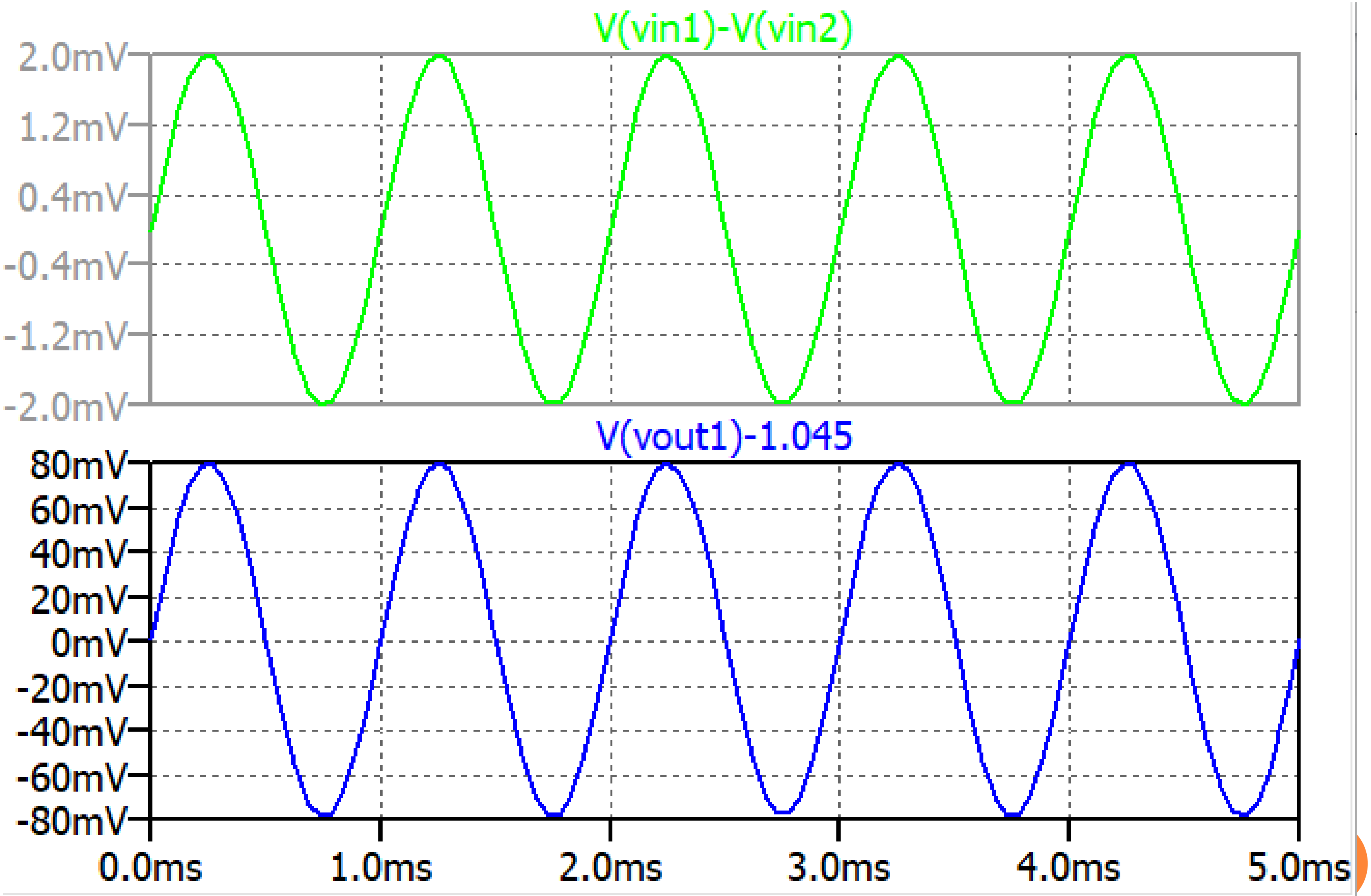
Result

Simulated Value	Specifications
Av= 39.8092 v/v	Av=40 v/v
BW=28.66 MHz	BW=25MHz
GBW=1.03 GHz	GBW=1 GHz
Rout=97.259 KΩ	Rout=93 KΩ
Iss= 70.3 μA	Iss= 71.6 μA
Vout(dc)=1.04 V	Vout(dc)=1.15 V

FREQUENCY ANALYSIS



Transient Analysis



Vin1-Vin2(pp)=4 mV   Vout1(pp)=158.68 mV   Gain=39.67

Common Source amplifier

For Second Stage op-amp

Specs:

Av=28

gm2=8 x 0.432 mS = 3.384 mS

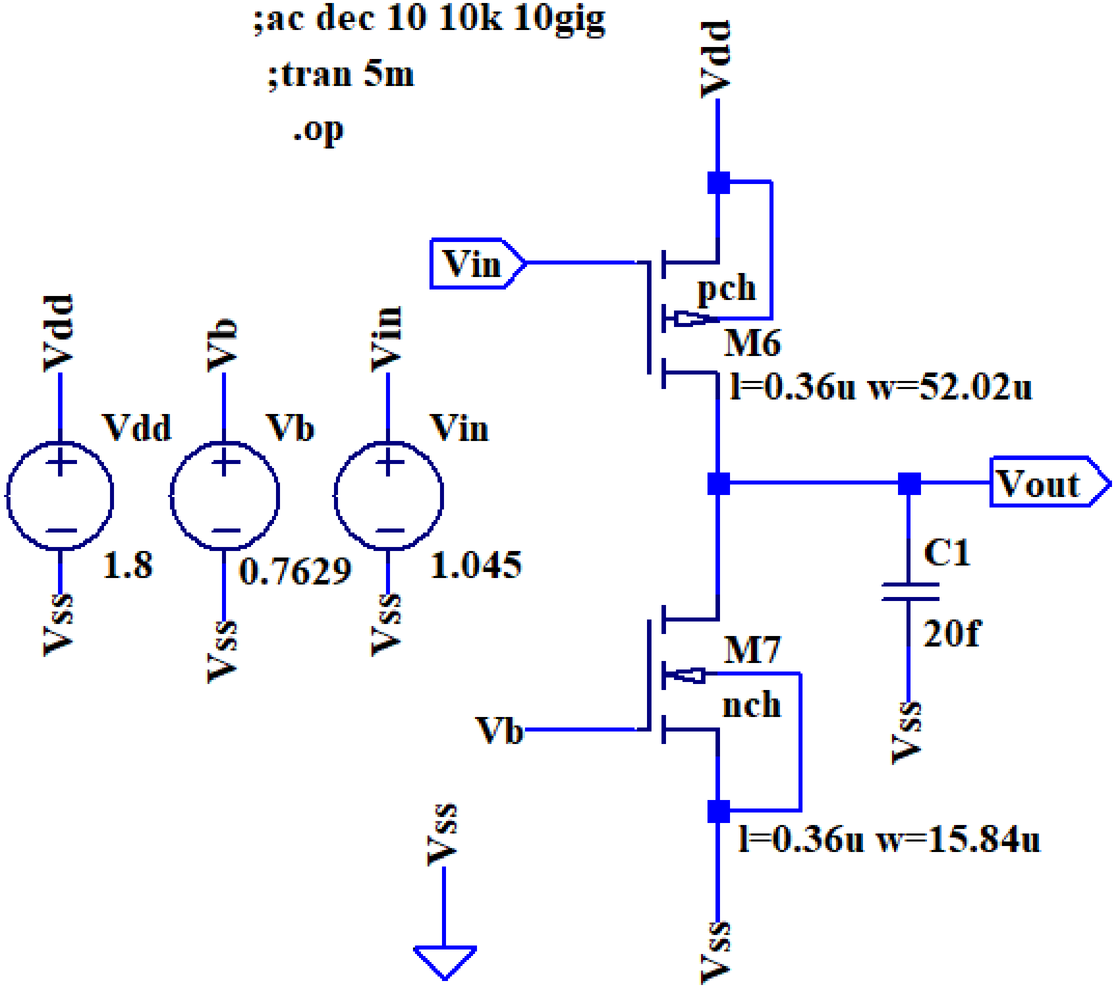
Rout2 = 8KΩ

- Vgs1=780 mV
- gm/id=5.466 id/w=11.9 ….from chart
- gm/gds=46.96 ….from chart
- Id=619 μA
- W6=52μm
- gds6=72.06 μS Ro6= 13.87 KΩ
- Ro7=18.9 KΩ gds7=52.9 μS

- (Id/gds)7=11.7
- gm/id=6.24 id/w=31.05
- W7=19.9 µm **W7=15.84 µm in Simulation**
- Vgs7=0.7629 V

Simulation

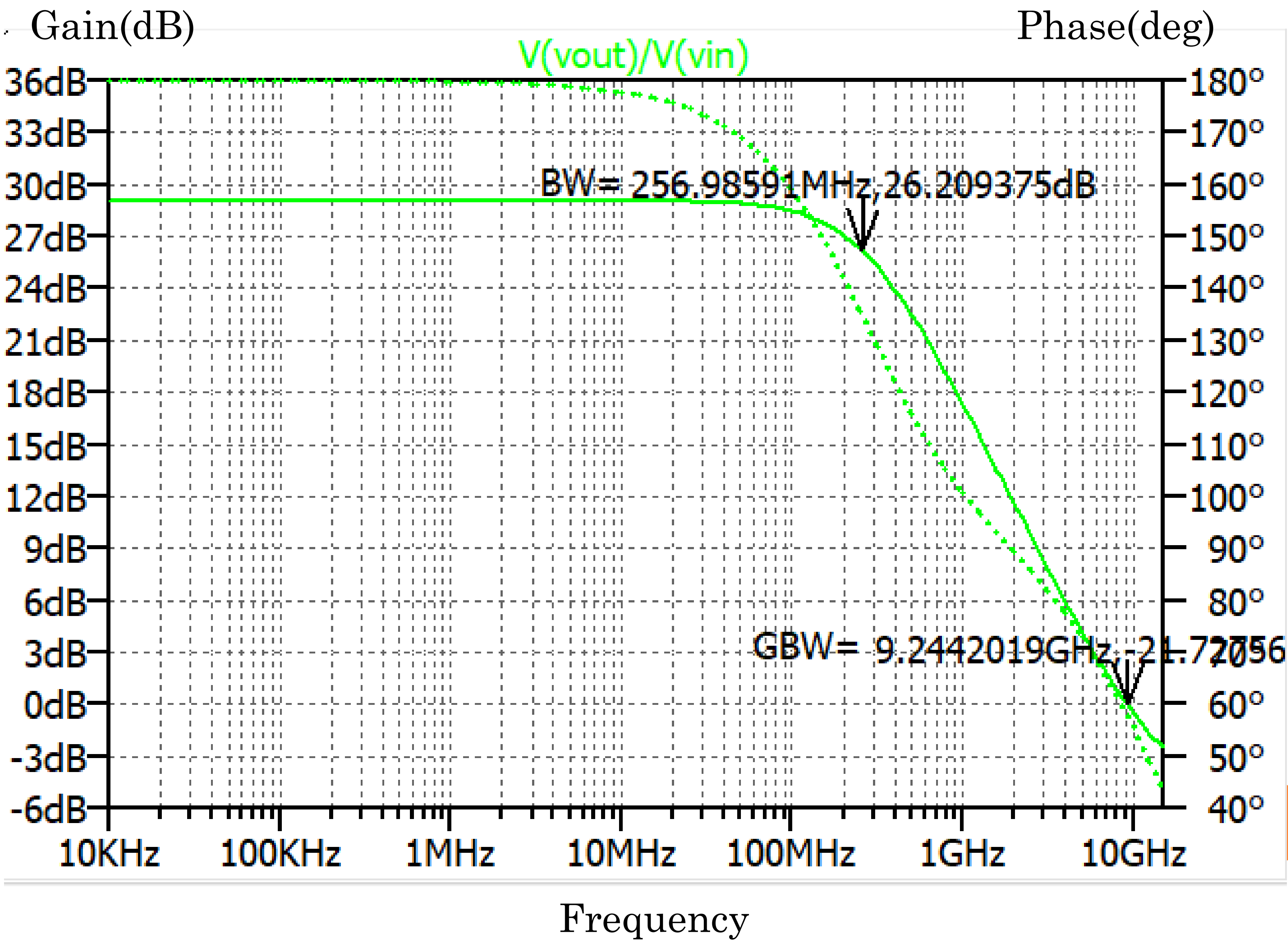
```
.include C:\Users\ASUS\Desktop\CMOS180.txt
.tf V(Vout) Vin
;ac dec 10 10k 10gig
;tran 5m
.op
```



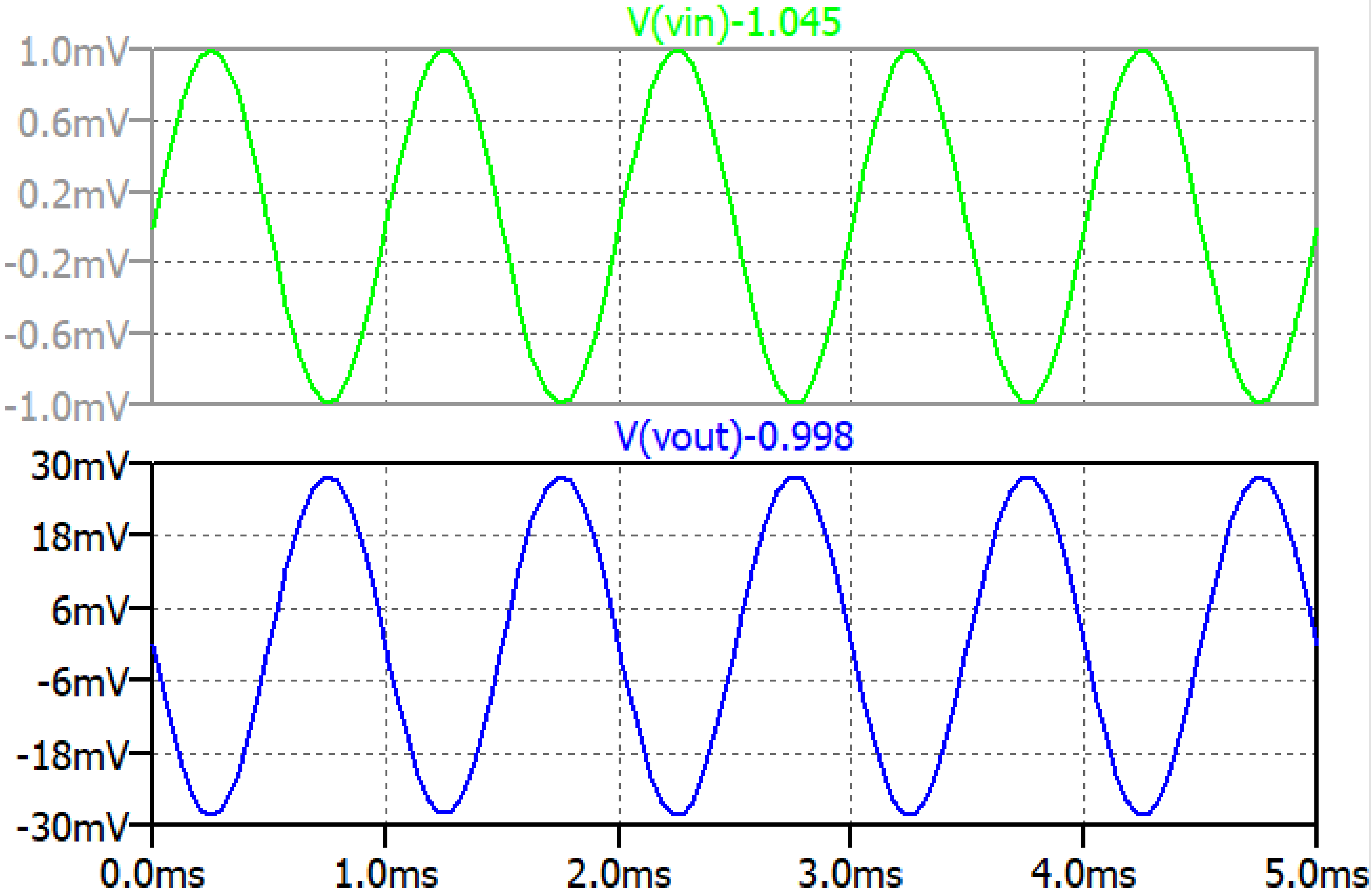
RESULT

Simulated Value	Specifications
Av= 28.34 v/v	Av=28 v/v
BW=256.9 MHz	
GBW=9. 24 GHz	
Rout=9.6 KΩ	Rout=8 KΩ
IB2= 494 µA	IB2= 619 µA
Vout(dc)=0.998 V	Vout(dc)=0.9 V

Frequency Response



Transient Analysis



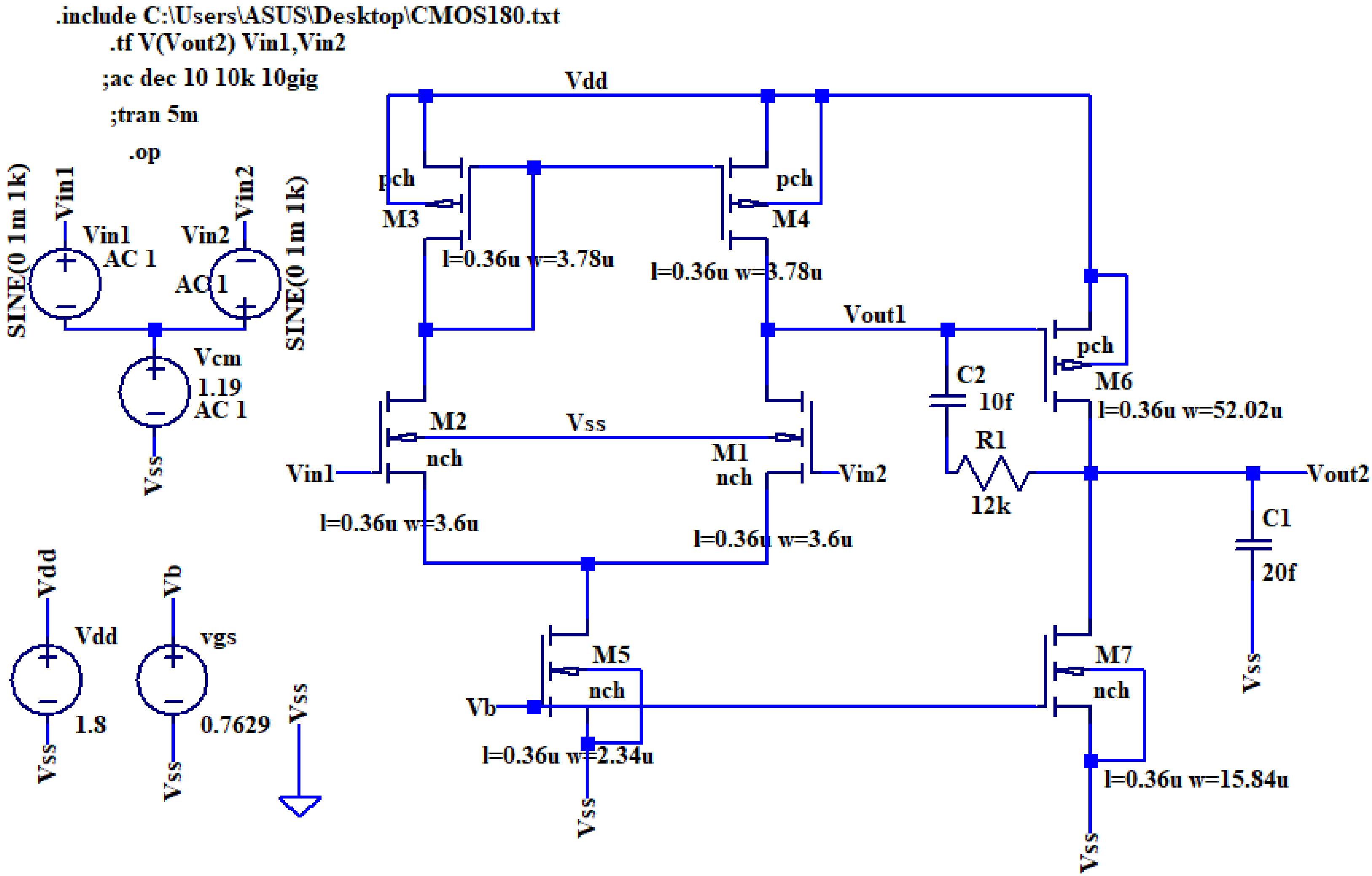
Vin(pp)=2 mV Vout(pp)=56.63 mV Gain=28.315

Project: Designing of two Stage Operational amplifier

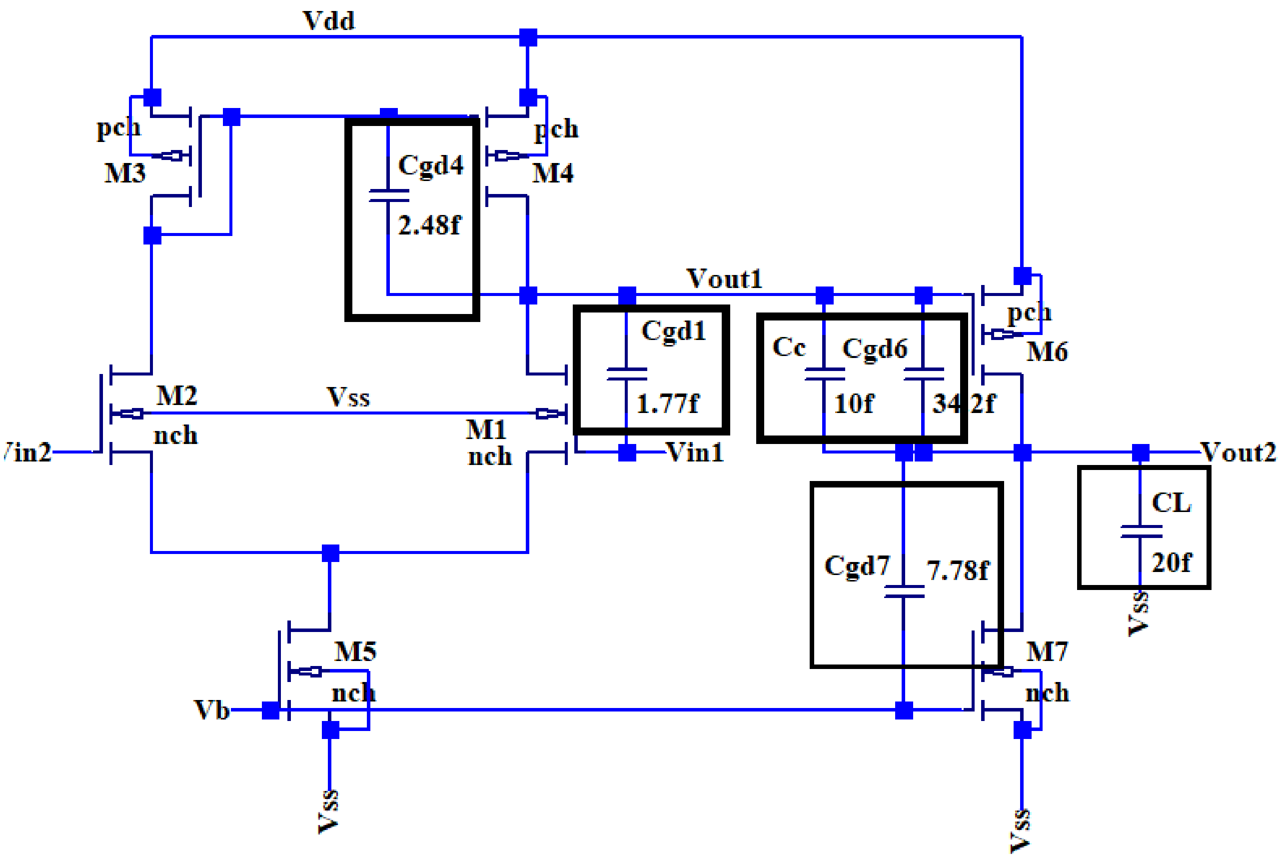
Specification	
Gain(Av)	≥ 1000 (60dB)
GBW	1GHz
Phase Margin	≥50
Load Capacitance	20 fF

PROJECT: TWO STAGE OP-AMP

Combining Stage-1 and Stage-2



CAPACITOR



C1=Capacitance at Node(Vout1)= Cgd4 + Cgd1 + { (Cgd6 + Cc)*(1+Av2)}

C1= 1.3 pF

C2=Capacitance at Node(Vout2)= CL + Cgd7 + { (Cgd6 + Cc)*(1 + $\frac{1}{Av2}$)}

C2=73.52 fF

Pole And Zero

- Dominant Pole
- Fp1 =$\frac{1}{2\pi.Rout1.C1}$
- Fp1= 1.2 MHz where Rout1=97.25 KΩ
- Fp2= Beyond 1GHz
- Sz=$\frac{1}{Cc(\frac{1}{Gm6}-Rz)}$
- Fz= -1.36GHz where Rz=12k, Gm2=2.95mS

Frequency Compensation

- Cc=10 fF (generally Cc=(0.3 – 0.5)*CL)
- Rz=12 KΩ (generally Rz=$^{1}/_{Gm2}$)
- But we have taken 12 KΩ for achieving Phase Margin of 45º.

Result

Simulated Value	Specifications
Av= 1139 v/v	Av $\geq$ 1000 v/v
BW=1.12 MHz	BW=1 MHz
GBW=1.02 GHz	**GBW=1 GHz**
Rout=9.68 KΩ	Rout=8 KΩ
Vout(dc)=0.97 V	Vout(dc)=0.9 V
IB1=70.3 µA, IB2= 493.24 µA Total Current=563.54 µA Vdd=1.8 Powe Discipation = 1.01 mW	- - - -
Phase Margin = 45º	Phase Margin = 50º
Gain Margin = 16.5 dB	-
CL=20 fF	CL=20 fF

Table

Stage 1	Stage 2
L=0.36µm	L=0.36µm
$W_{1,2}$ = 3.6µm $\frac{W}{L}$ =10	W_6=52.02µm $\frac{W}{L}$ =144.5
$gm_{1,2}$ = 0.419 mS	gm_6 = 2.59 mS
$W_{3,4}$ = 3.78µm $\frac{W}{L}$ =10 .5	W_7= 15.84 µm $\frac{W}{L}$ =44
$gm_{3,4}$ = 0.21 mS	gm_7 = 3.05 mS

Spice Error Log File

Semiconductor Device Operating Points:

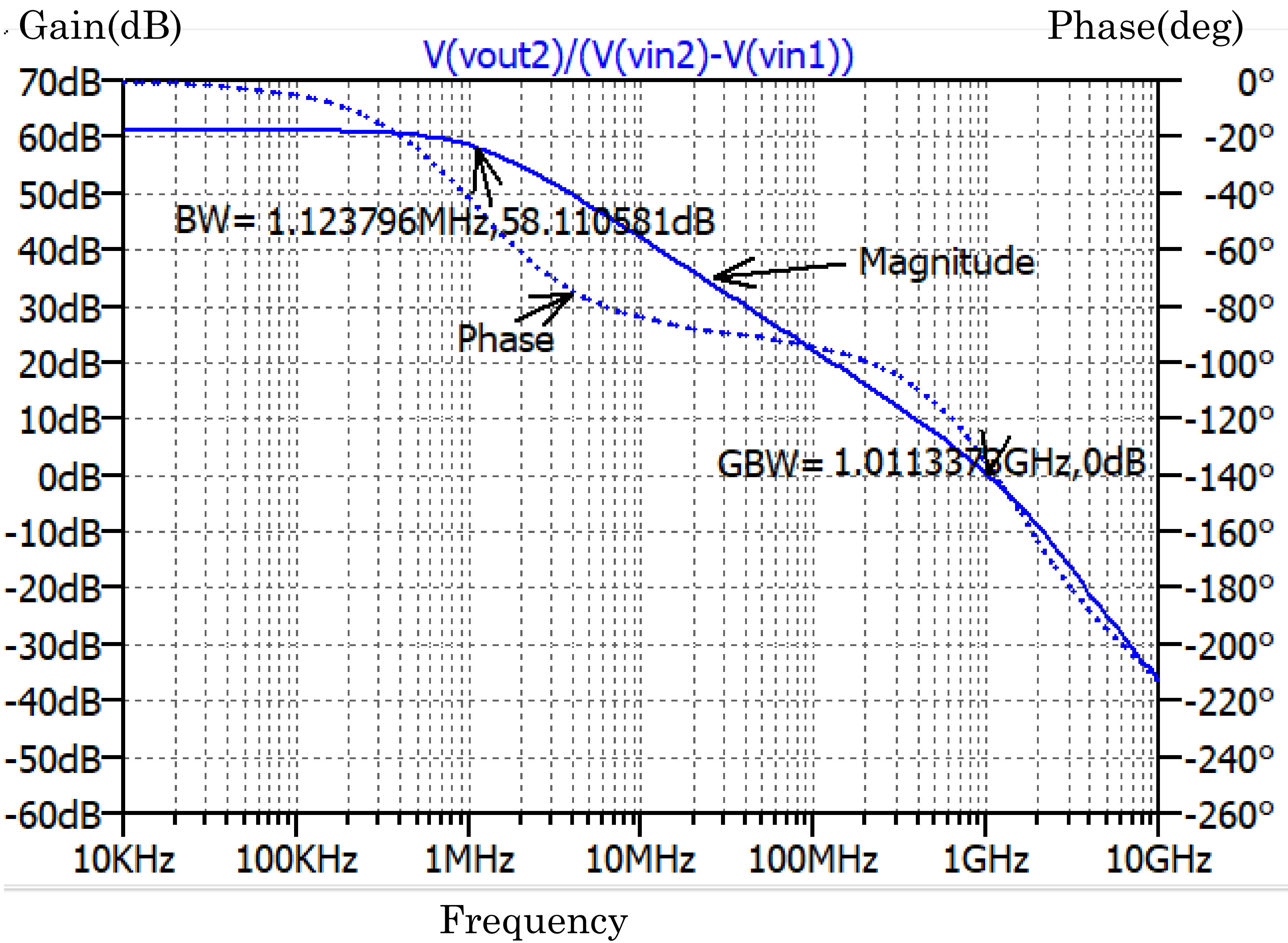
--- BSIM3 MOSFETS ---

Name:	m6	m3	m4	m7	m5	m2	m1
Model:	pch	pch	pch	nch	nch	nch	nch
Id:	-4.93e-04	-3.52e-05	-3.52e-05	4.93e-04	7.03e-05	3.52e-05	3.52e-05
Vgs:	-7.54e-01	-7.54e-01	-7.54e-01	7.63e-01	7.63e-01	7.40e-01	7.40e-01
Vds:	-8.26e-01	-7.54e-01	-7.54e-01	9.74e-01	4.50e-01	5.96e-01	5.96e-01
Vbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	-4.50e-01	-4.50e-01
Vth:	-4.50e-01	-4.48e-01	-4.48e-01	4.58e-01	4.62e-01	5.82e-01	5.82e-01
Vdsat:	-2.55e-01	-2.50e-01	-2.50e-01	2.19e-01	2.15e-01	1.38e-01	1.38e-01
Gm:	2.95e-03	2.11e-04	2.11e-04	3.05e-03	4.40e-04	4.19e-04	4.19e-04
Gds:	6.24e-05	4.69e-06	4.69e-06	4.09e-05	1.09e-05	5.73e-06	5.73e-06
Gmb	9.53e-04	6.66e-05	6.66e-05	7.91e-04	1.13e-04	9.52e-05	9.52e-05
Cbd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgsov:	3.42e-14	2.48e-15	2.48e-15	7.78e-15	1.15e-15	1.77e-15	1.77e-15
Cgdov:	3.42e-14	2.48e-15	2.48e-15	7.78e-15	1.15e-15	1.77e-15	1.77e-15
Cgbov:	2.98e-19	2.98e-19	2.98e-19	3.28e-19	3.28e-19	3.28e-19	3.28e-19
dQgdVgb:	1.78e-13	1.30e-14	1.30e-14	5.26e-14	7.80e-15	1.18e-14	1.18e-14
dQgdVdb:	-3.42e-14	-2.48e-15	-2.48e-15	-7.58e-15	-1.13e-15	-1.72e-15	-1.72e-15
dQgdVsb:	-1.38e-13	-1.01e-14	-1.01e-14	-4.27e-14	-6.32e-15	-9.53e-15	-9.53e-15
dQddVgb:	-3.43e-14	-2.50e-15	-2.50e-15	-7.81e-15	-1.19e-15	-1.78e-15	-1.78e-15
dQddVdb:	3.43e-14	2.49e-15	2.49e-15	7.79e-15	1.18e-15	1.78e-15	1.78e-15
dQddVsb:	1.04e-16	8.68e-18	8.68e-18	2.36e-17	1.14e-17	1.33e-17	1.33e-17
dQbdVgb:	-2.25e-14	-1.67e-15	-1.67e-15	-7.92e-15	-1.17e-15	-1.67e-15	-1.67e-15
dQbdVdb:	-2.52e-17	-2.70e-18	-2.70e-18	1.63e-17	-9.51e-18	7.38e-19	7.38e-19
dQbdVsb:	-1.10e-14	-7.45e-16	-7.45e-16	-3.25e-15	-4.67e-16	-4.71e-16	-4.71e-16

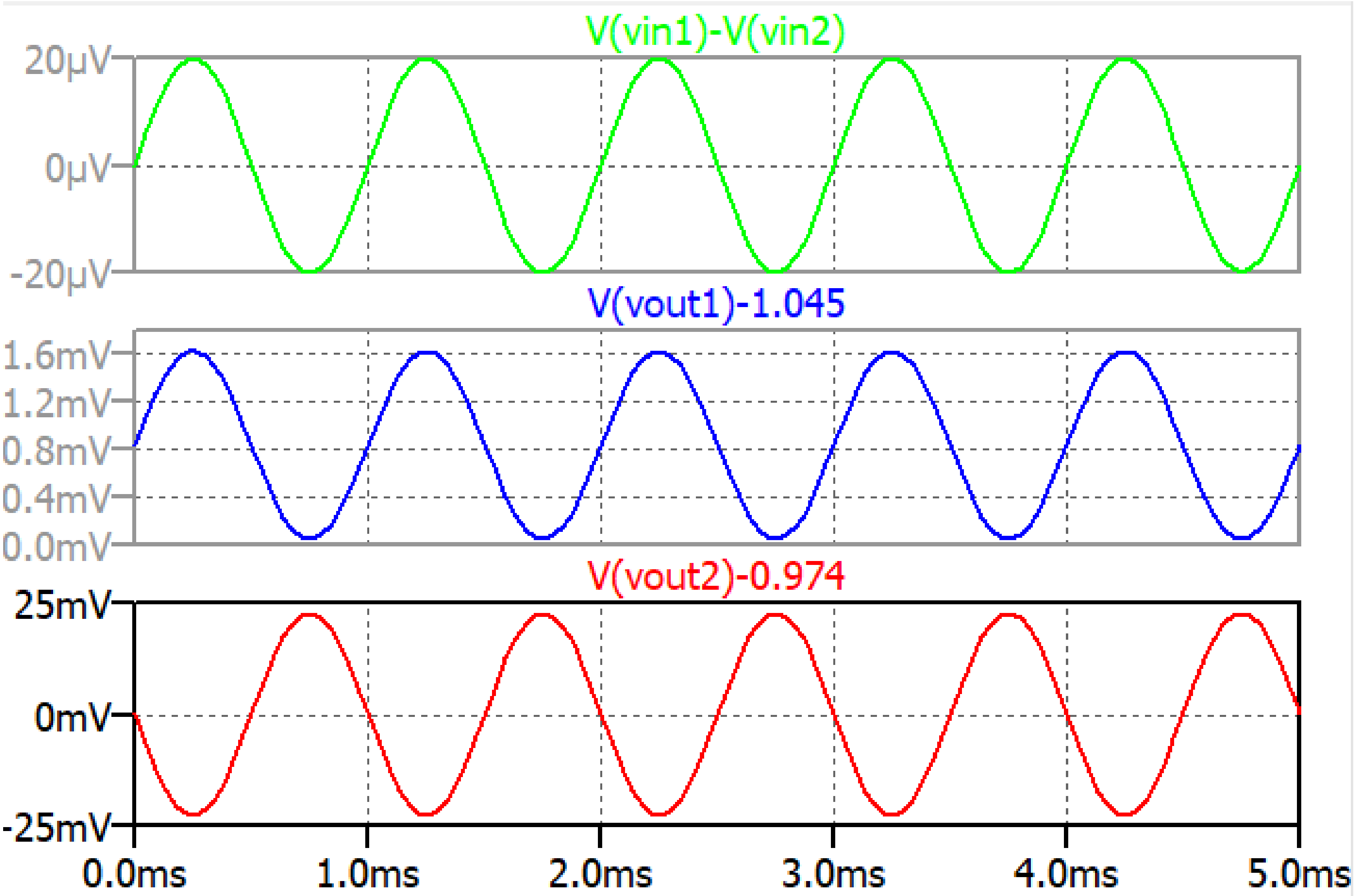
--- Transfer Function ---

Transfer_function:	-1139.14	transfer	
vin1#Input_impedance:	1e+020	impedance	
output_impedance_at_V(vout2):		9688.45	impedance

Frequency Response



Transient Analysis



Vin1-Vin2(pp)=40 µV   Vout2(pp)=45.54 mV   Gain=1138.5

Learn in this Internship

- Learn gmid methodology for designing Amplifier.
- How to Extract different charts used in gmid method
- Designed using ADT Toolbox
- Able to Design Amplifier with given Specification
- Completed project: Design of two Stage op-amp with gain bandwidth product of 1Ghz.

References

- IEEE.ORG
- The Design of Two-Stage Miller Op-Amp: The Final Verdict! | Dr. Hesham Omran, Youtube Link: https://youtu.be/PT31xAEd_v4

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- Afzal Malik
- Mohsin Hussain

&

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Thank you