Project Report Submission

For

Digital IC Design

(*ELE4620***)**

Title: Design a Full adder using CMOS transistor

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Submitted To

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Abstract

This study presents the design and implementation of a Full Adder circuit using CMOS transistor technology. The Full Adder is a fundamental component in digital circuits, crucial for arithmetic and logical operations. Leveraging CMOS technology, this research focuses on optimizing the circuit's performance metrics, such as speed, power efficiency, and area utilization. The Full Adder design is realized through the integration of complementary Metal-Oxide-Semiconductor (CMOS) transistors, utilizing their inherent advantages in terms of low power consumption, high noise immunity, and compatibility with integrated circuit manufacturing processes. Simulation and analysis are conducted using Cadence Virtuoso tools to assess the circuit's functionality, performance parameters, and scalability across different process nodes. The findings and insights from this study contribute to advancing the understanding and application of CMOS-based Full Adder circuits in modern digital systems.

Design step

Step 1: Design half Adder using CMOS transistor.

Figure 1 shows the schematic of half adder comprises XOR, Inverter, AND gate

Sum = A ^ B ---(1)
Carry = A . B ----(2)
Where A & B are inputs and sum & carry are outputs

Truth Table for Half Adder

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	1	1

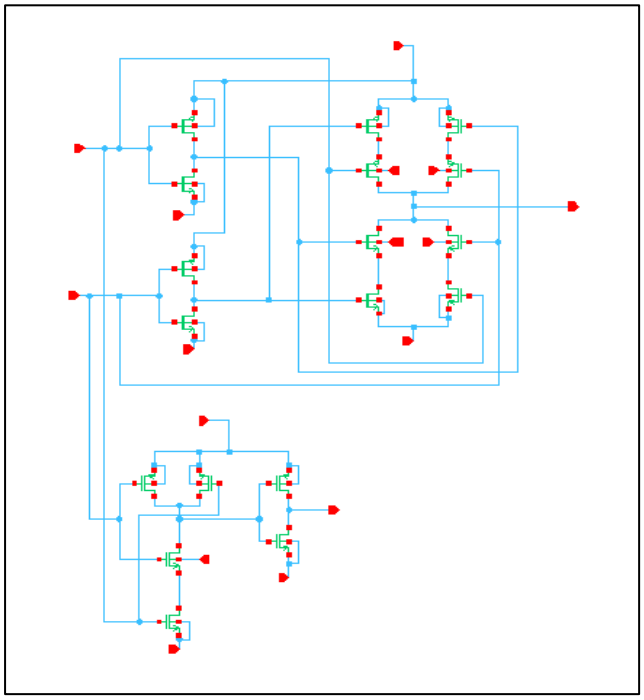


Figure 1 Half Adder

Step 2: Half adder Layout

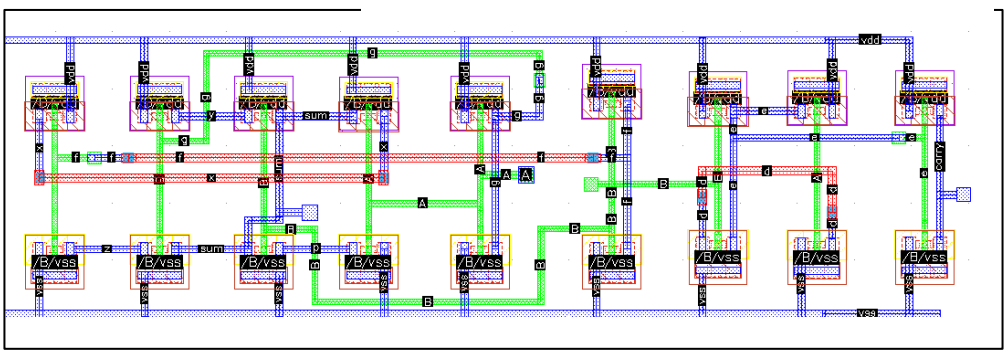


Figure 2 Half adder layout

Step 3: DRC Check (No DRC found)

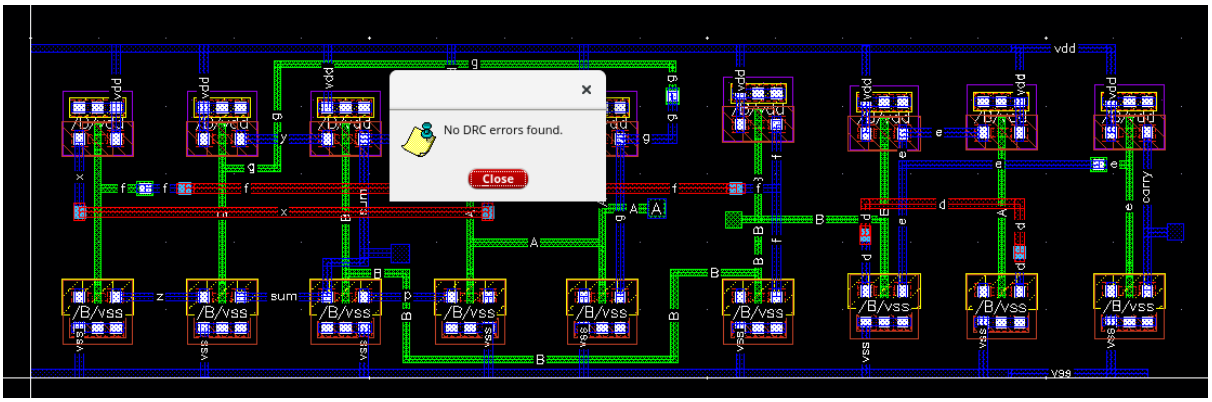


Figure 3 DRC Checking

Step 3: Half adder av extracted

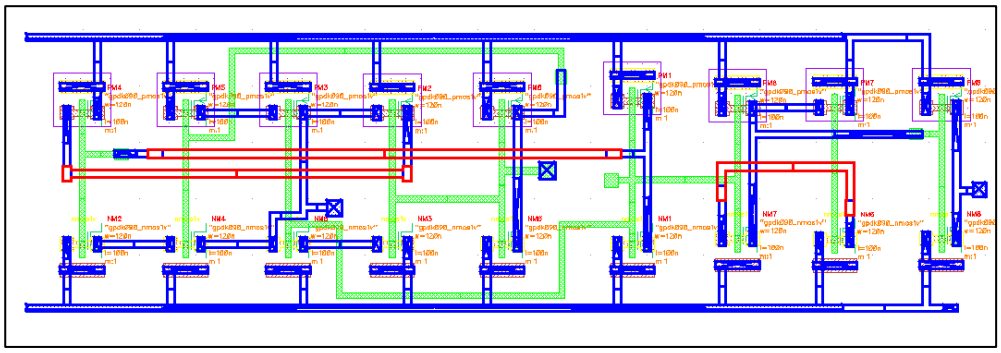


Figure 4 av-extracte view

Step 4: Data stream (GDS file)

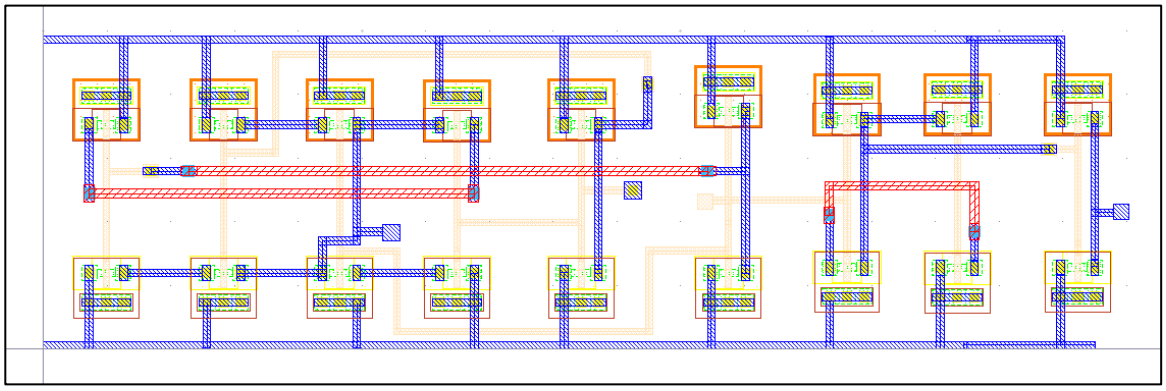


Figure 5 GDS extracted view

Step 5: Half Adder Testbench

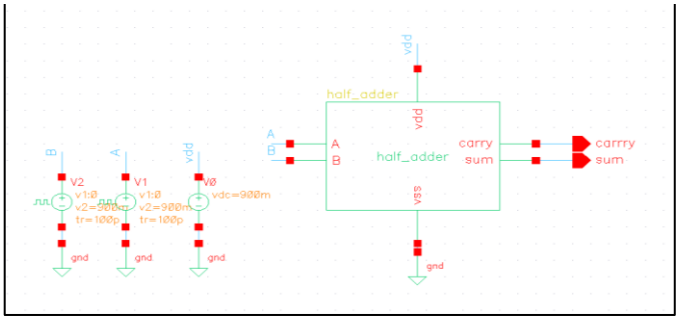


Figure 6 Half Adde Testbench

Step 6: Half Adder Waveform

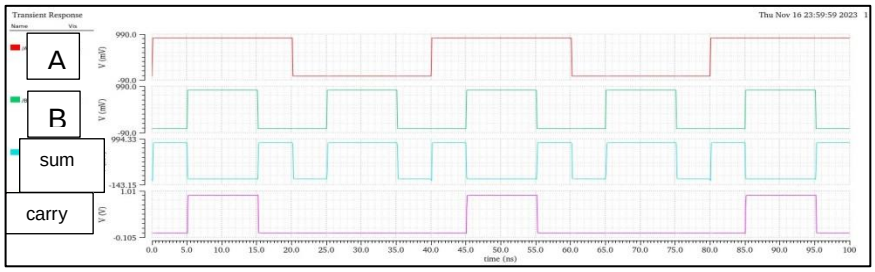


Figure 7 Half Adder Waveform

Step 7: OR Gate Schematic

OR gate Truth table

Y = A or B

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

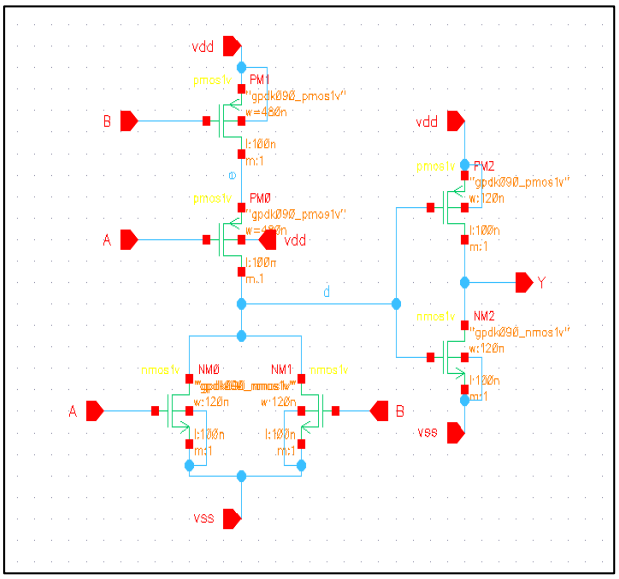


Figure 8 OR Gate Schematic

Step 8: Half Adder Layout

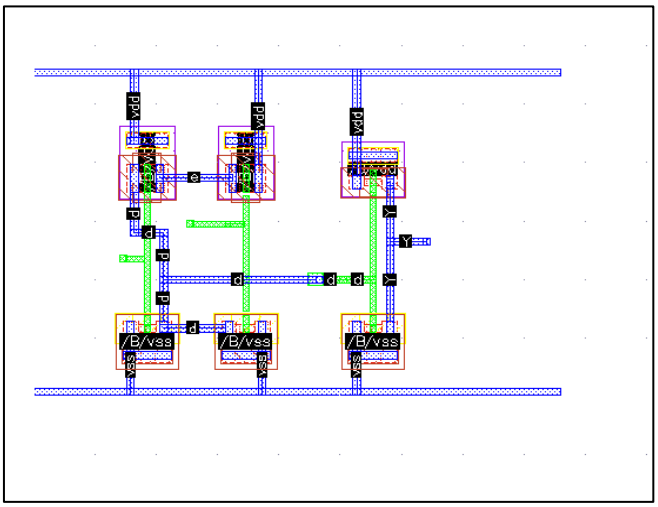


Figure 9 OR Gate Layout

Step 9: DRC Check

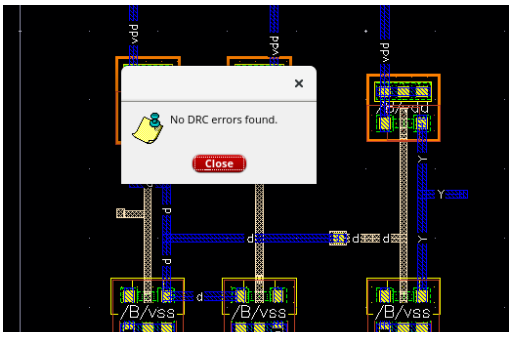


Figure 10 RDC View

Step 10: Data stram (GDS file)

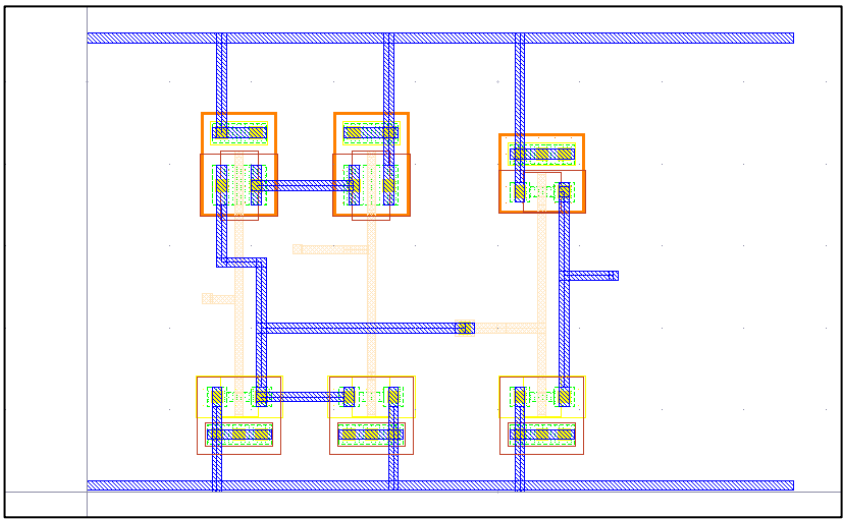


Figure 11 GDS View

Step 11: OR Gate Symbol

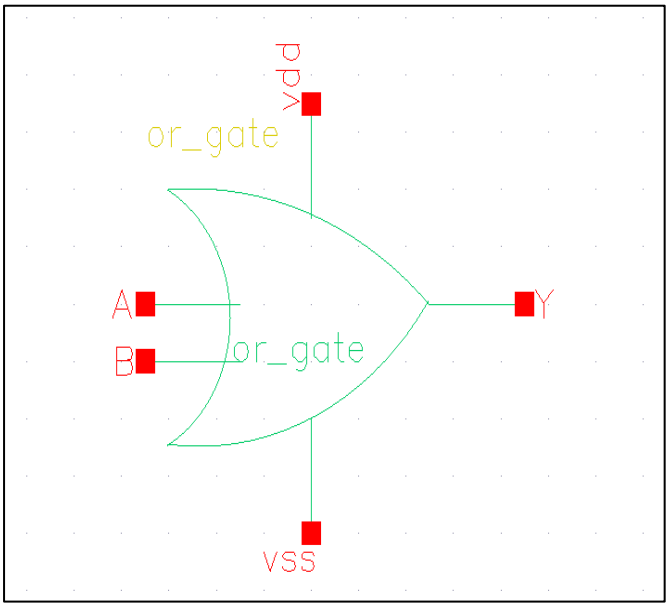


Figure 12 OR Gate symbol

Step 12: OR Gate Testbench

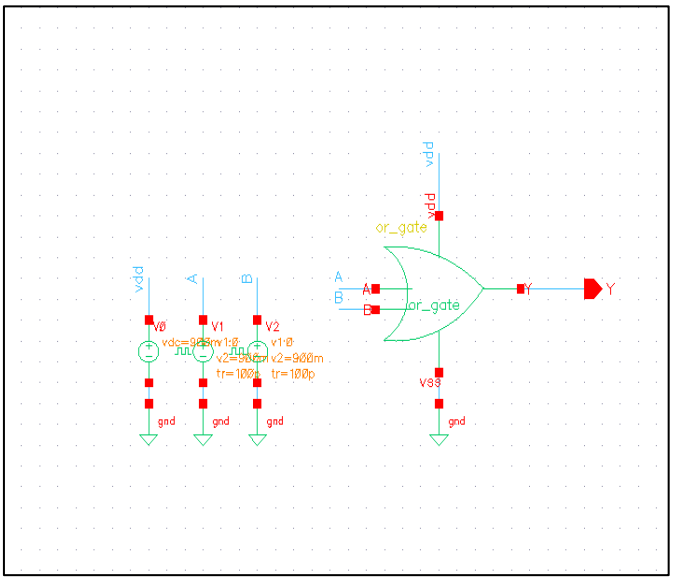


Figure 13 OR Gate Testbench

Step 13: OR Gate Waveform

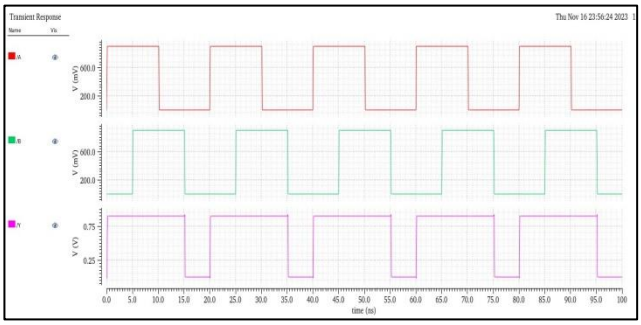


Figure 14 OR Gate waveform

Step 14: Full Adder Bock Diagram using HA & AND gate

Sum = A ^ B ^ cin
Carry = A.B + B.Cin + A.Cin

A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

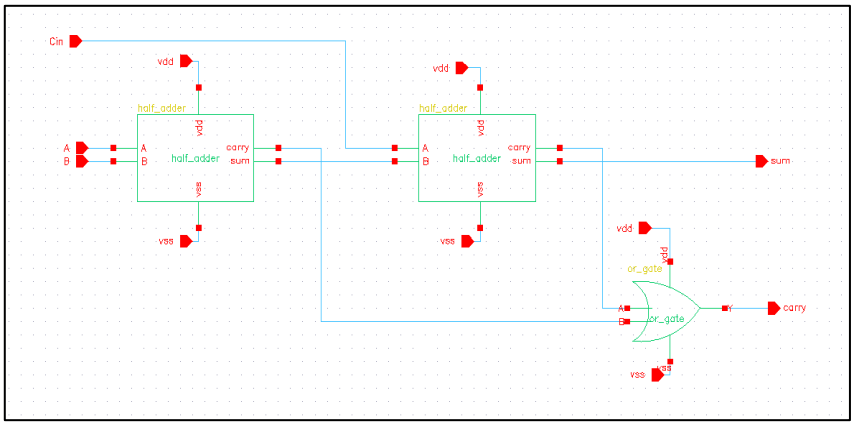


Figure 15 Full Adder Block Diagram

Step 15: Full Adder layout

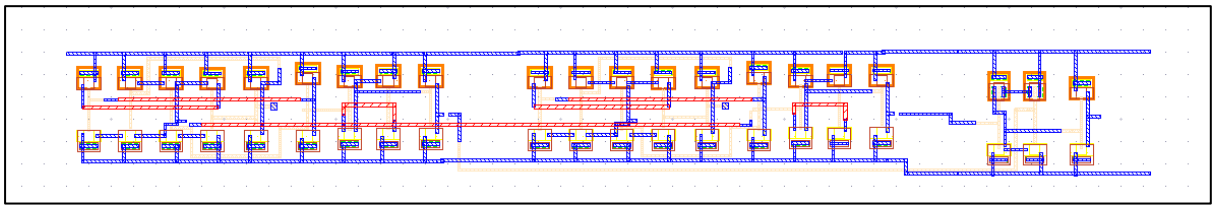


Figure 16 Full Adder Layout

Step 16: Full Adder Data stream (GDS)

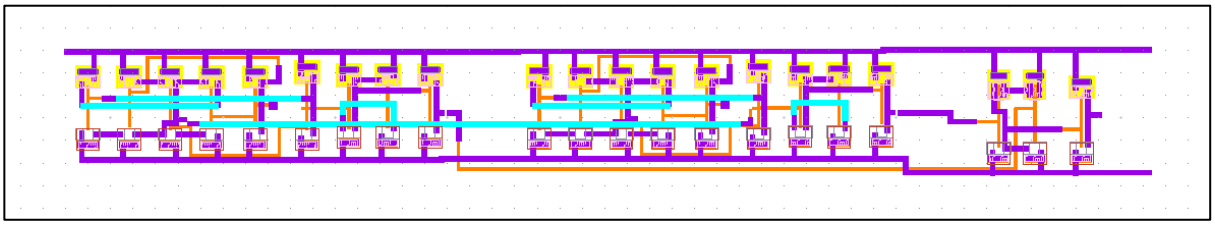


Figure 17 Full Adder GDS View

Step 17: Full Adder Testbench

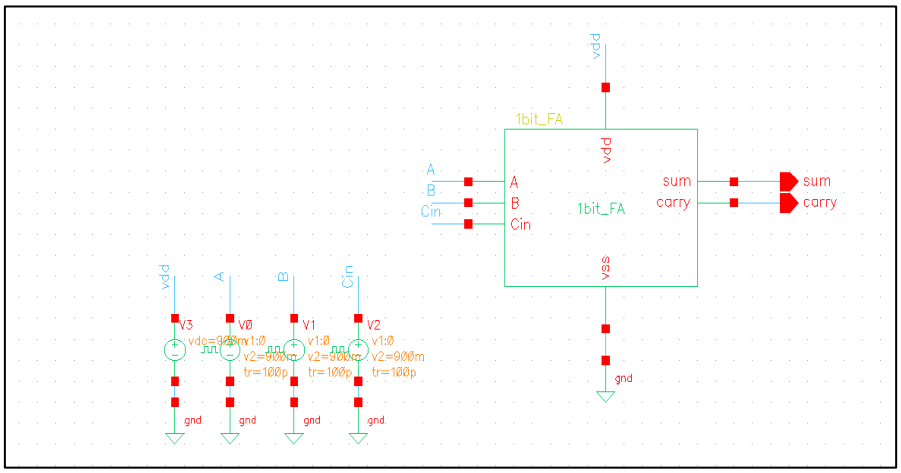


Figure 18 Full Adder Testbench

Step 18: Full Adder Waveform

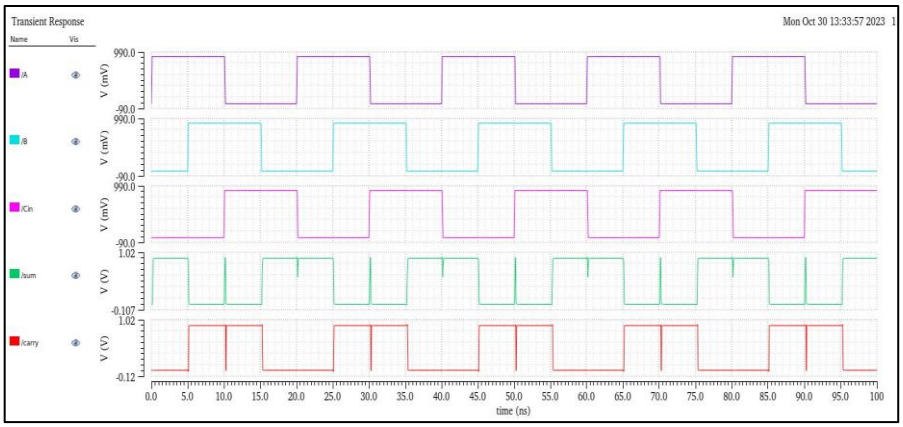
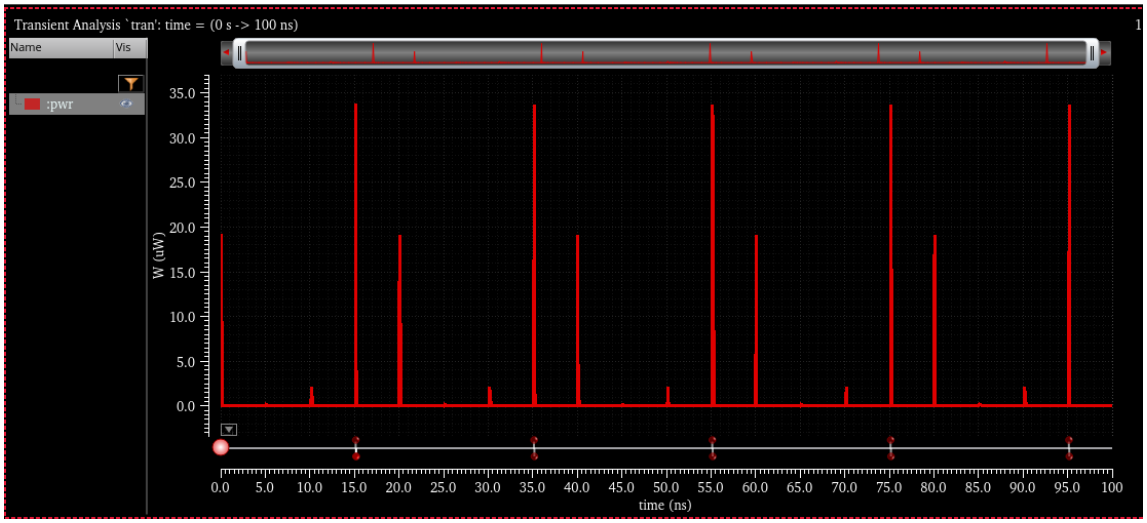


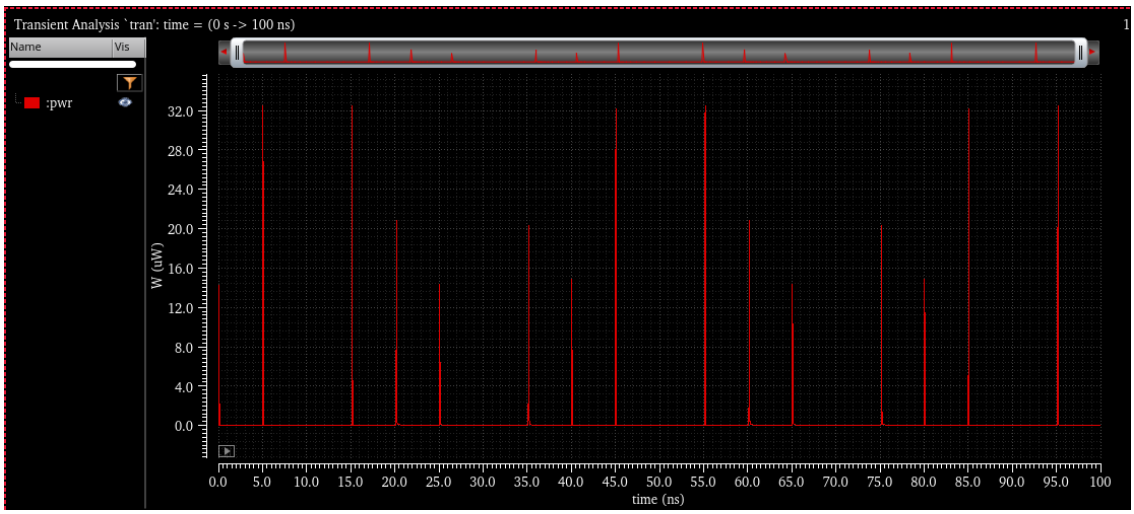
Figure 19 Ful Adde Waveform

Static and Dynamic Power

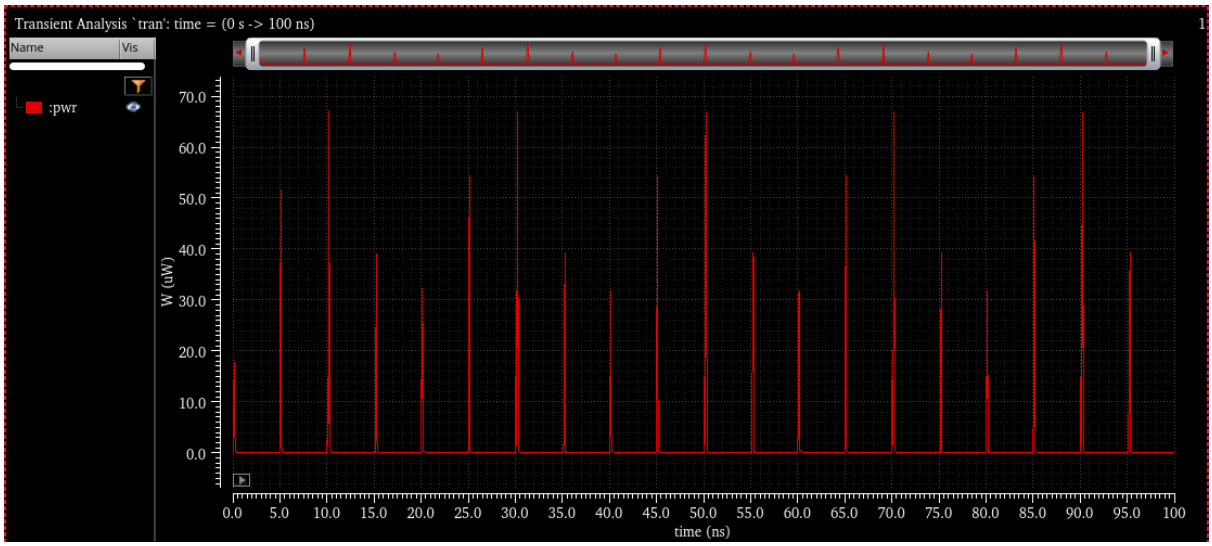
1. OR gate



2. Half adder



3. Full Adder



Delay Calculation

1. Delay between input A and sum for full adder is 158.9E-12 sec

Discussion

We've successfully implemented the schematic and layout designs for a half adder, an AND gate, and a full adder. Additionally, we verified the waveform output against the truth table. Following this, we conducted checks for Design Rule Checking (DRC) errors and extracted

RC parameters, generating a data stream. We performed calculations for both Static and Dynamic power, alongside measuring the delay for one input of the full adder