UNIT-VIII

COMPUTER ORGANIZATION ARCHITECTURE

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NOTES

CHAPTER 1

CONTROL UNIT, MACHINE INSTRUCTION & ADDRESSING MODES

OBJECTIVE QUESTIONS

1. TRAP

When an interrupt occur, an operating system?

(a) Ignores the interrupt

(b) Always change state of the interrupted process to blocked and schedules another process

(c) Always resumes execution of the interrupted process after process the current interrupt

(d) May change state of interrupted process to blocked & schedule same process

2. A processor needs software interrupt :

(a) Test the interrupt system of the processor

(b) Implements co-rottenness

(c) Obtained system services which need execution of privileged instruction

(d) Return from the sub-routene

3. A CPU generally handles an interrupt at by executing an interrupt service routene.

(a) As soon as interrupt rase

(b) By checking the interrupt register after finishing the execution of the current instruction

(c) By checking the interrupt register at the end of fetch cycle.

(d) By checking the interrupt register after regular time interval

4. The micro instruction store in the control memory of a processor have a width of 26 bits each micro instruction is divided into 3 fields

$field_1$ = micro operation of 13 bits

Assume that there are 8 flags. How many bits are there is in x field and y fields and what is the size of control memory in no of words.

(a) 10, 3, 1024 (b) 8, 5, 256

(c) 5, 8, 2048 (d) 10, 3, 512

5. Which of the following instruction is arithmetic.

(a) LDA 2000H (b) JC

(c) XOR (d) INR

6. Which of the following device should get higher priority in assigning interrupts ?

(a) Hard Disk (b) Printer

(c) Key board (d) Floppy disk

7. A CPU generally handles an interrupt by executing an interrupt service routine

(a) As soon as interrupt is raised.

(b) By checking interrupt register at the end of fetch cycle

(c) By checking the interrupt after finishing the execution of current instruction

(d) By checking the interrupt register at fixed time intervals

8. Which of the following statements is true?

(a) ROM is a read/write memory

(b) PC points to last instruction that was executed

(c) Stack works on the principle of LIFO

(d) All instructions affect the flag

9. An instruction used to set carry flag in computer can be classified as

(a) data transfer (b) process control

(c) logical (d) program control

10. Adding a new instruction is easy if CPU has

(a) Hardwired control unit

(b) Microprogrammed control unit

(c) Both a and b

(d) None of the above

11. The computation type instructions of a stack organized CPU was uses

(a) Two address instructions format

(b) One address instruction format

(c) Three address instruction format

(d) Zero address instruction format

12. If '1' is added for all bits in a register, the operation is known as

(a) Incrementing (b) Decrementing

(c) complimenting (d) Addition

13. Which of the following register is used for relocation of a program?

(a) Accumulator (b) stack pointer

(c) Program counter (d) Base registers

14. When a computer is first turned on and restarted a special type of absolute loader is executed called a

(a) Compile and go loader

(b) Boot loader

(c) Boot strap loader

(d) Relating loader

15. Which of the following may not definitely occur in an instruction cycle?

1. Fetch – cycle
2. Execution – cycle
3. Indirect cycle

(a) 1 only (b) 3 only

(c) 1 and 2 only (d) 2 and 3 only

16. In relative addressing mode the contents of which register is added to the address part of instruction to obtain effective address

(a) Program counter (b) Base register

(c) Index register (d) Stack pointer

17. Which is not an instruction code format of a basic computer

(a) Accumulator – reference instruction

(b) Memory – reference instruction

(c) Register – reference instruction

(d) Input – Output instruction

18. The most relevant addressing mode to write position – independent code is :

(a) Direct mode (b) Indirect mode

(c) Relative mode (d) Indexed mode

19. Which of the following addressing modes permits relocation without any change what so ever in the code?

(a) Indirect addressing

(b) Indexed addressing

(c) Base register addressing

(d) PC relative addressing

20. The number of memory references required for CPU to execute immediate address instructions (except Fetching)

(a) Zero (b) One

(c) Two (d) Three

21. A large – word – size computer

(a) can store smaller amount of data

(b) is normally used because it is bigger in size

(c) executes programs at a faster rate

(d) executes programs at a slower rate

22. The register which holds the address of the location to or from which data are to be transferred is known as

(a) index register

(b) instruction register

(c) memory address register

(d) memory data register

23. What are the states of the auxiliary carry (AC) and carry flag (CY) after executing the following 8085 programming?

```
MVI H,    5DH
MBI L,    6BH
MOV A,    H
ADD L
```

(a) AC = 0 and CY = 0

(b) AC = 1 and CY = 0

(c) AC = 1 and CY = 1

(d) AC = 0 and CY = 1

24. The most appropriate matching for the following pairs is-

Column-1:

X: Indirect addressing

Y: Immediate addressing

Z: Auto decrement addressing

Column-2:

1. Loops
2. Pointers
3. Constants

(a) X-3, Y-2, Z-1 (b) X-1, Y-3, Z-2

(c) X-2, Y-3, Z-1 (d) X-3, Y-1, Z-2

25. In the absolute addressing mode,

(a) The operand is inside the instruction

(b) The address of the operand is inside the instruction

(c) The register containing the address of the operand is specified inside the instruction

(d) The location of the operand is implicit

26. Which of the following addressing modes are suitable for program relocation at run time?

1. Absolute addressing
2. Base addressing
3. Relative addressing
4. Indirect addressing

(a) 1 and 4 (b) 1 and 2

(c) 2 and 3 (d) 1, 2 and 4

27. What is the most appropriate match for the items in the first column with the items in the second column-

Column-1:

X: Indirect addressing

Y: Indexed addressing

Z: Base register addressing

Column-2:

1. Array implementation
2. Writing relocatable code
3. Passing array as parameter

(a) X-3, Y-1, Z-2 (b) X-2, Y-3, Z-1

(c) X-3, Y-2, Z-1 (d) X-1, Y-3, Z-2

28. Which of the following addressing modes permits relocation without any change whatsoever in the code?

(a) Indirect addressing

(b) Indexed addressing

(c) Base register addressing

(d) PC relative addressing

29. Consider a three word machine instruction-

```
ADD A[R0], @B
```

The first operand (destination) "A[R0]" uses indexed addressing mode with R0 as the index register. The second operand operand (source)

"@B" uses indirect addressing mode. A and B are memory addresses residing at the second and the third words, respectively. The first word of the instruction specifies the opcode, the index register designation and the source and destination addressing modes. During execution of ADD instruction, the two operands are added and stored in the destination (first operand).

The number of memory cycles needed during the execution cycle of the instruction is-

(a) 3 (b) 4

(c) 5 (d) 6

30. Consider a hypothetical processor with an instruction of type LW R1, 20(R2), which during execution reads a 32-bit word from memory and stores it in a 32-bit register R_1. The effective address of the memory location is obtained by the addition of a constant 20 and the contents of register R_2. Which of the following best reflects the addressing mode implemented by this instruction for operand in memory?

(a) Immediate Addressing

(b) Register Addressing

(c) Register Indirect Scaled Addressing

(d) Base Indexed Addressing

31. In the case of, Zero-address instruction method the operands are stored in _____

(a) Registers (b) Accumulators

(c) Push down stack (d) Cache

32. The addressing mode which makes use of in-direction pointers is _____

(a) Indirect addressing mode

(b) Index addressing mode

(c) Relative addressing mode

(d) Offset addressing mode

33. In the following indexed addressing mode instruction, MOV 5(R1),LOC the effective address is _____

(a) EA = 5+R1 (b) EA = R1

(c) EA = [R1]. (d) EA = 5+[R1].

34. The addressing mode/s, which uses the PC instead of a general purpose register is _____

(a) Indexed with offset

(b) Relative

(c) direct

(d) both Indexed with offset and direct

35. When we use auto increment or auto decrements, which of the following is/are true?

1. In both, the address is used to retrieve the operand and then the address gets altered
2. In auto increment, the operand is retrieved first and then the address altered
3. Both of them can be used on general purpose registers as well as memory locations

(a) 1, 2, 3 (b) 2

(c) 1, 3 (d) 2, 3

36. The addressing mode, where you directly specify the operand value is _____

(a) Immediate (b) Direct

(c) Definite (d) Relative

37. The effective address of the following instruction is MUL 5(R1,R2).

(a) 5+R1+R2 (b) 5+(R1*R2)

(c) 5+[R1]+[R2]. (d) 5*([R1]+[R2])

38. _____ addressing mode is most suitable to change the normal sequence of execution of instructions.

(a) Relative

(b) Indirect

(c) Index with Offset

(d) Immediate

39. When an interrupt occurs, an operating system

(a) ignores the interrupt

(b) always changes state of interrupted process after processing the interrupt

(c) always resumes execution of interrupted process after processing the interrupt

(d) may change state of interrupted process to 'blocked' and schedule another process

40. Arrange the following configuration for CPU in decreasing order of operating speeds: Hardwired control, vertical micro-programming, horizontal micro-programming.

(a) Hardwired control, vertical micro programming, horizontal micro programming

(b) Hardwired control, horizontal micro programming, vertical microprogramming

(c) Horizontal micro programming, vertical micro programming, Hardwired control

(d) Vertical micro programming, horizontal micro programming, hardwired controls

41. A processor needs software interrupt to

(a) test the interrupt system of the processor

(b) implement co-routines

(c) obtain system services which need execution of privileged instructions

(d) return from subroutines

42. Horizontal microprogramming

(a) does not require use of signal decoders

(b) results in larger sized microinstructions than vertical microprogramming

(c) uses one bit for each control signal

(d) All of the above

43. What is the minimum size of ROM required to store the complete truth table of an 8-bit × 8-bit multiplier ?

(a) 32 K × 16 bits (b) 64 K × 16 bits

(c) 16 K × 32 bits (d) 64 K × 32 bits

44. Which one of the following is true for a CPU having a single interrupt request line and a single interrupt grant line?

(a) Neither vectored interrupt nor multiple interrupting devices are possible

(b) Vectored interrupts are not possible but multiple interrupting devices are possible

(c) Vectored interrupts and multiple interrupting devices are both possible

(d) Vectored interrupt is possible but multiple interrupting devices are not possible

45. Consider a CPU where all the instructions require 7 clock cycles to complete execution. There are 140 instructions in the instruction set. It is found that 125 control signals are needed to be generated by the control unit. While designing the horizontal micro-programmed control unit, single address field format is used for branch control logic. What is the minimum size of the control word and control address register?

(a) 125, 7 (b) 125, 10

(c) 135, 9 (d) 135, 10

46. The use of multiple register windows with overlap causes a reduction in the number of memory accesses for

1. function locals and parameters
2. register saves and restores
3. instruction fetches

(a) 1 only (b) 2 only

(c) 3 only (d) 1, 2 and 3

47. A CPU generally handles an interrupt by executing an interrupt service routine

(a) as soon as an interrupt is raised

(b) by checking the interrupt register at the end of fetch cycle

(c) by checking the interrupt register after finishing the execution of the current instruction

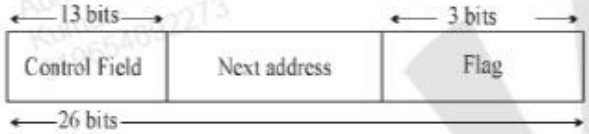
(d) by checking the interrupt register at fixed time intervals

❑❑❑

Answer Key

1. *Ans. (c)*
2. *Ans. (c)*

   A processor needs software interrupt to obtain system serivices means ISR (Interrupt service routen), which is needed for execution of interrupt or privilleged instruction.
3. *Ans. (b)*
4. *Ans. (a)*



   So next address field bits = 26 – (13 + 3) = 10

   Then total no of words = 2^{10} = 1024 words memory.
5. *Ans. (a)*
6. *Ans. (c)*
7. *Ans. (c)*
8. *Ans. (c)*
9. *Ans. (b)*
10. *Ans. (b)*
11. *Ans. (d)*
12. *Ans. (b)*
13. *Ans. (d)*
14. *Ans. (c)*
15. *Ans. (b)*
16. *Ans. (a)*
17. *Ans. (a)*
18. *Ans. (c)*
19. *Ans. (c)*
20. *Ans. (a)*
21. *Ans. (c)*
22. *Ans. (c)*
23. *Ans. (b)*
24. *Ans. (c)*
25. *Ans. (b)*
26. *Ans. (c)*
27. *Ans. (a)*
28. *Ans. (c)*
29. *Ans. (b)*
30. *Ans. (d)*
31. *Ans. (c)*
32. *Ans. (a)*
33. *Ans. (d)*
34. *Ans. (b)*
35. *Ans. (d)*
36. *Ans. (a)*
37. *Ans. (c)*
38. *Ans. (a)*
39. *Ans. (d)*

    An interrupt is a signal from a device attached to a computer or from a program within the computer that causes the main program that operates the computer to stop and figure out what to do next. After the interrupt signal is sensed, it may change state of interrupted process to 'blocked' and schedule another process.
40. *Ans. (b)*

    Configurations for CPU in decreasing order of operating speeds:

    Hardwired control > Horizontal micro-programming > Vertical micro-programming
41. *Ans. (c)*

    A processor needs software interrupt to obtain system services which need execution of privileged instructions.
42. *Ans. (d)*

    Features of horizontal micro-programming are:

    (a) doesn't require use of signal decoders

    (b) results in larger sized micro-instructions than vertical micro-programming

    (c) uses one bit for each control signal.

43. ***Ans. (b)***

Multiplying two 8 bit numbers will give result in maximum 16 bits.

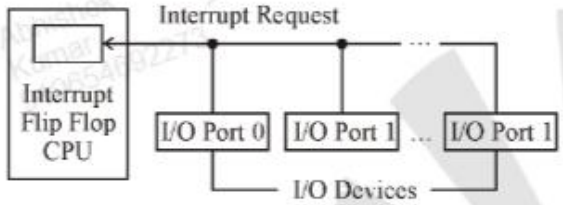
Total number of multiplications possible

$= 2^8 \times 2^8 = 64$ K.

Hence space required = 64 K × 16 bits.

44. ***Ans. (b)***

Consider the following figure



In single line interrupt system contains a single interrupt request line and a interrupt grant line. In this system it may be possible that more than one output devices request interrupt at the same time for example I/O port 0 to I/O port n may request an interrupt at the same time but only one request will be granted according to priority. So, In single interrupt system vectored interrupts are not possible but multiple interrupting devices are possible.

45. ***Ans. (b)***

Since it uses horizontal micro-programmed that requires 1 bit/control signal.

For 125 control signal we need 125 bit.

Total number of micro operation instructions = 140 * 7 = 980.

It requires 10 bit.

46. ***Ans. (c)***

The use of multiple register windows with overlap causes a reduction in the number of memory access for instruction fetches only.

47. ***Ans. (c)***

Interrupt handled by execution of interrupt service routine. It checks interrupt register after finishing the execution of current instruction.

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CHAPTER 2

PIPELINING

OBJECTIVE QUESTIONS

1. Comparing the time T_1 taken for a single instruction on a pipelined CPU with time T_2 taken on a non – pipelined but identical CPU, we can say that
   (a) $T_1 \leq T_2$
   (b) $T_1 \geq T_2$
   (c) $T_1 < T_2$
   (d) T_1, T_2 plus time taken for one instruction fetch cycle

2. Assuming that there are no branch instructions or data hazards, the number of cycles required to process 100 instructions through a 4-stage pipeline is
   (a) 102 (b) 103
   (c) 100 (d) 300

3. A processor has average instruction execution time as 2μs. The speed of the processor is
   (a) 1.0 MIPS (b) 2.0 MIPS
   (c) 0.5 MIPS (d) 0.75 MIPS

4. A non pipeline system takes 50 ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10 ns. The speed up ratio of the pipeline for 100 tasks, is
   (a) 2.76 (b) 3.76
   (c) 4.76 (d) 5.76

5. The performance of a pipelined processor suffers if
   (a) The pipeline stages have different delays
   (b) Consecutive instructions are dependant on each other
   (c) The pipeline stages share hard ware resources
   (d) All the above

6. Suppose a computer spends 90 percent of its time handling a particular type of computation when running a given program and its manufactures makes a change that improve its performance on that type of computation by a factor of 10. If the program originally took 1000 seconds to execute, what will its execution time be after the change?
   (a) 18 sec (b) 20 sec
   (c) 19 sec (d) 21 sec

7. A computer architect is designing the memory system for the next version of a processor. If the current version of the processor spends 40 percent of its time processing memory references, by how much must the architect speed up the memory system to achieve an overall speed up of 1.2?
   (a) 1.51 (b) 1.71
   (c) 1.61 (d) None of the above

8. In a pipelined RISC computer where all arithmetic instructions have the same CPI (cycles per instruction), which of the following actions would improve the execution time of a typical program?
   1. Increasing the clock cycle rate
   2. Disallowing any forwarding in the pipeline.
   3. Doubling the size of the instruction cache and the data cache without changing the clock cycle time
   (a) 1 only (b) 3 only
   (c) 2 only (d) 1 and 3 only

9. In a pipeline, the time of each sub-operation is given below

IF	ID	ALU	MEM	WB
150ns	50ns	200ns	150ns	50ns

the pipeline has 5 stages and executes 60 tasks in sequence. What is the speedup ratio?
   (a) 2.5 (b) 3.3
   (c) 2.9 (d) 3.7

10. Consider the following instruction sequence in a single-issue in order 5 stage pipeline (IF, ID, EX, MEM and WB)

First instruction to enter the pipeline

AD R_1 R_2 R_3
SUB R_2 R_3 R_1

Last instruction to enter the pipeline

MUL R_1 R_2 R_3

How many data hazards does the ID stage need to detect for this instruction sequence?

(a) 1 (b) 3
(c) 2 (d) 4

11. A four stage pipeline has the stage delays as 150, 120, 160 and 140 ns respectively. Registers are used between the stages and have a delay of 5 ns each. Assuming constant clocking rate, the total time taken to process 1000 data items on the pipeline will be-

(a) 120.4 microseconds
(b) 160.5 microseconds
(c) 165.5 microseconds
(d) 590.0 microseconds

12. Consider a non-pipelined processor with a clock rate of 2.5 gigahertz and average cycles per instruction of 4. The same processor is upgraded to a pipelined processor with five stages but due to the internal pipeline delay, the clock speed is reduced to 2 gigahertz. Assume there are no stalls in the pipeline. The speed up achieved in this pipelined processor is-

(a) 3.2 (b) 3.0
(c) 2.2 (c) 2.0

13. A non-pipelined single cycle processor operating at 100 MHz is converted into a synchronous pipelined processor with five stages requiring 2.5 ns, 1.5 ns, 2 ns, 1.5 ns and 2.5 ns respectively. The delay of the latches is 0.5 sec.

The speed up of the pipeline processor for a large number of instructions is-

(a) 4.5 (b) 4.0
(c) 3.33 (d) 3.0

14. We have 2 designs D1 and D2 for a synchronous pipeline processor. D1 has 5 stage pipeline with execution time of 3 ns, 2 ns, 4 ns, 2 ns and 3 ns. While the design D2 has 8 pipeline stages each with 2 ns execution time. How much time can be saved using design D2 over design D1 for executing 100 instructions?

(a) 214 ns (b) 202 ns
(c) 86 ns (d) 200 ns

15. The no of clock cycles are required to execute the loop

for (i = 1; i ≤ 2; i + t)

{

I_1 ;
I_2 ;
I_3 ;
I_4 ;

}

	S_1	S_2	S_3	S_4
I_1	2	1	1	1
I_2	1	3	2	2
I_3	2	1	1	3
I_4	1	2	2	2

(a) 16 (b) 23
(c) 26 (d) 30

16. Consider the following procedures. Assume that the pipeline registers have zero latency.

P1 : 4 stage pipeline with stage latencies 1 ns, 2 ns, 2 ns, 1 ns

P2 : 4 stage pipeline with stage latencies 1 ns, 1.5 ns, 1.5 ns, 1.5 ns

P3 : 5 stage pipeline with stage latencies 0.5 ns, 1 ns, 1 ns, 0.6 ns, 1 ns

P4 : 5 stage pipeline with stage latencies 0.5 ns, 0.5 ns, 1 ns, 1 ns, 1.1 ns Which procedure has the highest peak clock frequency?

(a) P1 (b) P2
(c) P3 (d) P4

17. Any condition that causes a processor to stall is called as _____

(a) Hazard (b) Page fault

(c) System error (d) None of the mentioned

18. The periods of time when the unit is idle is called as _____

(a) Stalls (b) Bubbles

(c) Hazards (d) Both Stalls and Bubbles

19. The contention for the usage of a hardware device is called _____

(a) Structural hazard

(b) Stalk

(c) Deadlock

(d) None of the mentioned

20. The situation wherein the data of operands are not available is called _____

(a) Data hazard (b) Stock

(c) Deadlock (d) Structural hazard

21. The stalling of the processor due to the unavailability of the instructions is called as ____

(a) Control hazard (b) structural hazard

(c) Input hazard (d) None of the mentioned

22. The time lost due to the branch instruction is often referred to as _____

(a) Latency

(b) Delay

(c) Branch penalty

(d) None of the mentioned

23. A 4-stage pipeline has the stage delays as 150, 120, 160 and 140 nanoseconds respectively. Registers that are used between the stages have a delay of 5 nanoseconds each. Assuming constant clocking rate, the total time taken to process 1000 data items on this pipeline will be

(a) 120.4 microseconds

(b) 160.5 microseconds

(c) 165.5 microseconds

(d) 590.0 microseconds

24. We have two designs D1 and D2 for a synchronous pipeline processor. D1 has 5 pipeline stages with execution times of 3 nsec, 2 usee. 4 nsec, 2 nsec and 3 nsec while the design D2 has 8 pipeline stages each with 2 nsec execution time.

How much time can be saved using design D2 over design D1 for executing 100 instructions?

(a) 214 nsec (b) 202 nsec

(c) 86 nsec (d) –200 nsec

25. A CPU has five-stages pipeline and runs at 1 GHz frequency. Instruction fetch happens in the first stage of the pipeline. A conditional branch instruction computes the target address and evaluates the condition in the third stage of the pipeline. The processor stops fetching new instructions following a conditional branch until the branch outcome is known. A program executes 10^9 instructions out of which 20% are conditional branches. If each instruction takes one cycle to complete on average, then total execution time of the program is

(a) 1.0 second (b) 1.2 seconds

(c) 1.4 seconds (d) 1.6 seconds

26. A nonpipelined single cycle processor operating at 100 MHz is converted into a synchronous pipelined processor with five stages requiring 2.5 nsec, 1.5 nsec, 2 nsec, 1.5 nsec and 2.5 nsec, respectively. The delay of the latches is 0.5 nsec. The speedup of the pipeline processor for a large number of instructions is

(a) 4.5 (b) 4.0

(c) 3.33 (d) 3.0

27. Which of the following are NOT true in a pipelined processor?

1. By passing can handle all Raw hazards.
2. Register renaming can eliminate all register carried WAR hazards.
3. Control hazard penalties can be eliminated by dynamic branch prediction.

(a) 1 and 2 only (b) 1 and 3 only

(c) 2 and 3 only (d) 1, 2 and 3

28. Consider a 4 stage pipeline processor. The number of cycles needed by the four instructions I1, I2, I3, I4 in stages S1, S2, S3, S4 is shown below:

	S1	S2	S3	S4
I1:	2	1	1	1
I2:	1	3	2	2
I3:	2	1	1	3
I4	1	2	2	2

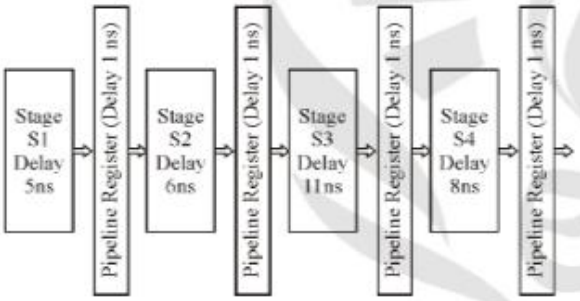
What is the number of cycles needed to execute the following loop?

for(i = 1 to 2) {I1; I2; I3; I4;}

(a) 16 (b) 23

(c) 28 (d) 30

29. Consider an instruction pipeline with four stages (SI, S2, S3 and S4) each with combinational circuit only. The pipeline registers are required between each stage and at the end of the last stage. Delays for the stages and for the pipeline registers are as given in the figure



What is the approximate speed up of the pipeline in steady state under ideal conditions when compared to the corresponding non-pipeline implementation?

(a) 4.0 (b) 2.5

(c) 1.1 (d) 3.0

30. Consider an instruction pipeline with five stages without any branch prediction: Fetch Instruction (FI), Decode Instruction (DI), Fetch Operand (FO), Execute Instruction (EI) and Write Operand (WO). The stage delays for FI, DI, FO, EI and WO are 5 ns, 7 ns, 10 ns, 8 ns and 6 ns, respectively. There are intermediate storage buffers after each stage and the delay of each buffer is 1 ns. A program consisting of 12 instruction I_1, I_2, I_3,..... I_{12} is execute in this pipelined processor. Instruction I_4 is the only branch instruction and its branch target is I_9. If the branch is taken during the execution of this program, the time (in ns) needed to complete the program is

(a) 132 (b) 165

(c) 176 (d) 328

31. Consider the following processors (ns stands for nanoseconds). Assume that the pipeline registers have zero latency.

P1: Four-stage pipeline with stage latencies 1 ns, 2 ns, 2 ns, 1 ns.

P2: Four-stage pipeline with stage latencies 1 ns, 1.5 ns, 1.5 ns, 1.5 ns.

P3: Five-stage pipeline with stage latencies 0.5 ns, 1 ns, 1 ns, 0.6 ns, 1 ns.

P4: Five-Stage pipeline with stage latencies 0.5 ns, 0.5 ns, 1 ns, 1 ns, 1.1 ns.

Which processor has the highest peak clock frequency?

(a) PI (b) P2

(c) P3 (d) P4

❑❑❑

Answer Key

1. *Ans. (a)*
2. *Ans. (b)*
3. *Ans. (c)*
4. *Ans. (c)*
5. *Ans. (d)*
6. *Ans. (c)*
7. *Ans. (b)*
8. *Ans. (d)*
9. *Ans. (c)*
10. *Ans. (c)*
11. *Ans. (c)*
12. *Ans. (a)*
13. *Ans. (c)*
14. *Ans. (b)*
15. *Ans. (b)*
16. *Ans. (c)*
17. *Ans. (a)*
18. *Ans. (d)*
19. *Ans. (a)*
20. *Ans. (a)*
21. *Ans. (a)*
22. *Ans. (c)*
23. *Ans. (b)*

No of stage (k) = 4

tp = max [stage delay] + Buffer delay

max [150, 120, 160 140] + 5 ns

160 + 5 = 165 ns

NO of task (n) = 1000

Total time taken on this pipeline

$= [k + (n - 1)]t_p$

$= [4 (1000 - 1)] \times 165$

$= [4 + 999] \times 165$

$= 1003 \times 165$

$= 165495$ ns

$= 165.5$ microseconds

24. *Ans. (b)*

Synchronous pipeline $[D_1]$

No of stage (K) = 5

tp = max[stage delay]

= max[3, 2, 4, 2, 3]

= 4 ns

n = 100

Total time to process 100 task [pipeline D_1]

$T_{D_1} = [k + (n - 1)]tp$

$= [5 + (100 - 1)] \times 4$ ns

$= [5 + 99] \times 4$ ns

$104 \times 4 = 416$ ns

Synchronous pipeline $[D_2]$

No of stage (K) = 8

t_p = max [stage delay]

t_p = max [2, 2, 2, 2, 2, 2, 2, 2]

= 2ns

n = 100

Total time to process 100 task [pipeline D_2]

$T_{D_2} = [k + (n - 1)]tp$

$= [8 + (100 - 1)] \times 2$

$= [8 + 99] \times 2$

$= 107 \times 2 = 214$ ns

Time can be saved using design (D_2) over design (D_1)

= 416 – 214

= 202 nseconds

25. *Ans. (c)*

No of stage (k) = 5

Segment delay $[t_p] = \dfrac{1}{\text{clock Rate}}$

$= \dfrac{1}{1\text{ GHz}}$

$$= \frac{1}{1\times10^{9}}$$

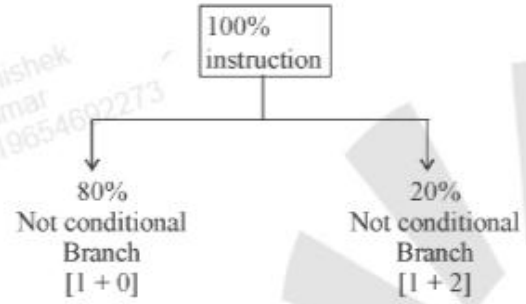
$$= 10^{-9} \text{ second}$$

Due to branch instruction (No of stall)

$$= i^{th}\text{stage} - 1$$

$$= 3 - 1 = 2$$

No of instruction = 10^9



$$CPI_{avg} = 0.8[1 + 0] + 0.2[1 + 2]$$

$$= 0.8 \times 1 + 0.2 \times 3$$

$$= 0.8 + 0.6$$

$$= 1.4$$

1 instruction execution time

$$= CPI_{avg} \times \text{cycle time}$$

$$= 1.4 \times 1 \text{ ns} = 1.4 \text{ ns}$$

Total instruction execution time

$$= 10^9 \times 1 \text{ instruction execution time}$$

$$= 10^9 \times 1.4 \text{ ns}$$

$$= 10^9 \times 1.4 \times 10^{-9} \text{ second}$$

$$= 1.4 \text{ seconds}$$

26. ***Ans. (3.33)***

Non pipelined processor

$$T_n \text{ [cycle time]} = \frac{1}{100 \text{ MHz}}$$

$$\frac{1}{100\times10^{6}} = \frac{1}{10^{8}}$$

$$T_n[\text{cycle}] = \frac{10^{-8}}{10}\times10 = \boxed{10 \text{ ns}}$$

For pipelined processor

No. of segment (K) = 5

t_p = max (segment delay) + Buffer delay

Max (2.5 ns, 1.5 ns, 2ns, 1.5 ns, 2.5 ns)+ 0.5

2.5 ns + 0.5 = 3 ns

$$\text{Speedup} = \frac{t_n}{t_p}$$

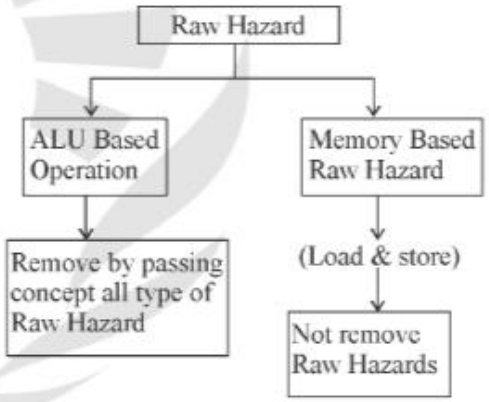
$$= \frac{\text{Execution time of non pipelind}}{\text{Execution time of pipeline}}$$

$$= 3.33$$

27. ***Ans. (b)***

By passing can handle all raw hazard → false

False statement By passing can't handle all raw hazard.



II. Register renaming can eliminate all register carried WAR Hazards. → True

Solution →

Register Remain can eliminate all WAR Hazards

II. Control Hazard Penalties can be eliminated By dynamic Branch Predictions → False

Solution

It cannot completely through it can reduce control Hazard Penalties.

In dynamic Branch Prediction only

Reduce Branch Penalties.

28. ***Ans. (b)***

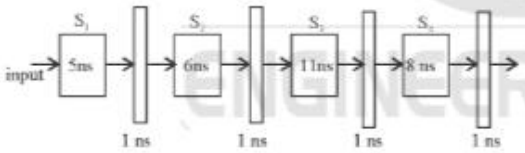
	S_1	S_2	S_3	S_4
I_1	2	1	1	1
I_2	1	3	2	2
I_3	2	1	1	3
I_4	1	2	2	2

Total number of cycle needed to compute the following loop

[i = 1 to 2], $\{I_1, I_2, I_3, I_4\}$

		S_1	S_2	S_3	S_4
I = 1	I_1	2	3	4	5
	I_2	3	6	8	10
	I_3	5	7	9	13
	I_4	6	9	11	15
I = 2	I_1	8	10	12	16
	I_2	9	13	15	18
	I_3	11	14	16	21
	I_4	12	16	18	23

29. ***Ans. (b)***



Non-pipeline cycle time (t_n) =

Sum of all segment delay

$S_1 + S_2 + S_3 + S_4$

5ns + 6ns + 11 hs + 8 ns

30 ns

Pipeline cycle time (t_p)

Max(segment Delay) + Buffer delay

Max [5,6,11,8] + 1 ns

= 11 ns + 1 ns

= 12 ns

$$\text{Speed up} = \frac{\text{Performance of Pipeline}}{\text{Performance of non Pipeline}}$$

$$= \frac{\text{Execution time of non-Pipeline}}{\text{Execution time of Pipeline}}$$

$$= \frac{30\text{ns}}{12\text{ns}} = 2.5$$

30. ***Ans. (165)***

No of stage (k) = 5

T_p = max (stage delay) + Buffer delay

max(5ns, 7ns, 10ns, 8ns, 6ns) + 1 ns

T_p = 10 ns + 1ns

T_p = 11 ns

No of stall due to branch instruction

= i^{th}stage −1

= (EXE)stage − 1

4 − 1 = 3

= [k + (n − 1)]

= [5 + (8–1)]

= 5 + 7 = 12

Extra cycle with stall = 3

Total No of cycle = 12 + 3 = 15

Total execution time in program

= No of cycle × cycle time

= No of cycle × cycle time

= 15× 11 = 165 ns

31. ***Ans. (c)***

Pippeline (P_1) :

t_p = max(stage delay)

= max (1, 2, 2, 1) = 2

$$\text{Clock Rate} = \frac{1}{\text{cycle time}} = \frac{1}{2\text{ns}}$$

$$\frac{1}{2}\times 10^9 \frac{1}{\text{second}} = 0.5 \text{ GHz}$$

Clock Rate $(P_1) = 0.5$ GHz

Pipeline (P_2) :

t_p = max (stage delay)
= max(1, 1.5, 1.5, 1.5)
= 1.5 ns

$$\text{Clock Rate} = \frac{1}{\text{Cycle time}}$$

$$\frac{1}{1.5 \text{ ns}} = \frac{10}{15}\times 10^9 \text{ 1/second}$$

clock rate = 0.66 GHz

Pipeline (P_3) :

t_p = max (stage delay)
= max (0.5, 1, 1, 0.6, 1)
t_p = 1 ns

$$\text{Clock rate} = \frac{1}{\text{cycle time}} = \frac{1}{\text{ns}}$$

$$= \frac{1}{1}\times 10^9 \frac{1}{\text{second}}$$

Clock Rate $P_3 = 1$ GHz

Pipeline (P_4) :

t_p = max (stage delay)
= max (0.5, 0.5, 1, 1, 1.1)
= 1.1 ns

$$= \frac{1}{\text{cycle time}} = \frac{1}{1.1\text{ns}}$$

$$= \frac{10}{11}\times 10^9$$

Clock Rate $P_4 = 0.9090$ GHz

Highest Peak Clock frequency = P_3

❑❑❑

CHAPTER 3

CACHE MEMORY

OBJECTIVE QUESTIONS

1. Consider a fully associative cache with 8 cache blocks and the following sequence of memory block requests
(4, 3, 25, 8, 19, 6, 25, 8, ; 16, 35, 45, 22, 8, 3, 16, 25, 7).
If LRU is used which cache block will have memory block 7?
(a) 4 (b) 5
(c) 6 (d) 7

2. Consider a 4-set associative memory with 16 cache blocks, the memory block request are in order
(0, 255, 1, 4, 3, 8, 133, 159, 216, 129, 63, 8, 48, 32, 73, 92, 155)
W.O.F. memory block will not be in cache if LRU is used?
(a) 3 (b) 8
(c) 129 (d) 216

3. Consider a 2-set associative memory has a total of 8-cache blocks. If LRU is used to replace for two memory block. Request (0, 3, 5, 9, 7, 0, 16, 55) Which memory block will present in the cache at the end of sequence?
(a) 0, 3, 5, 9, 16, 55 (b) 0, 3, 5, 7, 9, 16, 55
(c) 0, 5, 7, 9, 16, 55 (d) 3, 5, 7, 9, 16, 55

4. Consider a 2 set associative memory, consisting of 2^C memory blocks and 2C cache block the cache location for the memory block K is:
(a) K mod 2C (b) K mod 2^C
(c) K mod C (d) 2^C mod K

5. The search concept used in associative memory is
(a) parallel search (b) sequential search
(c) binary search (d) selection search

6. In which one of following page replacement policies, Belady's anomaly may occur?
(a) FIFO (b) O Optimal
(c) LRU (d) MRU

7. The essential content (s) in each entry of a page table is / are
(a) Virtual page number
(b) page frame number
(c) Both virtual page number & page frame number
(d) Access right information.

8. The address generated by a segmented programme is called
(a) Physical address (b) Virtual address
(c) Logical address (d) Effective address

9. Most widely used page replacement technique is
(a) LIFO (b) FIFO
(c) Polling (d) None

10. The capacity of memory unit is defined by number of words multiplied by number of bits per word. How many separate address and data lines are needed for a memory of 4K x 16?
(a) 10 address, 16 data lines
(b) 11 address, 8 data lines
(c) 12 address, 16 data lines
(d) 12 address, 12 data lines

11. The content addressable memory is also known as
(a) Cache memory
(b) Main memory
(c) Associative memory
(d) Auxiliary memory

12. The average memory access time of a computer can be improved considerably by using the

(a) Main memory (b) Hard disk

(c) S – RAM (d) Pen drive

13. The databus width of a 2048 x 8 bits is

(a) 8 (b) 10

(c) 12 (d) 16

14. A computer system has a 4K word cache organized in block, set associative manner with 4 blocks per set 64 words per block. The number of bits in the SET and WORD fields of main memory address formula is

(a) 15, 4 (b) 6, 4

(c) 7, 2 (d) 4, 6

15. Scratchpad memory is a _____ memory.

(a) Last – in First out

(b) First – in First out

(c) Local permanent memory

(d) Local temporary memory

16. One of the most widely used mapping technique is

(a) Associative

(b) Direct mapping

(c) Set Associative mapping

(d) None

17. Address space is divided into _____ and memory spade is divided into _____ respectively.

(a) Blocks & Pages

(b) pages & blocks

(c) Blocks & Modules

(d) Modules & Blocks

18. Virtual memory is

(a) Simple to implement

(b) used on all major commercial operating systems

(c) less efficient in utilization of memory

(d) useful when fast I/O devices are not available

Linked Answer Question : 19 & 20

Statement : Consider a machine with a byte addressable main memory of 2^{16} bytes. Assume that a direct mapped data mapped data cache consisting of 32 lines of 64 bytes each is used in the system. A 50 × 50 two dimensional array of bytes is stored is main memory starting from memory location 1100H. Assume that data cache is initially empty. The complete array is accessed twice assume that contents of data cache do not change in between the two accesses.

19. Consider the following program segment. Here R_1, R_2 and R_3 are the general purpose registers.

	Instruction	Operation	Instruction size (no of words)
Loop:	MOV R_1 (3000)	$R_1 \leftarrow M(3000)$	2
	MOV R_2, (R_3)	$R_2 \leftarrow ? M(R_3)$	1
	ADD R_2, R_1	$R_2 \leftarrow R_1 + R_2$	1
	MOV (R_3), R_2	$M(R_3) ? \leftarrow R_2$	1
	INC R_3	$R_3 \leftarrow ? R_3 + 1$	1
	DEC R_1	$R_1 \leftarrow R_1 - 1$	1
	BNZ Loop	Branch on not zero	2
	HALT	Stop	1

Assume that content memory location 3000 is 10 and content of register R3 is 2000. The content of each of memory locations from 2000 to 2010 is 100. The program is loaded from memory location 1000. All the numbers are in decimal.

Assume that the memoryis word addressable. The number of Memory reference for accessing the data i executing the program completely is

(a) 10 (b) 11

(c) 20 (d) 21

20. Consider the following page reference string

102, 203, 4024, 227, 156, 527, 656, 253, 183, 207, 308, 745, 623, 345, 242, 112, 223, 321, 622

A page size is 100 bytes. How many page faults will occur with LRU replacement algorithm with 5 frames?

(a) 10 (b) 7

(c) 8 (d) 11

21. If the cache needs an access time of 20 ns and the main memory 120 ns, then the average access time of a CPU is (assume hit-ratio is 80%)

(a) 30 ns (b) 35 ns

(c) 40 ns (d) 45 ns

22. A set-associative cache consists of 60 lines, or blocks divided into four-line sets. Main memory consists 2 K block of 512 words each. In the format of main memory addresses, what is size of tag, set and word is?

(a) 7, 4, 8 (b) 9, 2, 7

(c) 8, 4, 7 (d) 7, 2, 9

23. Suppose a cache is 10 times faster than main memory, and suppose that the cache can be used 90% of the time. How much speed up do we gain by using the cache?

(a) 4.7 (b) 5

(c) 5.6 (d) 5.3

24. A computer system contains a cache. Un-cached memory access takes 7 times longer than access to cache. If cache has a hit ratio 0.9. The ratio of efficiency of cached memory access time to Un-cached memory access time, is?

(a) 0.10 (b) 0.24

(c) 0.19 (d) 0.30

25. The main memory of a computer has 2cm cache blocks while the cache has 2c blocks. If the cache uses the set associative mapping scheme with 2 blocks per set, then block k of the main memory maps to the set:

(a) (k mod m) of the cache

(b) (k mode 2 c) of the cache

(c) (k mod c) of the cache

(d) (k mod 2 cm) fo the cache

26. A block-set associative cache memory consist of 128 blocks divided into four block sets. The main memory consists of 16.374 blocks and each block contains 256 eight bit words.

1. How many bits are required for addressing the main memory?

2. How many bits are needed to represent the TAG, SET and WORD fields?

27. The total size of address space in a virtual memory system is limited by

(a) the length of MAR

(b) The available secondary storage

(c) the available main memory

(d) All of the above

28. A CPU has 32-bit memory address and a 256 KB cache memory. The cache is organized as a 4-way set associative cache with cache block size of 16 bytes. The number of sets in the cache and the size of tag (in bits) field respectively equals to

(a) 2^{12} and 10 (b) 2^{12} and 12

(c) 2^{16} and 12 (d) 2^{16} and 10

29. If the level of memory hierarchy has a hit ratio of 75 percent, memory request take 12 ns to complete if they hit in the level, and memory request that miss in the level take 100 ns to complete, what is the average access time of the level?

(a) 32 ns (b) 33 ns

(c) 34 ns (d) 35 ns

30. A memory system contains cache, a main memory and a virtual memory. The access time of cache is 5ns, and it has 80% hit rate. the access time of main memory is 100 ns, and it has 99.5% hit rate. The access time of virtual memory is 10 millisecond. What it the average access time of the hierarchy?

(a) 8024 (b) 10024

(c) 12024 (d) None of the above

31. The number successful accesses to memory stated as a fraction is called as _____

(a) Hit rate (b) Miss rate

(c) Success rate (d) Access rate

32. The number failed attempts to access memory, stated in the form of a fraction is called as _____

(a) Hit rate (b) Miss rate

(c) Failure rate (d) Delay rate

33. In associative mapping during LRU, the counter of the new block is set to '0' and all the others are incremented by one, when _____ occurs.

(a) Delay (b) Miss

(c) Hit (d) Delayed hit

34. In LRU, the referenced blocks counter is set to'0? and that of the previous blocks are incremented by one and others remain same, in the case of _____

(a) Hit (b) Miss

(c) Delay (d) None of the mentioned

35. If hit rates are well below 0.9, then they're called as speedy computers.

(a) True

(b) False

36. The extra time needed to bring the data into memory in case of a miss is called as _____

(a) Delay (b) Propagation time

(c) Miss penalty (d) None of the mentioned

37. The miss penalty can be reduced by improving the mechanisms for data transfer between the different levels of hierarchy.

(a) True

(b) False

38. The reason for the implementation of the cache memory is _____

(a) To increase the internal memory of the system

(b) The difference in speeds of operation of the processor and memory

(c) To reduce the memory access and cycle time

(d) All of the mentioned advertisement

39. The effectiveness of the cache memory is based on the property of _____

(a) Locality of reference

(b) Memory localisation

(c) Memory size

(d) None of the mentioned

40. The temporal aspect of the locality of reference means _____

(a) That the recently executed instruction won't be executed soon

(b) That the recently executed instruction is temporarily not referenced

(c) That the recently executed instruction will be executed soon again

(d) None of the mentioned

41. The spatial aspect of the locality of reference means _____

(a) That the recently executed instruction is executed again next

(b) That the recently executed won't be executed again

(c) That the instruction executed will be executed at a later time

(d) That the instruction in close proximity of the instruction executed will be executed in future

42. The correspondence between the main memory blocks and those in the cache is given by _____

(a) Hash function (b) Mapping function

(c) Locale function (d) Assign function

43. The algorithm to remove and place new contents into the cache is called _____

(a) Replacement algorithm

(b) Renewal algorithm

(c) Updation

(d) None of the mentioned

44. The write-through procedure is used _____

(a) To write onto the memory directly

(b) To write and read from memory simultaneously

(c) To write directly on the memory and the cache simultaneously

(d) None of the mentioned

45. The bit used to signify that the cache location is updated is _____

(a) Dirty bit (b) Update bit

(c) Reference bit (d) Flag bit

46. The copy-back protocol is used _____

(a) To copy the contents of the memory onto the cache

(b) To update the contents of the memory from the cache

(c) To remove the contents of the cache and push it on to the memory

(d) None of the mentioned

47. The approach where the memory contents are transferred directly to the processor from the memory is called _____

(a) Read-later

(b) Read-through

(c) Early-start

(d) None of the mentioned

48. The principle of locality justifies the use of

(a) Interrupts (b) DMA

(c) Polling (d) Cache Memory

49. The main memory of a computer has 2 cm blocks while the cache has 2 c blocks. If the cache uses the set associative mapping scheme with 2 blocks per set, then block k of the main memory maps to the set

(a) (k mod m) of the cache

(b) (k mod c) of the cache

(c) (k mod 2 c) of the cache

(d) (k mod 2 cm) of the cache

50. More than one word are put in one cache block to

(a) exploit the temporal locality of reference in a program

(b) exploit the spatial locality of reference in a program

(c) reduce the miss penalty

(d) none of the above

51. Consider a system with 2 level cache. Access times of Level 1 cache, Level 2 cache and main memory are 1 ns, 10 ns, and 500 ns, respectively. The hit rates of Level 1 and Level 2 caches are 0.8 and 0.9 respectively. What is the average access time of the system ignoring the search time within the cache?

(a) 13.0 ns (b) 12.8 ns

(c) 12.6 ns (d) 12.4 ns

52. A dynamic RAM has a memory cycle time of 64 nsec. It has to be refreshed 100 times per msec and each refresh takes 100 nsec. What percentage of the memory cycle time is used for refreshing?

(a) 10 (b) 6.4

(c) 1 (d) 0.64

53. Consider a direct mapped cache of size 32 KB with block size 32 bytes. The CPU generates 32 bit addresses. The number of bits needed for cache indexing and the number of tag bits are respectively

(a) 10, 17 (b) 10, 22

(c) 15, 17 (d) 5, 17

54. A cache line is 64 bytes. The main memory has latency 32ns and bandwidth 1 GB/s. The time required to fetch the entire cache line from the main memory is

(a) 32 ns (b) 64 ns

(c) 96 ns (d) 128 ns

55. Consider a 4-way set associative cache consisting of 128 lines with a line size of 64 words. The CPU generates a 20-bit address of a word in main memory. The number of bits in the TAG, LINE and WORD fields are respectively

(a) 9, 6, 5 (b) 7, 7, 6

(c) 7, 5, 8 (d) 9, 5, 6

56. For inclusion to hold between two cache level L1 and L2 in a multilevel cache hierarchy, which of the following are necessary?

1. L1 must be a write-through cache
2. L2 must be write-through cache
3. The associativity of L2 must be greater that of L1
4. The L2 cache must be at least as large as the L1 cache

(a) 4 only

(b) 1 and 2 only

(c) 1, 2 and 4 only

(d) 1, 2, 3 and 4

57. In an instruction execution pipeline, the earliest that the data TLB (Translation Look a side Buffer) can be accessed is

(a) before effective address calculation has started

(b) during effective address calculation

(c) after effective address calculation has completed

(d) after data cache lookup has completed

58. How many 32K × 1 RAM chips are needed to provide a memory capacity of 256 K-bytes?

(a) 8 (b) 32

(c) 64 (d) 128

59. In a k-way set associative cache, the cache is divided into v sets, each of which consists of k lines. The line of a set are placed in sequence on after another. The lines in set s are sequenced before the lines in set (s + 1). The main memory blocks numbered 0 onwards. The main memory block numbered 'j' must be mapped to any one of the cache lines from

(a) (j mod v) * k to (j mod v) * k + (k – 1)

(b) (j mod v) * (j mod v) + (k – 1)

(c) (j mod k) to (j mod k) + (v – 1)

(d) (j mod k) * v (j mod k) * v + (v – 1)

60. A RAM chip has capacity of 1024 words of 8 bits each (1K × 8). The number of 2 × 4 decoders with enable line needed to construct a 16 K × 16 RAM from 1K × 8RAM is

(a) 4 (b) 5

(c) 6 (d) 7

61. An access sequence of cache block address of length N and contains n unique block addresses. The number of unique block addresses between two consecutive accesses to the same block address is bounded above by k. What is the miss ratio if the access sequence is passed through a cache of associativity $A \geq k$ exercising least recently used replacement policy?

(a) n/N (b) $1/N$

(c) $1/A$ (d) k/n

62. The size of the physical address space of a processor is 2^P bytes. The word length is 2^W bytes. The capacity of cache memory is 2^N bytes, the size of each cache block is 2^M words. For a k-way set-associative cache memory, the length (in number of bits) of the tag field is

(a) $P-N-\log_2 k$

(b) $P-N+\log_2 k$

(c) $P-N-M-W-\log_2 k$

(d) $P-N-M-W+\log_2 k$

63. A certain processor uses a fully associative cache of size 16 kB. The cache block size is 16 bytes. Assume that the main memory is byte addressable and uses a 32-bit address. How many bits are required for the Tag and the Index fields respectively in the addresses generated by the processor?

(a) 28 bits and 4 bits (b) 24 bits and 4 bits

(c) 24 bits and 0 bits (d) 28 bits and 0 bits

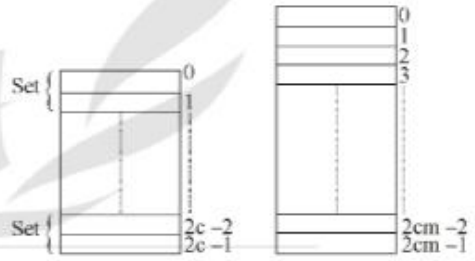
❑❑❑

Answer Key

1. *Ans. (b)*
2. *Ans. (d)*
3. *Ans. (c)*
4. *Ans. (c)*
5. *Ans. (a)*
6. *Ans. (a)*
7. *Ans. (a)*
8. *Ans. (c)*
9. *Ans. (b)*
10. *Ans. (c)*
11. *Ans. (c)*
12. *Ans. (c)*
13. *Ans. (a)*
14. *Ans. (d)*
15. *Ans. (d)*
16. *Ans. (c)*
17. *Ans. (b)*
18. *Ans. (b)*
19. *Ans. (d)*
20. *Ans. (c)*
21. *Ans. (a)*
22. *Ans. (d)*
23. *Ans. (b)*
24. *Ans. (d)*
25. *Ans. (b)*
26. *Ans. (*)*
27. *Ans. (b)*
28. *Ans. (a)*
29. *Ans. (c)*
30. *Ans. (b)*
31. *Ans. (a)*
32. *Ans. (b)*
33. *Ans. (b)*
34. *Ans. (a)*
35. *Ans. (b)*
36. *Ans. (c)*
37. *Ans. (a)*
38. *Ans. (b)*
39. *Ans. (a)*
40. *Ans. (c)*
41. *Ans. (d)*
42. *Ans. (b)*
43. *Ans. (a)*
44. *Ans. (c)*
45. *Ans. (a)*
46. *Ans. (b)*
47. *Ans. (c)*
48. *Ans. (d)*

The principle of locality justifies the use of cache memory.

49. *Ans. (b)*



Set Associative Cache Main Memory

# of set in set associative cache

$$= \frac{\text{\# of blocks in cache}}{\text{\# of blocks in one set}}$$

$$= \frac{2c}{2} = c$$

# of sets in cache = c

Therefore, the block k of the main memory maps to the set (k mod c) of the cache.

50. *Ans. (b)*

There are two types of locality of reference:

1. **Temporal :** A recently executed instruction is likely to be executed again very soon.

2. **Spatial:** Instructions in close proximity to a recently executed instruction are also likely to be executed soon.

The spatial aspect suggest that instead of fetching just one item from the main memory to the cache, it is useful to fetch several items that reside at adjacent address as well.

Therefore more than one work are put in one cache block to exploit the spatial locality of reference in the program.

51. ***Ans. (c)***

Access time

$= t_1h_1 + (1-h_1)h_2t_2 + (1- h_1)(1-h_2)t_m$

$= 1*0.8 + 0.2*0.9*10 + 0.2*0.1*500$

$= 0.8 + 1.8 + 10 = 12.6$ ns.

52. ***Ans. (c)***

Time for Memory cycle time = 64nsec

Time for refresh = 100nsec

Number of refreshes in a memory cycle

So, in 64nsec = (64nsec×100 Times)/1msec

$= 64\times10^{-4}$

So, time for refresh in a memory cycle

$= 100 \text{ ns}*64*10^{-4}$

$= 64 * 10^{-2}$ ns

$= 0.64$ nsec

So, percentage of time spent for refresh

$= (64 * 10^{-2}/64) * 100$

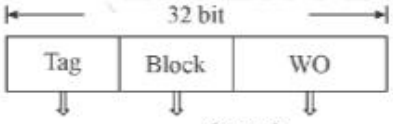
$= 1\%$

53. ***Ans. (a)***

Cache Size = 32 KB

Block Size = 32 Byte

Mapping = Direct Mapping



$= 32 - (10 + 5) = 17$ Bit

$\log_2\left(\frac{CMS}{BS}\right)$

$\log_2\left(\frac{32KB}{32Byte}\right)$

$\log_2\left(\frac{2^{15}}{2^5}\right)$

$= \log_2(2^{10})$

$= 10 \log_2 2$

$= 10$ bit

$\log_2$(Block Size)

$= \log_2$(32 Byte)

$= \log_2 2^5 = 5\log_2 2$

$= 5$ bit

Index = No. of block in cache memory

= 10 bit

Tag bit = 17 bit (10, 17)

54. ***Ans. (c)***

For 1 sec it is 10^9 bytes, for 64 bytes ?

$= 64*1/10^9 = 64$ ns

MM latency is 32 ns.

Total time required to place cache line

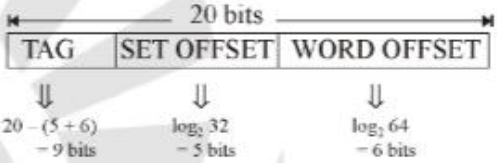
$= 64 + 32 = 96$ ns.

55. ***Ans. (d)***

4-way set associative

lines = 128

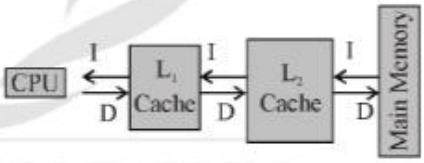
Block size = 64 words



Number of set $= \frac{\#\text{ lines}}{4} = \frac{128}{4} = 32$

56. ***Ans. (b)***

Consider the following diagram :



L_1 and L_2 both are write through caches. This two conditions are necessary.

57. ***Ans. (b)***

In instruction execution pipeline, the earliest that the data TLB can be accessed during effective address calculation has started.

58. ***Ans. (c)***

Basic RAM = 32 K × 1

Design RAM = 256 K × 8

No. of RAM $= \frac{256\text{ K}\times8}{32\text{ K}\times1}$

$$= \frac{2^{18} \times 2^3}{2^{15} \times 2^0} = 64$$

It require 8 parallel line and in each parallel line 8 serial RAM chip are required.

59. ***Ans. (a)***

Main memory block 'j' mapped to any of cache line. Cache line range is:

(j mod v)*k → (j mod v)*k + (k – 1)

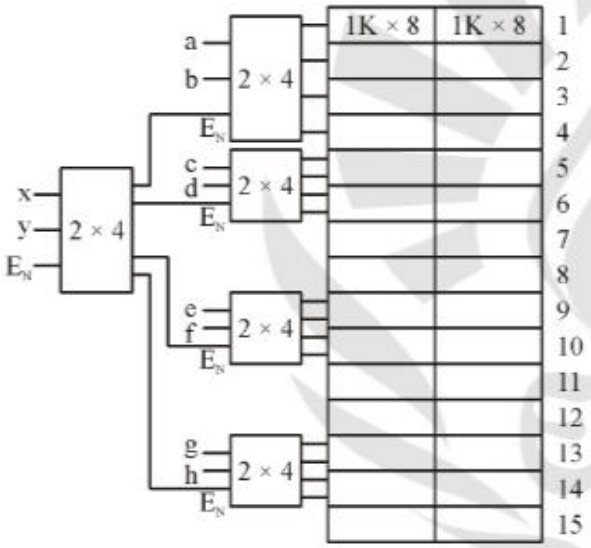
60. ***Ans. (b)***

We need 16 K × 16 RAM from 1 K × 8 RAM

So, number of chips required

$$= \frac{16K \times 16}{1K \times 8} = 16 \times 2$$

So we need 16 output lines



∴ We need 5 decoders.

61. ***Ans. (a)***

Miss ratio = n/N, if the access sequence is passed through a cache of associativity A ≥ k exercising least-recently used replacement policy.

62. ***Ans. (b)***

MM space = 2^P bytes

physical Address (PA) size = P bits

CM size = 2^N bytes

Block size = 2^M words

= 2^M words * 2^W bytes/word

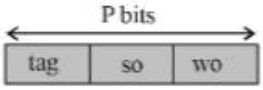
= $2^{(M+W)}$ bytes

$$\text{Number of lines} = \frac{\text{CM size}}{\text{Block size}} \Rightarrow \frac{2^N}{2^{M+W}}$$

$$= 2^{N-M-W}$$

$$\text{Number of sets} = \frac{\text{Number of lines in cache}}{\text{P – way}}$$

$$= \frac{2^{N-M-W}}{K}$$



$$= 2\log_2 \frac{2^{N-M-W}}{K} \log_2 2^{M+W}$$

$$= \log_2 2^{N-M-W} - \log_2 K$$

$\Rightarrow$ (N–M–W–log2K)

∴ Tag size

$\Rightarrow$ P – (N–M–W–$\log_2$ K+M+W

P – N+$\log_2$K

63. ***Ans. (d)***

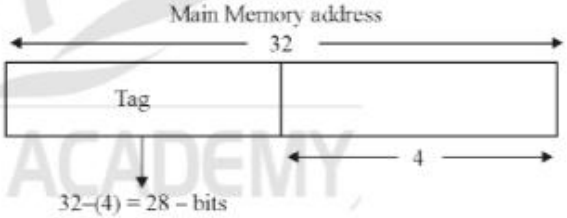
Cache size = 16 KB

Block size = 16B = 2^4 B

$\Rightarrow$ Block offset = 4 – bits

Main memory address = 32 – bits

In fully associative cache main memory address format



In fully associative cache, there is no any index. Hence,

Tag = 28 bits

Index = 0 – bits

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CHAPTER 4

SECONDARY MEMORY

OBJECTIVE QUESTIONS

Common Data Questions : 1 & 2

A hard disk has 63 sectors per track, 10 platters each with 2 recording surfaces and 1000 cylinders. The address of a sector is given has triple (c,h,s), where C is cylinder number, h is surface number, S is sector number. Thus the 0th sector is addressed as (0,0,0) the 1st sector as (0,0,1) and so on :

1. The address (400, 16, 29) corresponds to sector number :

(a) 505035 (b) 505036

(c) 505037 (d) 505038

2. The address of 1039th sector is

(a) (0,15,31)

(b) (0,16,30)

(c) (0,16,31)

(d) (0,17, 31)

3. The main difference b/w RISC over a CISC that a RISC has

(a) Fewer instructions

(b) Fewer addressing modes

(c) More processing

(d) All the above

4. The capacity of memory unit is defined by number of words multiplied by number of bits per word. How many separate address and data lines are needed for a memory of 4K x 16?

(a) 10 address, 16 data lines

(b) 11 address, 8 data lines

(c) 12 address, 16 data lines

(d) 12 address, 12 data lines

5. A certain moving arm disk storage, with one head, has the following specifications.

Number of tracks/ recording surface = 200

Disk rotation speed = 2400 rpm

Track storage capacity = 62,500 bits

The average latency of the device is p m sec and the data transfer rate is Q bits/sec.

The values of P and Q respectively are

(a) 12.5 ns, 2.5×10^6 bits

(b) 12.5ns, 2.5×10^4 bits

(c) 12.5ns, 2.5×10^3 bits

(d) none of these

6. What is the average time to read or write a 512 byte sector for a typical disk with average seek time 9 ms, transfer rate 4 MB 1 sec, and the disk rotates at 72 rpm, and the controller overhead is 1ms. Assume that the disk is idle so that there are no queuing delays.

(a) 14.3 ms (b) 4.275 ms

(c) 13.3 ms (d) 0.125 ms

7. The seek time of a disk is 30 ms. It rotates at the rate of 30 rotations per second. Each pack has a capacity of 300 words. The access time is approximately?

(a) 47 ms (b) 60 ms

(c) 50 ms (d) 62 ms

8. The disk system consists of which of the following:

(i). Disk (ii) Disk drive

(iii) Disk controller

(a) i and ii (b) i , ii and iii

(c) ii and iii (d) None of these

9. The set of corresponding tracks on all surfaces of a stack of disks form a _____
   (a) Cluster (b) Cylinder
   (c) Group (d) Set

10. The data can be accessed from the disk using _____
   (a) Surface number (b) Sector number
   (c) Track number (d) All of the mentioned

11. The read and write operations usually start at _____ of the sector.
   (a) Center
   (b) Middle
   (c) From the last used point
   (d) Boundaries

12. To distinguish between two sectors we make use of _____
   (a) Inter sector gap (b) Splitting bit
   (c) Numbering bit (d) None of the mentioned

13. The _____ process divides the disk into sectors and tracks.
   (a) Creation (b) Initiation
   (c) Formatting (d) Modification

14. The access time is composed of _____
   (a) Seek time
   (b) Rotational delay
   (c) Latency
   (d) Both Seek time and Rotational delay

15. The disk drive is connected to the system by using the _____
   (a) PCI bus (b) SCSI bus
   (c) HDMI (d) ISA

16. _____ is used to deal with the difference in the transfer rates between the drive and the bus.
   (a) Data repeaters
   (b) Enhancers
   (c) Data buffers
   (d) None of the mentioned

17. _____ is used to detect and correct the errors that may occur during data transfers.
   (a) ECC
   (b) CRC
   (c) Checksum
   (d) None of the mentioned

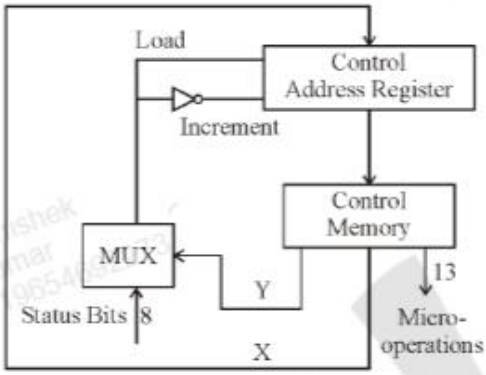
18. For the daisy chain scheme of connecting I/O devices, which of the following statements is true?
   (a) It gives nonuniform priority to various devices
   (b) It gives uniform priority to all devices
   (c) It is only useful for connecting slow devices to a processor device
   (d) It requires a separate interrupt pin on the processor for each device

19. A micro program control unit is required to generate a total of 25 control signals. Assume that during any microinstruction at most two control signals are active. Minimum number of bits required in the control word to generate the required control signal
   (a) 2 (b) 25
   (c) 10 (d) 12

20. I/O redirection
   (a) implies changing the name of a file
   (b) can be employed to use an existing file as input file for a program
   (c) implies connection 2 programs through a pipe
   (d) none of the above

21. The main difference(s) between a CISC and A RISC processor is/are that a RISC processor typically
   (a) has fewer instructions
   (b) has fewer addressing modes
   (c) has more registers
   (d) is easier to implement using hard-wired control logic

22. The microinstructions stored in the control memory of a processor have a width of 26 bits. Each microinstruction is divided into three fields: a micro-operation field of 13 bits, a next address field (X), and a MUX select field (Y). There are 8 status bits in the inputs of the MUX.



How many bits are there in the X and Y fields, and what is the size of the control memory in number of words?

(a) 10, 3,1024 (b) 8, 5, 256

(c) 5, 8, 2048 (d) 10, 3, 512

23. A hard disk with a transfer rate of 10 M bytes/second is constantly transferring data to memory using DMA. The processor runs at 600 MHz, and takes 300 and 900 clock cycles to initiate and complete DMA transfer respectively. If the size of the transfer is 20 Kbytes, what is the percentage of processor time consumed for the transfer operation?

(a) 5.0% (b) 1.0%

(c) 0.5% (d) 0.1%

Linked Answer Questions 24

A disk has 8 equidistant tracks. The diameters of the innermost and outermost tracks are 1 cm and 8 cm respectively. The innermost track has a storage capacity of 10 MB.

24. If the disk has 20 sectors per track and is currently at the end of the 5th sector of the inner-most track and the head can move at a speed of 10 meters/sec and it is rotating at constant angular velocity of 6000 RPM, how much time will it take to read 1 MB contiguous data starting from the sector 4 of the outer-most track?

(a) 13.5 ms (b) 10 ms

(c) 9.5 ms (d) 20 ms

25. A device with data transfer rate 10 KB/sec is connected to a CPU. Data is transferred byte-wise. Let the interrupt overhead be 4 usec. The byte transfer time between the device interface register and CPU or memory is negligible. What is the minimum performance gain of operating the device under interrupt mode over operating it under program controlled mode?

(a) 15 (b) 25

(c) 35 (d) 45

26. Consider a disk drive with the following specifications.

16 surfaces. 512 tracks/surface, 512 sectors/track. 1 KB/sector, rotation speed 3000 rpm. The disk is operated in cycle stealing mode whereby whenever one byte word is ready it is sent to memory: similarly, for writing, the disk interface reads a 4 byte word from the memory in each DMA cycle. Memory cycle time is 40 nsec. The maximum percentage of time that the CPU gets blocked during DMA operation is

(a) 10 (b) 25

(c) 40 (d) 50

27. Consider a disk pack with 16 surfaces, 128 tracks per surface and 256 sectors per track. 512 bytes of data are stored in a bit serial manner in a sector. The capacity of the disk pack and the number of bits required to specify a particular sector in the disk are respectively

(a) 256 Mbyte, 19 bits (b)256 Mbyte, 28 bits

(c) 512 Mbyte, 20 bits (d)64 Gbyte, 28 bits

28. A hard disk system has the following parameters: Number of tracks = 500

Number of sectors/track =100

Number of bytes /sector = 500

Time taken by the head to move from one track to adjacent track = 1 ms Rotation speed = 600 rpm. What is the average time taken for transferring 250 bytes from the disk?

(a) 300.5 ms (b) 255.5 ms

(c) 255 ms (d) 300 ms

Common Data for Q.28 and 29

A hard disk has 63 sectors per track, 10 platters each with 2 recording surfaces and 1000 cylinders. The address of a sector is given as a triple (c, h, s), where c is the cylinder number, h is the surface number and s is the sector number. Thus, the 0^{th} sector is addressed as (0, 0, 0), the 1st sector as (0, 0, 1), and so on.

29. The address (400,16, 29) corresponds to sector number:

(a) 505035 (b) 505036

(c) 505037 (d) 505038

30. The address of 1039^{th} sector is

(a) (0, 15, 31) (b) (0, 16, 30)

(c) (0, 16, 31) (d) (0, 17, 31)

31. An application loads 100 libraries at start-up. Loading each library requires exactly one disk access. The seek time of the disk to a random location is given as 10 ms. Rotational speed of disk is 6000 rpm. If all 100 libraries are loaded from random locations on the disk, how long does it take to load all libraries? (The time to transfer data from the disk block once the head has been positioned at the start of the block may be neglected.)

(a) 0.50 s (b) 1.50 s

(c) 1.25 s (d) 1.00 s

❑❑❑

Answer Key

1. *Ans. (c)*
2. *Ans. (c)*
3. *Ans. (d)*
4. *Ans. (c)*
5. *Ans. (a)*
6. *Ans. (a)*
7. *Ans. (a)*
8. *Ans. (b)*
9. *Ans. (b)*
10. *Ans. (d)*
11. *Ans. (d)*
12. *Ans. (a)*
13. *Ans. (c)*
14. *Ans. (d)*
15. *Ans. (b)*
16. *Ans. (d)*
17. *Ans. (a)*
18. *Ans. (a)*

The daisy-chinning method of establishing priority consists of a serial connection of all devices that request an interrupt. The device with the highest priority is placed in the first position, followed by lower-priority devices up to the device with the lowest priority, which is placed last in the chain. The farther the device is from the first position, the lower is its priority. Therefore daisy-chain gives non-uniform priority to various devices.

19. *Ans. (c)*

5 bits	5 bits

5 bits to identify first and 5 bits to identify second including the case when one of them not present. So total bits required = 10

20. *Ans. (c)*

I/O redirection implies connection two programs through a pipe.

21. *Sol.*

(a), (b), (c), (d)

The major characteristics of a RISC processor are:

1. Relatively few instructions.
2. Relatively few addressing modes
3. More registers
4. Hardwired rather than micro programmed control

22. *Ans. (a)*

Total Size of micro instruction = 26 bits

Size of micro-operation =13 bits

Mux input = 8 bit

So select line field size Y $\Rightarrow 8 = 2^3 \Rightarrow 3$ bits

Next address field size =13 – 3

= 10 bits

Size of control memory

$= 2^{10} = 1024$

23. *Ans. (d)*

Data transfer rate = 10M bytes/sec

$= 10 \times 2^{10}$ Kbyte/sec

Size of transfer = 20 Kbytes

$10 \times 2^{10} \times x\% = 20$

$10 \times 2^{10} \times x/100 = 20$

$$x = \frac{20 \times 100}{10 \times 2^{10}}$$

$$x = \frac{200}{1024}$$

$x = 0.19\%$

or $x = 0.10\%$

24. *Ans. (a)*

Radius of inner track is 0.5 cm (where the head is standing) and the radius of outermost track is 4 cm. So the header has to seek (4 – 0.5) = 3.5 cm.

Head can move 10 meters/sec, It will take 3.5 ms to seek 3.5 cm.

Since 6000 RPM, In 1 rotation, it takes 10ms to read 20 sectors.

Angular velocity is constant and header is now end of 5th sector. To keep the head at the beginning of 4th sector it must rotate 18 sectors. If 20 sectors can read in 10 ms, 18 sectors can read in 9 ms.

In 1 Rotation, it takes 10ms to read 10MB data. To read 1MB data, we require 1 msec.

Total time required = 3.5 ms (to reach outermost track from innermost track) + 9 (to keep the head at the desired sector in the outermost track) + 1 ms (to read 10 MB data) Total time required = 13.5 msec

25. ***Ans. (b)***

$ET_{prog\text{-}IO}$: 10 kB $\Rightarrow$ 1 sec

1 B $\Rightarrow$? sec

$ET_{prog\text{-}IO}$ = 100 µsec

$ET_{INT\text{-}IO}$ = 4 µsec

S = 100/4 = 25

26. ***Ans. (b)***

Revolution Per minute = 3000 RPM

Or3000/60 = 50RPS

In one track rotation it can read = 512 KB

In 50 RPS it can read = 512 × 50

For 1 byte read = 1/(512 × 50) = 39.06 ns

$\Rightarrow$ For 4 bytes it takes 156 ns

Percentage of time that the CPU gets blocked during DMA operation = $\frac{40}{156} \times 100 \simeq 25\%$.

27. ***Ans. (a)***

No. of surfaces = 16

No. of tracks/sector = 128

No. of sector/track = 256

Total size of disk = 16 × 128 × 256 × 512 bytes

= $2^4 \times 2^7 \times 2^8 \times 2^9$ bytes

= $2^8 \times 2^{20}$ bytes

= 2^8 Mega bytes

= 256MB

28. ***Ans. (d)***

RPM = 600.

So, rotational delay = 60/600 = 0.1 sec.

In 1 rotation, we can transfer the whole data in a track.

Tack capacity = Track * bytes per track

= 100 * 500 = 50,000 bytes.

In 0.1 sec, we can transfer 50.000 bytes.

Hence time to transfer 250 bytes

= 0.1 * 250/ 50,000 = 0.5 ms

Avg. rotational delay = 0.5 * rotational delay

= 0.5 * 0.1s = 50 ms

Average seek time = (0 + 1 + 2 + ... + 499)/500 (as time to move between successive tracks is 1 ms and we have 500 such tracks)

= 499 * 250/ 500 = 249.5

Average time to transfer = Average seek time + Average rotational delay + Data transfer time Average time for transferring 250 bytes

= 249.5 + 50 + 0.5 = 300 ms.

29. ***Ans. (c)***

The address <400, 16, 29> corresponds to sector no.

400 × 2 × 10 × 63 + 16 × 63 + 29 = 505037

30. ***Ans. (c)***

The address <0, 16, 31> corresponds to sector no.

16 × 63 + 31 = 1039

31. ***Ans. (b)***

Rotational speed = 6000 rpm

Average latency = $\left(\frac{60\text{sec}}{6000}\right)/2$ = 5 msec

Avg access time

= Avg latency + Avg seek time

= 5 ms + 10 ms = 15 msec

Time to load 1 library is Avg latency + Avg seek time

= 15 msec

Time to load 100 libraries

= 100 × 15 msec

= 1.5 sec

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CHAPTER 5

INPUT AND OUTPUT INTERFACE

OBJECTIVE QUESTIONS

1. In daisy chain scheme for connecting input/output device which of the following statement is correct?
   (a) It gives non uniform priority to various devices
   (b) It gives uniform priority to all devices
   (c) Use to connect slow devices only to the processor
   (d) A separate interrupt pin on processor for each device
2. A multi – user, multi – processing operating system cannot be implemented on hardware that does not support
   (a) Address translation
   (b) DMA for disk transfer
   (c) Atleast two modes CPU execution (privileged and non – privileged)
   (d) all of the above
3. In serial communication employing 8 data bits, a parity bit and 2 stop bits, the minimum baud rate required to sustain a transfer rate of 300 characters per second is
   (a) 2400 baud (b) 19200 baud
   (c) 3300 baud (d) 1200 baud
4. An I/O processor controls the flow of information between
   (a) cache memory and I/O devices
   (b) main memory and I/O devices
   (c) two I/O devices
   (d) cache and main memories
5. The total size of address space in a virtual memory system is limited by
   (a) the length of MAR
   (b) the available secondary storage
   (c) the available main memory
   (d) all of the above
6. A CPU has two modes privileged and non privileged. In order to change the mode from privileged to non-privileged
   (a) A hardwired interrupt is needed
   (b) A software interrupt is needed
   (c) A privileged instruction is needed
   (d) A non-privileged instruction is needed
7. Which of the following is true and which one is false?
   1. Hard real time systems are required to complete a taks without any guarantee amount of time.
   2. Multilevel feedback queen scheduling allows a process to move between quinces.
   3. Turnaround time, waiting time and response time are to be minimum and CPU utilization ad throughput are to be maximized.
   (a) FFT (b) TFT
   (c) FTT (d) FTF
8. An I/O processor controls the flow of information between
   (a) Cache memory I/O device
   (b) Main memory and I/O devices
   (c) Two I/O devices
   (d) Cache and main memories
9. In the programmed I/O method , the CPU stays in a program loop to.....
   (a) Indicate that it is ready for data transfer
   (b) Indicate that it completed data transfer
   (c) Indicate that it completed data transfer
   (d) None of these

10. The An asynchronous serial communication controller that uses a start stop scheme for controlling the serial I/O of a system is programmed for a string of length 7 bit, one parity bit (odd parity) and one stop bit. the transmission rate us 1000 bits/second, then how many strings can be transmitted per second?

(a) 100 (b) 200

(c) 50 (d) 150

11. On receiving an interrupt from an I/O device, the CPU

(a) halts for a predetermined time

(b) hands over control of address bus and data bus to the interrupting device

(c) branches of the interrupt service routing immediately

(d) branches off the interrupt service routine after completion of the current instruction

12. Which of the following is/are functions of an I/O module?

1. Control and timing
2. Processor communication
3. Device communication
4. Data buffering
5. Error detection

(a) 1, 2 and 3 only (b) 1 and 2 only

(c) 1, 2, 3 and 4 only (d) All are true

13. In memory-mapped I/O _____

(a) The I/O devices and the memory share the same address space

(b) The I/O devices have a separate address space

(c) The memory and I/O devices have an associated address space

(d) A part of the memory is specifically set aside for the I/O operation

14. The usual BUS structure used to connect the I/O devices is _____

(a) Star BUS structure

(b) Multiple BUS structure

(c) Single BUS structure

(d) Node to Node BUS structure

15. In intel's IA-32 architecture there is a separate 16 bit address space for the I/O devices?

(a) False (b) True

16. The advantage of I/O mapped devices to memory mapped is _____

(a) The former offers faster transfer of data

(b) The devices connected using I/O mapping have a bigger buffer space

(c) The devices have to deal with fewer address lines

(d) No advantage as such

17. The system is notified of a read or write operation by _____

(a) Appending an extra bit of the address

(b) Enabling the read or write bits of the devices

(c) Raising an appropriate interrupt signal

(d) Sending a special signal along the BUS

18. To overcome the lag in the operating speeds of the I/O device and the processor we use _____

(a) Buffer spaces (b) Status flags

(c) Interrupt signals (d) Exceptions

19. The method of accessing the I/O devices by repeatedly checking the status flags is _____

(a) Program-controlled I/O

(b) Memory-mapped I/O

(c) I/O mapped

(d) None of the mentioned

20. The method of synchronising the processor with the I/O device in which the device sends a signal when it is ready is

(a) Exceptions (b) Signal handling

(c) Interrupts (d) DMA

21. The method which offers higher speeds of I/O transfers is _____

(a) Interrupts

(b) Memory mapping

(c) Program-controlled I/O

(d) DMA

22. The process wherein the processor constantly checks the status flags is called as

(a) Polling

(b) Inspection

(c) Reviewing

(d) Echoing

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Answer Key

1. *Ans. (a)*

   In daisy chain scheme or serial scheme all input/ output devices generate the interrupt so a higher priority input/output devices is firstly access the data from memory so it provice a non uniform priority to various devices.

2. *Ans. (d)*
3. *Ans. (c)*
4. *Ans. (b)*
5. *Ans. (a)*
6. *Ans. (b)*
7. *Ans. (c)*
8. *Ans. (b)*
9. *Ans. (a)*
10. *Ans. (a)*
11. *Ans. (d)*
12. *Ans. (d)*
13. *Ans. (a)*
14. *Ans. (c)*
15. *Ans. (b)*
16. *Ans. (c)*
17. *Ans. (d)*
18. *Ans. (b)*
19. *Ans. (a)*
20. *Ans. (c)*
21. *Ans. (d)*
22. *Ans. (a)*

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