

UNIT-IV

DIGITAL LOGICS

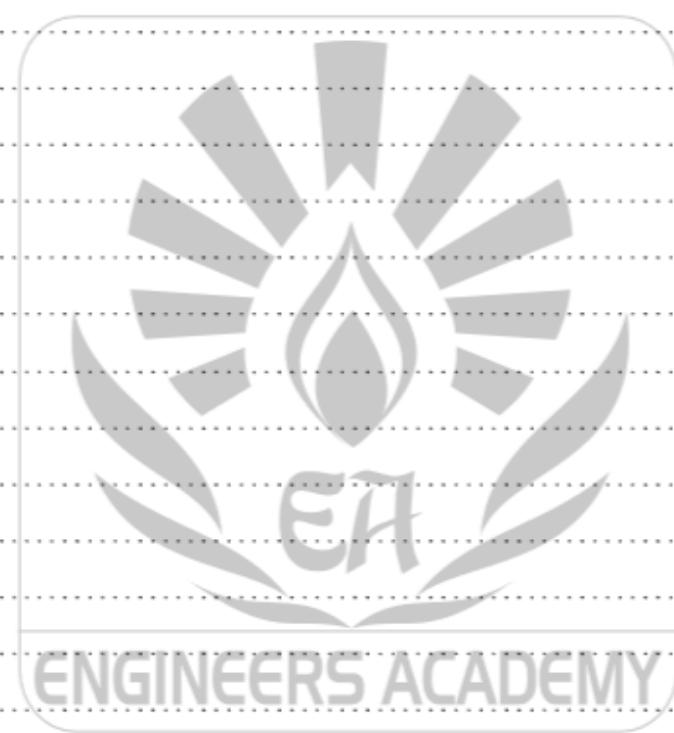
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NOTES

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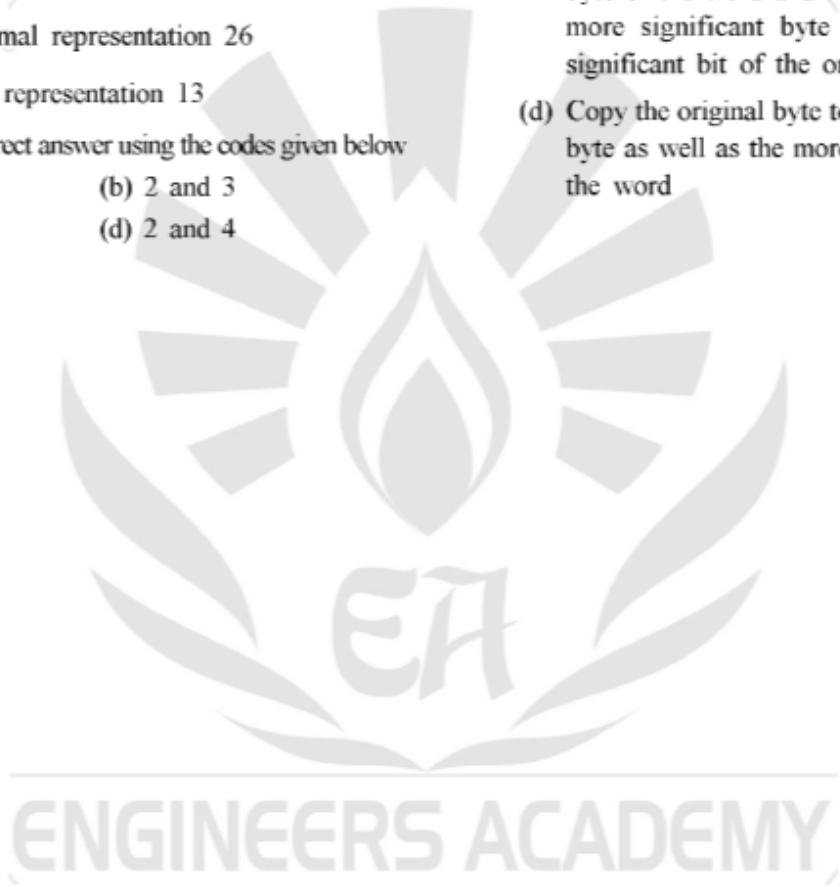
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NUMBER SYSTEM

OBJECTIVE QUESTIONS

1. The binary number 00001011 when represented in BCD format, is given by
 (a) 00001011 (b) 10111011
 (c) 00010001 (d) 10001000
2. When two numbers are added in excess-3 code and the sum is less than 9, then in order to get the correct answer it is necessary to
 (a) subtract 0011 from the sum
 (b) add 0011 to the sum
 (c) subtract 0110 from the sum
 (d) add 0110 to the sum
3. Gray code of the decimal number 13 is
 (a) 1010 (b) 1101
 (c) 1011 (d) 1001
4. The binary representation 100110 is numerically equivalent to
 (a) the decimal representation 46
 (b) the octal representation 46
 (c) the octal representation 26
 (d) the decimal representation 26
5. The number 7F in Hexadecimal number system is equivalent to the decimal number
 (a) 255 (b) 256
 (c) 128 (d) 127
6. Decimal 43 in Hexadecimal and BCD number system is respectively
 (a) B2, 0100 0011
 (b) 2B, 0100 0011
 (c) 2B, 0011 0100
 (d) B2, 0100 0100
7. The decimal value 0.25
 (a) is equivalent to the binary value 0.1
 (b) is equivalent to the binary value 0.01
 (c) is equivalent to the binary value 0.00111
 (d) cannot be represented precisely in binary
8. Which of the following operations do result in $(EA)_{16}$?
 1. $(AB)_{16} + (3F)_{16}$
 2. $(BC)_{16} - (CB)_{16}$
 3. $(FE)_{16} - (14)_{16}$
- Select the correct answer using the code given below
 (a) 1 and 2 (b) 1 and 3
 (c) 2 and 3 (d) 1, 2 and 3
9. Match List-I (Binary) with List-II (Decimal) and select the correct answer using the codes given below the lists
- | List-I | List-II |
|-------------|---------|
| A. 10101010 | 1. 128 |
| B. 11110000 | 2. 240 |
| C. 10001000 | 3. 170 |
| D. 10000000 | 4. 136 |
- Codes :**
- | A | B | C | D |
|-------|---|---|---|
| (a) 3 | 2 | 4 | 1 |
| (b) 2 | 3 | 1 | 4 |
| (c) 2 | 4 | 1 | 3 |
| (d) 3 | 1 | 2 | 4 |

10. What is the octal equivalent of decimal 0.3125?
- (a) 0.42 (b) 0.3125
 (c) 0.24 (d) 0.12
- Codes :
- | | A | B | C | D |
|-----|---|---|---|---|
| (a) | 3 | 1 | 4 | 2 |
| (b) | 1 | 2 | 3 | 4 |
| (c) | 3 | 2 | 4 | 1 |
| (d) | 4 | 1 | 2 | 3 |
11. Match List-I (Octal) with List-II (Binary) and select the correct answer using the codes given below the lists:
- | List-I | List-II |
|--------|-----------|
| A. 75 | 1. 010110 |
| B. 65 | 2. 110101 |
| C. 37 | 3. 111101 |
| D. 26 | 4. 011111 |
- Codes :**
- | | A | B | C | D |
|-----|---|---|---|---|
| (a) | 3 | 1 | 4 | 2 |
| (b) | 2 | 1 | 3 | 4 |
| (c) | 3 | 2 | 4 | 1 |
| (d) | 4 | 2 | 3 | 1 |
12. In hexadecimal arithmetic, the result of $(77)_{16} - (3B)_{16}$ is equal to
- (a) $3D_{16}$ (b) $3C_{16}$
 (c) 60_{16} (d) 73_{16}
13. The decimal equivalent of hexadecimal number 2A0F is
- (a) 17670 (b) 17607
 (c) 17067 (d) 10767
14. The binary equivalent of hexadecimal number 4F2D is
- (a) 0101 1111 0010 1100
 (b) 0100 1111 0010 1100
 (c) 0100 1110 0010 1101
 (d) 0100 1111 0010 1101
15. Match list-I (Hexadecimal) with list-II (Octal) and select the correct answer by using the codes given below the lists
- | List-I | List-II |
|--------|---------|
| A. 68 | 1. 150 |
| B. 8C | 2. 214 |
| C. 4F | 3. 117 |
| D. 5D | 4. 135 |
16. F's complement of $(2BFD)_{16}$ is
- (a) E 304 (b) D 403
 (c) D 402 (d) C 403
17. Given $(125)_R = (203)_5$, the value of radix R will be
- (a) 16 (b) 10
 (c) 8 (d) 6
18. If $(327)_9 = (X)_5$, then the value of X is given by
- (a) 327 (b) 268
 (c) 2033 (d) 3302
19. Which of the following is a self-complementing code?
- (a) 8421 code (b) Excess 3 code
 (c) Pure binary code (d) Gray code
20. Which one of the following is a non-valid BCD code?
- (a) 0111 1001 (b) 0101 1011
 (c) 0100 (d) 0100 1001
21. An equivalent 2's complement representation of the 2's complement number 1101 is
- (a) 110100 (b) 001101
 (c) 110111 (d) 111101
22. The greatest negative number which can be stored in a 8-bit register using 2's complement arithmetic is
- (a) -256 (b) -255
 (c) -127 (d) -128
23. The binary number 111 represents
- (a) -3 in sign magnitude system and -1 in two's complement system
 (b) 7 in signs magnitude system and -1 in two's complement system
 (c) -3 in sign magnitude system and -3 in two's complement system
 (d) 7 in signs magnitude system and -3 in two's complement system.



□ □ □

- 2BFD

D402

Hence F's complement of $(2BFD)_{16}$ is D40217. *Ans. (d)*

$$(125)_R = (203)_5$$

We convert both sides into decimal equivalents

$$1 \times R^2 + 2R^1 + 5 \times R^0 = 2 \times 5^2 + 3 \times 5^0$$

$$R^2 + 2R + 5 = 50 + 3$$

$$R^2 + 2R - 48 = 0$$

$$R^2 + 8R - 6R - 48 = 0$$

$$R(R+8) - 6(R+8) = 0$$

$$R = 6, -8$$

Hence positive value of R is 6 which is radix.

18. *Ans. (c)*

$$(327)_9 = (X)_5$$

To get value of x, we first convert left side into its decimal equivalent.

$$\begin{aligned}(327)_9 &= 3 \times 9^2 + 2 \times 9^1 \times 7 \times 9^0 \\&= 243 + 18 + 7 \\&= (268)_{10}\end{aligned}$$

Now we convert this decimal number into base 5 by 5 progressively

		Generated Integer
5	268	3
5	53	3
5	10	3
5	2	0
		2

$= (2033)_5$

Hence $X = 2033$ **Note :** Any number with any base r can be converted to decimal number and vice-versa.**(i) Decimal to Base r :** For integer part divide the decimal number by r progressively. For fractional part multiply by r progressively.**(ii) Base r to Decimal :** Multiply each digit by its corresponding weight and add all.19. *Ans. (b)*

The Excess-3 code is a self complementing code.

Note :

- 2421 code is also a self complementing code.
- A code is called a self complementing code if l's complement of the coded number yield 9's complement of the number itself.

20. *Ans. (b)*21. *Ans. (d)*22. *Ans. (d)*23. *Ans. (a)*24. *Ans. (a)*25. *Ans. (c)*26. *Ans. (c)*27. *Ans. (c)*

$$2C\ H + 4F\ H = 7B\ H$$

$$5E\ H + 1A\ H = 78\ H$$

$$3B\ H + 6D\ H = A8\ H$$

$$5A\ H + 2C\ H = 86\ H$$

28. *Ans. (d)*29. *Ans. (c)*

2	28
2	14-0
2	7-0
2	3-1
	1-1

$$(28)_{10} = (11100)^2$$

$$+28 = 011100$$

 \downarrow 2's complement

$$-28 = 011100$$

 \rightarrow 2's complement :

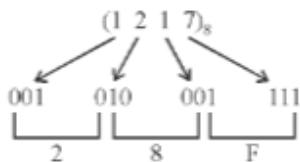
To represent in 16 bits, using sign extension

place 1's at MSB for Negative numbers.

$$(-28)_{10} = [1111\ 1111\ 1110\ 0100]_2$$

30. *Ans. (b)*

$$(1217)_8 = (028F)_{16}$$



31. *Sol.*

**Given number in
No. is -ve 2's complement form**
0000 0000 0000 1011 ← 2's of the number.

∴ Decimal equivalent is -11.

32. *Ans (c)*

$$00\ 1111\ 00\ 110\ 110\ 1000.....0$$

$$S = 0, E = 01111100, M = 11011010.....0$$

$$\text{Expression value} = (-1)^S \times 1.M \times 2^{E-127}$$

$$\begin{aligned} &= (-1) \times 1.110110100 \times 2^{-3} = 1.85_{10} \times \frac{1}{8} \\ &= 0.23 = 2.3 \times 10^{-1} \end{aligned}$$

33. *Ans. (a)*

$$\begin{aligned} (123456)_8 &= (001\ 010\ 011\ 100\ 101\ 110)_2 \\ &= (00\ 1010\ 0111\ 0010\ 1110)_2 \\ &= (A72E)_{16} \\ &= (00\ 10\ 10\ 01\ 11\ 00\ 10\ 11\ 10)_2 \\ &= (22130232)_4 \end{aligned}$$

34. *Ans. (a, b)*

Zero has two representations in

(a) Sign magnitude as

- (i) 0000
- (ii) 1000

(b) 1's complement as

- (i) 0000
- (ii) 1111

35. *Sol.*

Number of bits n = 16

In sign 2's complement representation the range is

$$\begin{aligned} &= -2^{15} \text{ to } + (2^{15} - 1) \\ &= -32768 \text{ to } + 32767 \end{aligned}$$

$$\therefore X = 65536$$

In sign magnitude representation the range is

$$\begin{aligned} &= -(2^{15} - 1) \text{ to } + (2^{15} - 1) \\ &= -32767 \text{ to } + 32767 \end{aligned}$$

$$\therefore Y = 65535$$

Hence, X - Y = 1

36. *Ans. (a)*

$$\begin{aligned} \text{1's complement range} &= -(2^{n-1} - 1) \text{ to } (2^{n-1} - 1) \\ &= -(2^5 - 1) \text{ to } (2^5 - 1) \\ &= -31 \text{ to } 31 \end{aligned}$$

37. *Ans. (a)*

To represent decimal number into BCD number each decimal number is represented in 4-bits while converting in BCD numbers, as

$$1 \rightarrow 0001 \quad 3 \rightarrow 0011$$

$$8 \rightarrow 1000 \quad 5 \rightarrow 0101$$

$$5 \rightarrow 0101 \quad 7 \rightarrow 0111$$

$$6 \rightarrow 0110$$

$$(1856357) = \underbrace{0000}_{1\text{byte}} \quad \underbrace{00011000}_{1\text{byte}} \quad \underbrace{0101}_{1\text{byte}}$$

$$\underbrace{0110}_{1\text{byte}} \quad \underbrace{00110101}_{1\text{byte}} \quad \underbrace{0111}_{1\text{byte}}$$

So total 4 bytes are required.

38. *Ans. (a)*

We have to find out the number of 1's in the binary representation of

$$(4 \times 4096) + (9 \times 256) + (7 \times 16) + 5$$

This is a decimal number

Now, we can write this decimal number as

$$4 \times 16^3 + 9 \times 16^2 + 7 \times 16^1 + 5 \times 16^0 = (4975)_{16}$$

then we convert this hexadecimal number as

$$(4 \quad 9 \quad 7 \quad 5)_{16}$$

↓ ↓ ↓ ↓

$$(0100 \quad 1001 \quad 0111 \quad 0101)_2$$

Then total number of 1's are 8.

39. *Ans. (b)*

$$\begin{aligned} 1. (100110)_2 &= 1 \times 2^5 + 0 \times 2^4 + 0 \times 2^3 + 1 \times 2^2 \\ &\quad + 1 \times 2^1 + 0 \times 2^0 \\ &= 32 + 4 + 2 = 38 \end{aligned}$$

$$\therefore (100110)_2 = (38)_{10}$$

2. 100 110 forming groups of 3 bits
4 6

$$(100110)_2 = (46)_8$$

3. By forming groups of 4 bits, we get $\frac{0010}{2} \quad \frac{0110}{6}$

$$(100110)_2 = (26)_{16}$$

$$\begin{array}{r} \text{Decimal} \quad 1 \quad 3 \\ \text{Add 3 to each bit} \quad \underline{+3} \quad \underline{+3} \\ \hline 4 \quad 6 \end{array}$$

Converting the above sum into its BCD

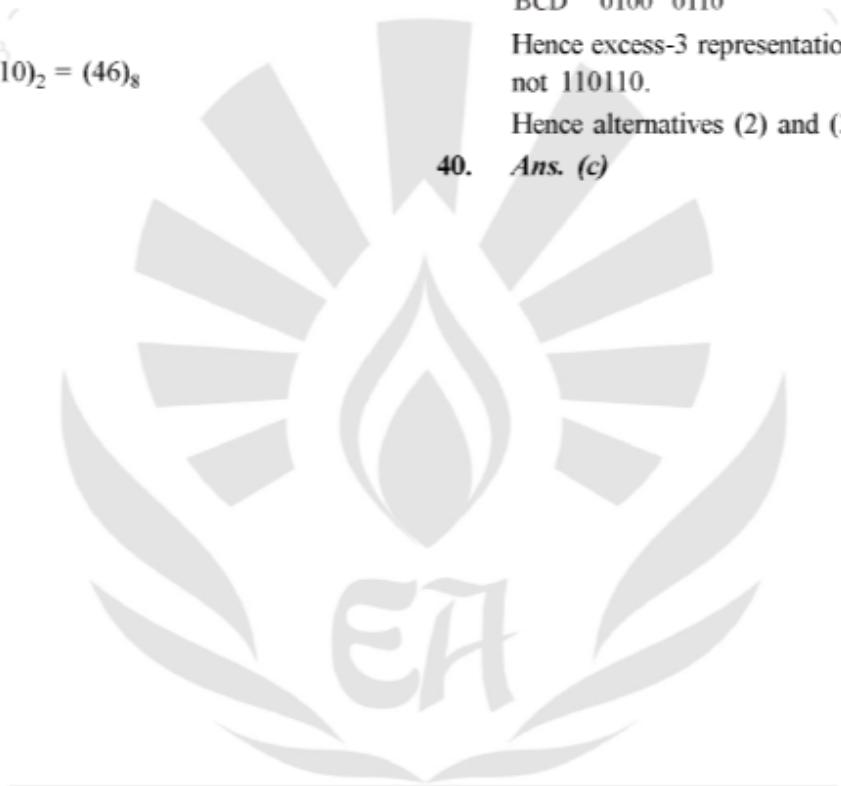
We have

$$\begin{array}{l} \text{Sum} \rightarrow \quad 4 \quad 6 \\ \text{BCD} \quad \downarrow \quad \downarrow \\ 0100 \quad 0110 \end{array}$$

Hence excess-3 representation of 13 is 1000110 not 110110.

Hence alternatives (2) and (3) are correct only.

40. *Ans. (c)*



ENGINEERS ACADEMY

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MINIMIZATION

OBJECTIVE QUESTIONS

CHAPTER

2

1. With 4 Boolean variables, how many Boolean expressions can be formed?
 - (a) 16
 - (b) 256
 - (c) 1024 (1K)
 - (d) 64 K (64×1024)
2. For the product-of-sums expression $L = (X + Y)(\bar{X} + \bar{Z})$, the equivalent sum-of-products expression will be
 - (a) $XY + \bar{X}\bar{Z}$
 - (b) $\bar{X}\bar{Y} + XZ$
 - (c) $\bar{X}Y + X\bar{Z}$
 - (d) $X\bar{Y} + \bar{X}Z$
3. A, B and C are three Boolean variables. Which one of the following Boolean expressions cannot be minimized any further?
 - (a) $Z = A\bar{B}\bar{C} + A\bar{B}\bar{C} + ABC + \bar{A}\bar{B}\bar{C}$
 - (b) $Z = A\bar{B}\bar{C} + A\bar{B}\bar{C} + ABC + \bar{A}\bar{B}\bar{C}$
 - (c) $Z = A\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C} + ABC + \bar{A}\bar{B}\bar{C}$
 - (d) $Z = \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} + ABC + \bar{A}\bar{B}\bar{C}$
4. While obtaining minimal sum of products expression
 - (a) all don't cares are ignored
 - (b) all don't cares are treated as logic ones
 - (c) all don't cares are treated as logic zeros
 - (d) only such don't cares that aid minimization are treated as logic ones
5. The product-of-sum expression for given truth table is

X	Y	Z
0	0	1
0	1	0
1	0	1
1	1	0
6. If X, Y and Z are Boolean variables, then the expression $X(X + \bar{X}Y) + Z(X + Y + Z)$ is equal to
 - (a) $X + \bar{X}Y$
 - (b) $X + Y + Z$
 - (c) XYZ
 - (d) XZ
7. In boolean algebra if $F = (A + B)(\bar{A} + C)$. Then
 - (a) $F = AB + \bar{A}C$
 - (b) $F = AB + \bar{A}\bar{B}$
 - (c) $F = AC + \bar{A}B$
 - (d) $F = A\bar{A} + \bar{A}B$
8. The logical expression $y = A + \bar{A}B$ is equivalent to
 - (a) $y = AB$
 - (b) $y = \bar{A}B$
 - (c) $y = \bar{A} + B$
 - (d) $y = A + B$
9. The Boolean function $A + BC$ is a reduced form of
 - (a) $AB + BC$
 - (b) $(A + B)(A + C)$
 - (c) $\bar{A}B + A\bar{B}C$
 - (d) $(A + C)B$
10. Boolean expression for the output of XNOR (Equivalent) logic gate with inputs A and B is
 - (a) $A\bar{B} + \bar{A}B$
 - (b) $\bar{A}\bar{B} + AB$
 - (c) $(\bar{A} + B)(A + \bar{B})$
 - (d) $(\bar{A} + \bar{B})(A + B)$

11. The simplified form of the Boolean expression $Y = (\bar{A}\bar{B}C + D)(\bar{A}\bar{D} + \bar{B}\bar{C})$ can be written as
 (a) $\bar{A}\bar{D} + \bar{B}\bar{C}D$
 (b) $A\bar{D} + B\bar{C}D$
 (c) $(\bar{A} + D)(\bar{B}C + \bar{D})$
 (d) $A\bar{D} + BCD$
12. The logic $Y = AB + \bar{A} + \bar{B}$ is equivalent to
 (a) $Y = AB$ (b) $Y = \bar{A} + \bar{B}$
 (c) $Y = 1$ (d) $Y = 0$
13. The logic function $f = \overline{(xy)} + \overline{(x\bar{y})}$ is the same as
 (a) $f = (x+y)(\bar{x}+\bar{y})$
 (b) $f = \overline{(\bar{x}+\bar{y})} + (x+y)$
 (c) $f = \overline{(xy)}(xy)$
 (d) None of the above
14. According to boolean algebra, $(A + \bar{B} + \bar{A}B)$ equal to
 (a) 1 (b) 0
 (c) $A\bar{B}$ (d) $\bar{A}B$
15. The simplified form of Boolean function $(\bar{A} + B)(A + \bar{C})(\bar{B} + \bar{C})$ is
 (a) $(A + B)\bar{C}$ (b) $(A + \bar{B})\bar{C}$
 (c) $(\bar{A} + B)\bar{C}$ (d) $(\bar{A} + \bar{B})\bar{C}$
16. The complement of boolean expression $F = (X + \bar{Y} + Z)(\bar{X} + \bar{Z})(X + Y)$ is
 (a) $XYZ + X\bar{Z} + \bar{Y}Z$ (b) $\bar{X}Y\bar{Z} + XZ + \bar{X}\bar{Y}$
 (c) $\bar{X}Y\bar{Z} + XZ + \bar{Y}\bar{Z}$ (d) $XYZ + \bar{X}\bar{Y}$
17. In the logic equation

$$A(A + \bar{B}C + C) + \bar{B}(C + \bar{A} + BC) + (A + \bar{B}C + A\bar{C}) = 1$$
 if $C = \bar{A}$ then
 (a) $A + B = 1$ (b) $\bar{A} + B = 1$
 (c) $A + \bar{B} = 1$ (d) $A = 1$
18. A Boolean function can be expressed
 (a) as sum of maxterms or product of minterms
 (b) as product of maxterms or sum of minterms
 (c) parity as product of maxterms and partly as sum minterms
 (d) partly as sum of maxterms and partly os minterms
19. The minimized form of the Boolean expression $F(A, B, C) = \prod (0, 2, 3)$ is
 (a) $A + \bar{B}C$ (b) $A + B\bar{C}$
 (c) $\bar{A}\bar{C} + B$ (d) $\bar{A}\bar{B}\bar{C} + AB$
20. The reduced form of the Boolean expression $A[B + C(\bar{A}B + AC)]$ is
 (a) $\bar{A}B$ (b) $A\bar{B}$
 (c) AB (d) $AB + B\bar{C}$
21. The Karnaugh map for a four variable boolean function is given in figure. The correct boolean sum of product is
- | | PQ | 00 | 01 | 11 | 10 |
|----|----|----|----|----|----|
| RS | 00 | 0 | 0 | 0 | 0 |
| | 01 | 1 | 0 | 0 | 1 |
| | 11 | 1 | 0 | 0 | 1 |
| | 10 | 0 | 1 | 0 | 0 |
- (a) $PQRS + \bar{Q}S$
 (b) $\bar{P}QR\bar{S} + \bar{Q}S$
 (c) $PQR + Q\bar{S}$
 (d) $PQRS + \bar{Q}$
22. The minimal sum of products form of $f = \bar{A}\bar{B}CD + \bar{A}BC + BCD$ is
 (a) $\bar{A}C + BD$ (b) $ACD + \bar{A}BC$
 (c) $AC + \bar{B}D$ (d) $A\bar{B} + C\bar{D}$

23. Which one of the following is the dual-form of the Boolean identity $AB + \bar{A}C = (A + C)(\bar{A} + B)$
- $AB + \bar{A}C = AC + \bar{A}B$
 - $(A + B)(\bar{A} + C) = (A + C)(\bar{A} + B)$
 - $(A + B)(\bar{A} + C) = AC + \bar{A}B$
 - $AB + \bar{A}C = AB + \bar{A}C + BC$
24. The number of switching function of 3 variables is
- 8
 - 64
 - 128
 - 256
25. $Y = f(A, B) = \prod M(0, 1, 2, 3)$ represents (M is Maxterm)
- NOR gate
 - NAND gate
 - OR gate
 - a situation where output is independent of input
26. The simplified form of a logic function $(\bar{A}\bar{B})(\bar{A}B)$ is
- 1
 - AB
 - $\bar{A} + \bar{B}$
 - $\bar{A}B + A\bar{B}$
27. Two Boolean expression are given below out of these in
- $(X + Y)(X + Z) = X + YZ$
 - $X(X + Y) = X$
- both 1 and 2 are correct
 - both 1 and 2 are wrong
 - 1 is correct but 2 is wrong
 - 1 is wrong but 2 is correct
28. The boolean expression $\bar{Y}Z + \bar{X}Z + \bar{X}Y$ is logically equivalent to
- \overline{XYZ}
 - $YZX + \overline{XYZ}$
 - $YZ + XZ + XY$
 - $\overline{XYZ} + \overline{XYZ} + \overline{XY}Z + \overline{XYZ}$
29. Which of the following statements is not correct?
- $x + \bar{x}y = x$
 - $x(\bar{x} + y) = xy$
 - $x + xy = x$
 - $zx + z\bar{x}y = zx + zy$
30. The boolean expression $(X + Y)(X + \bar{Y}) + (\bar{X}\bar{Y}) + \bar{X}$ simplifies to
- X
 - Y
 - XY
 - $X + Y$
31. What is dual of $X + \bar{X}Y = X + Y$
- $X + Y = XY$
 - $\bar{X} + XY = XY$
 - $X(\bar{X} + Y) = XY$
 - $X(\bar{XYZ} + XYZ + \bar{XYZ})$
32. What is dual of $A + [B(A + C)] + D$
- $A + [(B(A + C)] + C$
 - $A[B + AC]D$
 - $A + [B(A + C)]D$
 - $A[B(A + C)]D$
33. The boolean expression $F(X, Y, Z) = \bar{X}Y\bar{Z} + \bar{X}\bar{Y}\bar{Z} + XY\bar{Z} + XYZ$ converted into canonical product of sum (POS) form is
- $(X + Y + Z)(X + Y + \bar{Z})(X + \bar{Y} + \bar{Z})(\bar{X} + Y + \bar{Z})$
 - $(X + \bar{Y} + Z)(\bar{X} + Y + \bar{Z})(\bar{X} + \bar{Y} + Z)(\bar{X} + \bar{Y} + \bar{Z})$
 - $(X + Y + Z)(\bar{X} + \bar{Y} + \bar{Z})(X + \bar{Y} + Z)(\bar{X} + \bar{Y} + \bar{Z})$
 - $(X + \bar{Y} + \bar{Z})(\bar{X} + Y + Z)(\bar{X} + \bar{Y} + Z)(X + Y + Z)$
34. If $X = 1$ in the logic equation $[X + Z\{\bar{Y} + (\bar{Z} + X\bar{Y})\}] = 1$ then
- $Y = Z$
 - $Y = \bar{Z}$
 - $Z = 1$
 - $Z = 0$



ANSWER KEY

1. *Ans. (d)*

With n Boolean variables, we can form (2^{2^n}) different Boolean expression.

For $n = 4$

We can form

$$2^{2^4} = 2^{16} = 2^6 \times 2^{10}$$

Since $2^{10} = 1\text{ K}$ or 1024

$$\therefore 2^6 \times 2^{10} = 64\text{ K}$$

or (64×1024) Boolean expressions.

2. *Ans. (c)*

We are provided with the POS expression

$$\begin{aligned} L &= (\bar{X} + \bar{Z})(X + Y)I \\ &= (\bar{X} + \bar{Z})(X + Y)(X + \bar{X}) \\ L &= (\bar{X} + \bar{Z})(X + \bar{X}Y) \\ &= \bar{X}Y + \bar{Z}X + \bar{X}Y\bar{Z} \\ L &= \bar{X}Y(1 + \bar{Z}) + \bar{Z}X \\ &= \bar{X}Y + \bar{Z}X \end{aligned}$$

3. *Ans. (c)*

4. *Ans. (d)*

A function with don't care combinations is simplified to obtain minimal SOP expression the value can be assigned to selected don't care combination. This is done order to increase the number of 1's in the selected groups, wherever further simplification is possible.

Also, a don't care combination need not be used in grouping if it does not cover a large number of 1's.

5. *Ans. (b)*

X	Y	Z
0	0	1
0	1	$0 \rightarrow (X + \bar{Y})$
1	0	1
1	1	$0 \rightarrow (\bar{X} + \bar{Y})$

$$F = (X + \bar{Y})(\bar{X} + \bar{Y})$$

6. *Ans. (d)*

$$\begin{aligned} X(X + \bar{X}Y)Z(X + Y + Z) \\ &= (XX + X\bar{X}Y)Z(X + Y + Z) \\ &= (X + 0)Z(X + Y + Z) \\ &= ZXZ + XZY + XZZ \\ &= XZ + XZY + XZ \\ &= XZ [1 + Y + 1] \\ &= XZ[1] \\ &= XZ \end{aligned}$$

7. *Ans. (c)*

$$\begin{aligned} F &= (A + B)(\bar{A} + C) \cdot I \\ F &= (A + B)(\bar{A} + C)(A + \bar{A}) \\ F &= (A + B)(\bar{A} + AC) \\ F &= \bar{A}B + AC + ABC \\ &= \bar{A}B + AC(I + B) \\ F &= \bar{A}B + AC \end{aligned}$$

8. *Ans. (d)*

$$\begin{aligned} Y &= A + \bar{A}B \\ &= (A + \bar{A})(A + B) \\ &= (A + B) \end{aligned}$$

9. *Ans. (b)*

$$A + BC = (A + B)(A + C) \quad (\text{distributive property})$$

10. *Ans. (c)*

$$\begin{aligned} Y &= AB + \bar{A}\bar{B} \\ &= (AB + \bar{A})(AB + \bar{B}) \\ &= (\bar{A} + A)(\bar{A} + B)(\bar{B} + B)(\bar{B} + A) \\ Y &= (\bar{A} + B)(A + \bar{B}) \end{aligned}$$

11. *Ans. (a)*

$$\begin{aligned} (\bar{A}BC + D)(\bar{A}D + \bar{B}\bar{C}) \\ &= (\bar{A}BC)(\bar{A}D) + (\bar{A}BC)(\bar{B}\bar{C}) + D(\bar{A}D) + D(\bar{B}\bar{C}) \\ &= \bar{A}BCD + 0 + D\bar{A} + \bar{B}CD \\ &= \bar{A}D(I + BC) + \bar{B}CD \\ &= \bar{A}D + \bar{B}CD \end{aligned}$$

12. Ans. (c)

$$\begin{aligned} Y &= AB + \bar{A} + \bar{B} \\ &= (\bar{A} + B) + \bar{B} \\ &= \bar{A} + 1 \\ &= 1 \end{aligned}$$

13. Ans. (d)

$$\begin{aligned} f &= \overline{(xy)} + \overline{(xy)} \\ &= \overline{(xy)(xy)} \\ &= \overline{(x+y)(x+y)} \\ &= \overline{xx} + \overline{x}\overline{y} + xy + y\overline{y} \\ &= 0 + \overline{x}\overline{y} + xy + 0 \\ &= \overline{x}\overline{y} + xy \end{aligned}$$

14. Ans. (a)

$$\begin{aligned} Y &= A + \bar{B} + \bar{A}B \\ &= A + (\bar{B} + \bar{A}B) \\ &= A + (\bar{B} + \bar{A})(\bar{B} + B) \\ &= A + (\bar{B} + \bar{A})I \\ &= A + \bar{A} + \bar{B} \\ &= 1 + \bar{B} \\ &= 1 \end{aligned}$$

15. Ans. (c)

$$\begin{aligned} (\bar{A} + B)(A + \bar{C})(\bar{B} + \bar{C}) &= (\bar{A} + B)(A\bar{B} + A\bar{C} + \bar{C}B + \bar{C}\bar{C}) \\ &= (\bar{A} + B)(A\bar{B} + A\bar{C} + \bar{C}B + \bar{C}) \\ &= (\bar{A} + B)[(A\bar{B} + (A + \bar{B} + 1)\bar{C})] \\ &= (\bar{A} + B)[A\bar{B} + \bar{C}] \\ &= (\bar{A} + B)(A\bar{B}) + (\bar{A} + B)\bar{C} \\ &= \bar{A}(A\bar{B}) + B(A\bar{B}) + (\bar{A} + B)\bar{C} \\ &= 0 + 0 + (\bar{A} + B)\bar{C} \\ &= (\bar{A} + B)\bar{C} \end{aligned}$$

16. Ans. (b)

17. Ans. (c)

18. Ans. (b)

19. Ans. (a)

20. Ans. (c)

$$F = A[B + C(\overline{AB} + \overline{AC})]$$

$$F = A[B + C\overline{A}(\overline{B} + \overline{C})]$$

$$F = A[B + C(\bar{A} + \bar{B}\bar{C})]$$

$$F = AB + AC[\bar{A} + \bar{B}\bar{C}]$$

$$F = AB$$

21. Ans. (b)

		PQ	00	01	11	10
		RS	00	01	11	10
		00	0	0	0	01
		01	1	0	0	1
		11	1	0	0	1
		10	0	(1)	0	0

$$Y = \bar{Q}S + \bar{P}QRS$$

22. Ans. (b)

23. Ans. (c)

24. Ans. (d)

For n variables, the number of switching functions

$$= 2^{2^n}$$

$$\text{For } n = 3$$

$$\text{Number of switching functions} = 2^{2^3} = 2^8 = 256$$

25. Ans. (d)

$$Y = f(A, B) = \prod M (0, 1, 2, 3)$$

A		0	1	
B		0	0	
0		0	0	
1		0	0	

⇒ = y = 0

Thus output is 0 for all inputs. It is independent of the input.

26. Ans. (a)

$$\begin{aligned}
 Y &= \overline{(AB)(\bar{A}B)} \\
 &= \overline{(\bar{A}B)} + \overline{(\bar{A}B)} \\
 &= \overline{\overline{\bar{A}}} + \overline{\overline{\bar{B}}} + \overline{\overline{\bar{A}}} + \overline{\overline{\bar{B}}} \\
 &= A + B + A + \bar{B} \\
 &= A + (B + \bar{B}) \\
 &= A + 1 = 1
 \end{aligned}$$

27. Ans. (a)

28. Ans. (a)

29. Ans. (a)

30. Ans. (a)

Let $F = (X + Y)(X + \bar{Y}) + \overline{(XY + \bar{X})}$

$$\begin{aligned}
 F &= X + X\bar{Y} + XY + \overline{(XY\bar{X})} \\
 &= X + (\bar{X} + Y)X \\
 &= X + XY = X
 \end{aligned}$$

31. Ans. (c)

$$X + \bar{X}Y = X + Y$$

Its dual will be

$$X[\bar{X} + Y] = XY$$

32. Ans. (b)

$$F = A + [B(A + C)] + D$$

then its dual will be

$$F_D = A[B + AC]D$$

33. Ans. (a)

$$F(X, Y, Z) = \bar{X}Y\bar{Z} + X\bar{Y}\bar{Z} + XY\bar{Z} + XYZ$$

		YZ	00	01	11	10	
		X	0	$\boxed{0}$	$\boxed{0}$	$\boxed{0}$	1
0	1	1	$\boxed{0}$	1		1	

$$F = (X + Y + Z)(X + Y + \bar{Z})(X + \bar{Y} + \bar{Z})$$

$$(\bar{X} + Y + \bar{Z})$$

34. Ans. (d)

$$\underbrace{[x + z(\bar{y} + (\bar{z} + xy))]}_1 \underbrace{[\bar{x} + \bar{z}(x + y)]}_z = 1$$

$$\bar{Z} = 1$$

$$Z = 0$$



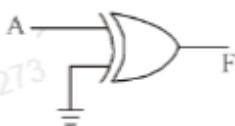
LOGIC GATES

CHAPTER

3

OBJECTIVE QUESTIONS

1. The output of the logic gate in figure is



- (a) 0 (b) 1
 (c) A (d) F

2. The balance equation $Z = \bar{A}\bar{B} + \bar{A}B$ can be realized using only

- (a) AND gates (b) OR gates
 (c) NAND gates (d) NOT gates

3. Match List-I with List-II and select the correct answer using the codes given below the Lists

List-I

- | | |
|---------------------------|------------------------------|
| A. $A \oplus B = 0$ | 1. $A \neq B$ |
| B. $\overline{A + B} = 0$ | 2. $A = B$ |
| C. $\bar{A}B = 0$ | 3. $A = 1 \text{ OR } B = 1$ |
| D. $A \oplus B = 1$ | 4. $A = 1 \text{ OR } B = 0$ |

List-II

3. A NAND gate is equivalent to an OR gate with its outputs inverted.

4. A NOR gate is equivalent to an AND gate with its outputs inverted.

Which of these statements are correct?

- (a) 1 and 2 (b) 2 and 3
 (c) 3 and 4 (d) 1 and 4

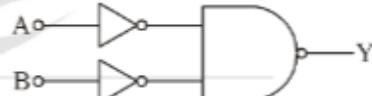
5. Which logic gate is similar to the function of two series switches connected in a circuit

- (a) AND (b) OR
 (c) NAND (d) All of these

6. When an input signal $A = 100101$ is applied to a NOT gate, its output is

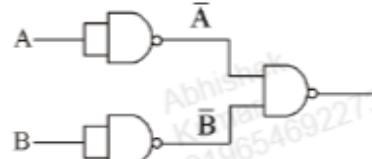
- (a) 100100 (b) 000101
 (c) 100101 (d) 011010

7. The logic circuit shown below, is equivalent to a



- (a) NOR gate (b) OR gate
 (c) AND gate (d) NAND gate

8. What would be the output of circuit built using NAND gates shown in figure given below

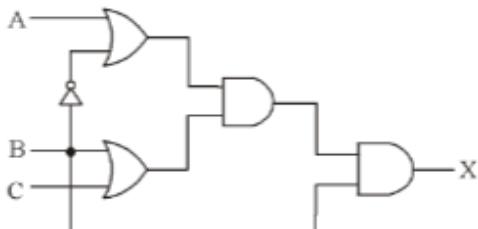


- (a) AB (b) A + B
 (c) $\bar{A} + \bar{B}$ (d) $\bar{A}\bar{B} + \bar{A}\bar{B}$

4. Consider the following statements :

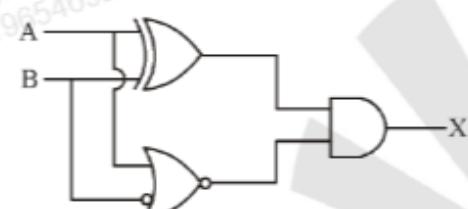
1. A NAND gate is equivalent to an OR gate with its inputs inverted.
2. A NOR gate is equivalent to an AND gate with its inputs inverted.

9. The output X of the logic circuit shown in the figure is



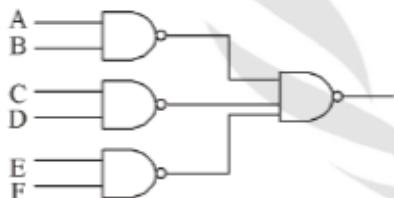
- (a) $A + BC$ (b) BC
 (c) AB (d) $AB + C$

10. The output X of the circuit shown in the figure will be



- (a) AB (b) $\bar{A}B$
 (c) $\bar{A}\bar{B}$ (d) $\bar{A}\bar{B}$

11. The output of the gated network shown in the figure is



- (a) $(\bar{A}\bar{B})(\bar{C}\bar{D})(\bar{E}\bar{F})$
 (b) $\bar{A}\bar{B} + \bar{C}\bar{D} + \bar{E}\bar{F}$
 (c) $AB + CD + EF$
 (d) $(A + B)(C + D)(E + F)$

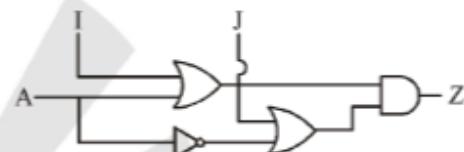
12. Which one of the following is equivalent of AND-OR realization.

- (a) NAND-NOR realization
 (b) NOR-NOR realization
 (c) NOR-NAND realization
 (d) NAND-NAND realization

13. The Boolean expression $X(P, Q, R) = \prod(0, 6)$ is to be realized using only two 2 input gates. Which are these gates?

- (a) AND and OR
 (b) NAND and OR
 (c) AND and XOR
 (d) OR and XOR

14. The circuit shown above is to be used to implement the function $Z = f(A, B) = \bar{A} + B$. What values are to be selected for I and J?

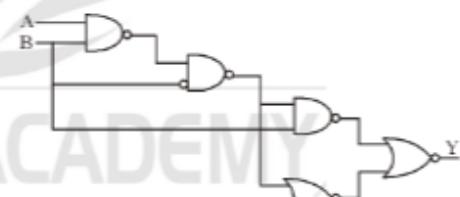


- (a) $I = 0, J = B$ (b) $I = 1, J = B$
 (c) $I = B, J = 1$ (d) $I = B, J = 0$

15. Boolean expression for the output of X-NOR (Equivalent) logic gate with inputs A and B is

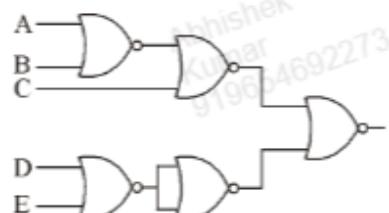
- (a) $A\bar{B} + \bar{A}B$ (b) $\bar{A}\bar{B} + AB$
 (c) $(\bar{A} + B)(A + \bar{B})$ (d) $(\bar{A} + \bar{B})(A + B)$

16. For the logic circuit shown in figure, the simplified Boolean expression for the output Y is



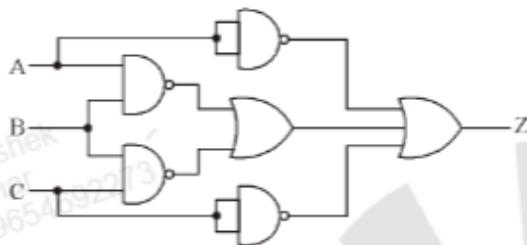
- (a) $A + B + C$ (b) A
 (c) B (d) C

17. The circuit shown in the given figure realizes the function



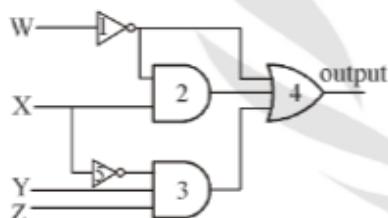
- (a) $(\overline{A+B}+C)(\overline{D}\overline{E})$
 (b) $(\overline{A+B}+C)(D\overline{E})$
 (c) $(A+\overline{B+C})(\overline{D}E)$
 (d) $(A+B+\overline{C})(\overline{D}\overline{E})$

18. In the given combinational circuit, the output Z is



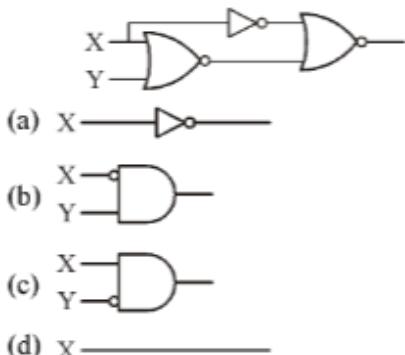
- (a) $\overline{A}+\overline{B}+\overline{C}$ (b) \overline{ABC}
 (c) $\overline{AB}+\overline{BC}+\overline{AC}$ (d) Above all

19. If the output of a logic gate is '1' when all its inputs are at logic '0', the gate is either.
 (a) NAND or a NOR
 (b) a NAND or an EX-NOR
 (c) an OR or a NAND
 (d) an EX-OR or an EX-NOR
20. Consider following gate network

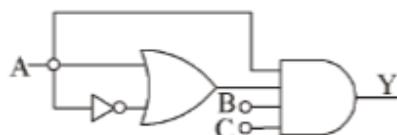


- Which one of the following gates is redundant?
 (a) Gate 1 (b) Gate 2
 (c) Gate 3 (d) Gate 4

21. The logic circuit shown in the given figure can be minimized to

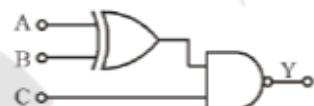


22. The Boolean expression for the output Y in the logic circuit is



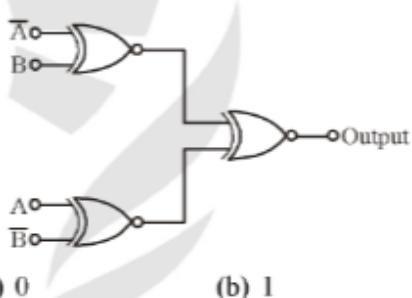
- (a) $A\bar{B}C$ (b) ABC
 (c) \overline{ABC} (d) $\overline{A}\overline{B}\overline{C}$

23. The Boolean expression for the output of the logic circuit shown is



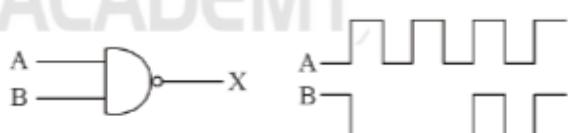
- (a) $Y = \overline{AB} + AB + \overline{C}$ (b) $Y = \overline{A}\overline{B} + A\overline{B} + \overline{C}$
 (c) $Y = \overline{A}\overline{B} + \overline{A}\overline{B} + C$ (d) $Y = \overline{A}B + \overline{A}\overline{B} + C$

24. The output of the circuit in the figure is equal to



- (a) 0 (b) 1
 (c) $\overline{AB} + A\overline{B}$ (d) $(\overline{AB})(\overline{A}\overline{B})$

25. The given figure shows a NAND gate with input waveforms A and B

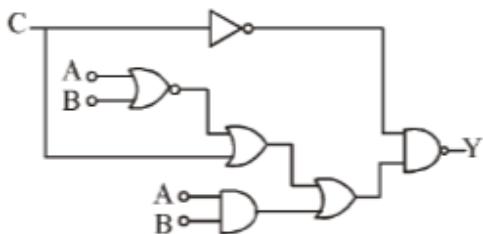


The correct output waveform X of the gate is

- (a) (b)
 (c) (d)

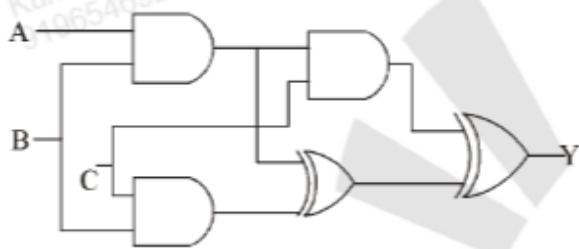
26. A three-input NAND gate is to be used as an inverter. Which one of the following measures will achieve better results?
- The two inputs not used are kept open
 - The two inputs not used are connected to ground ('0' level)
 - The two inputs not used are connected to logic ('1' level)
 - None of the above
27. How is inversion achieved using Ex-OR gate?
- Giving input signal to the two input lines of the gate tied together
 - Giving input to one input line and logic zero to the other line
 - Giving input to one input line and logic one to the other line
 - Inversion cannot be achieved using Ex-OR gate
28. What is the minimum of NAND gates required to implement $A + A\bar{B} + A\bar{B}C$?
- 0
 - 1
 - 4
 - 7
29. Match List-I (Boolean function) with List-II (Minimum number of two-input NAND gates) and select the correct answer using the codes given below the Lists
- | List-I | List-II |
|--|---------|
| A. $Y = A\bar{B}C + \bar{A}BC$ | 1. Five |
| B. $Y = \bar{A}\bar{B} + AB + \bar{C}$ | 2. Four |
| C. $Y = A\bar{B} + \bar{A}\bar{B} + A\bar{B}C$ | 3. Six |
- Codes :**
- | A | B | C |
|-------|---|---|
| (a) 3 | 1 | 2 |
| (b) 1 | 3 | 2 |
| (c) 2 | 1 | 3 |
| (d) 1 | 2 | 3 |
30. The Boolean expression $Y(A, B, C) = A + BC$, is to be realized using 2-input gates of only one type. What is the minimum number of gates required for the realization?
- 1
 - 2
 - 3
 - 4 or more
31. If X and Y are Boolean variables, which one of the following is the equivalent of $X \oplus Y \oplus XY$?
- $X + \bar{Y}$
 - $X + Y$
 - 0
 - 1
32. Assuming that only the X and Y logic inputs are available and their complements \bar{X} and \bar{Y} are not available, what is the minimum number of two-input NAND gates required to implement $X \oplus Y$?
- 2
 - 3
 - 4
 - 5
33. Consider three 4 variable functions f_1 , f_2 and f_3 , which are expressed in sum of midterms as
- $$f_1 = \Sigma(0, 2, 5, 8, 14)$$
- $$f_2 = \Sigma(2, 3, 6, 8, 14, 15)$$
- $$f_3 = \Sigma(2, 7, 11, 14)$$
- For the following circuit with one AND gate and one XOR gate, the output function f can be expressed as:
-
- (a) $\Sigma(2, 14)$
(b) $\Sigma(2, 7, 8, 11, 14)$
(c) $\Sigma(0, 2, 3, 5, 6, 7, 8, 11, 14, 15)$
(d) $\Sigma(7, 8, 11)$

34. In the circuit shown in the figure, if $C = 0$, the expression for Y is



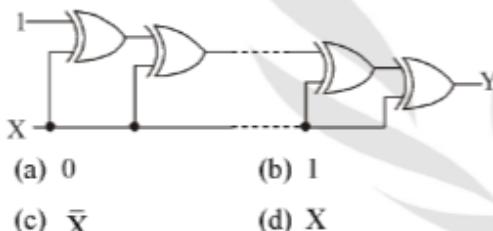
- (a) $Y = A\bar{B} + \bar{A}B$ (b) $Y = A + B$
 (c) $Y = \bar{A} + \bar{B}$ (d) $Y = AB$

35. The output of the combinational circuit given below is



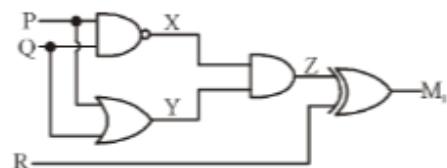
- (a) $A+B+C$ (b) $A(B+C)$
 (c) $B(C+A)$ (d) $C(A+B)$

36. If the input to the digital circuit consisting of a cascade of 20 XOR-gates is X , then the output Y is equal to



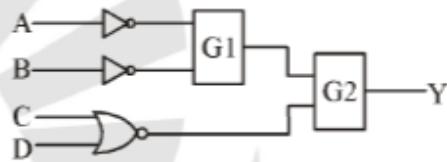
- (a) 0 (b) 1
 (c) \bar{X} (d) X

37. Which of the following Boolean Expressions correctly represents the relation between P , Q , R and M_1 ?



- (a) $M_1 = (P \text{ OR } Q) \text{ XOR } R$
 (b) $M_1 = (P \text{ AND } Q) \text{ XOR } R$
 (c) $M_1 = (P \text{ NOR } Q) \text{ XOR } R$
 (d) $M_1 = (P \text{ XOR } Q) \text{ XOR } R$

38. In the figure shown, the output Y is required to be $Y = AB + \bar{C}\bar{D}$. The gates $G1$ and $G2$ must be,

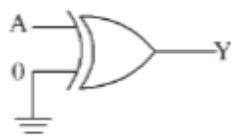


- (a) NOR, OR (b) OR, NAND
 (c) NAND, OR (d) AND, NAND

□□□

ANSWER KEY

1. Ans. (c)



$$Y = \overline{A}\overline{B} + A\overline{B} = \overline{A} \cdot 0 + A \cdot \overline{0} = 0 + A \cdot 1$$

$$Y = A$$

2. Ans. (c)

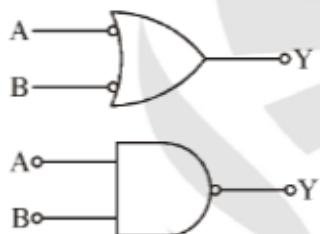
$$Z = A\overline{B} + \overline{A}B$$

It is a XOR gate, it can be realized using NAND gates only as NAND gate is universal gate.

3. Ans. (b)

4. Ans. (a)

Inverted input OR gate is equivalent to the NAND gate



		Y			
A	B	\bar{A}	\bar{B}	$\bar{A} + \bar{B}$	$\bar{A}\bar{B}$
0	0	1	1	1	1
0	1	1	0	1	1
1	0	0	1	1	1
1	1	0	0	0	0

Inverted input AND gate is equivalent to NOR gate



		Y			
A	B	\bar{A}	\bar{B}	$\bar{A}\bar{B}$	$\bar{A} + \bar{B}$
0	0	1	1	1	1
0	1	1	0	0	0
1	0	0	1	0	0
1	1	0	0	0	0

5. Ans. (a)



The electrical equivalent circuit of an AND gate is shown above where two switches A and B are connected in series.

If both the switches are closed, then the output is HIGH.

Ans. (d)

The NOT gate performs the basic logical function called inversion or complementation.

$$Y = \bar{A}$$

$$A = 100101$$

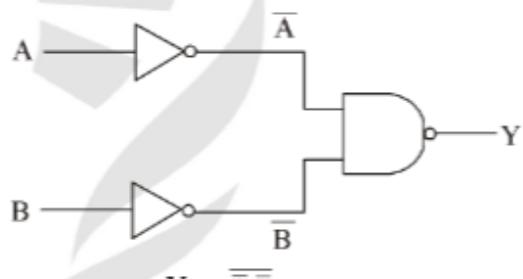
$$\Rightarrow \bar{A} = 011010$$

Hint :

1 is converted to '0'.

0 is converted to '1'.

Ans. (b)



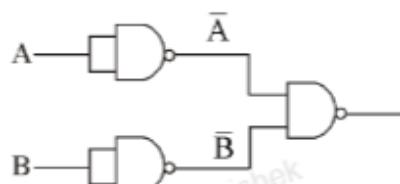
$$Y = \overline{\bar{A}\bar{B}}$$

$$= \bar{\bar{A}} + \bar{\bar{B}}$$

$$= A + B$$

Thus the logic circuit shown behaves as OR gate

8. Ans. (b)

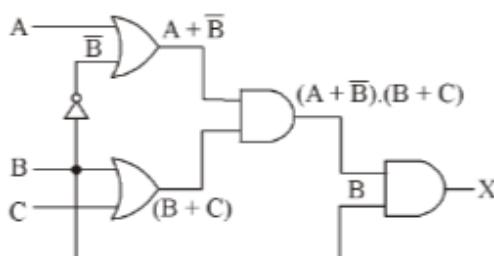


$$Y = \overline{\bar{A}\bar{B}}$$

$$= \bar{\bar{A}} + \bar{\bar{B}}$$

$$= A + B$$

9. Ans. (c)



$$X = (A + \bar{B})(B + C)B$$

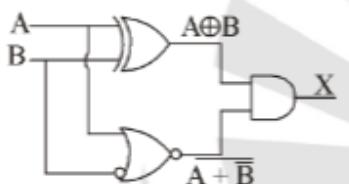
$$X = (AB + AC + \bar{B}C)B$$

$$= AB + ABC$$

$$= AB(1 + C)$$

$$X = AB$$

10. Ans. (b)

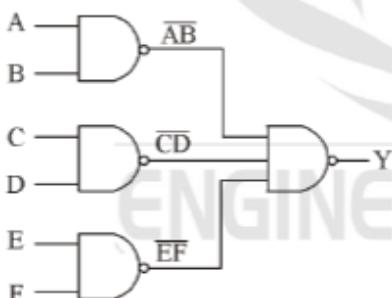


$$X = (A \oplus B)(A + \bar{B})$$

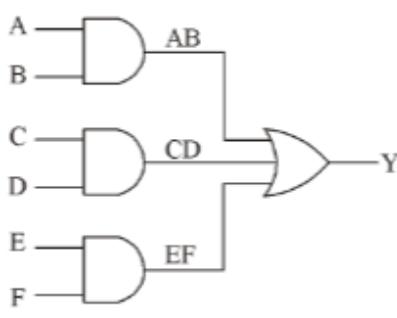
$$X = (\bar{A}B + A\bar{B})(\bar{A}B)$$

$$X = \bar{A}B + 0 = \bar{A}B$$

11. Ans. (c)



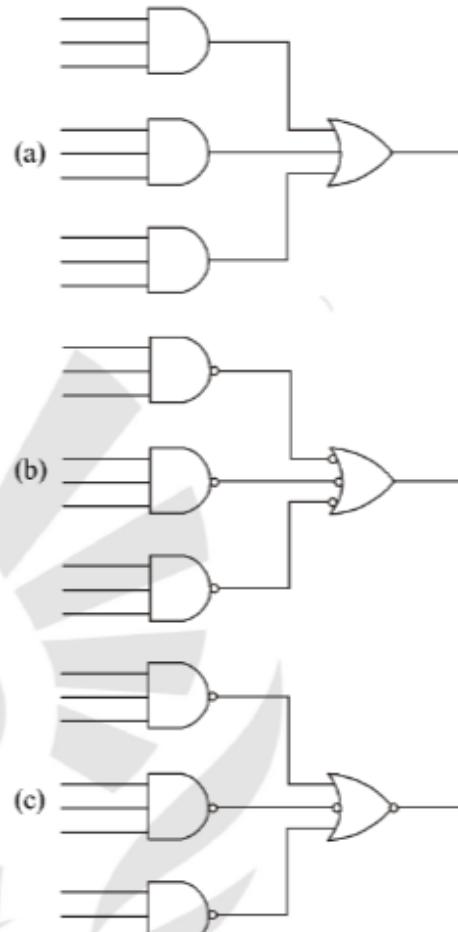
This circuit can be drawn as



$$Y = AB + CD + EF$$

12. Ans. (d)

A two level AND-OR gate network can be easily converted to a NAND-NAND gate network



13. Ans. (d)

$$X(P, Q, R) = \Pi(0, 6)$$

		PQ	00	01	11	10
		R	0			
		0	0			
1	1	0				0

$$Y = (P + Q + R)(\bar{P} + Q + \bar{R})$$

$$= Q(P + \bar{P}) + Q + P\bar{R} + Q\bar{R} + R\bar{P} + RQ$$

$$= Q(P + \bar{P} + 1 + \bar{R} + R) + P\bar{R} + \bar{P}R$$

$$= Q + P\bar{R} + \bar{P}R$$

$$= Q + (P \oplus R)$$

Hence we need OR gate and XOR gate.

14. Ans. (b)
 15. Ans. (c)
 16. Ans. (c)
 17. Ans. (a)
 18. Ans. (d)
 19. Ans. (a), (b)

If the output of a logic gate is '1' when all the inputs are at logic '0' the gate is either.
 NAND gate :

$$Y = \overline{A \cdot B} = \overline{0 \cdot 0} = \overline{0} = 1$$

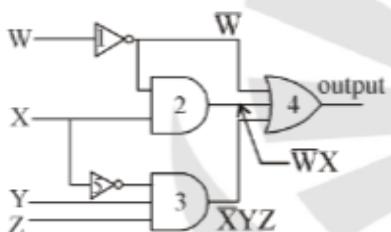
NOR gate :

$$Y = \overline{A + B} = \overline{0 + 0} = \overline{0} = 1$$

Ex-NOR :

$$Y = AB + \overline{A} \cdot \overline{B} = 0 \cdot 0 + \overline{0} \cdot \overline{0} = 0 + 1 = 1$$

20. Ans. (b)



$$\text{Output} = \overline{W} + \overline{W}X + \overline{X}YZ$$

$$\text{Output} = \overline{W}(1 + X) + \overline{X}YZ$$

$$= \overline{W} + \overline{X}YZ$$

So, we can say that gate number 2 is redundant

21. Ans. (d)

22. Ans. (b)



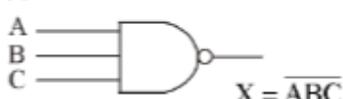
$$Y = A(A + \overline{A})BC = ABC$$

23. Ans. (a)

24. Ans. (b)

25. Ans. (a)

26. Ans. (c)



Suppose using three input NAND gate we want to invert the input A then it is possible if

$$ABC = A11 = A$$

then $X = \overline{A}$ for $B = C = \text{logic 1}$

27. Ans. (c)

Inverter using the Ex-OR gate



$$X = \overline{AB} + A\overline{B} = A \oplus B$$

Suppose we have to invert the input A i.e. output must be

$$X = \overline{A}1 + 0A = \overline{A}$$

and it is possible if and only if other inputs are Logic 1 or High



28. Ans. (a)

$$F = A + A\overline{B} + A\overline{B}C$$

$$F = A[1 + \overline{B} + \overline{B}C]$$

$$F = A$$

There is no need of any NAND gate to realize A since it is given input.

29. Ans. (a)

30. Ans. (c)

31. Ans. (b)

$$F = X \oplus Y \oplus XY$$

$$= X \oplus Y[\overline{Y}(XY) + Y(\overline{XY})]$$

$$= X \oplus Y\overline{X}$$

$$= \overline{X}(Y\overline{X}) + X(\overline{Y}\overline{X})$$

$$= \overline{XY} + X(\overline{Y} + X)$$

$$= \overline{XY} + X\overline{Y} + X$$

$$= \overline{XY} + (\overline{Y} + 1)X$$

$$= X + XY$$

$$F = (X + Y)$$

32. Ans. (c)

33. Ans. (d)

$$f = [f_1 \cdot f_2] \oplus f_3 = [f_1 \cap f_2] \oplus f_3$$

$$f_1 = \Sigma(0, 2, 5, 8, 14)$$

$$f_2 = \Sigma(2, 3, 6, 8, 14, 15)$$

$$f_1 \times f_2 = f_1 \cap f_2 = \Sigma[2, 8, 14]$$

\therefore Common terms in f_1 and f_2

[If both cases present then that term absent in f]

$$\text{Now } f_1 \times f_2 \oplus f_3$$

$$f_1 \times f_2 = \Sigma(2, 8, 14)$$

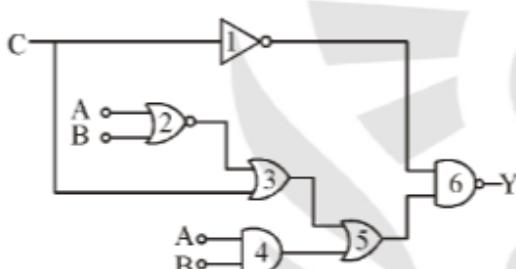
$$f_3 = \Sigma(2, 7, 11, 14)$$

$$f = f_1 \times f_2 \oplus f_3$$

$$= \Sigma(7, 8, 11)$$

$$f = \Sigma(7, 8, 11)$$

34. Ans. (a)



Output of gate 1: \bar{C}

Output of gate 2: $(\bar{A} + B)$

Output of gate 3: $(\bar{A} + \bar{B}) + C$

Output of gate 4: AB

Output of gate 5: $(\bar{A} + \bar{B} + C) + AB$

Output of gate 6 is output Y i.e.

$$\begin{aligned} Y &= \overline{\bar{C}(\bar{A} + \bar{B} + C) + AB} \\ &= C + \overline{(\bar{A} + \bar{B} + C + AB)} \end{aligned}$$

Using demorgan's theorem

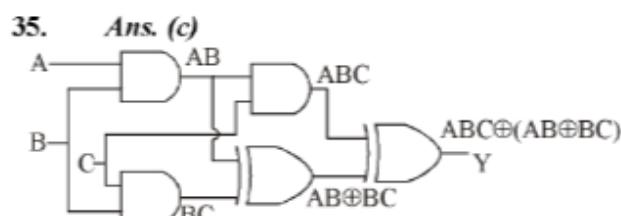
$$= C + \overline{(A + B)} \bar{C} (AB)$$

$$= C + (A + B) \bar{C} (\bar{A} + \bar{B})$$

Given in question $C = 0$,

$$\text{So, } Y = 0 + (A + B) \bar{0} (\bar{A} + \bar{B})$$

$$= \bar{A}B + A\bar{B}$$



$$= ABC \oplus (AB \oplus BC)$$

$$= ABC \oplus B(A \oplus C)$$

$$= ABC(B(A \oplus C)) + \bar{ABC}(B(A \oplus C))$$

$$= ABC(\bar{B} + \bar{A}\bar{C} + AC) + \bar{A} + \bar{B} + \bar{C}(\bar{ABC} + ABC)$$

$$= ABC + \bar{ABC} + ABC$$

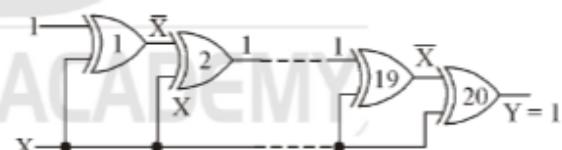
$$= BC[A + \bar{A}] + ABC$$

$$= BC + AB\bar{C}$$

$$= B[C + \bar{C}A]$$

$$= B(C + A)$$

36. Ans. (b)



The output of 1st Ex-OR gate or odd numbered Ex-OR gate is \bar{X} the output of the even numbered Ex-OR gate will be

$$\begin{aligned} \bar{\bar{X}}X + \bar{X}\bar{X} &= XX + \bar{X}\bar{X} \\ &= X + \bar{X} = 1 \end{aligned}$$

So, the output of the 20th Ex-OR gate which is even numbered is logic 1.

37. Ans. (d)

$$X = \overline{PQ} = \bar{P} + \bar{Q}$$

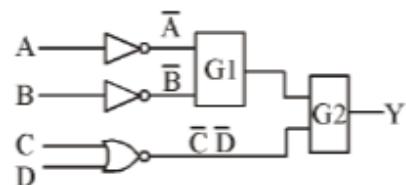
$$Y = P + Q$$

$$Z = (P + Q)(\bar{P} + \bar{Q})$$

$$M_1 = (P\bar{Q} + Q\bar{P}) \oplus R$$

$$M_1 = P \oplus Q \oplus R$$

38. Ans. (a)



$$Y = AB + \bar{C}\bar{D}$$

G1 = NOR gate \bar{A} NOR $\bar{B} = AB$

G2= OR gate $AB + \bar{C}\bar{D}$

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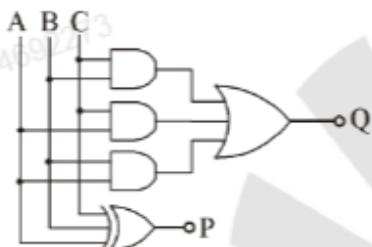
CHAPTER

4

COMBINATIONAL CIRCUITS

OBJECTIVE QUESTIONS

1. In the circuit of figure A, B, C are the inputs and P, Q are the two outputs. The circuit is a



- (a) half adder where P is the sum of Q is the carry
 (b) half adder where P is the carry and Q is the sum
 (c) full adder where P is the sum and Q is the carry
 (d) full adder where P is the carry and Q is the sum

2. The addition of two binary variables A and B results into a SUM and a CARRY output. Consider the following expressions for the SUM and CARRY outputs

1. $\text{SUM} = AB + \bar{A}\bar{B}$
2. $\text{SUM} = \bar{A}\bar{B} + \bar{A}B$
3. $\text{CARRY} = AB$
4. $\text{CARRY} = A + B$

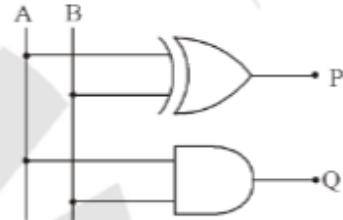
Which of these expressions are correct?

- (a) 1 and 3 (b) 2 and 3
 (c) 2 and 4 (d) 1 and 4

3. For a binary half-subtractor having two inputs A and B, the correct sets of logical expressions for the outputs D (= A minus B) and X (= borrow) are

- (a) $D = AB + \bar{A}\bar{B}$, $X = \bar{A}B$
 (b) $D = \bar{A}\bar{B} + \bar{A}B$, $X = A\bar{B}$
 (c) $D = \bar{A}B + A\bar{B}$, $X = \bar{A}B$
 (d) $D = AB + \bar{A}\bar{B}$, $X = A\bar{B}$

4. The half-adder circuit in the given figure has inputs AB = 11



The logic level of P and Q output will be

- (a) P = 0 and Q = 0 (b) P = 0 and Q = 1
 (c) P = 1 and Q = 0 (d) P = 1 and Q = 1

5. The Truth table for half adder is

(a) A	B	S	C	(b) A	B	S	C
0	0	0	1	0	0	1	1
0	1	0	1	0	1	1	0
1	0	1	0	1	0	0	1
1	1	1	0	1	1	0	1

(c) A	B	S	C	(d) A	B	S	C
0	0	0	0	0	0	0	0
0	1	1	0	0	1	0	0
1	0	1	0	1	0	0	0
1	1	0	1	1	1	1	1

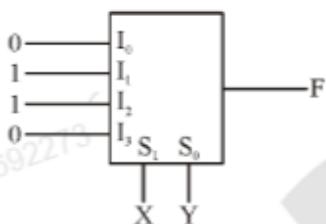
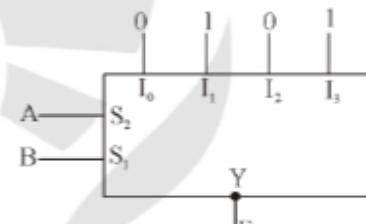
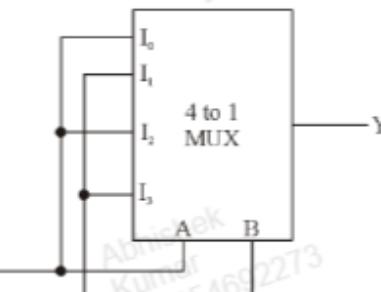
6. In a 4-bit full adder, how many half adders and OR gates are required?

- (a) 8 and 4 (b) 7 and 4
 (c) 7 and 3 (d) 8 and 3

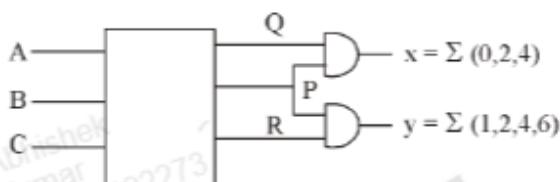
7. The logic circuit given in the figure represents a



- (a) Full adder (b) Half adder
 (c) Half subtractor (d) Boolean multiplier

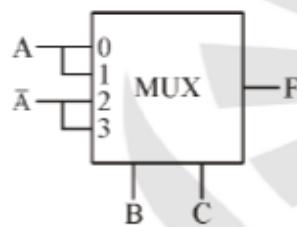
8. A combinational circuit is one in which the output depends on the
 (a) input combination at that time
 (b) input combination and the previous output
 (c) input combination at that time and the previous input combination
 (d) present output and the previous output
9. What is the output $F(X, Y)$ of the multiplexer resulting from the input logical values ?
- 
- (a) An Ex-OR gate (b) A NOR gate
 (c) An AND gate (d) A NAND gate
10. To construct a 2^{10} input multiplexer, the required number of 2 input multiplexers is
 (a) 31 (b) 63
 (c) 127 (d) 1023
11. An 8 input multiplexer is to be built with a tree network of 2 input multiplexers. The number of 2 input multiplexers required is
 (a) 4 (b) 8
 (c) 6 (d) 7
12. A full adder can be made out of
 (a) two half adders
 (b) two half adders and a NOT gate
 (c) two half adders and an OR gate
 (d) two half adders and an AND gate
13. A full-adder can be implemented with half-adders and OR gates. A 4-bit parallel full adder without any initial carry requires
 (a) 8 half adders, 4 OR gates
 (b) 8 half adders, 3 OR gates
 (c) 7 half adders, 4 OR gates
 (d) 7 half adders, 3 OR gates
14. If both the inputs to a half adder are 1, the Sum and Carry outputs are, respectively
 (a) 0, 0 (b) 0, 1
 (c) 1, 0 (d) 1, 1
15. The number of 4-to-16 decoders required to make a 8-to-256 line decoder is
 (a) 16 (b) 17
 (c) 32 (d) 64
16. The following switching functions are to be implemented using a decoder.
 $f_1 = \Sigma m(1, 2, 4, 8, 10, 14)$
 $f_2 = \Sigma m(2, 5, 9, 11)$
 $f_3 = \Sigma m(2, 4, 5, 6, 7)$
- The minimum configuration of the decoder should be
 (a) 2 to 4 line (b) 3 to 8 line
 (c) 4 to 16 line (d) 5 to 32 line
17. A system which accepts an M-bit word and establishes the state '1' on one and only one of 2^M output lines is called
 (a) decoder (b) demultiplexer
 (c) multiplexer (d) encoder
18. The function 'F' implemented by the multiplexer chip shown in the figure is
- 
- (a) A (b) B
 (c) $\bar{A}B$ (d) $A\bar{A} + \bar{A}B$
19. A gate having two inputs (A, B) and one output (Y) is implemented using a 4 to 1 multiplexer as shown in figure. A_1 (MSB) and A_0 are the control bits and $I_0 - I_3$ are the inputs to the multiplexer
- 
- the gate is
 (a) NAND (b) NOR
 (c) X-OR (d) OR

20. Given a combinational network with three inputs A, B, and C. Three intermediate outputs P, Q, R, and two outputs X = PQ = $\Sigma(0, 2, 4)$ and Y = PR = $\Sigma(1, 2, 4, 6)$ as shown below, find the smallest function P (Containing minimum number of minterms that can produce the output X and Y.



- (a) $\Sigma(2, 4)$ (b) $\Sigma(0, 1, 2, 4, 6)$
 (c) $\Sigma(3, 5, 7)$ (d) $\Sigma(1, 2, 6)$

21. The logic realized by the adjoining circuit is



- (a) $F(A, B, C) = A \oplus B$
 (b) $F(A, B, C) = A \oplus C$
 (c) $F(A, B, C) = A \odot B$
 (d) $F(A, B, C) = A \odot C$

22. Consider the following statements :

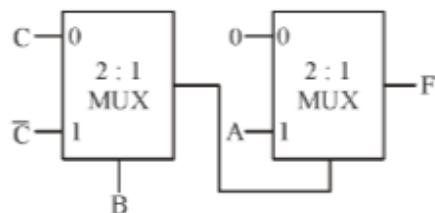
A multiplexer

1. selects one of the several inputs and transmits it to a single output.
2. routes the data from a single input to one of many output.
3. converts parallel data into serial data.
4. is a combinational circuit.

Which of these statements are correct?

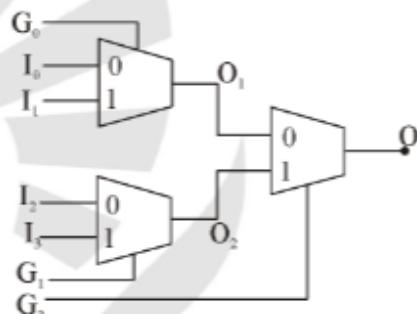
- (a) 1, 2 and 4 (b) 2, 3 and 4
 (c) 1, 3 and 4 (d) 1, 2 and 3

23. The boolean function F implemented in figure below using two input multiplexers is



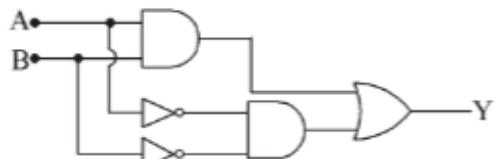
- (a) $A\bar{B}C + A\bar{B}\bar{C}$ (b) $ABC + A\bar{B}\bar{C}$
 (c) $\bar{A}BC + \bar{A}\bar{B}\bar{C}$ (d) $\bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C}$

24. The cell of a field programmable gate array is shown in figure. It has three 2 to 1 multiplexers with their select lines G_0, G_1, G_2 and 4 digital signal input lines I_0, I_1, I_2 and I_3 . The logical function that relates the output O to the select and signal input lines is



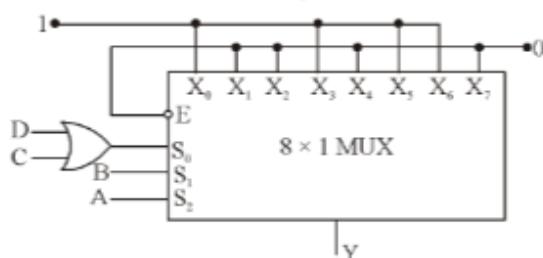
- (a) $\bar{G}_0\bar{G}_1I_2 + \bar{G}_0G_1I_3 + \bar{G}_2\bar{G}_1I_0 + G_2\bar{G}_1I_1$
 (b) $\bar{G}_0I_2 + \bar{G}_0G_1 + G_2I_0 + G_2\bar{G}_1I_1 + G_0$
 (c) $\bar{G}_0\bar{G}_2I_0 + G_0\bar{G}_2I_1 + G_2\bar{G}_1I_2 + G_2G_1I_3$
 (d) $G_2G_1I_2 + \bar{G}_2\bar{G}_1I_3 + G_2G_0I_0 + G_0\bar{G}_2I_1$

25. The logic circuit of figure is a



- (a) half adder (b) XOR
 (c) equality detector (d) full adder

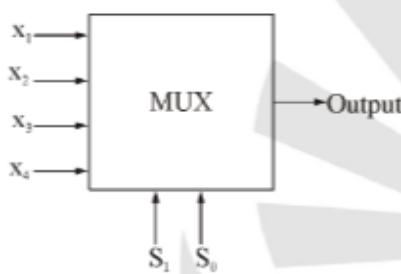
26. Consider the following circuit:



In the above TTL circuit, S_2 to S_0 are select lines and X_7 to X_0 are input lines. S_0 and X_0 are LSBs. What is the output Y ?

- (a) Indeterminate (b) $A \oplus B$
 (c) $\overline{A \oplus B}$ (d) $Y = \overline{A \oplus B \oplus (D + C)}$

27. In the figure shown



$X_1 \rightarrow$ High

$X_2 \rightarrow$ High

$X_3 \rightarrow$ High

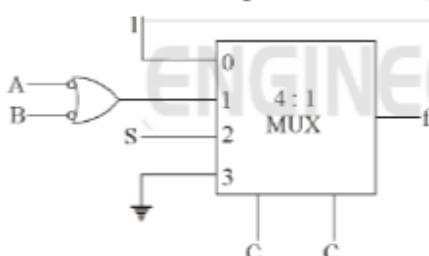
$X_4 \rightarrow$ Low

S_1 and S_0 are control inputs.

This multiplexer is equivalent to

- (a) NAND gate (b) AND gate
 (c) OR gate (d) EXNOR gate

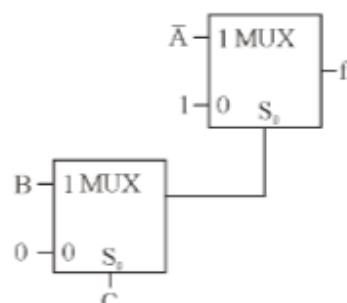
28. Consider the following circuit:



Which one of the following gives the function implemented by the MUX-based digital circuit?

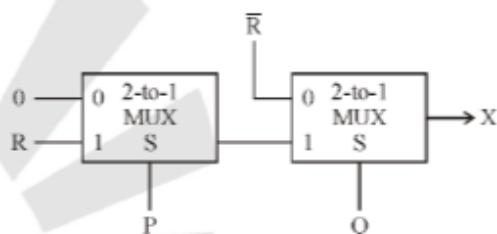
- (a) $f = C_2 \bar{C}_1 S + \bar{C}_2 C_1 (\bar{A} + \bar{B})$
 (b) $f = C_2 \bar{C}_1 S + C_2 C_1 (\bar{A} + \bar{B})$
 (c) $f = \bar{A} \bar{B} + S$
 (d) $f = \bar{C}_2 \bar{C}_1 + C_2 \bar{C}_1 S + \bar{C}_2 C_1 \bar{A} \bar{B}$

29. The network shown in figure implements



- (a) NOR gate (b) NAND gate
 (c) XOR gate (d) XNOR gate

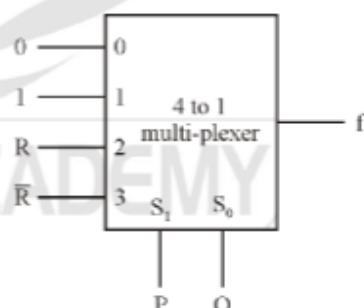
30. Consider the two cascaded 2-to-1 multiplexers as shown in the figure.



The minimal sum of products form of the output X is

- (a) $\overline{PQ} + PQR$ (b) $\overline{PQ} + QR$
 (c) $PQ + \overline{PQ}R$ (d) $\overline{QR} + PQR$

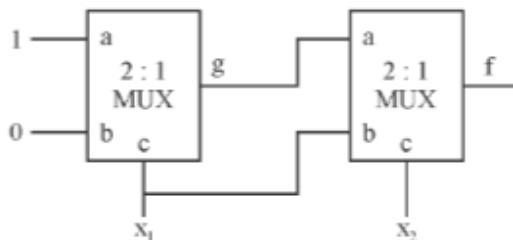
31. Consider the 4 to 1 multiplexer with two select lines S_1 and S_0 given below.



The minimal sum-of-products form of the Boolean expression for the output f of the multiplexer is

- (a) $\overline{PQ} + Q\bar{R} + P\bar{Q}R$
 (b) $\overline{PQ} + \overline{PQ}\bar{R} + P\bar{Q}R + P\bar{Q}R$
 (c) $\overline{PQR} + \overline{PQ}\bar{R} + Q\bar{R} + P\bar{Q}R$
 (d) $P\bar{Q}\bar{R}$

32. Consider the circuit shown below. The output of a 2 : 1 MUX is given by the function $(a\bar{c} + bc)$.

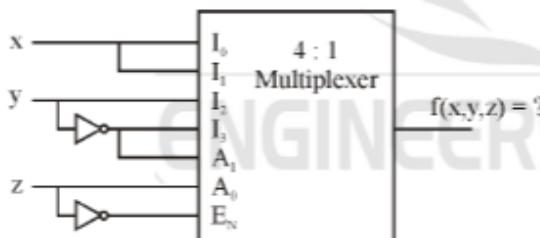


Which of the following is true?

- (a) $f = \bar{x}_1 + x_2$
- (b) $f = x_1x_2 + x_1\bar{x}_2$
- (c) $f = x_1x_2 + \bar{x}_1\bar{x}_2$
- (d) $f = x_1 + x_2$

33. How many 3-to-8 line decoders with an enable input are needed to construct a 6-to-64 line decoder without using any other logic gates?
- (a) 7
 - (b) 8
 - (c) 9
 - (d) 10

34. Consider the following multiplexer where I_0, I_1, I_2, I_3 are four data input lines selected by two address line combinations $A_1A_0 = 00, 01, 10, 11$ respectively and f is the output of the multiplexer, EN is the Enable input.



The function $f(x, y, z)$ implemented by the above circuit is

- (a) $xy\bar{z}$
- (b) $xy + z$
- (c) $x + y$
- (d) None of these

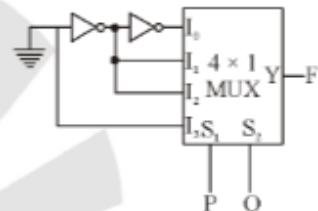
35. To add two m-bit numbers, the required number of half adder is

- (a) $2m - 1$
- (b) $2^m - 1$
- (c) $2m + 1$
- (d) $2m$

36. Which one of the following statements describes the operation of a multiplexer?

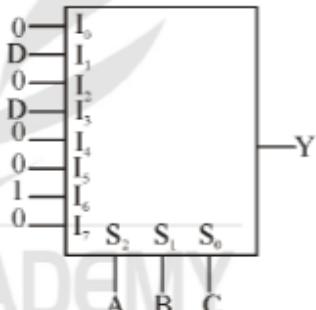
- (a) A logic circuit used to generate coded output
- (b) A logic circuit used to generate F 's complement
- (c) A logic circuit that accepts two or more inputs and allows one of them at a time to get through the output
- (d) A logic circuit that transmits one input to several output lines

37. The logic function implemented by the circuit below is (ground implies a logic '0')



- (a) $F = \text{AND}(P, Q)$
- (b) $F = \text{OR}(P, Q)$
- (c) $F = \text{XNOR}(P, Q)$
- (d) $F = \text{XOR}(P, Q)$

38. An 8-to-1 multiplexer is used to implement a logical function Y as shown in the figure. The output



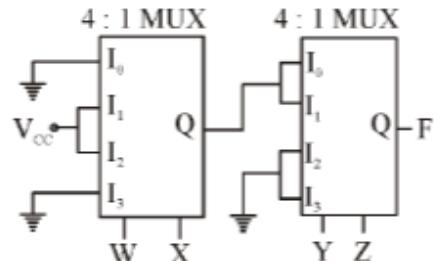
- (a) $Y = A\bar{B}C + A\bar{C}D$
- (b) $Y = \bar{A}BC + A\bar{B}C$
- (c) $Y = ABC + \bar{A}CD$
- (d) $Y = \bar{A}\bar{B}D + \bar{A}\bar{B}C$

39. What are the minimum number of 2-to-1 multiplexers required to generate a 2-input AND gate and a 2-input Ex-OR gate?

- (a) 1 and 2
- (b) 1 and 3
- (c) 1 and 1
- (d) 2 and 2

40. The output Y of a 2-bit comparator is logic 1 whenever the 2-bit input A is greater than the 2-bit input B. The number of combination for which the output is logic 1, is
(a) 4 (b) 6
(c) 8 (d) 10

41. In the circuit shown, W and Y are MSBs of the control inputs. The output F is given by

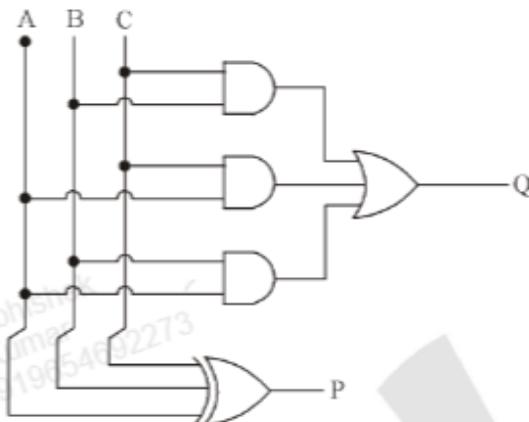


- (a) $F = W\bar{X} + \bar{W}X + \bar{Y}\bar{Z}$
(b) $F = W\bar{X} + \bar{W}X + \bar{Y}Z$
(c) $F = W\bar{X}\bar{Y} + \bar{W}X\bar{Y}$
(d) $F = (\bar{W} + \bar{X})\bar{Y}\bar{Z}$

□□□



ANSWER KEY

1. *Ans. (c)*

$$P = A \oplus B \oplus C$$

$$Q = AB + BC + CA$$

The expression of the circuit shown represents a full adder with P as the sum output and Q as the carry output.

2. *Ans. (b)*

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Expression for sum (S)

A	B	0	1
0	0	0	1
1	0	1	0

$$S = A\bar{B} + \bar{A}B$$

Expression for carry (C)

A	B	0	1
0	0	0	0
1	0	0	1

$$C = AB$$

3. *Ans. (c)*

The half subtractor is a combinational circuit which is used to perform subtraction of two bits.

Truth table

A	B	D	X
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Expression for D

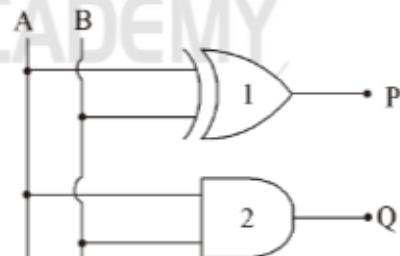
A	0	1
0	0	①
1	①	0

$$D = A\bar{B} + \bar{A}B$$

Expression for X (Borrow)

A	0	1
0	0	0
1	0	①

$$X = \bar{A}B$$

4. *Ans. (b)*

Half adder is a combinational circuit that performs binary addition of two bits

$$P = \text{Sum } S = A \oplus B$$

$$= A\bar{B} + \bar{A}B$$

$$Q = \text{Carry } C = AB$$

For $A = 1, B = 1$
 $S = A \oplus B$
 $= 1 \oplus 1 = 0$
 $C = A \cdot B$
 $= 1 \cdot 1 = 1$
 $\Rightarrow P = 0, Q = 1$

5. *Ans. (c)*

Truth table of half adder is

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

6. *Ans. (c)*

7. *Ans. (b)*



The logic circuit represents a half adder.

$$C = AB$$

$$S = A \oplus B = \bar{A}\bar{B} + \bar{A}B + A\bar{B}$$

A half adder is a combinational circuit that performs addition of two binary bits.

8. *Ans. (a)*

A combinational circuit is one in which the output depends on the input combination at that time. Combinational logic circuits do not have memory.

9. *Ans. (a)*

Given that, $S_1 = X, S_0 = Y$

$$I_0 = I_3 = 0, I_1 = I_2 = 1$$

$$F = \bar{S}_1\bar{S}_0I_0 + \bar{S}_1S_0I_1 + S_1\bar{S}_0I_2 + S_1S_0I_3$$

$$F = \bar{X}Y + X\bar{Y} = X \oplus Y$$

Thus the output of the MUX resulting into an Ex-OR gate.

10. *Ans. (d)*

To construct 2^{10} input multiplexer the required number of 2 input multiplexers are

$$\begin{aligned} 2^n - 1 &= 2^{10} - 1 \\ &= 1024 - 1 \\ &= 1023 \end{aligned}$$

11. *Ans. (d)*

To construct the (8×1) MUX using (2×1) MUX, we require

$$\frac{8}{2} = 4 \quad \text{Level-1}$$

$$\frac{4}{2} = 2 \quad \text{Level-2}$$

$$\frac{2}{2} = 1 \quad \text{Level-3}$$

$$\text{Total} = 4 + 2 + 1 = 7 \text{ MUX}$$

12. *Ans. (c)*

13. *Ans. (d)*

14. *Ans. (b)*

If both the inputs of the half adder are 1

$$\begin{aligned} A &= B = 1 \\ \text{then } S &= A \oplus B \\ &= 1 \oplus 1 = 0 \\ C &= AB = 1 \end{aligned}$$

15. *Ans. (b)*

We have to construct the (8×256) decoder using (4×16) decoder then total number of the (4×16) decoders are

$$\frac{256}{16} = 16 \quad \text{Level-1}$$

$$\frac{16}{16} = 1 \quad \text{Level-2}$$

$$\text{Total} = 16 + 1 = 17 \text{ MUX}$$

16. *Ans. (c)*

$$f_1 = \sum m(1, 2, 4, 8, 10, 14)$$

$$f_2 = \sum m(2, 5, 9, 11)$$

$$f_3 = \sum m(2, 4, 5, 6, 7)$$

These three switching are to be implemented using a decoder. It is clear that the highest minterm in the above three switching functions is m_{14} and we know that a decoder with n -input lines contain 2^n output lines. Actually these are the all possible minterms.

If we use a decoders of configuration (4×16) when we will have minterms from $(m_0 - m_{15})$ and we can implement the given switching functions.

17. Ans. (a)

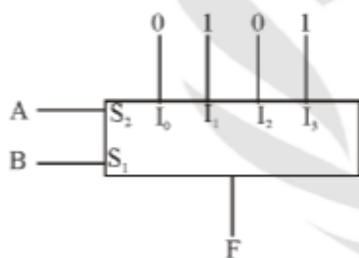
A system which accepts an M -bit word and establishes the state-1 on one and only one of 2^M output lines is called a decoder

A decoder identifies or recognizes or detects a particular code.



Only one output is high for each input code

18. Ans. (b)



$$\begin{aligned} F &= \bar{A}\bar{B}I_0 + \bar{A}BI_1 + A\bar{B}I_2 + ABI_3 \\ &= \bar{A}\bar{B}0 + \bar{A}B1 + A\bar{B}0 + AB1 \\ &= \bar{A}B + AB \\ &= (\bar{A} + A)B = B \end{aligned}$$

19. Ans. (d)

$$\begin{aligned} Y &= \bar{A}\bar{B}I_0 + \bar{A}BI_1 + A\bar{B}I_2 + ABI_3 \\ &= \bar{A}\bar{B}A + \bar{A}BB + A\bar{B}A + ABB \\ &= \bar{A}B + A\bar{B} + AB \\ &= \bar{A}B + A = A + B \end{aligned}$$

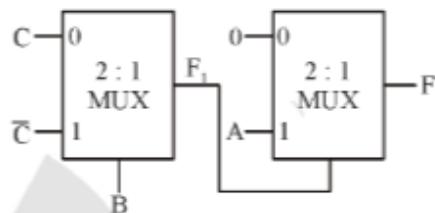
20. Ans. (b)

21. Ans. (a)

$$\begin{aligned} F &= \bar{B}\bar{C}I_0 + \bar{B}\bar{C}I_1 + B\bar{C}I_2 + BC\bar{I}_3 \\ &= \bar{B}\bar{C}A + \bar{B}CA + B\bar{C}\bar{A} + BC\bar{A} \\ &= \bar{B}A + B\bar{A} \\ &= A \oplus B \end{aligned}$$

22. Ans. (c)

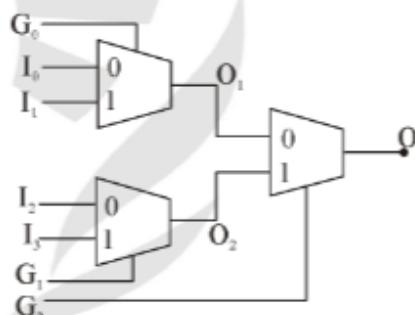
23. Ans. (a)



$$F_1 = C\bar{B} + \bar{C}B$$

$$\begin{aligned} F &= \bar{F}_10 + F_1A \\ &= 0 + (C\bar{B} + \bar{C}B)A \\ &= ABC + ABC \end{aligned}$$

23. Ans. (c)



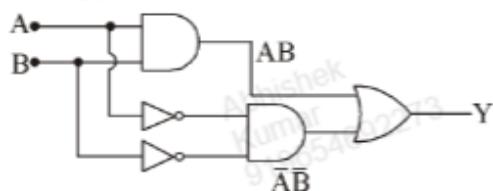
$$O_1 = \bar{G}_0I_0 + G_0I_1$$

$$O_2 = \bar{G}_1I_2 + G_1I_3$$

$$O = \bar{G}_2O_1 + G_2O_2$$

$$\begin{aligned} &= \bar{G}_2(\bar{G}_0I_0 + G_0I_1) + G_2(\bar{G}_1I_2 + G_1I_3) \\ &= \bar{G}_2\bar{G}_0I_0 + \bar{G}_2G_0I_1 + G_2\bar{G}_1I_2 + G_2G_1I_3 \end{aligned}$$

25. Ans. (c)

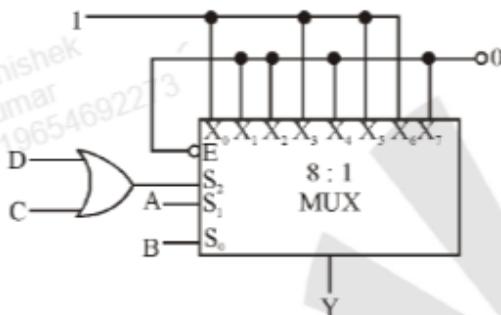


$$Y = AB + A\bar{B}$$

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

The output comes only when $A = B$. So the logic circuit shown is an equality detector.

26. *Ans. (d)*



$$Y = \bar{S}_2 \bar{S}_1 \bar{S}_0 + \bar{S}_2 S_1 S_0 + S_2 \bar{S}_1 S_0 + S_2 S_1 \bar{S}_0$$

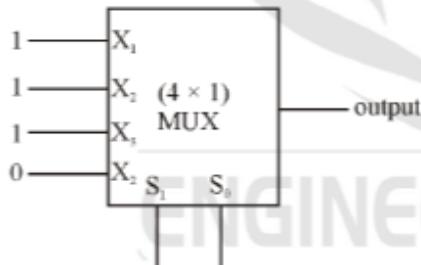
$$Y = (\bar{S}_2 \bar{S}_1 + S_2 S_1) \bar{S}_0 + (\bar{S}_2 S_1 + S_2 \bar{S}_1) S_0$$

$$Y = (\bar{S}_2 \oplus S_1) \bar{S}_0 + (S_2 \oplus S_1) S_0$$

$$Y = \bar{S}_2 \oplus S_1 \oplus S_0$$

$$Y = (D + C) \oplus B \oplus A$$

27. *Ans. (a)*



$$\text{Output} = \bar{S}_1 \bar{S}_0 1 + \bar{S}_1 S_0 1 + S_1 \bar{S}_0 1$$

$$= \bar{S}_1 (\bar{S}_0 + S_0) + S_1 \bar{S}_0$$

$$= \bar{S}_1 + S_1 \bar{S}_0$$

$$= (\bar{S}_1 + S_1)(\bar{S}_0 + \bar{S}_0)$$

$$= (\bar{S}_1 + \bar{S}_0)$$

$$\text{Output} = \bar{S}_1 S_0 \quad (\text{NAND operation})$$

28. *Ans. (d)*

$$\text{Given, } S_1 = C_2$$

$$S_0 = C_1$$

$$I_3 = 0$$

$$I_2 = S$$

$$I_1 = \bar{A} + \bar{B} = \overline{AB}$$

$$I_0 = 1$$

$$f = \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3$$

$$f = \bar{C}_2 \bar{C}_1 1 + \bar{C}_2 \bar{C}_1 (\overline{AB}) + C_2 \bar{C}_1 S + C_2 C_1 0$$

$$f = \bar{C}_2 \bar{C}_1 + C_2 \bar{C}_1 S + \bar{C}_2 C_1 (\overline{AB})$$

29. *Ans. (b)*

30. *Ans. (d)*

$$\text{MUX-1 output} \Rightarrow \bar{P}(0) + P(R) = PR$$

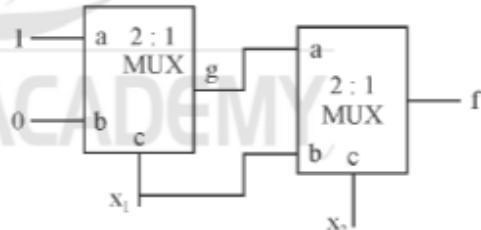
$$\begin{aligned} \text{MUX-2 output} &\Rightarrow X = \bar{Q}(\bar{R}) + Q(PR) \\ &= \bar{Q}\bar{R} + PQR \end{aligned}$$

31. *Ans. (a)*

Using given multiplexer:

$$\begin{aligned} f &= \bar{P}Q + P\bar{Q}R + PQ\bar{R} \\ &= Q[\bar{P} + P\bar{R}] + P\bar{Q}R \\ &= Q[(\bar{P} + P)(\bar{P} + \bar{R})] + P\bar{Q}R \\ &= Q[\bar{P} + \bar{R}] + P\bar{Q}R \\ &= \bar{P}Q + Q\bar{R} + P\bar{Q}R \end{aligned}$$

32. *Ans. (c)*



The output g is

$$g = 1\bar{x}_1 + 0x_1 = \bar{x}_1$$

The output f is

$$f = g\bar{x}_2 + x_1 x_2$$

$$f = \bar{x}_1 \bar{x}_2 + x_1 x_2$$

33. Ans. (c)

For the construction of a 6×64 decoder by using

3×8 line decoder $\frac{64}{8} = 8 + 1 \rightarrow$ extra decoder
for combining the result $6 \times 64 \xrightarrow{8+1} 3 \times 8$

34. Ans. (a)

The output function $f(x, y, z)$ is given as

$$\begin{aligned} f(x, y, z) &= E(\bar{A}_1\bar{A}_0I_0 + \bar{A}_1A_0I_1 + A_1\bar{A}_0I_2 + A_1A_0I_3) \\ &= \bar{z}(y\bar{z}x + yz\bar{x} + \bar{y}zy + \bar{y}\bar{z}\bar{y}) \\ &= \bar{z}(xy\bar{z} + xyz + 0 + \bar{y}z) \\ &= xyz + xyz\bar{z} + 0\bar{z} + \bar{z}zy \\ &= xy\bar{z} + 0 + 0 + 0 = xy\bar{z} \end{aligned}$$

Therefore, option (a) is correct.

35. Ans. (a)

36. Ans. (c)

A multiplexer (MUX) or data selector is a logic circuit that accepts several data inputs (two or more) and allows only one of them at a time to get through to the output.

37. Ans. (d)

P	Q	F
0	0	0
0	1	1
1	0	1
1	1	0

$$F = P \oplus Q$$

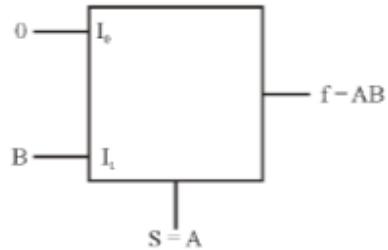
38. Ans. (c)

Depending upon the select lines one input is transferred to the output in multiplexer.

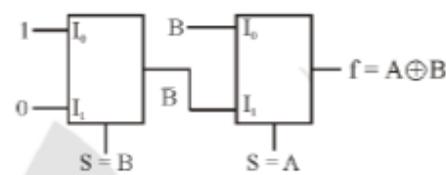
A	B	C	Y
0	0	0	0
0	0	1	D
0	1	0	0
0	1	1	D
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

$$\begin{aligned} Y &= \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}CD + A\bar{B}\bar{C} \\ &= \bar{A}CD(\bar{B} + B) + ABC \\ &= \bar{A}CD + ABC \end{aligned}$$

39. Ans. (a)



AND, '1 MUX'



EXOR, '2 MUX'

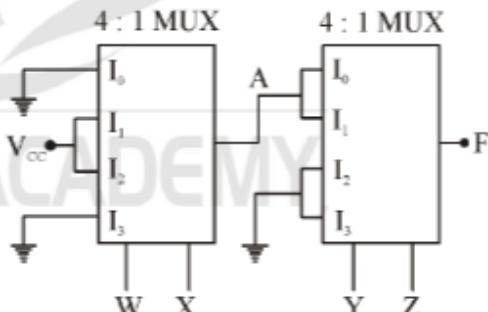
40. Ans. (b)

Output will be 1 if $A > B$.

- If $B = 00$ then there will be three combinations for which output will be 1 i.e. when $A = 01, 10$, or 11 .
- If $B = 01$ there will be two conditions i.e. $A = 10$ and 11 .
- If $B = 10$ there will be one condition i.e. $A = 11$.

So total 6 combinations are there for which output will be 1.

41. Ans. (c)



For the state equation of $4 : 1$ MUX, we know that

$$\begin{aligned} A &= \bar{W}\bar{X}I_0 + \bar{W}XI_1 + W\bar{X}I_2 + WXI_3 \\ &= \bar{W}X + W\bar{X} \quad (\text{Since } V_{CC} = 1) \end{aligned}$$

Now, output F

$$\begin{aligned} F &= \bar{Y}\bar{Z}I_0 + \bar{Y}ZI_1 + Y\bar{Z}I_2 + YZI_3 \\ &= \bar{W}X\bar{Y}\bar{Z} + W\bar{X}\bar{Y}\bar{Z} + \bar{W}X\bar{Y}Z + W\bar{X}YZ \\ &= \bar{W}XY(\bar{Z} + Z) + W\bar{X}Y(\bar{Z} + Z) \\ &= W\bar{X}\bar{Y} + W\bar{X}Y \end{aligned}$$

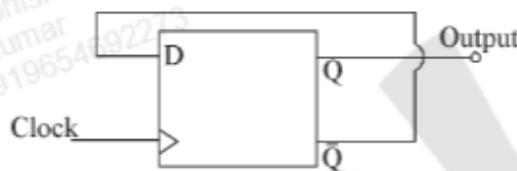
SEQUENTIAL CIRCUITS

CHAPTER

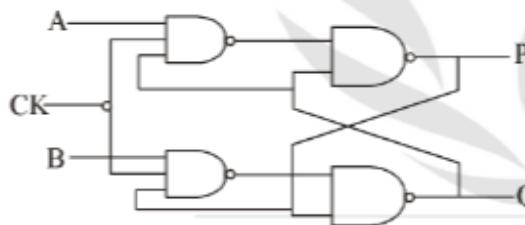
5

OBJECTIVE QUESTIONS

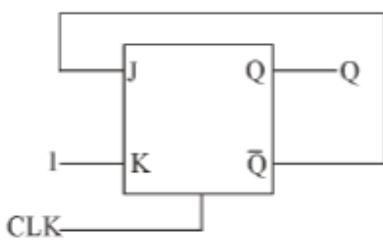
1. For the circuit shown in the given figure, the frequency of the output Q will be



- (a) Twice the inputs clock frequency
 (b) Half the input clock frequency
 (c) Same as the input clock frequency
 (d) Inverse of the propagation delay of the FF
2. Given A = 1, B = 1, Q_n = 0 and P_n = 1, what will be output Q_{n+1} and P_{n+1}, when the clock input (CK) is applied ?



- (a) Q_{n+1} = 0, P_{n+1} = 0
 (b) Q_{n+1} = 0, P_{n+1} = 1
 (c) Q_{n+1} = 1, P_{n+1} = 0
 (d) Q_{n+1} = 1, P_{n+1} = 1
3. Consider the following JK flip-flop



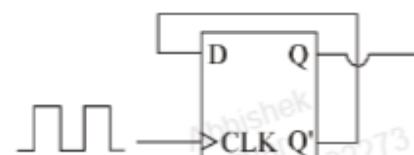
In the above JK flip-flop, J = \bar{Q} and K = 1. Assume that the flip-flop was initially cleared and then clocked for 6 pulses. What is the sequence at the Q output?

- (a) 010000 (b) 011001
 (c) 010010 (d) 010101
4. The characteristic equation for the next state (Q_{n+1}) of a JK flip-flop is
- (a) Q_{n+1} = JQ_n + K \bar{Q}_n
 (b) Q_{n+1} = $\bar{J}\bar{Q}_n + \bar{K}Q_n$
 (c) Q_{n+1} = J $\bar{Q}_n + Q_n\bar{K}$
 (d) Q_{n+1} = JQ_n + KQ_n
- (where Q_n represents the present state)

5. The characteristic equation of the T-flip-flop is given by

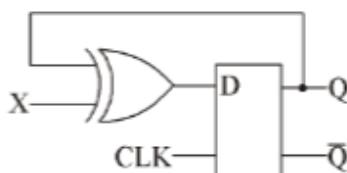
- (a) Q_{n+1} = $\bar{T}Q + T\bar{Q}$ (b) Q_{n+1} = $\bar{Q}\bar{T}$
 (c) Q_{n+1} = TQ (d) Q_{n+1} = T \bar{Q}

6. The frequency of the clock signal applied to the rising edge triggered D flip-flop shown in the figure given above is 10 kHz. What is the frequency of the signal available at Q?



- (a) 20 kHz (b) 10 kHz
 (c) 5 kHz (d) 2.5 kHz

7. The digital circuit shown in figure works as a



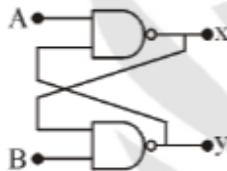
- (a) JK flip-flop (b) Clocked RS flip-flop
 (c) T flip-flop (d) Ring counter

8. For a flip-flop formed from two NAND gates as shown in figure the unusable state corresponds to



- (a) X = 0, Y = 0 (b) X = 0, Y = 1
 (c) X = 1, Y = 0 (d) X = 1, Y = 1

9. In figure A = 1 and B = 1, the input B is now replaced by a sequence 101010....., the outputs x and y will be

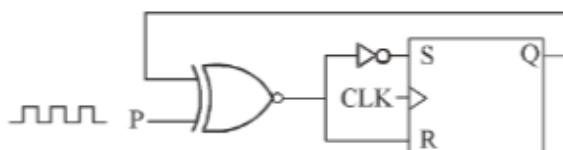


- (a) fixed at 0 and 1, respectively
 (b) x = 1010... and y = 0101...
 (c) x = 1010... and y = 1010...
 (d) fixed at 1 and 0, respectively

10. A switch-tail ring counter is made by using a single D flip-flop. The resulting circuit is a

- (a) SR flip-flop (b) JK flip-flop
 (c) D flip-flop (d) T flip-flop

11. Consider the circuit, the next state Q+ is



- (a) PQ (b) P̄Q̄
 (c) P⊕Q (d) P ⊙ Q̄

12. A sequence detector is required to give a logical output of 1 whenever the sequence 1011 is detected in the incoming pulse stream. Minimum number of flip-flops needed to build the sequence detector is

- (a) 4 (b) 3
 (c) 2 (d) 1

13. The number of flip flops required in a decade counter is

- (a) 2 (b) 3
 (c) 4 (d) 10

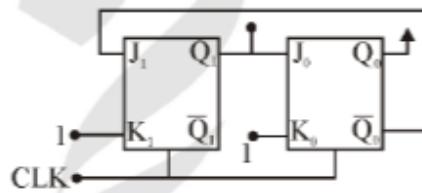
14. A 10 MHz square wave clocks a 5-bit ripple counter. The frequency of the third flip-flop's output would be

- (a) 2 MHz (b) 1.25 MHz
 (c) 50 MHz (d) 615 MHz

15. If a mod-6 counter is constructed using 3 flip-flops, the counter will skip

- (a) 4 counts (b) 3 counts
 (c) 0 count (d) 2 counts

16. Figure show below is a mod-K counter, here K sequence

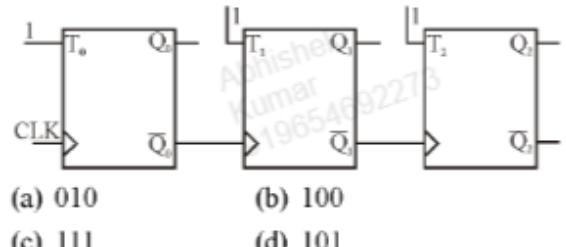


- (a) 1 (b) 2
 (c) 3 (d) 4

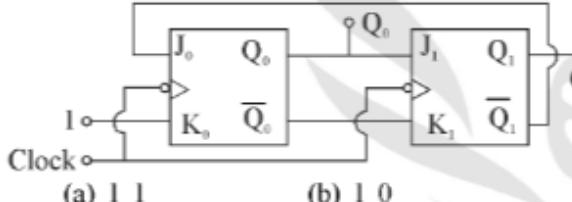
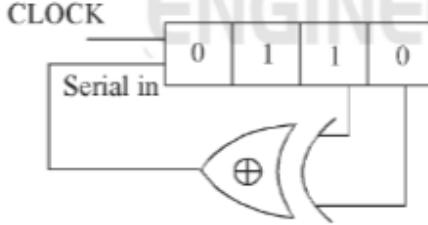
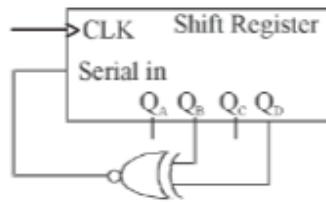
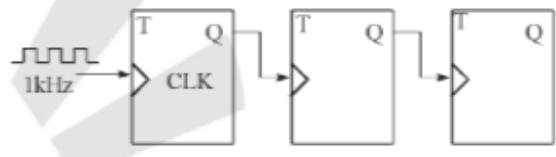
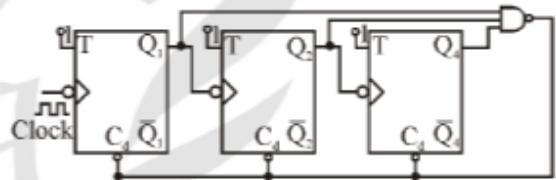
17. A module-5 counter can be made using a minimum number of JK flip-flops equal to

- (a) two (b) three
 (c) one (d) four

18. Figure shows a ripple counter using positive edge triggered flip-flops. If the present state of the counter is Q₂Q₁Q₀ = 011, then its next state (Q₂Q₁Q₀) will be



- (a) 010 (b) 100
 (c) 111 (d) 101

19. The number of unused states in a 4-bit Johnson counter is
 (a) 2 (b) 4
 (c) 8 (d) 12
20. A ring counter consisting of five flip-flop will have
 (a) 5 states (b) 10 states
 (c) 32 states (d) infinite states
21. A four bit synchronous counter uses flip-flop with propagation delay time of 15 ns each. The maximum possible time required for change of state will be
 (a) 15 ns (b) 30 ns
 (c) 45 ns (d) 60 ns
22. A divide-by- 78 counter can be realized by using
 (a) 6 numbers of mod-13 counters
 (b) 13 numbers of mod-6 counters
 (c) one mod-13 counter followed by one mod-6 counters
 (d) 13 numbers of mod-13 counters
23. In the circuit as shown above, assuming initially $Q_0 = Q_1 = 0$. Then the states of Q_0, Q_1 immediately after the 333rd pulse are

 (a) 1 1 (b) 1 0
 (c) 0 1 (d) 0 0
24. Consider the following shift right register:

- The initial contents of the 4-bit serial-in parallel-out, shift right register shown above are 0110. What will be the contents of the register after 3 clock pulses are applied?
 (a) 0000 (b) 0101
 (c) 1010 (d) 1111
25. A 4-bit serial -in-parallel-out shift register is used with a feedback as shown in figure

- If the output is 0000 initially, the output repeats after
 (a) 4 clock cycles (b) 6 clock cycles
 (c) 15 clock cycles (d) 16 clock cycles
26. The output of the circuit shown below will be of the frequency

 (a) 125 Hz (b) 250 Hz
 (c) 500 Hz (d) 750 Hz
27. The circuit given below is that of a

 (a) Mod-5 counter (b) Mod-6 counter
 (c) Mod-7 counter (d) Mod-8 counter
28. In a ripple counter the state whose output has a frequency equal to $1/8^{\text{th}}$ that of clock signal applied to the first stage also has an output periodicity equal to $1/8^{\text{th}}$ that of the output signal obtained from the last stage. The counter is
 (a) Modulo-8 (b) Modulo-6
 (c) Modulo-64 (d) Modulo-16
29. Minimum number of JK flip-flops needed to construct a BCD counter is
 (a) 2 (b) 3
 (c) 4 (d) 5

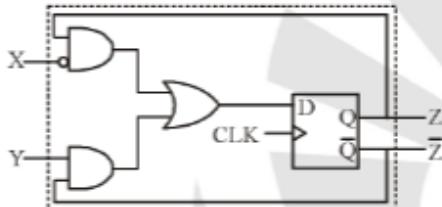
30. Consider the following conditions

1. $t_p < \Delta t$
2. $\Delta t < T$
3. $t_p > \Delta t$
4. $\Delta t > T$

where t_p = pulse width, Δt = propagation delay and T = clock period. The race around condition in the flip-flop can be avoided if conditions

- (a) 1 and 2 are satisfied
- (b) 1 and 4 are satisfied
- (c) 2 and 3 are satisfied
- (d) 3 and 4 are satisfied

31. A sequential circuit using D flip-flop and logic gates is shown in figure, where X and Y are the input and Z is the output. The circuit is



- (a) SR Flip-Flop with inputs $X = R$ and $Y = S$
- (b) SR Flip-Flop with inputs $X = S$ and $Y = R$
- (c) JK Flip-Flop with inputs $X = J$ and $Y = K$
- (d) JK Flip-Flop with inputs $X = K$ and $Y = J$

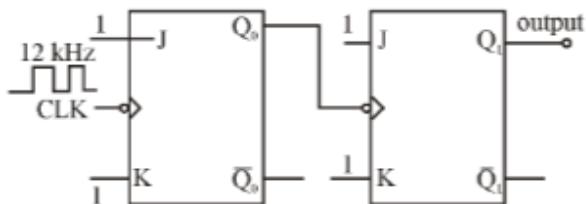
32. In a JK flip flop the output Q_n is 1. It does not change when a clock pulse is applied. The possible combination of J_n and K_n could be (\times denote don't care)

- (a) \times and 0
- (b) \times and 1
- (c) 0 and \times
- (d) 1 and \times

33. A 4 bit ripple counter and a 4 bit synchronous counter are made using flip flops having a propagation delay of 10 ns each. If the worst case delay in the ripple counter and the synchronous counter be R and S respectively, then

- (a) $R = 10 \text{ ns}$, $S = 40 \text{ ns}$
- (b) $R = 40 \text{ ns}$, $S = 10 \text{ ns}$
- (c) $R = 10 \text{ ns}$, $S = 30 \text{ ns}$
- (d) $R = 30 \text{ ns}$, $S = 10 \text{ ns}$

34. An input frequency of 12 kHz is applied to the JK flip-flop arrangement shown in the given figure. The resulting output frequency will be

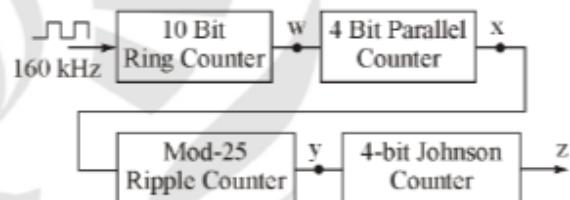


- (a) 24 kHz
- (b) 12 kHz
- (c) 6 kHz
- (d) 3 kHz

35. The initial state of MOD-16 down counter is 0110. After 37 clock pulses, the state of the counter will be

- (a) 1011
- (b) 0110
- (c) 0101
- (d) 0001

36. The frequency of the pulse at z in the network shown in figure is



- (a) 10 Hz
- (b) 160 Hz
- (c) 40 Hz
- (d) 5 Hz

37. 12 MHz clock frequency is applied to a cascaded counter of mod-3 counter, mod-4 counter and mod-5 counter. What are the lowest output frequency and the overall respectively?

- (a) 200 kHz, 60
- (b) 1 MHz, 60
- (c) 3 MHz, 12
- (d) 4 MHz, 12

38. A 4 bit mod-16 ripple counter uses JK flip flops. If the propagation delay of each flip flop is 50 ns, the maximum clock frequency that can be used is equal to

- (a) 20 MHz
- (b) 10 MHz
- (c) 8 MHz
- (d) 5 MHz

39. The mod number of a Johnson counter will be always equal to the number of flip flops used is

 - same
 - twice
 - 2^N where N is the number of flip flops
 - None of these

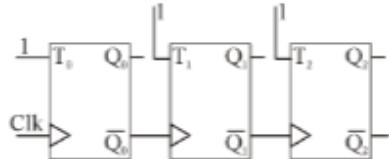
40. Consider a 4 bit Johnson counter with an initial value of 0000. The counting sequence of this counter is

 - 0, 1, 3, 7, 15, 14, 12, 8, 0
 - 0, 1, 3, 5, 7, 9, 11, 13, 15, 0
 - 0, 2, 4, 6, 8, 10, 12, 14, 0
 - 0, 8, 12, 14, 15, 7, 3, 1, 0

41. The total number of 1's in a 15-bit shift register is to be counted by clocking into a counter which is preset to 0. The counter must have which one of the following?

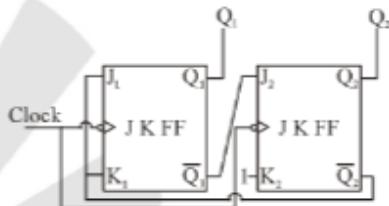
(a) 4-bits	(b) 5-bits
(c) 16-bits	(d) 6-bits

42. Figure shows a ripple counter using positive edge triggered flip-flops. If the present state of the counter is $Q_2Q_1Q_0 = 011$, then its next state ($Q_2Q_1Q_0$) will be



- (a) 010 (b) 100
 (c) 111 (d) 101

43. What are the counting states (Q_1 , Q_2) for the counter shown in the figure below?



- (a) 11, 10, 00, 11, 10,....
 - (b) 01, 10, 00, 01, 10,....
 - (c) 00, 11, 01, 10, 00,....
 - (d) 01, 10, 00, 01, 10,....

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ANSWER KEY

1. *Ans. (b)*
 2. *Ans. (c)*
 3. *Ans. (d)*

Truth table of J K flip flop

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Hence the sequence at the Q output is 010101

4. *Ans. (c)*

The characteristic equation for the next state ($Q_n + 1$) of a JK flip flop is

$$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$

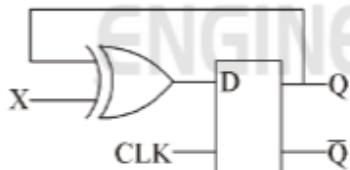
5. *Ans. (a)*

The characteristic equation of the T flip flop is given by

$$\begin{aligned} Q_{n+1} &= Q^+ \\ &= T\bar{Q}_n + \bar{T}Q_n \\ \Rightarrow Q^+ &= \bar{T}Q + T\bar{Q} \end{aligned}$$

6. *Ans. (c)*

7. *Ans. (c)*



The above digital circuit shown works as a T flip flop.

This shows realization of T flip flop using D flip flop. Here X is the input of the flip flop

$$D = X\bar{Q} + \bar{X}Q$$

8. *Ans. (a)*

9. *Ans. (a)*

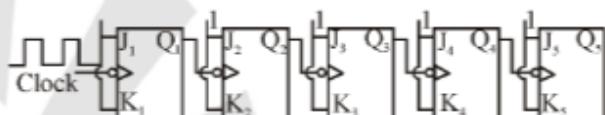
10. *Ans. (d)*

11. *Ans. (c)*
 12. *Ans. (c)*
 13. *Ans. (c)*

To design a BCD or Decade (MOD-10) counter that has ten states i.e 0 to 9, the number of flip flops required is four.

$$\begin{aligned} N &= 10 \\ 2^{n-1} \leq N \leq 2^n \\ \Rightarrow 2^3 \leq 10 \leq 2^4 \\ \Rightarrow n &= 4 \end{aligned}$$

14. *Ans. (b)*



Consider the ripple counter shown above. Here the input consists of a sequence of pulses of frequency f_0 .

Q_1 changes only when the clock input makes a transition from 1 to 0. Thus, at the first negative transition of the clock, Q_1 changes from 0 to 1 and at the second negative transition of the clock Q_1 shifts from 1 to 0. Therefore, two input pulses will result in a single pulse in Q_1 . Hence

frequency of Q_1 will be $\frac{f_0}{2}$. Similarly frequency of Q_2 signal will be $\frac{f_0}{4}$. Similarly frequency of

Q_3 will be $\frac{f_0}{8}$. Given that $f_0 = 10$ MHz

\therefore The frequency of third flip flops output

$$= \frac{f_0}{8} = \frac{10}{8} = 1.25 \text{ MHz}$$

15. *Ans. (d)*

The NAND gate output is connected to CLEAR inputs of each flip flop. As long as the NAND gate output is HIGH, it will have no effect on the counter. When the NAND gate output goes Low, it will clear all flip flops and the counter immediately goes to the 000 state.

The outputs of the counter Q_B and Q_C are given as inputs to the NAND gate. The NAND gate output goes low whenever $Q_B = Q_C = 1$. This condition will occur when the counter goes from the 101 state to the 110 state (on the sixth input pulse).

The low at the NAND gate output will clear the counter to the 000 state. Once the flip flops have been cleared, the NAND gate output goes back to HIGH, since $Q_B = Q_C = 1$ condition no longer exists.

Therefore the counting sequence is 000 → 001 → 010 → 011 → 100 → 101 → 000 → Thus counter essentially skips 110 and 111 states going only through six different states. Thus MOD-6 counter skips 2 counts.

16. **Ans. (c)**

17. **Ans. (b)**

The number of flip flops required (n) for the desired MOD number- N is given as

$$2^{n-1} \leq N \leq 2^n$$

For $N = 5$

$$2^2 \leq 5 \leq 2^3$$

$$\Rightarrow n = 3$$

18. **Ans. (b)**

The counter circuit shown in figure is a 3 bit ripple up counter using positive edge triggered flip flops.

Present state 011		
Next State 100		
Q_2	Q_1	Q_0
0	0	0
0	0	1
0	1	0
0	1	PS
1	0	CNS
1	0	1
1	1	0
1	1	1

19. **Ans. (c)**

The number of unused states in an n bit Johnson counter = $2^n - 2n$.

For 4 bit Johnson counter number of unused states = $2^4 - 2 \times 4 = 8$

20. **Ans. (a)**

The number of distinct states in the ring counter, i.e. the mod of the ring counter is equal to the number of flip flops used in the counter.

An n bit ring counter can count n bits where as an n bit ripple counter can count 2^n bits.

Thus a ring counter consisting of five flip flop will have 5 states.

21. **Ans. (a)**

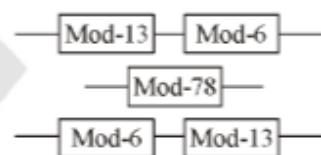
In synchronous counters, the speed limitation of ripple counters is overcome by applying clock pulses simultaneously to all the flip flops which

leads to the settling time of the counter being equal to the propagation delay of a single flip flop. Propagation delay time of a single flip flop = 15 ns Thus time required for change of state will be 15 ns

22. **Ans. (c)**

Ripple counters can be connected in cascade to increases the modulus of the counter. A mod M and a mod- N counter in cascade give a mod- MN counter.

Thus a divide by-78 counter can be realized by using one mode-13 counter followed by one mod-6 counter



Note : The order of cascading does not affect the frequency division.

23. **Ans. (d)**

24. **Ans. (c)**

25. **Ans. (b)**

26. **Ans. (a)**

27. **Ans. (c)**

28. **Ans. (c)**

29. **Ans. (c)**

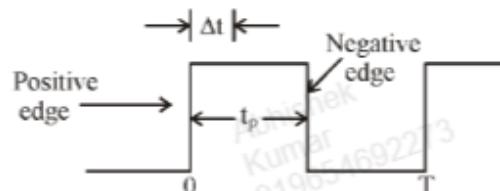
To construct a BCD counter that has ten states i.e. (0 to 9) the number of JK flip flops required is four.

30. **Ans. (a)**

The truth table of JK flip flop is

J_n	K_n	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	\bar{Q}_n

Let the inputs to JK flip flop are $J = K = 1$ and $Q = 0$.



A pulse shown above is applied at clock input. After a time interval Δt , the output will change to $Q = 1$ to $Q = 0$.

Hence we find that for the duration t_p of clock pulse, the output will oscillate back and forth between 0 and 1. At the end of clock pulse, the value of Q is uncertain.

This situation is referred to as race around condition. The race around condition can be avoided if

$$t_p < \Delta t < T$$

31. *Ans. (d)*
32. *Ans. (a)*
33. *Ans. (b)*

In a ripple counter each flip flop is triggered by the output from the previous flip flop which limits its speed of operation. The settling time in ripple counters is the cumulative sum of the individual settling times of flip flops.

Propagation delay of one flip flop = 10 ns
 \therefore Settling time of 4 bit ripple counter = 40 ns
 In synchronous counters the speed limitation of ripple counters is overcome by applying clock pulses simultaneously to all the flip flops which leads to the settling time of the counter being equal to the propagation delay of a single flip flop.
 Propagation delay of one flip flop = 10 ns
 Settling time of 4 bit synchronous counter = 10 ns
 $\therefore R = 40 \text{ ns}$
 $S = 10 \text{ ns}$

34. *Ans. (d)*

Input frequency $f_{in} = 12 \text{ kHz}$

This circuit is used to divide or scale down the input frequency. Such circuits are called frequency divider. Here number of flip flops, $n = 2$

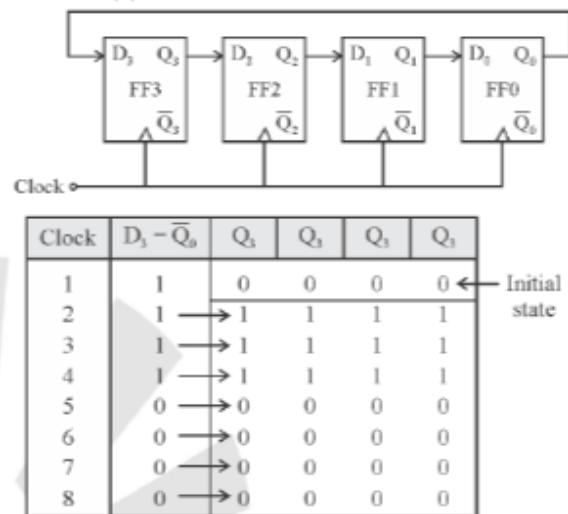
$$\therefore f_0 = \frac{f_{in}}{2^2} = \frac{12}{4} = 3 \text{ kHz}$$

35. *Ans. (d)*

Clock pulse	Output
0	0110
:	:
16	0111
17	0110
:	:
32	0111
33	0110
34	0101
35	0100
36	0011
37	0010
38	0001

Hence after 37 clock pulses, the state of the counter will be 0001.

36. *Ans. (d)*
37. *Ans. (a)*
38. *Ans. (d)*
39. *Ans. (b)*
40. *Ans. (d)*



Hence the switching sequence is:

0, 8, 12, 14, 15, 7, 3, 1, 0.

41. *Ans. (a)*
42. *Ans. (b)*

$$Q_2 Q_1 Q_0 = 011$$

1st clock $Q_2 Q_1 Q_0 = 100$

$$\bar{Q}_0 = 1 \text{ (trigger } T_1\text{)}$$

$$\bar{Q}_1 = 1 \text{ (trigger } T_2\text{)}$$

43. *Ans. (a)*

Initial conditions are not given so by default is

$$Q_1 Q_2 = 00$$

Now make the table according to this condition

Clock	J_1	K_1	J_2	K_2	Q_1	Q_2
0	1	1	1	1	0	0
1	1	1	1	1	1	1
2	0	0	0	1	1	0
3					0	0

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