Mini Project-2B: FPGA Design Project Review 1
(Semester VI)

Vivekanand Education Society's Institute of Technology

Electronics and Telecommunication Engineering

Name of Supervisor: Dr.(Mrs.) Saylee Gharge

Implementation and Analysis of 16 x 16 Vedic Multiplier

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Problem Statement

- To **design, implement and analyze** 16 x 16 Vedic Multiplier using Urdhva -Tiryagbhyam Veda.
- Urdhva -Tiryagbhyam Veda means “Vertical and crosswise technique”.
- In conventional multipliers number of partial products to be added is the main parameter that determines the performance of the multiplier. In conventional method, partial products are summated only after every partial product is obtained. Whereas, in Vedic technique, partial products are obtained vertically and simultaneously once all the elements of a column are obtained, respective partial products are added. Hence, leads to advancement in speed over the conventional method.

Literature Survey

Sr. No.	Title of Technical paper	Name of Author	Year of public-cation	Name of Journal	Methodology	Results	Drawbacks/ limitations
1.	FPGA Implementation of high speed 8-bit Vedic multiplier using barrel shifter.	Pavan Kumar U.C.S, Saiprasad Goud A, A.Radhik	2013	IEEE	8-bit Vedic multiplier compared with conventional multiplier like conventional vedic multiplier, array multiplier, Braun multiplier, modified booth multiplier and Wallace tree multiplier.	Achieved an improvement in the reduction of delay with 45% when compared to array multiplier, booth multiplier and conventional Vedic multiplier implementation on FPGA.	Conventional Vedic multiplier has more propagation delay than Vedic multiplier using barrel shifter.
2.	Modified High Speed 32-bit Vedic Multiplier Design and Implementation	M.Bala Murugesh, S.Nagaraj, J.Jayasree, G.Vijay Kumar Reddy	2020	IEEE	First, a 4-bit Vedic multiplier is designed and in the same manner the size of Vedic multiplier is increased up to 32-bit i.e., 8-bit, 16-bit, and then 32-bit using RCA and then by using CSA.	The paper proposed that when it comes to the terms of time delay then the proposed system is more efficient than existing multipliers.	Drawbacks (propagation delay) due to RSA can be eradicated by using adders of different architectures can be used like Carry Save Adder to make the design faster.
3.	Design and FPGA Implementation of High Speed Vedic Multiplier	Sudeep.M. C, Sharath Bimba.M, Mahendra Vucha.	2014	Internatio nal Journal of Computer Applicati ons.	8 bit multiplier using 2 and 4 bit multiplier. The major change adopted here in the architecture is that they have used Kogge stone algorithm to add partial product.	the proposed technique of multiplication using Urdhva Tiragbyam algorithm and Kogge Stone algorithm causes less latency when compared to available techniques.	Higher speeds can be achieved by making use of pipelining and parallel processing techniques.

Sr. No.	Title of Technical paper	Name of Author	Year of public-cation	Name of Journal	Methodology	Results	Drawbacks/ limitations
4.	Performance comparison of conventional multiplier and Vedic Multiplier Using Simulator.	Dr. G.S. Sunitha, Rakesh H.M	2018	International Journal of Engineering and Manufacturing Science.	The proposed Vedic multiplier is compared with existing conventional multipliers like Booth and Baugh woolly which are coded in Verilog and simulation is done in Xilinx.	The performance metrics of multipliers such as area and delay are determined and compared.	Vedic multiplier shows improved performance but the area occupied by Baugh Wooley Multiplier is 3% lesser than Vedic multiplier and 16% lesser than Booth Multiplier.
5.	Design and Implementation of 64 Bit Multiplier using Vedic Algorithm	Amish Jais, Prasanna Palsodkar	2016	IEEE	Highly efficient 64 bit multiplier for the mantissa calculation using rule or sutra of Vedic mathematics called Urdhva Tiryagbhyam Sutra.	The proposed multiplier has a better delay than previously designed multiplier of a same bit number.	64 x 64 Vedic multiplier using 2,4,8,16,32 bit multiplier has larger delay than 64 x 64 bit multiplier using 8,18,32 bit multiplier.
6.	Design and Implementation of 32bit Complex Multiplier using Vedic Algorithm	Ankush Nikam, Swati Salunke, Sweta Bhurse	2015	IJERT	Design of 32 bit Multiplier using the Indian Vedic Mathematics. Also presents comparison of 8bit, 16bit, 32 bit complex multiplier on various performance parameters like power and delay.	The 32 x 32 bit multiplier using Vedic algorithm is implemented using VHDL and Verilog and functionally verified using Xilinx ISE 14.2	As the number of bits increased, the hardware for the multiplier design increases as well.

Comparison/competition in the market & Research Gap

- **Comparison in the market:**

Vedic multiplier using Urdhva Tiryagbyam sutra shows improved performance in terms of delay and area utilization when compared to many conventional multipliers like Booth Multiplier, Baugh Wooley Multiplier, Wallace Multiplier, Array multiplier etc. Hence, the cost of production as well as hardware for the multiplier reduces significantly.

- **Research Gap:**

Many papers have proposed the design and analyzed 8 x 8 Vedic, 16 x 16 Vedic, 32 x 32 Vedic and 64 x 64 Vedic multiplier but only the implementation of 8 x 8 Vedic Multiplier has been done by few authors because of some limitations. Limitations are implementation of hardware for higher bits is difficult of FPGA boards. Also as the bits of the multiplier increases the area occupied on chip for implementation of the Vedic Multiplier increases.

Proposed Solution

- The project “16 x 16 Vedic Multiplier” will be implemented using Urdhva -Tiryagbhyam Veda.

- The 16 x 16 Vedic Multiplier will require the following modules:
  i. 8 x 8 Vedic multiplier.
  ii. 4 x 4 Vedic multiplier.
  iii. 2 x 2 Vedic multiplier.
  iv. n-bit Adders.

- The analysis for gate delay, computation time, look up tables, slices, total delay, no. of bounded IOB’s, etc will be performed for the described multiplier.

Tools and FPGA used

1. FPGA board: EDGE Spartan 7 FPGA Development Board

- EDGE Spartan 7 FPGA Development board is the low cost and feature rich FPGA kit which is upgraded from EDGE Spartan 6 kit.

- Its features includes FPGA, SPI FLASH, Wi-Fi, Bluetooth, ADC, DAC, LCD, 7 segment, VGA, PS2, Stereo Jack, buzzer, Push Button, Slide Switch, LED, Temperature Sensor, LDR and UART. The Board also provides additional interface like CMOS Camera and TFT Display at the expansion connectors.

- Board Features:
  Xilinx XC7S15 FTGB196-1 Spartan-7 FPGA IC, 8MB SPI FLASH Memory, On-Board USB JTAG Programmer, USB to UART Interface ,WIFI Interface, Low Power Bluetooth Interface, 12 bit VGA Interface, 8 Channel SPI ADC, Temperature Sensor, LDR Interface, SPI DAC, 2×16 LCD Display, 4 Digit Seven Segment Display, 5v Buzzer, PS2 compatible USB interface.

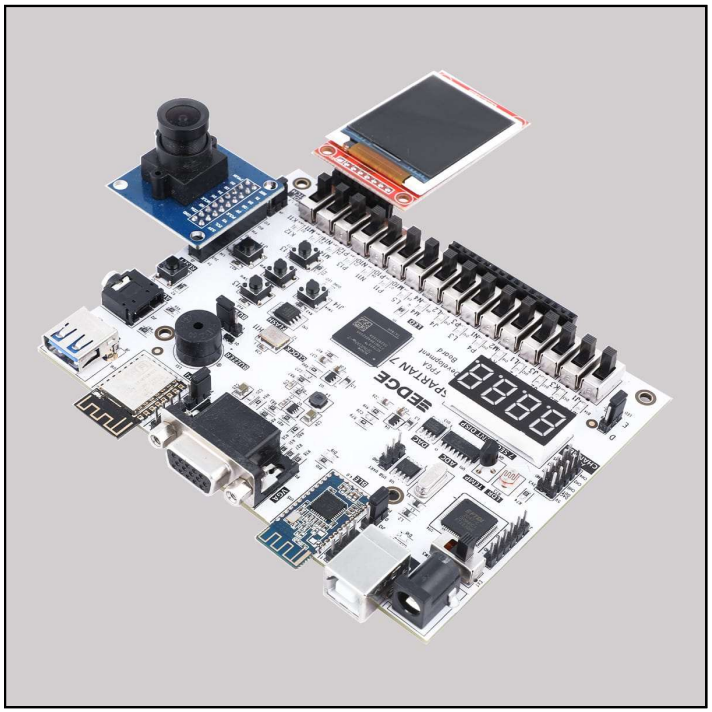


Fig no.14 EDGE Spartan 7 FPGA Board

2. Simulation Tool: Vivado 2019.1 HLx Edition

Algorithm for 2 x 2 Vedic Multiplier

```
              1     0
            x 1     0
-----------------------------------------
      1     |   1   0     |      0
    x 1     | x 1   0     |    x 0
------------|-------------|-----------
      1     |  0 + 0 = 0  |      0
------------|-------------|-----------
   carry = 0|   carry = 0 | carry = 0
------------|-------------|-----------
     STEP 3 |    STEP 2   |  STEP 1


              2     5
            x 2     5
-----------------------------------------
      2     |   2   5     |      5
    x 2     | x 2   5     |    x 5
------------|-------------|-----------
   4+2 = 6  | 10+10+2 = 2 |      5
------------|-------------|-----------
   carry = 0|   carry = 2 | carry = 2
------------|-------------|-----------
     STEP 3 |    STEP 2   |  STEP 1
```

Fig no.1 2 x 2 Vedic Multiplication (Algorithm)

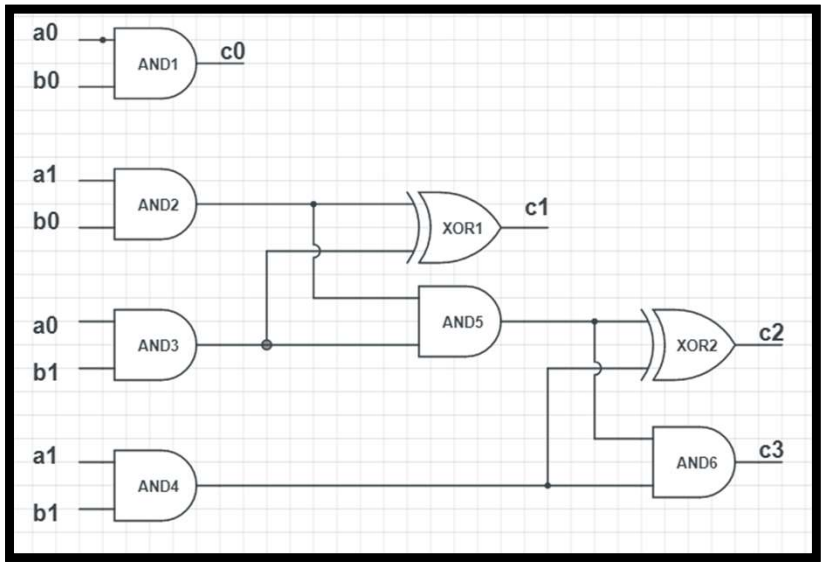


Fig no. 2 2 x 2 Vedic Multiplier Circuit Diagram

4 x 4 and 8 x 8 Vedic Multiplier

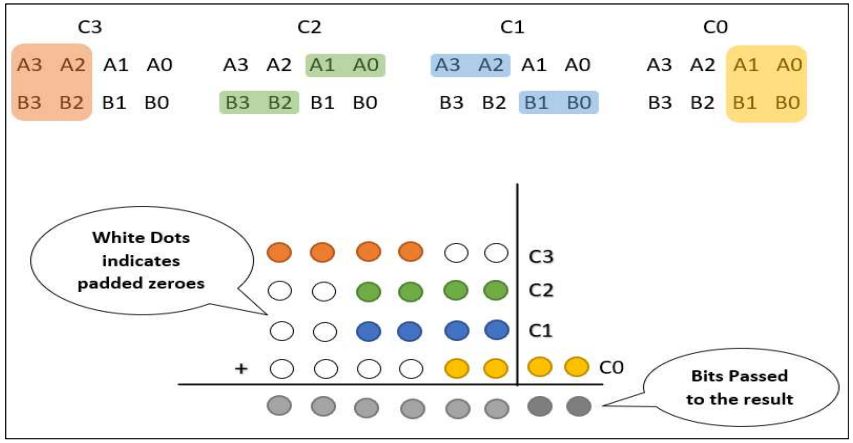


Fig no.3 Algorithm of 4 x 4 Vedic Multiplier

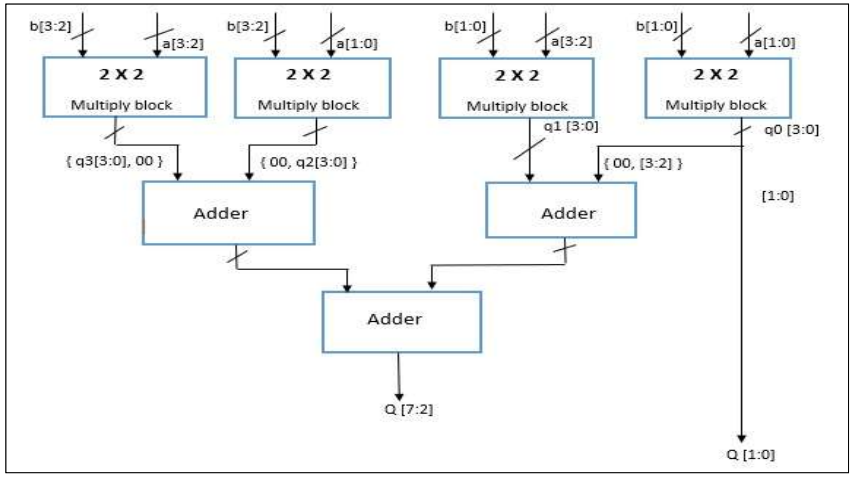


Fig no.4 Block Diagram of 4 x 4 Vedic Multiplier

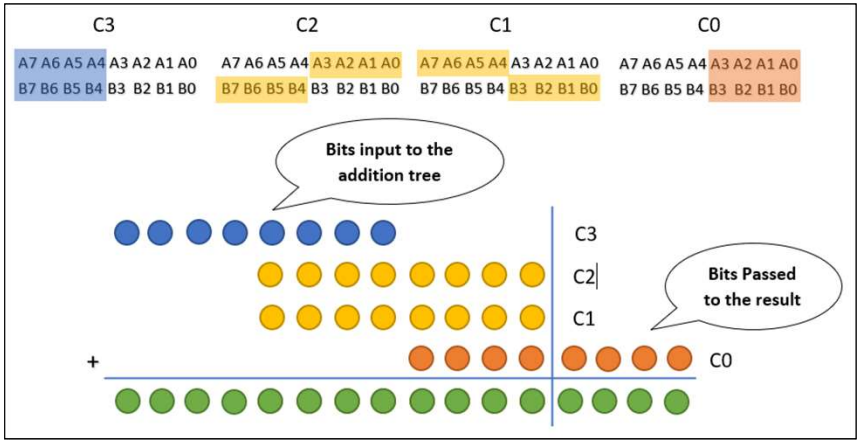


Fig no.5 Algorithm of 8 x 8 Vedic Multiplier

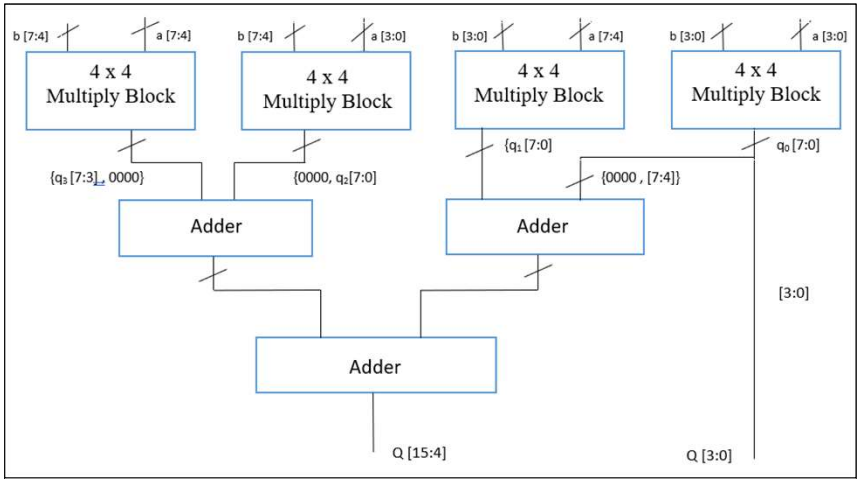


Fig no.6 Block Diagram of 8 x 8 Vedic Multiplier

16 x 16 Vedic Multiplier

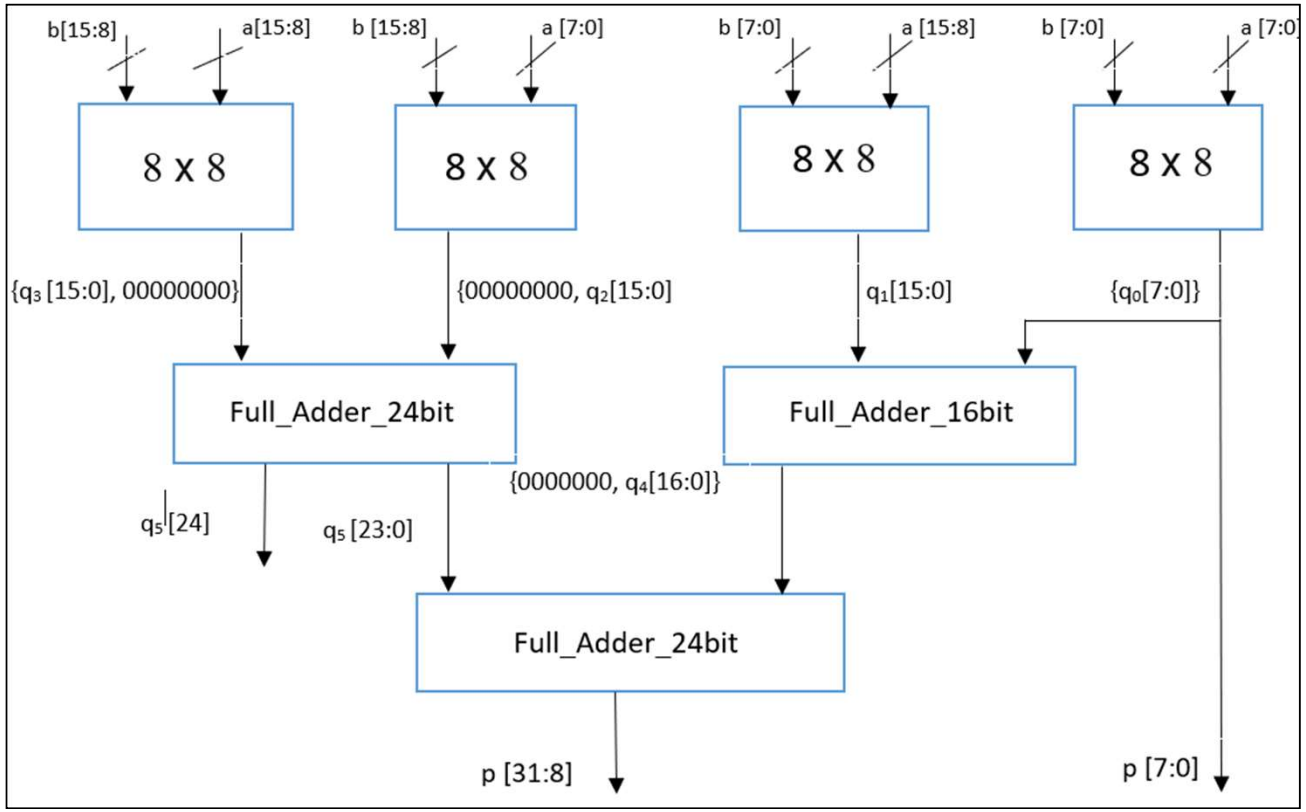


Fig no.7 Block Diagram of 16 x 16 Vedic Multiplier

Software Implementation

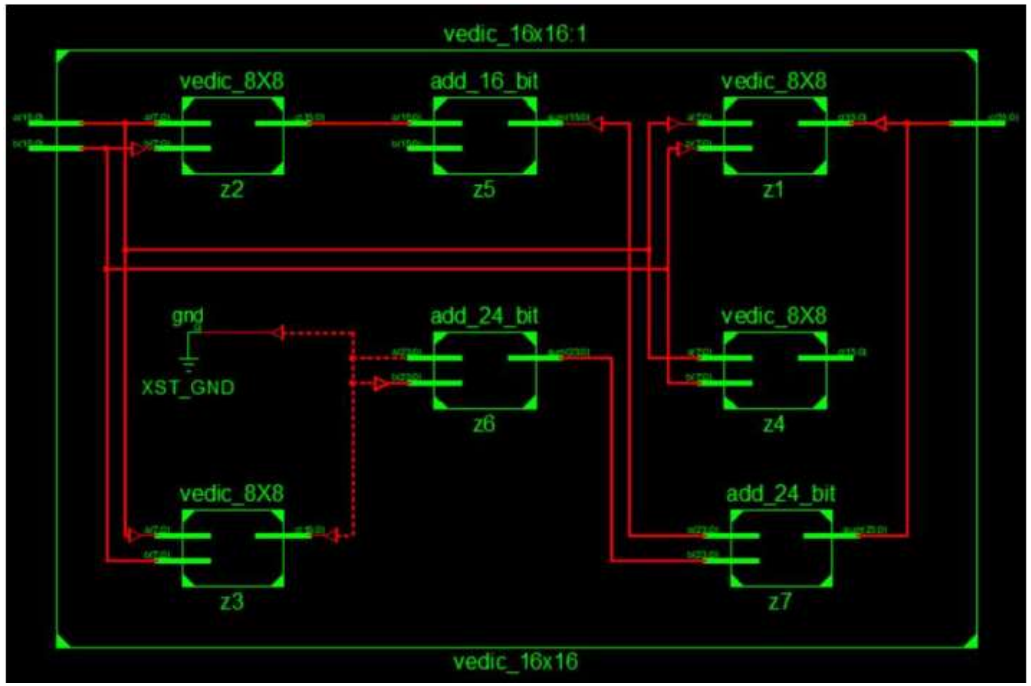


Fig no.8 RTL Schematic of 16-bit Vedic Multiplier

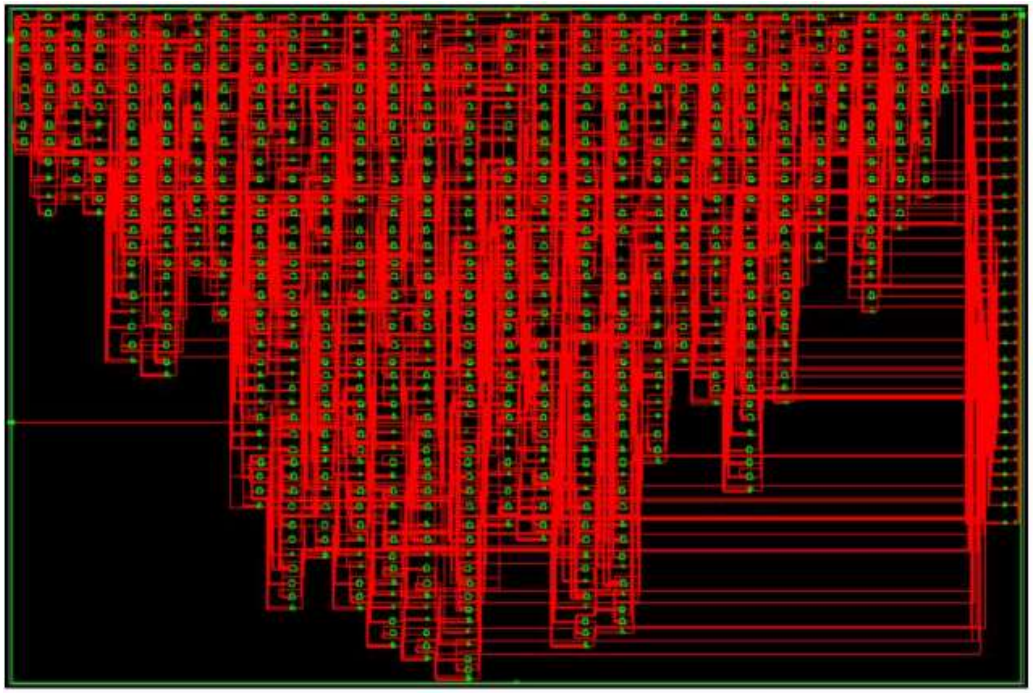


Fig no.9 Technology Schematic of 16-bit Vedic Multiplier

Software Implementation

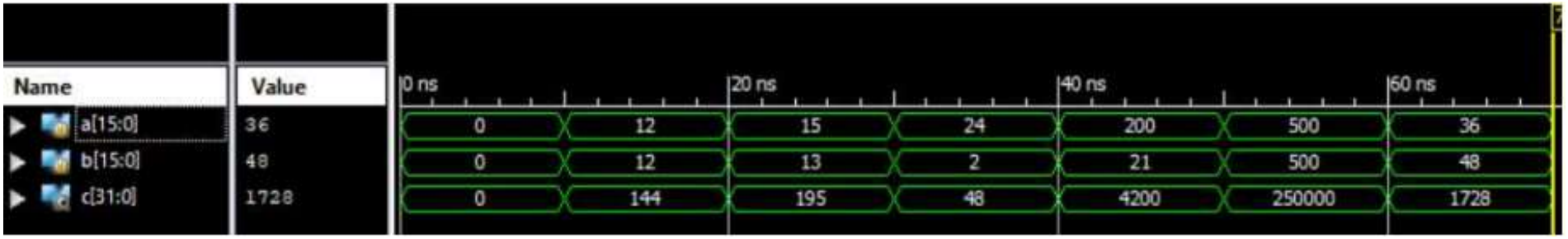


Fig no.10 Simulation results of 16-bit Vedic Multiplier

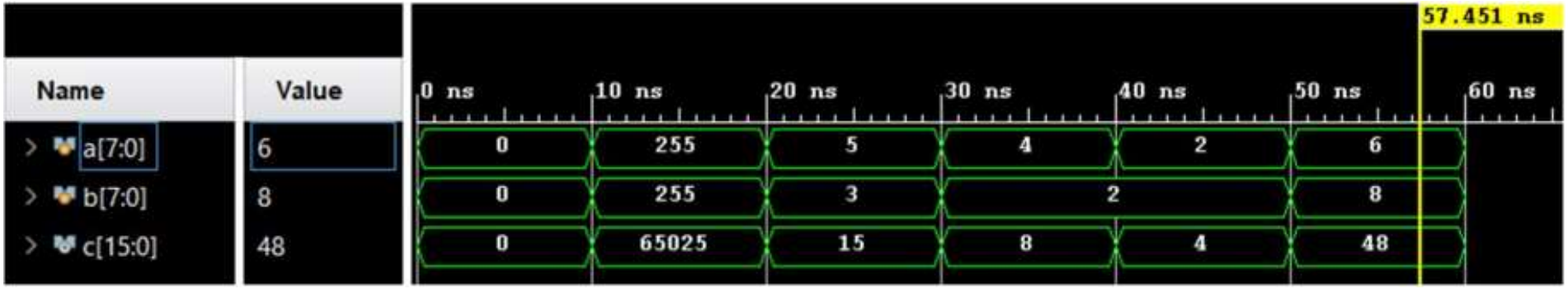
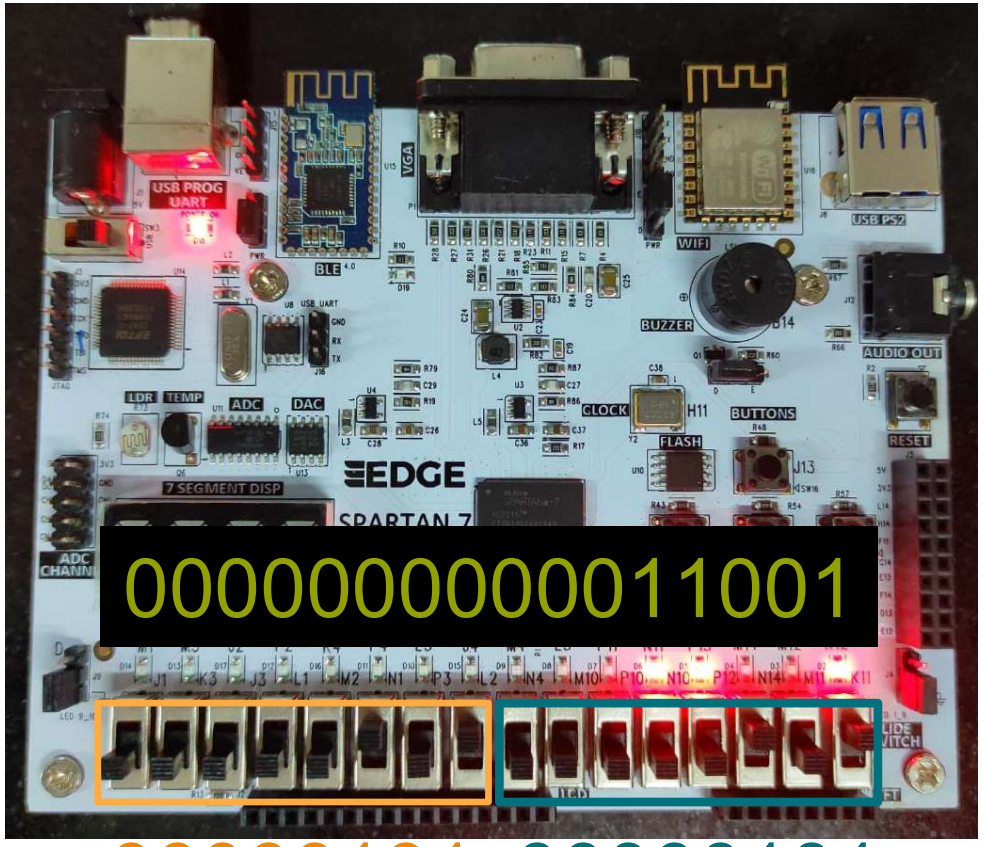


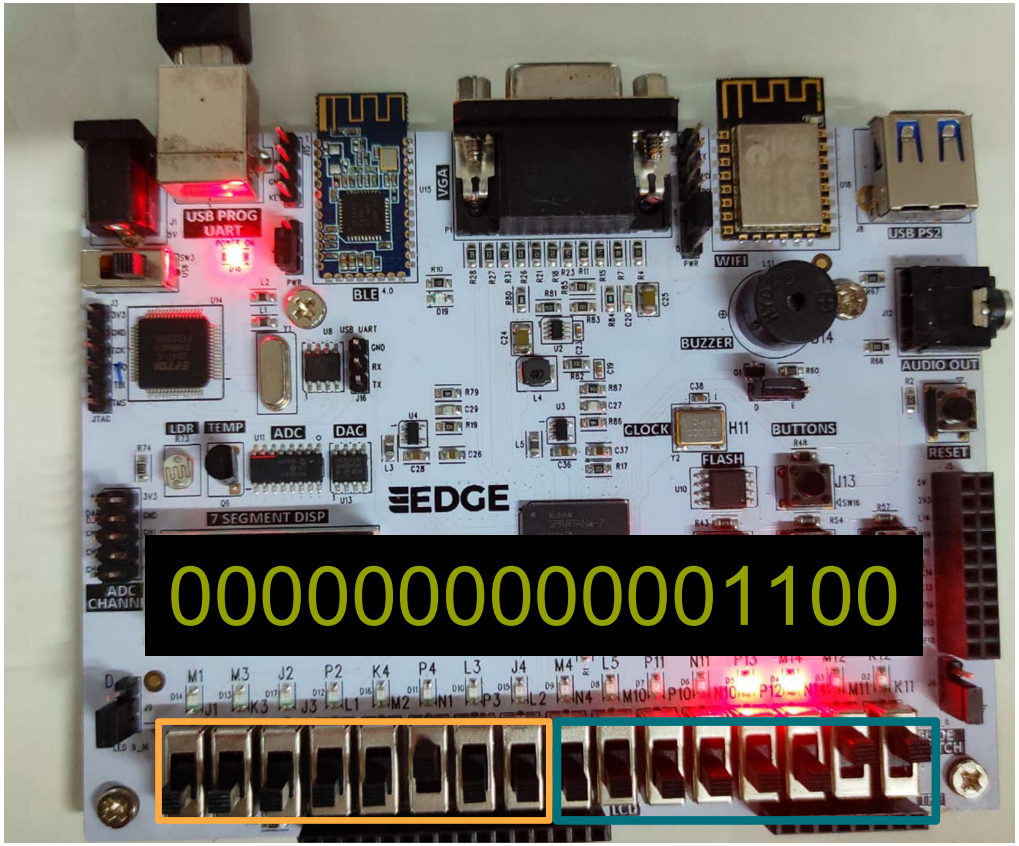
Fig no.11 Simulation results of 8-bit Vedic Multiplier

Hardware Implementation



00000101 00000101

Fig no.12 Implementation of 5 x 5 multiplication for 8-bit VM



00000100 00000011

Fig no.13 Implementation of 4 x 3 multiplication for 8-bit VM

Comparison Table

- Comparison of 8-bit Vedic Multiplier, Wallace Tree Multiplier and Array Multiplier.

Device Used - 6slx9tqg144-2			
Multipliers	**Path delay(ns)**	**Slice LUTs**	**On-chip Power (mW)**
Vedic Multiplier	17.154	91	50.84
Wallace Multiplier	23.545	93	54.55
Array Multiplier	28.870	84	65.41

Table 1: Comparison Table of 8-bit Vedic Multiplier, Wallace Tree Multiplier and Array Multiplier.

Time Chart


January 2022
W1
W2
W3
W4
Literature Survey
February 2022
W1
W2
W3
W4
Finished Verilog Coding
Verified with simulation
March 2022
W1
W2
W3
W4
Ordered the FPGA Board
Implemented the design on FPGA
April 2022
W1
W2
W3
W4
Testing and Troubleshooting
Final Submission

Conclusion

- 8-bit Vedic Multiplier was implemented on EDGE Spartan 7 FPGA board simulated on Vivado Hlx and Xilinx ISE.
- Vedic Multiplier has less propagation delay which is directly proportional to a greater speed than the Wallace Tree and the Array multipliers.
- Vedic Multiplier can be used in cases where speed and power consumption are both important factors.

- **Future Scope**
- Implementation of the complete ALU is possible using Vedic Multiplier Methods.
- Using DSP and ADSP processors, various transforms like FFTs and the IFFTs can be calculated.

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