Experiment-3:

Implementing CMOS-NAND & CMOS-NOR using Microwind 2.

Objective:

We have to create CMOS-NAND and CMOS-NOR layout diagram using Microwind2 and then run it on Microwind2 finally checking its validation of using Timing diagram on Microwind2.

Theory:

i.   Truth Table For COMS-NAND:

A	B	Q_1	Q_2	Q_3	Q_4	Output
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	1
1	0	OFF	ON	ON	OFF	1
1	1	OFF	OFF	ON	ON	0

Table 3.2 Truth table of NAND gate

ii.   Truth Table For COMS-NOR:

A	B	Q_1	Q_2	Q_3	Q_4	Output
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	0
1	0	OFF	ON	ON	OFF	0
1	1	OFF	OFF	ON	ON	0

Table 3.3 Truth table for NOR gate

iii.   Schematic Diagram for CMOS-NAND:
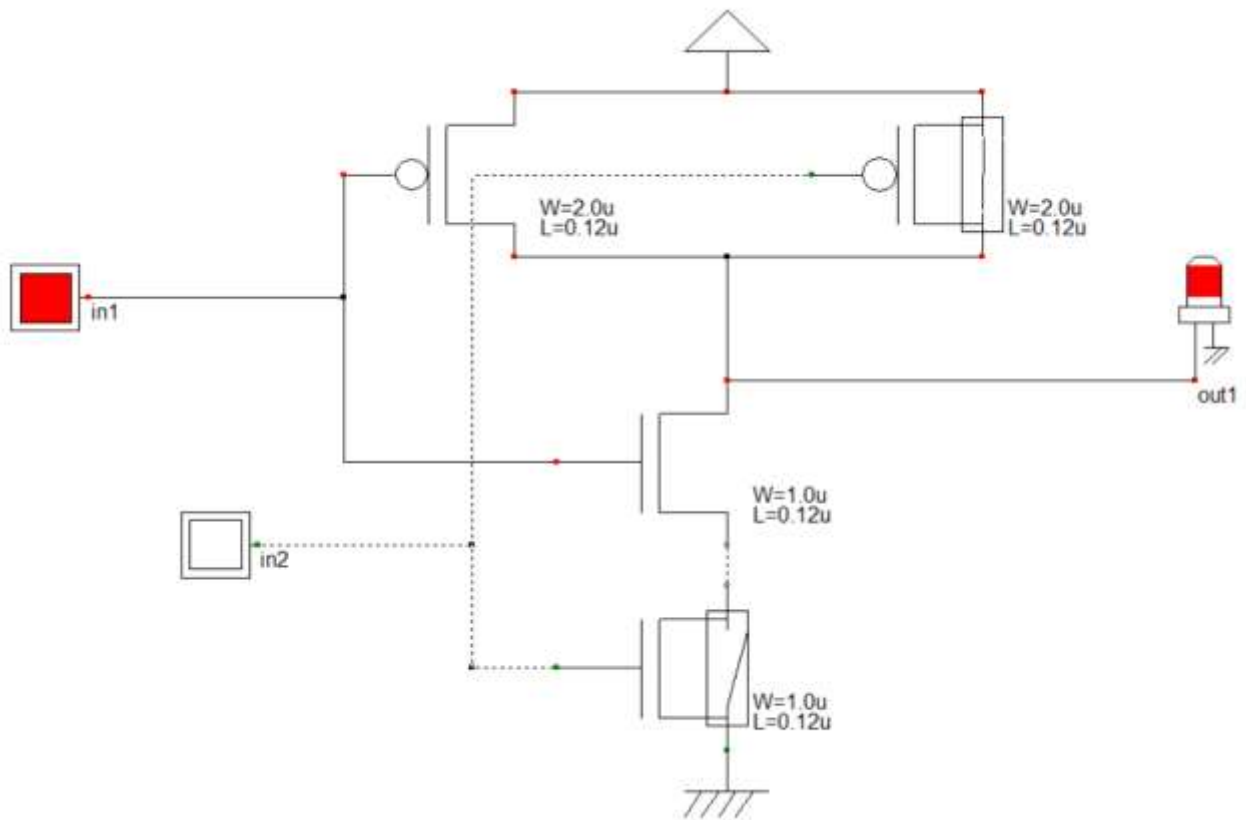
iv.   Schematic Diagram for CMOS-NOR:
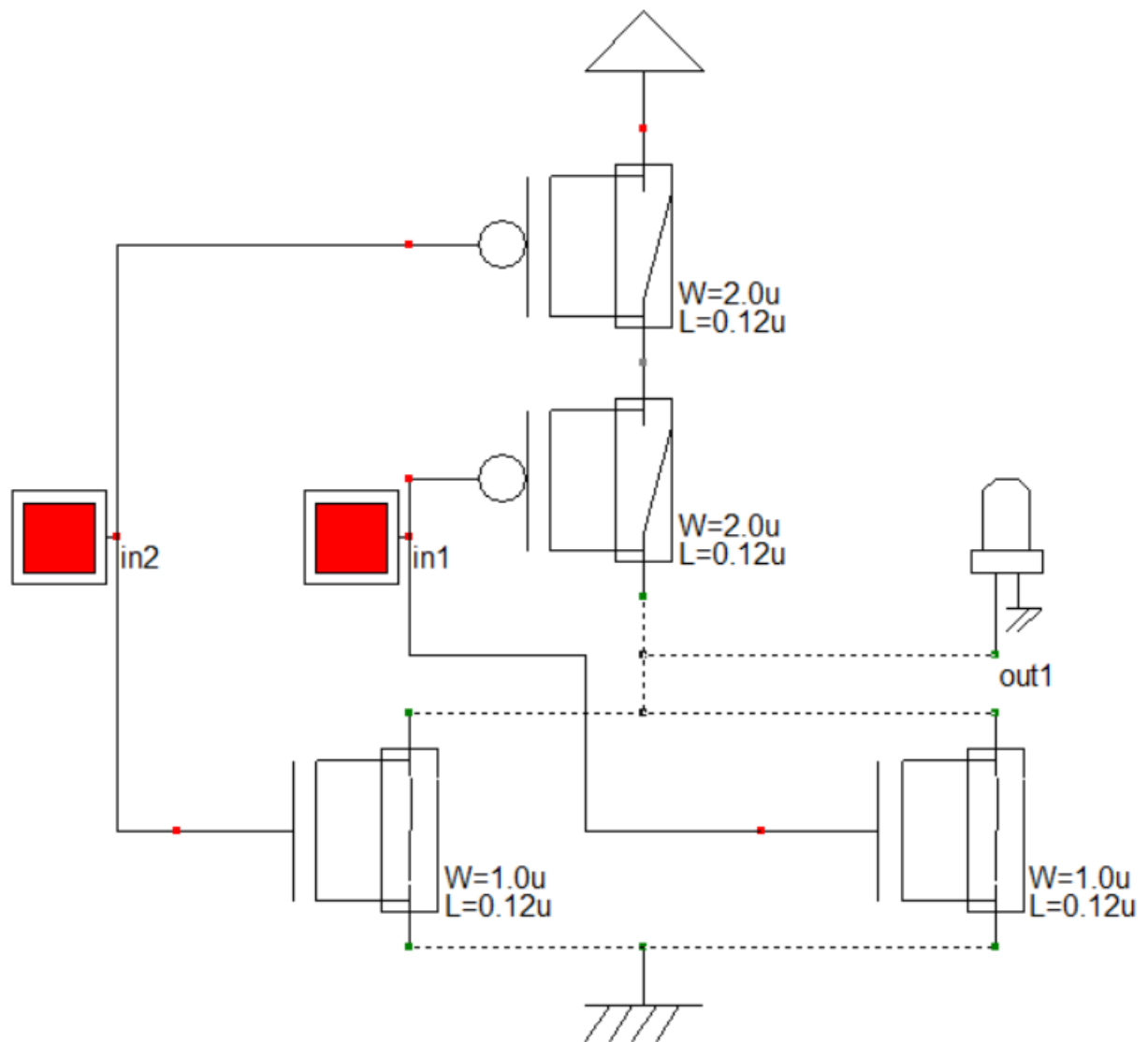
Procedure:

1. At first creating a Schematic Diagram on DHCH2/3.
2. Then save this file as '.sch' format from DHCH2/3.
3. Next in the 'File' option of DHCH2/3, choose 'Make Verilog File'.
4. Next in Microwind2 'File' option, choose 'Select Foundry' option and set the rule 'CMOS 025.RUL'.
5. Finally in Microwind2 'Compile' option, choose 'Compile Verilog File' option and run the '.sch' file that previously saved from DHCH2/3.
6. To see the 'Timing Diagram' press 'Run Simulation' option on Microwind2.
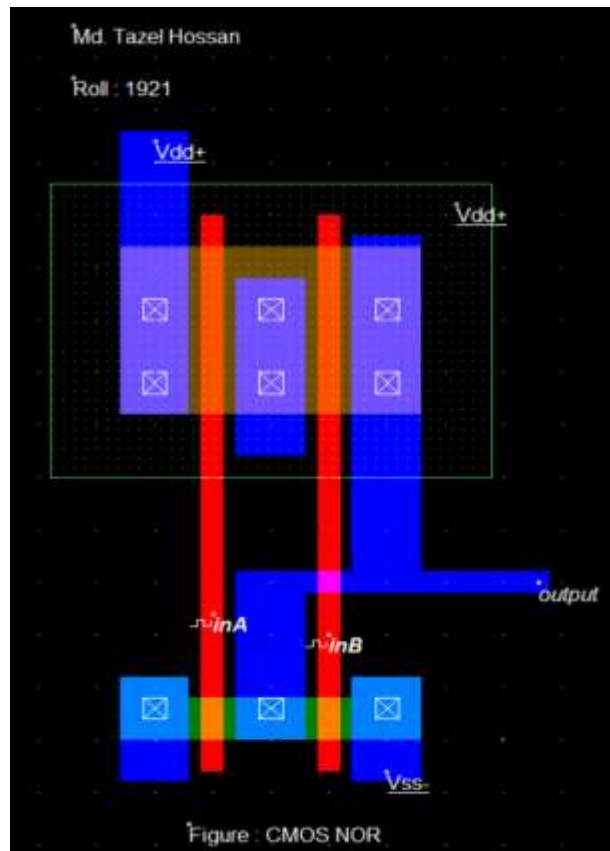
Result:

i.   Layout Diagram for COMS-NAND:

Figure : CMOS NAND
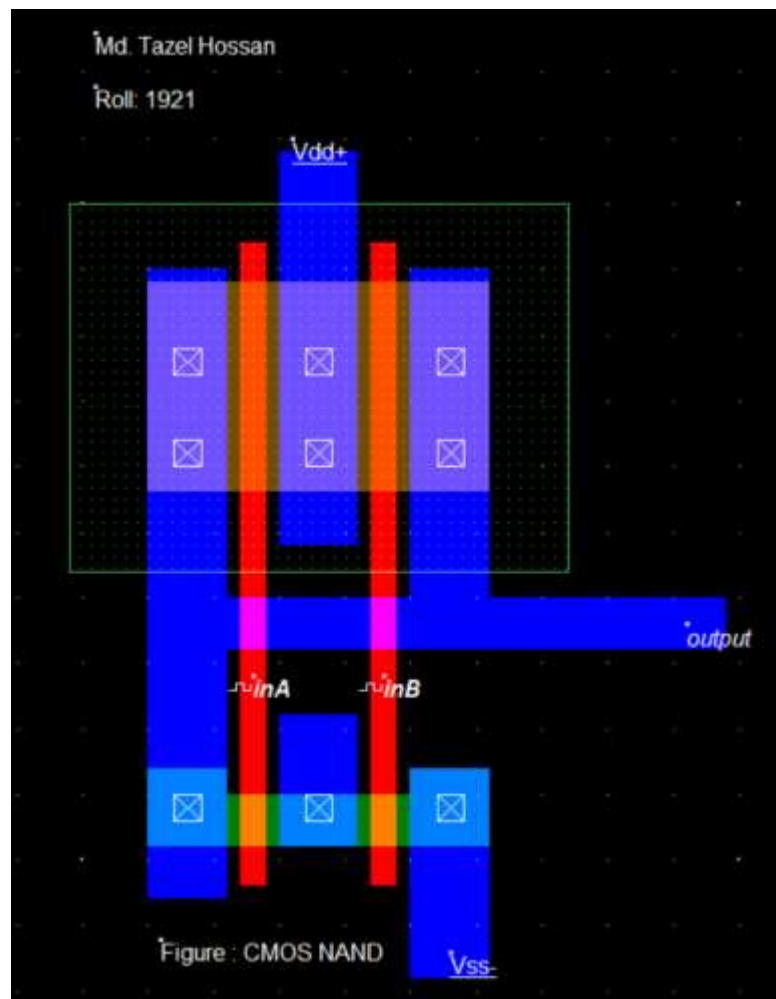
ii.   Timing Diagram for CMOS-NAND
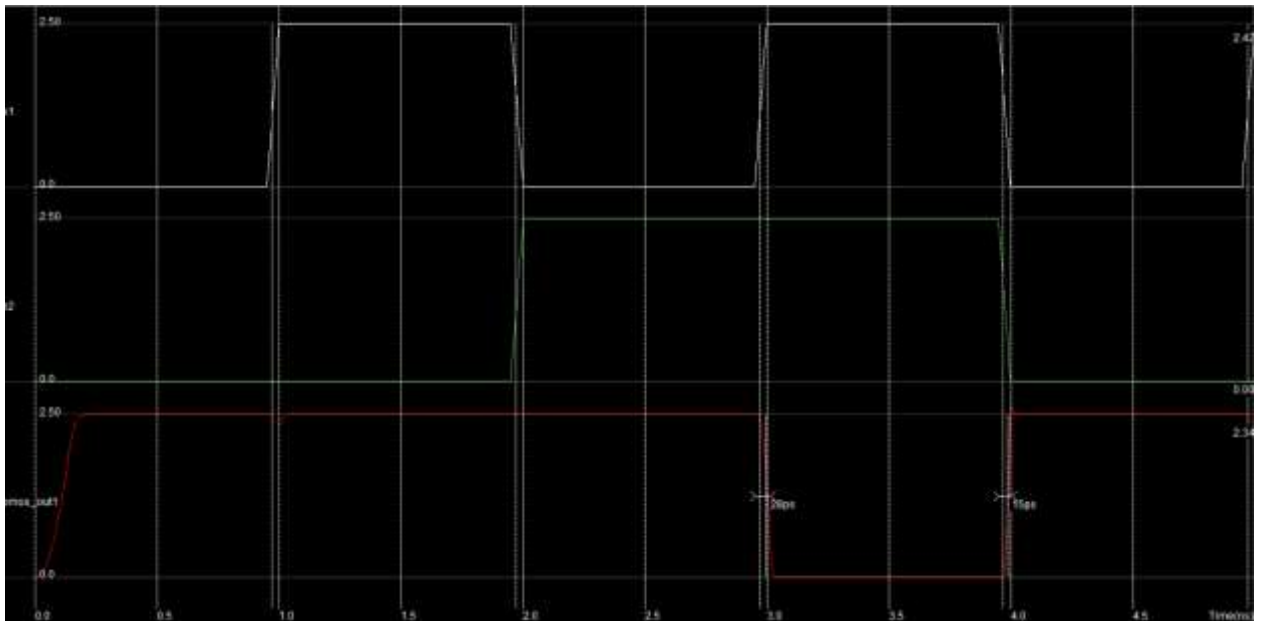
iii.   Layout Diagram for CMOS-NOR

Figure : CMOS NOR

iv. Timing Diagram for CMOS-NOR