Experiment-4:

Design & implementation of XOR gate on silicon using ASCII design tools (DHCH2 & Microwind2).

Objective:

We have to create XOR gate layout diagram using DHCH2 and then run it on Microwind2 finally checking its validation of using Timing diagram on Microwind2.

Theory:

i. Truth Table For X-OR Gate:

Inputs		Output
A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

ii. Truth Table For X-OR:

Inputs		Output
A	B	X
0	0	1
0	1	0
1	0	0
1	1	1

iii. Schematic Diagram for X-OR:

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Roll#:1921

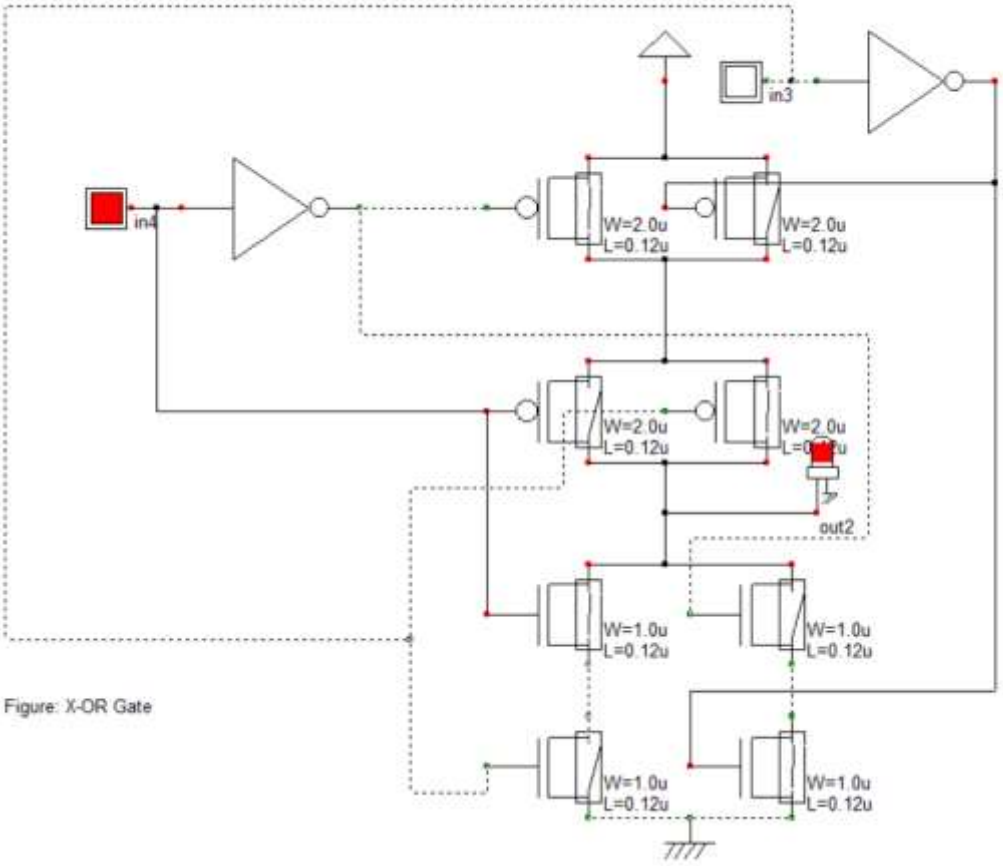


Figure: X-OR Gate

iv. Schematic Diagram for X-NOR:

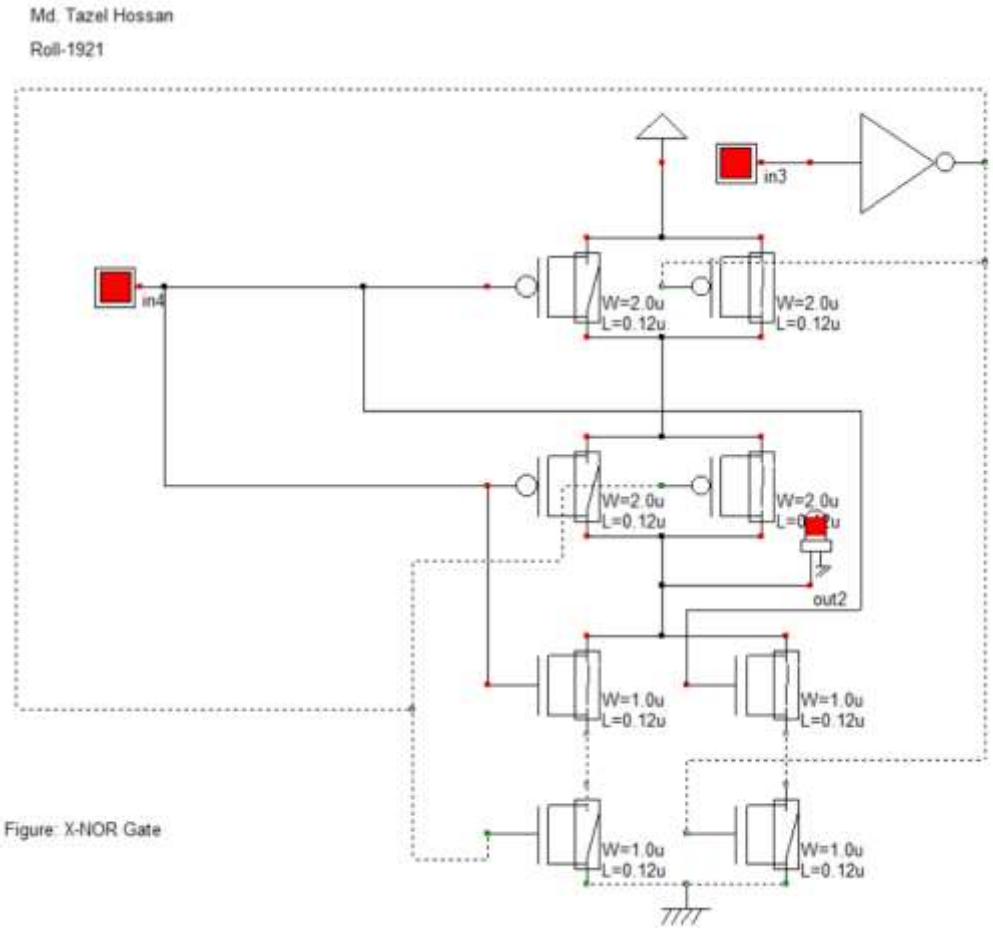


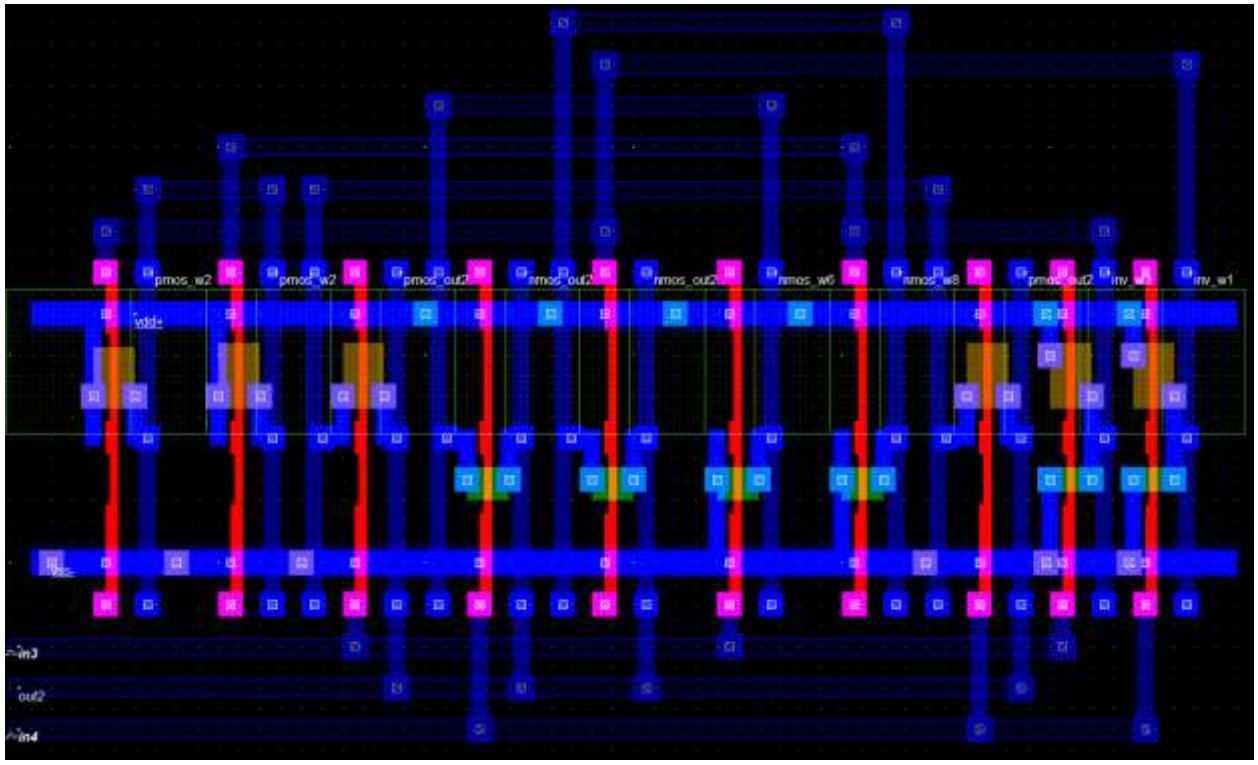
Figure: X-NOR Gate

Procedure:

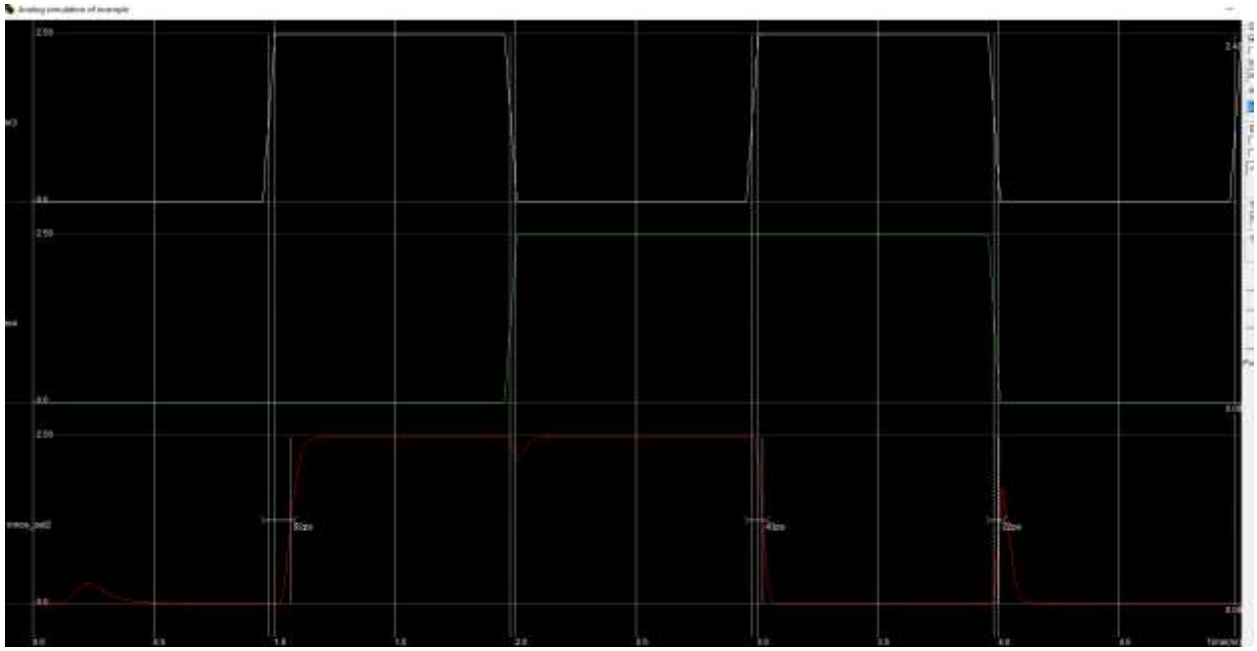
1. At first creating a Schematic Diagram on DHCH2/3.
2. Then save this file as '.sch' format from DHCH2/3.
3. Next in the 'File' option of DHCH2/3, choose 'Make Verilog File'.
4. Next in Microwind2 'File' option, choose 'Select Foundry' option and set the rule 'CMOS 025.RUL'.
5. Finally in Microwind2 'Compile' option, choose 'Compile Verilog File' option and run the '.sch' file that previously saved from DHCH2/3.
6. To see the 'Timing Diagram' press 'Run Simulation' option on Microwind2.

Result:

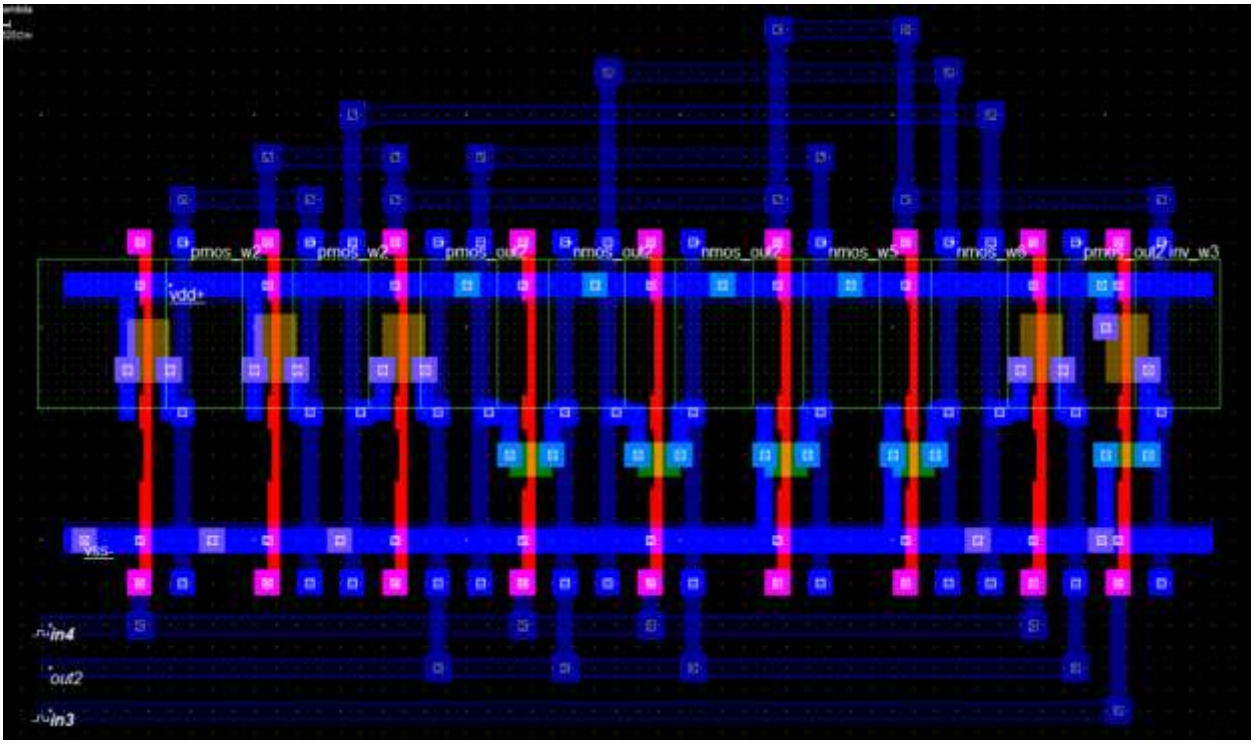
i. Layout Diagram for X-OR:



ii. Timing Diagram for CMOS-NAND



iii. Layout Diagram for X-NOR



iv. Timing Diagram for X-NOR