Experiment-2:

Implementing CMOS-NOR using DHCH2/3 & Microwind 2.

Objective:

We have to create CMOS-NOR schematic diagram using DHCH2/3 and then run its Verilog file on Microwind2 to generate Layout diagram and finally checking its validation of using Timing diagram on Microwind2.

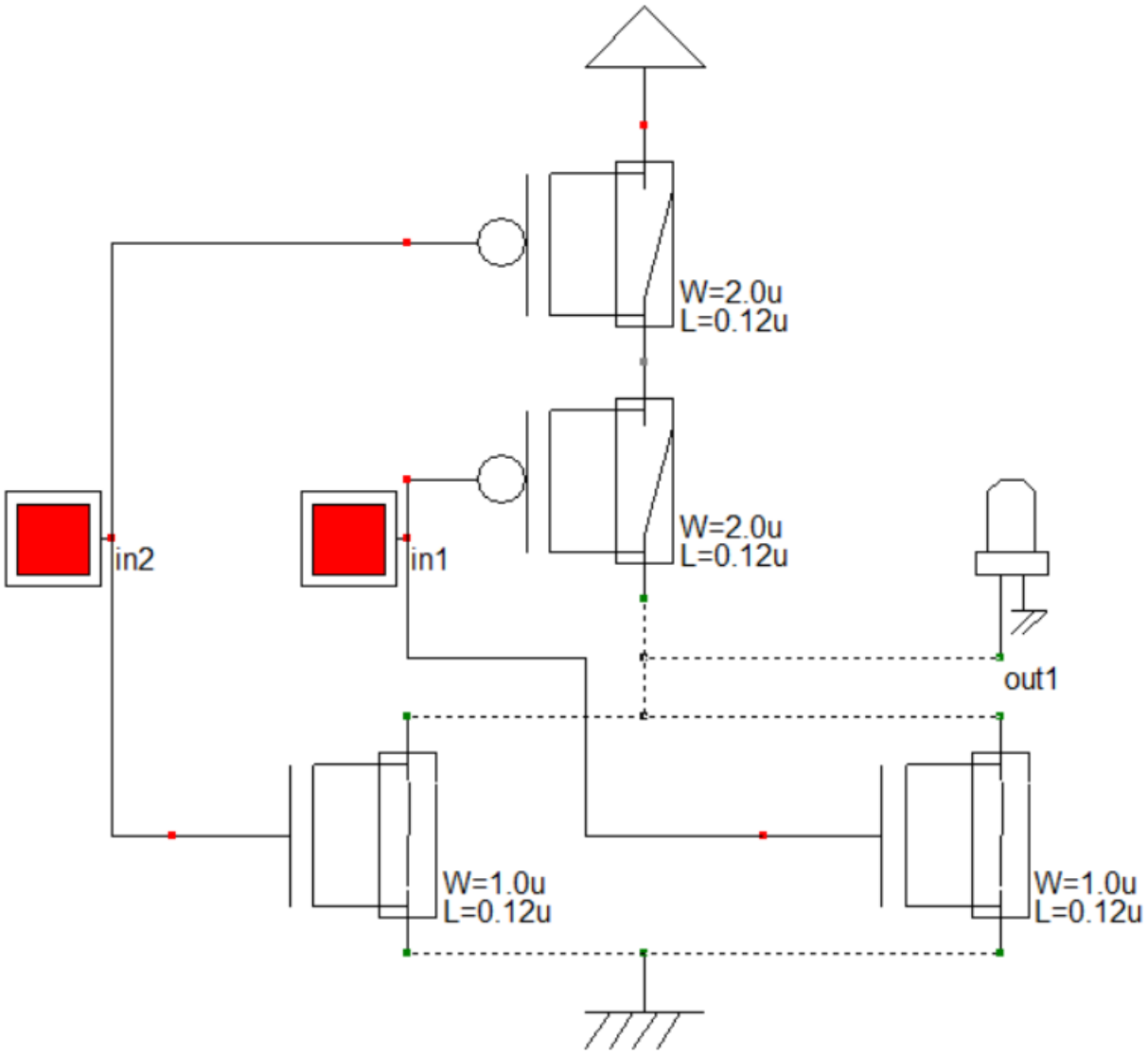
Theory:

i. Truth Table:

A	B	Q_1	Q_2	Q_3	Q_4	Output
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	0
1	0	OFF	ON	ON	OFF	0
1	1	OFF	OFF	ON	ON	0

Table 3.3 Truth table for NOR gate

ii. Schematic Diagram:

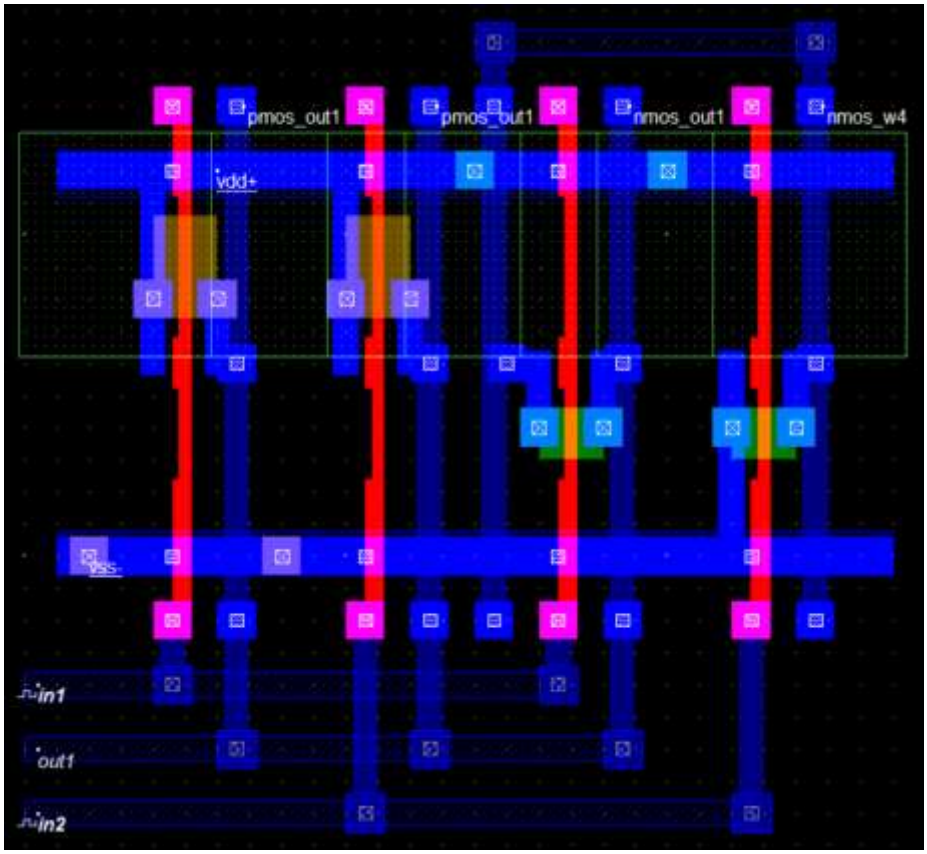


Procedure:

1. At first creating a Schematic Diagram on DHCH2/3.
2. Then save this file as '.sch' format from DHCH2/3.
3. Next in the 'File' option of DHCH2/3, choose 'Make Verilog File'.
4. Next in Microwind2 'File' option, choose 'Select Foundry' option and set the rule 'CMOS 025.RUL'.
5. Finally in Microwind2 'Compile' option, choose 'Compile Verilog File' option and run the '.sch' file that previously saved from DHCH2/3.
6. To see the 'Timing Diagram' press 'Run Simulation' option on Microwind2.

Result:

i. Layout Diagram:



ii. Timing Diagram: