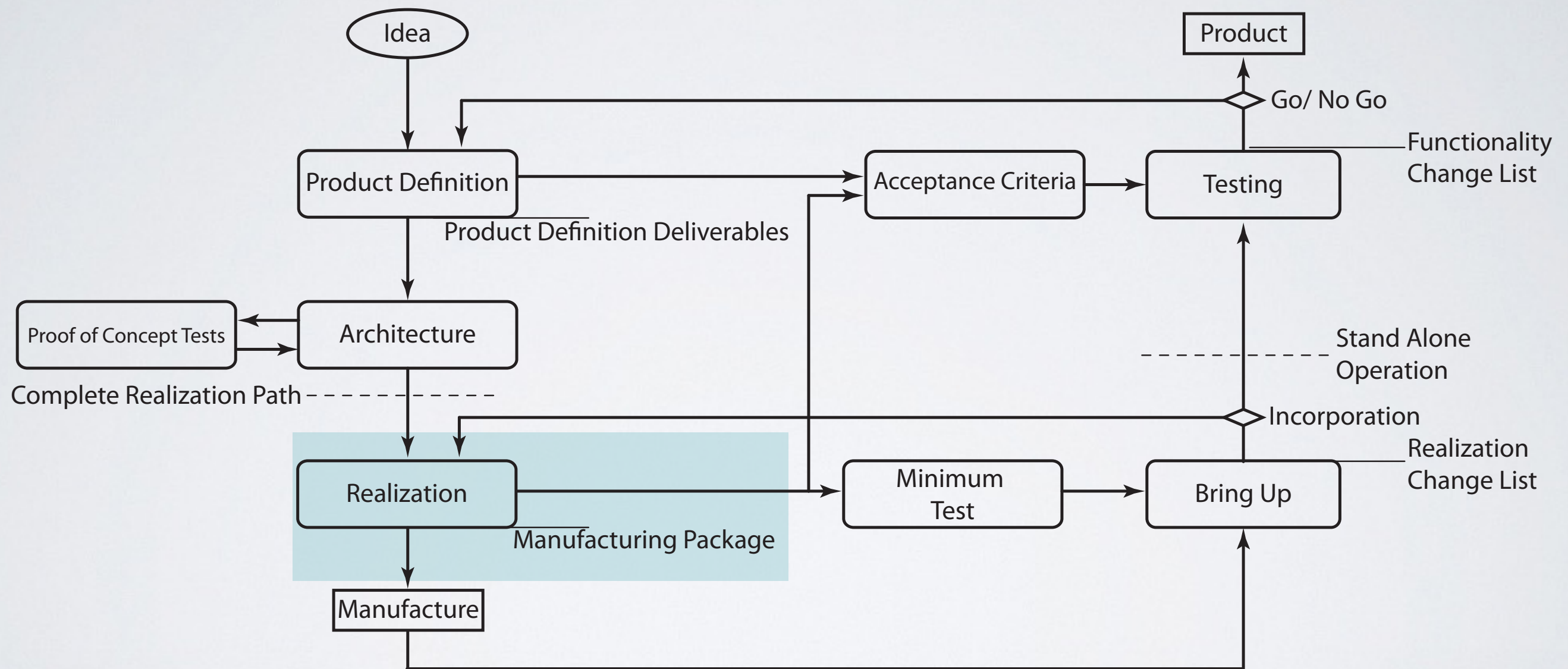


REALIZATION PHASE

The Engineer Accelerator
Malcolm Knapp

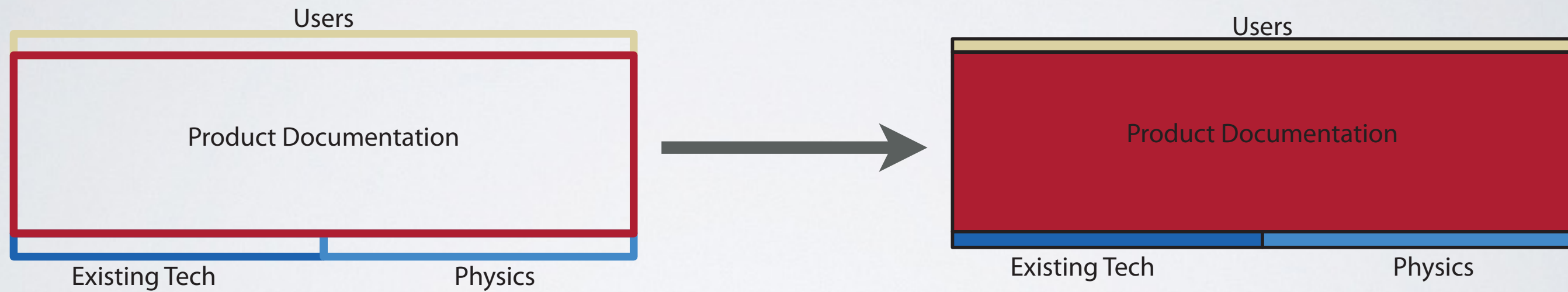
DEVELOPMENT PHASE



GOAL

TO GENERATE THE
MANUFACTURING PACKAGE

PROCESS

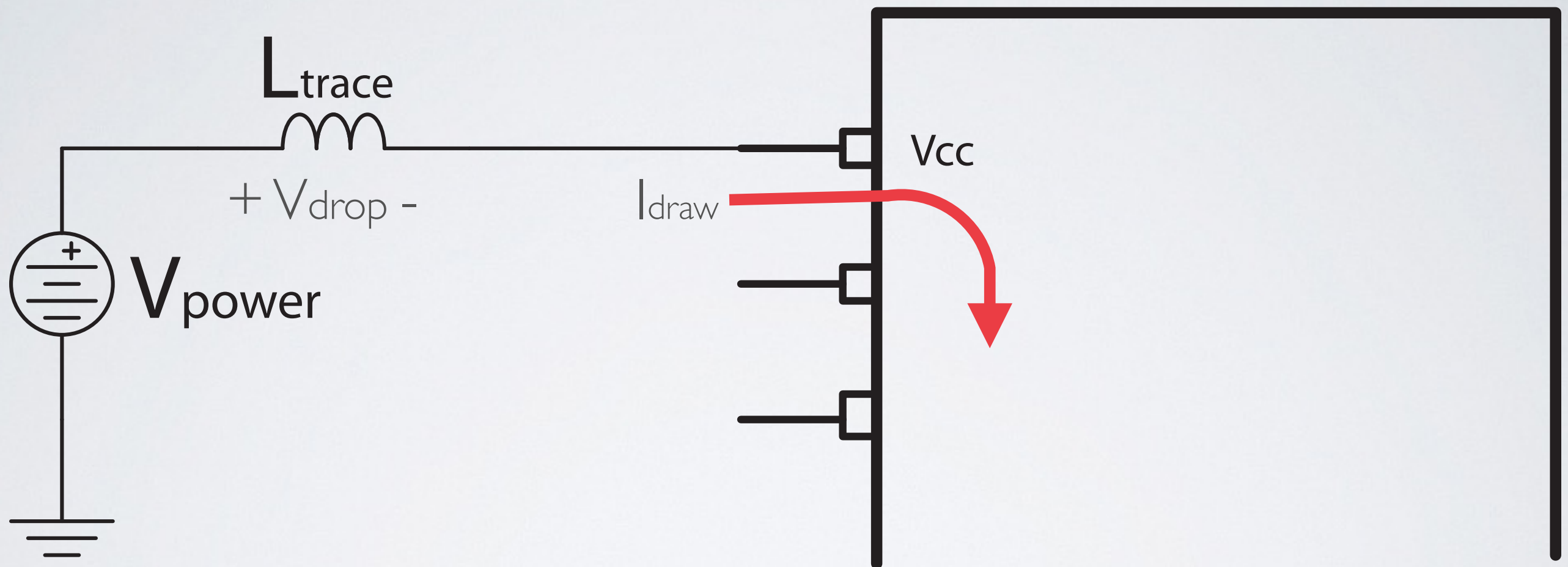


REALIZATION ACTIVITIES

- Detailed Design
 - Bypassing
 - Damage Protection
 - ESD and EMI Protection
 - Design for Test
- Board Design
 - BOM Entry
 - Cable Design
 - Manufacturing Package

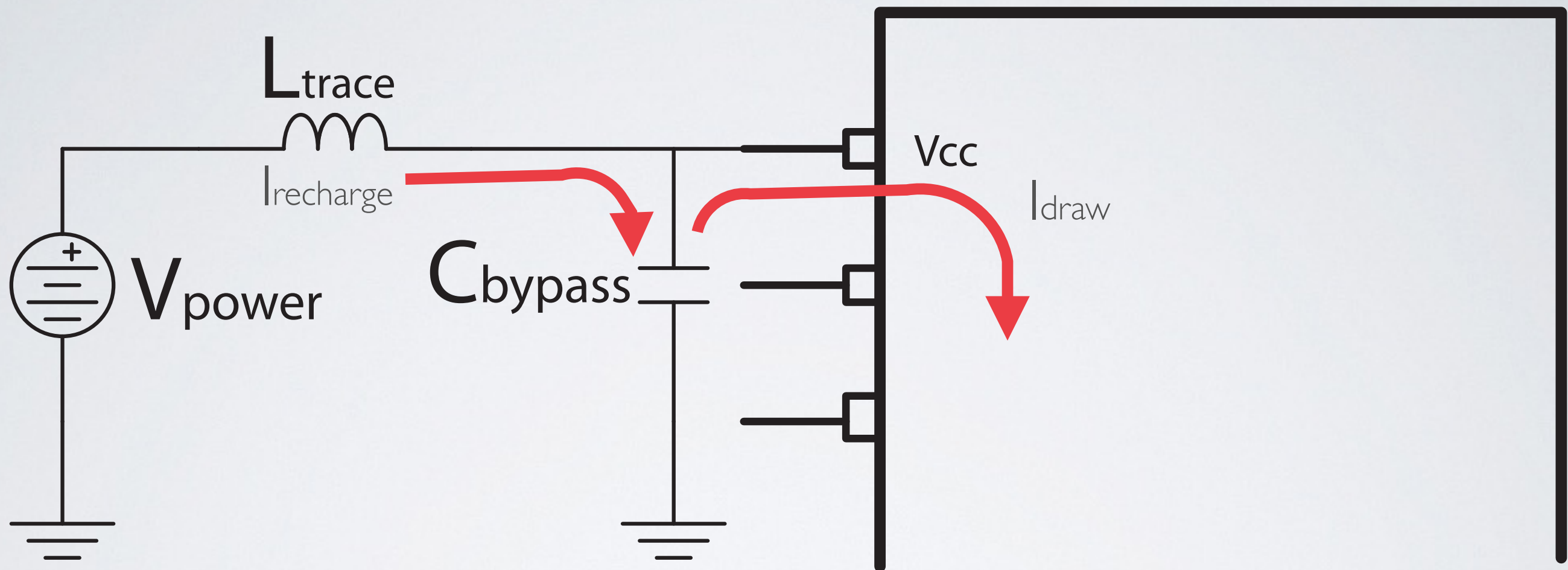
DETAILED DESIGN

BYPASSING



$$V_{\text{cc}} = V_{\text{power}} - V_{\text{drop}}$$

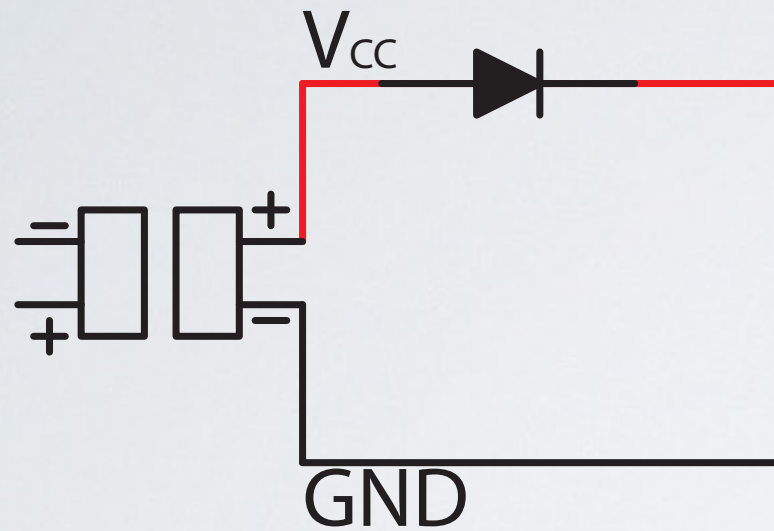
BYPASSING



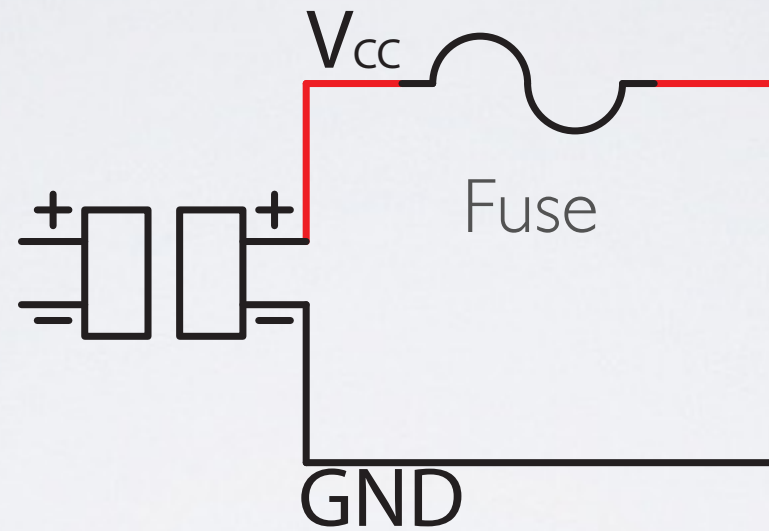
Place Bypass capacitor by each power pin

DAMAGE PROTECTION

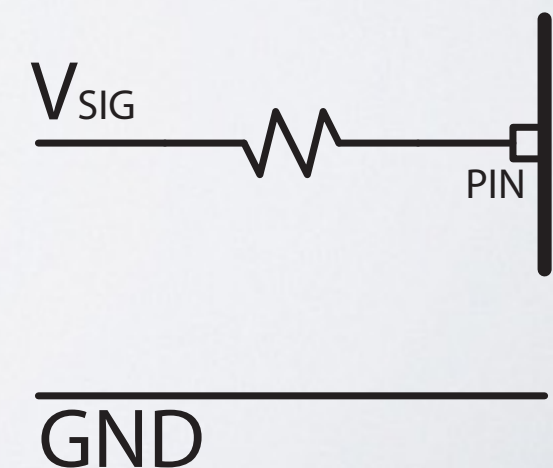
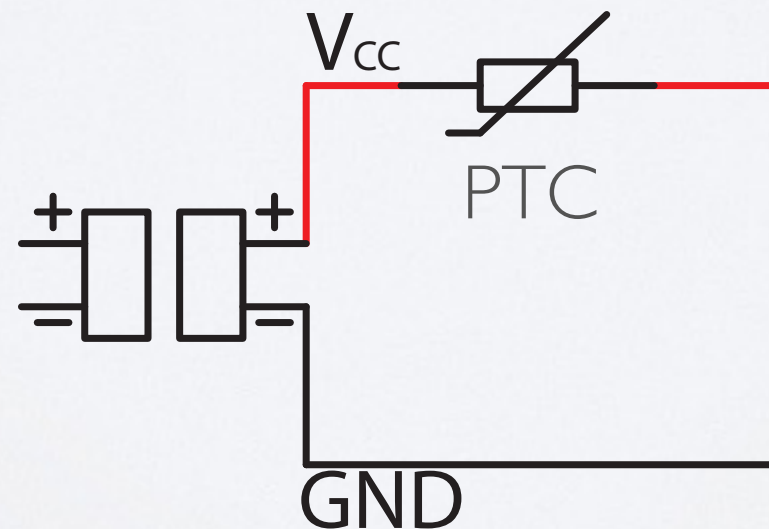
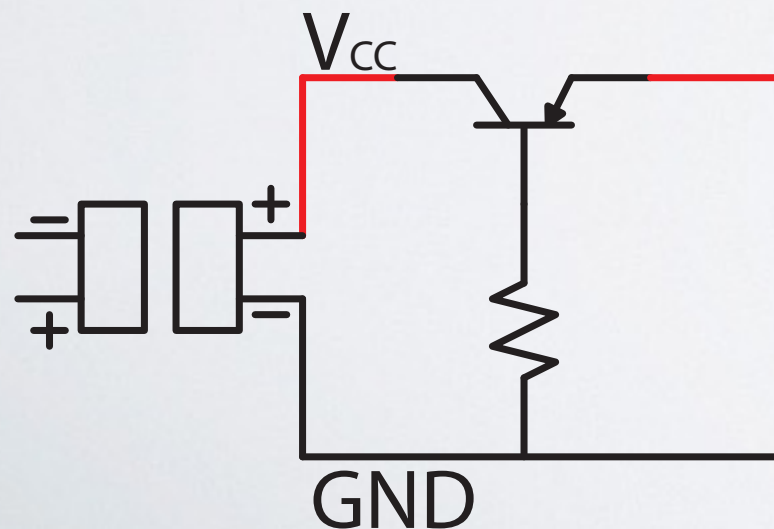
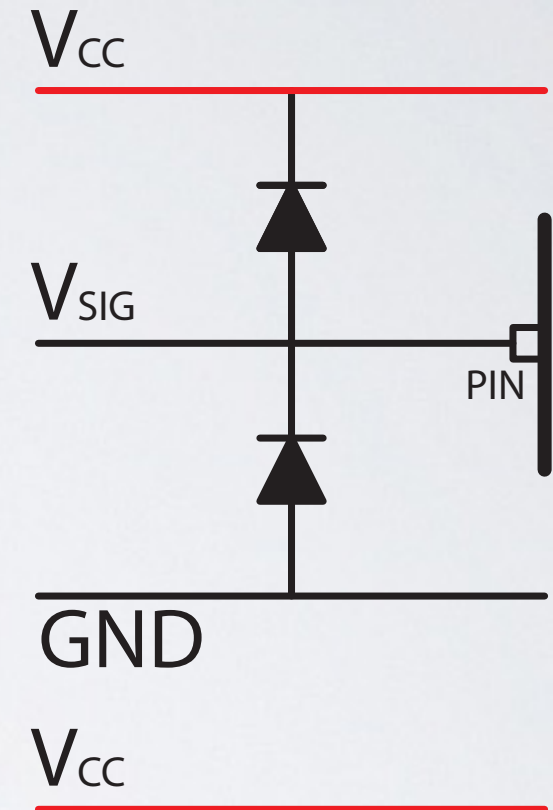
Reverse Polarity



Short Circuit

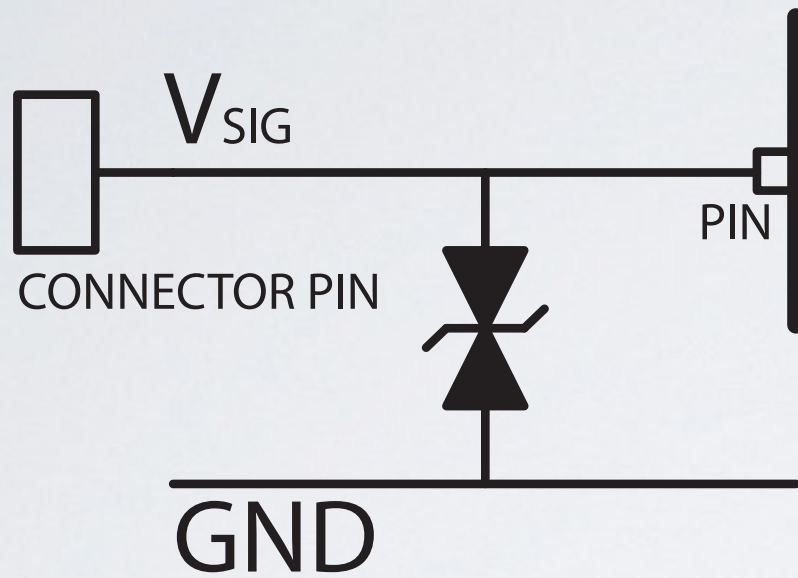


Over Voltage
Over Current

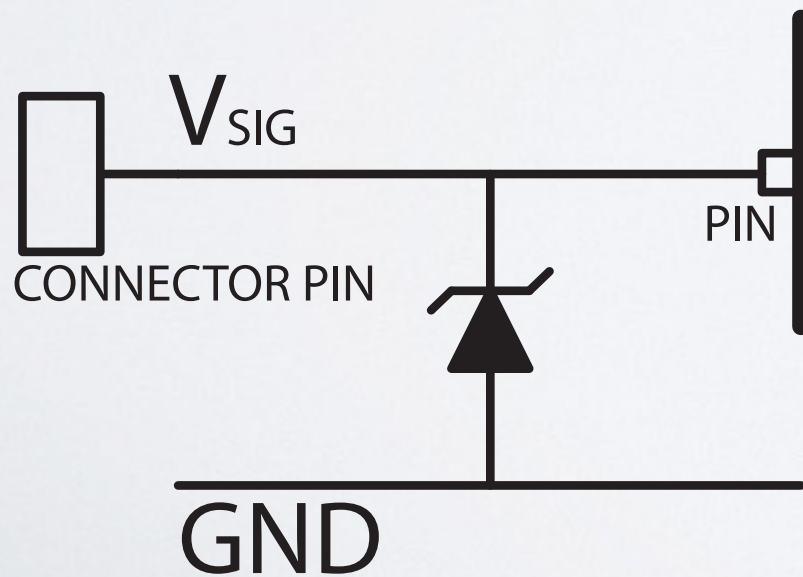


ESD Protection

V_{CC}

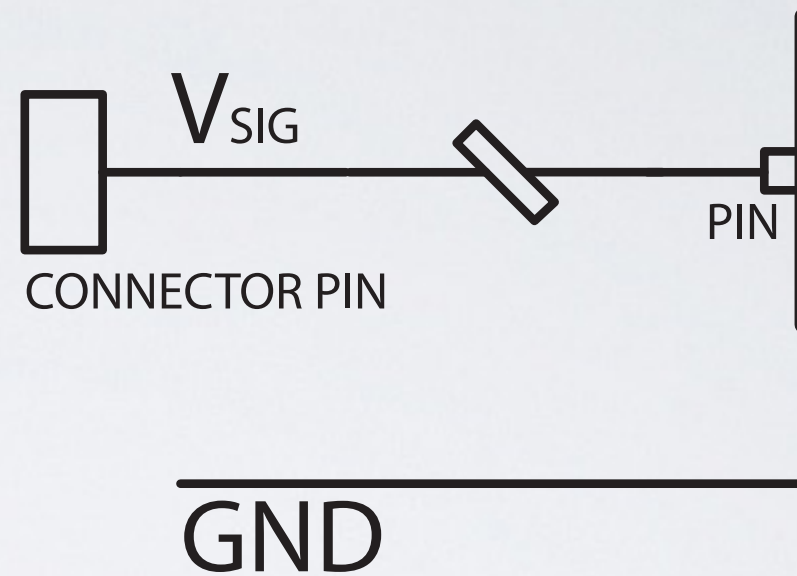


V_{CC}

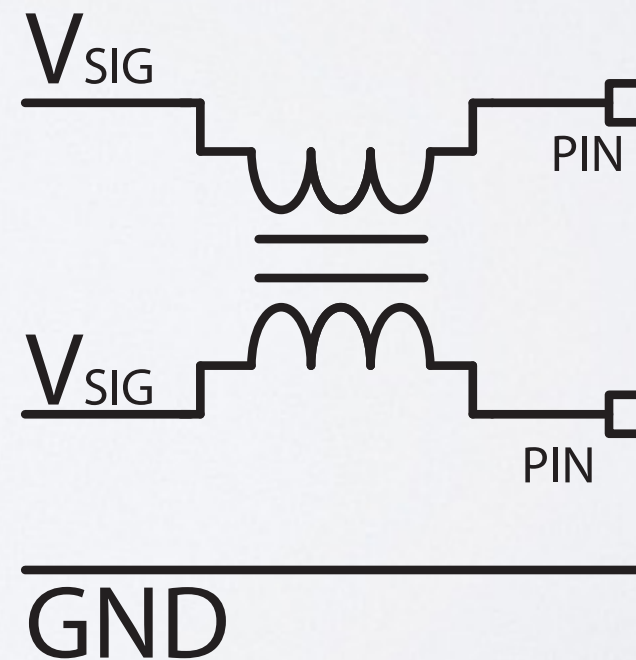


EMI Protection

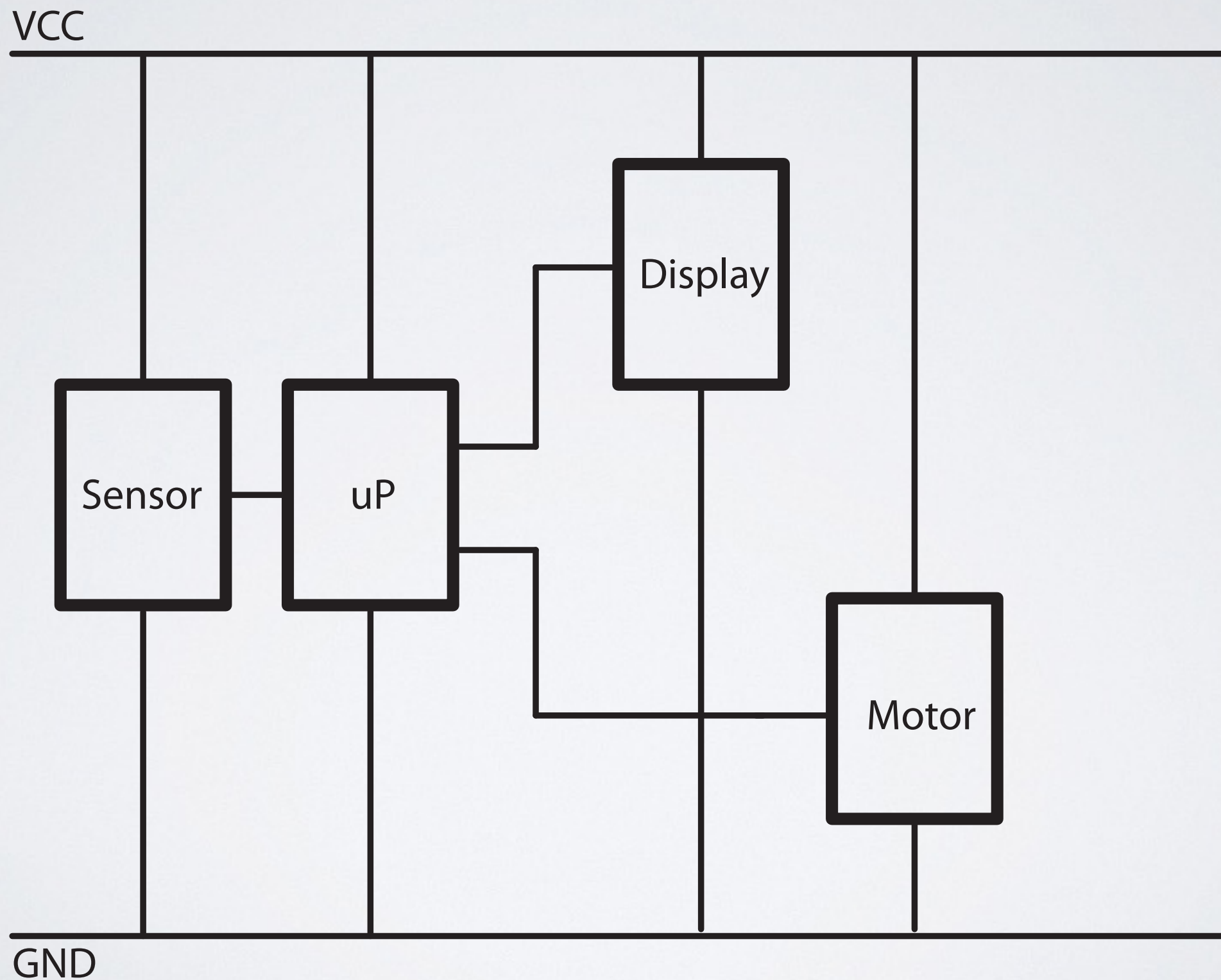
V_{CC}



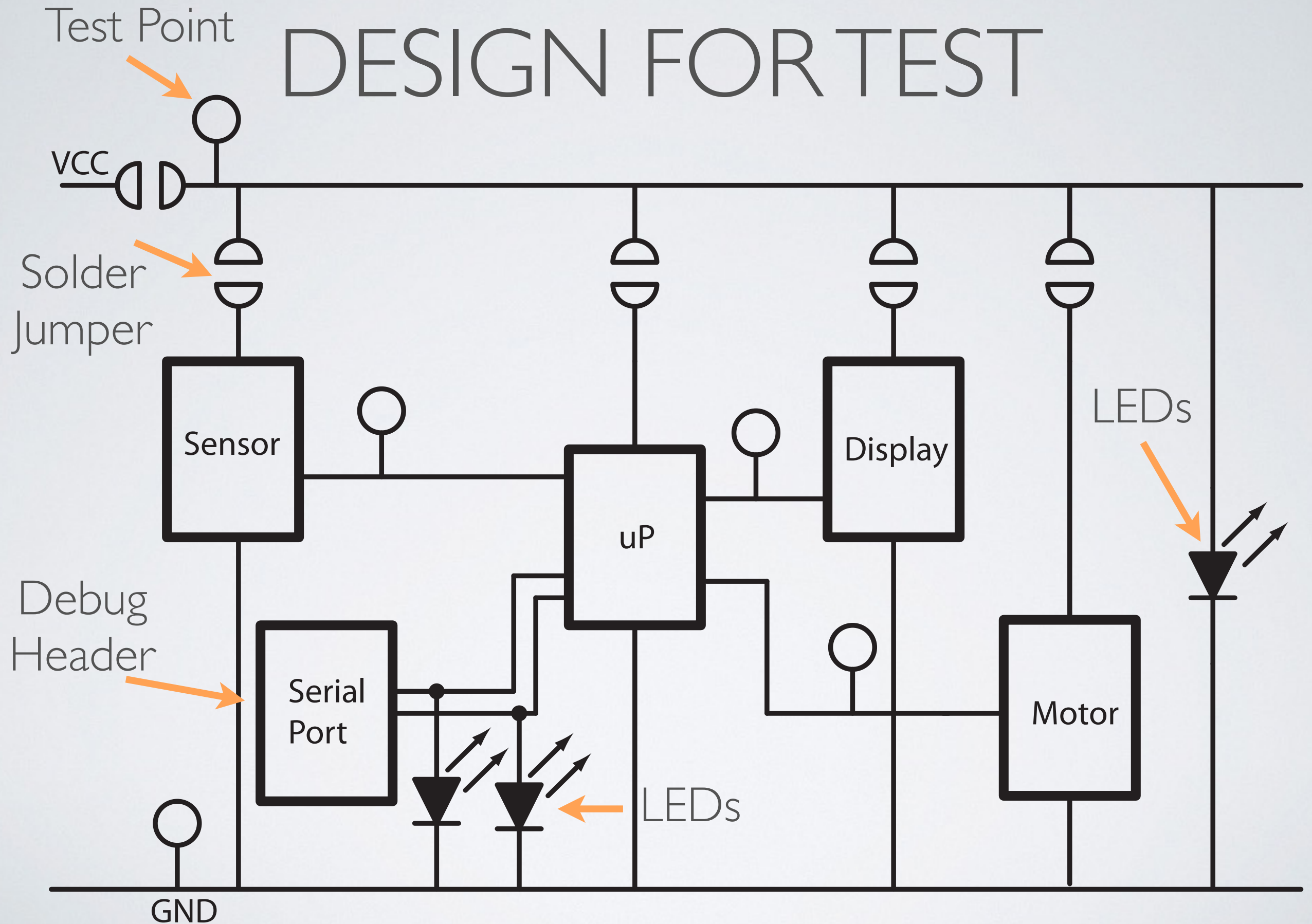
V_{CC}



DESIGN FOR TEST



DESIGN FOR TEST



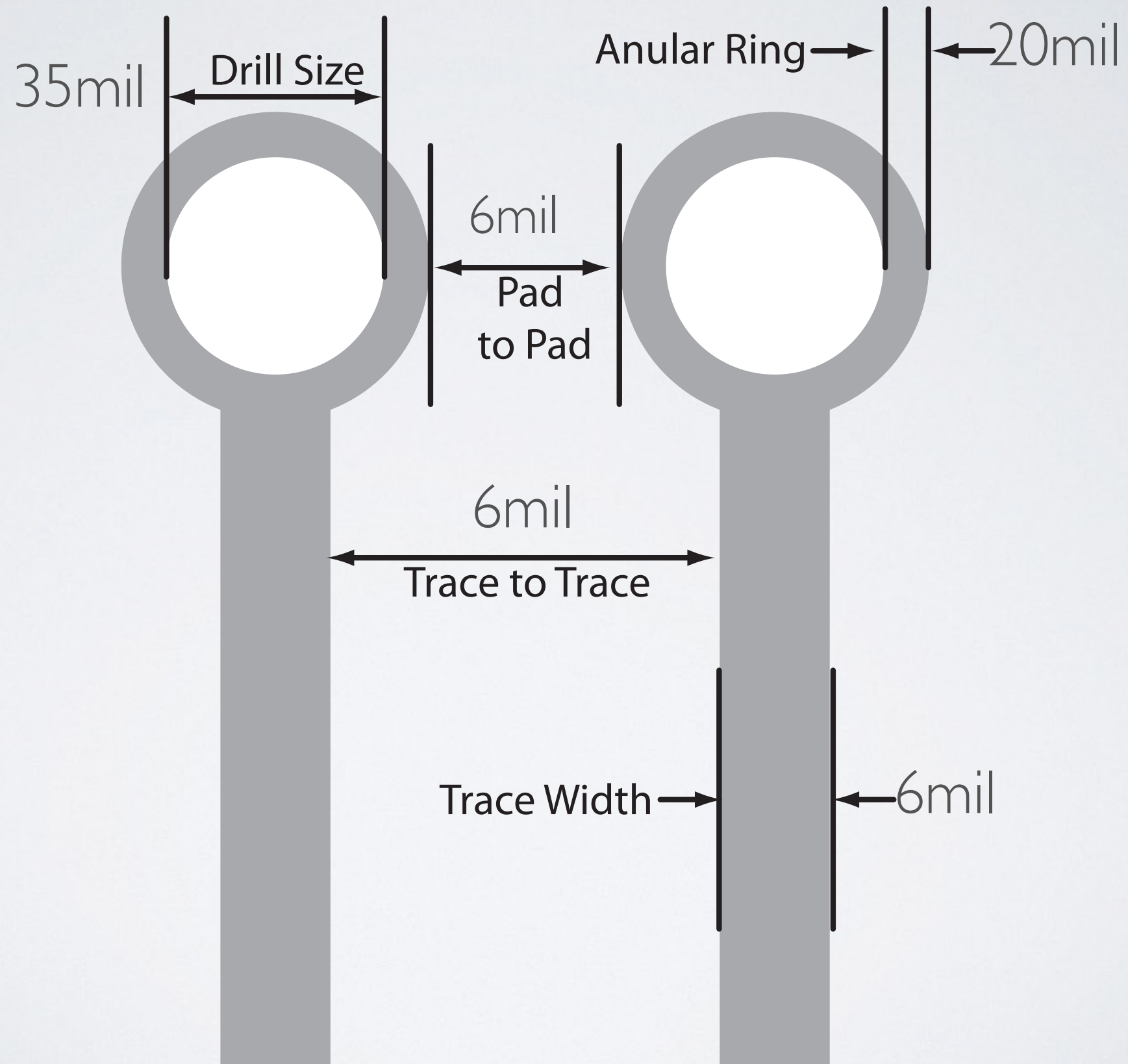
CONSTRAINTS

- Design Guidelines
- Manufacturing
- Physical
 - Thermal
 - Electromagnetic Interference

SCHEMATIC DESIGN GUIDELINES

LAYOUT DESIGN GUIDELINES

LAYOUT DESIGN RULES



DELIVERABLES

- PCB
 - Library
 - Schematic Capture
 - Layout
- Full BOM
- Cable Definition
- Manufacturing Package

DESIGN REVIEW

- Design File Release for Review
- Feedback
- Determination of Resolution
- Design File Update and Role Rev
- Design File Resolution Check
- Design File Release

PHASE TRANSITION

- Design Review completed
- Release of the Manufacturing Package