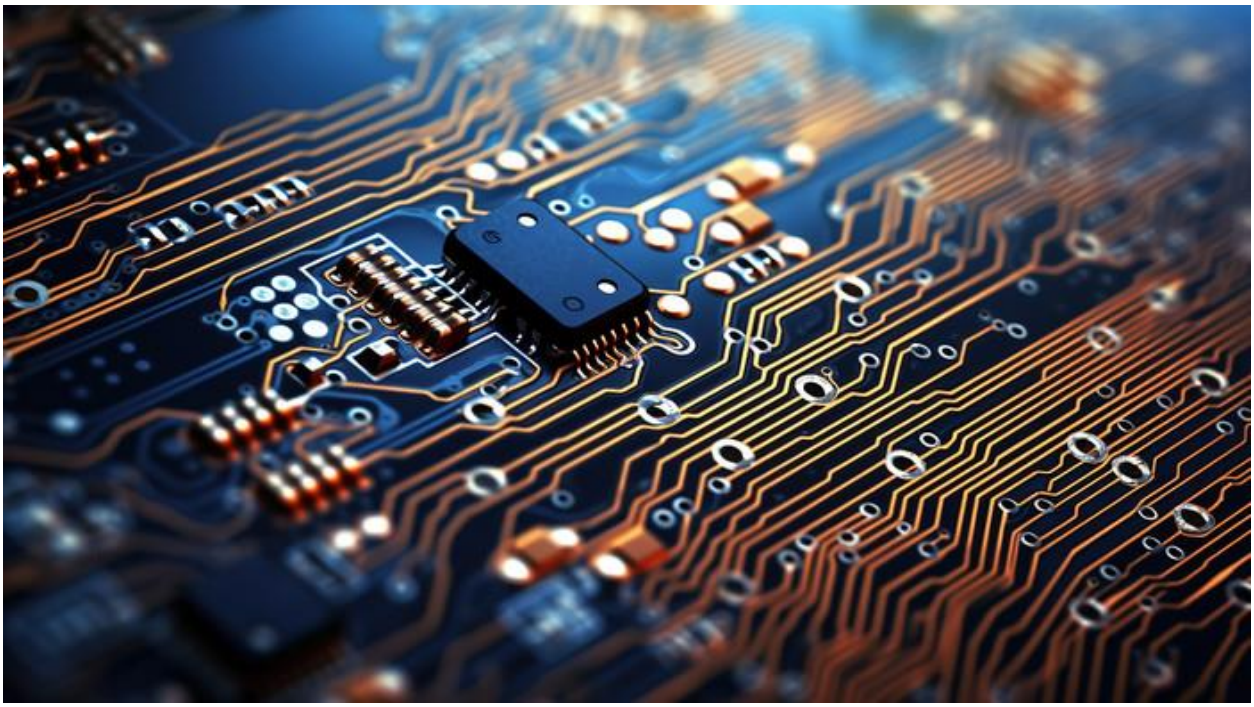

Design Project 2E03

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ENGPHYS 2E04

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Overview

Through this lab, we focused on utilizing the content learned from lab 7 and implemented it into the design project. We did this through the goal of trying to gain the output of my student number in binary code. This would be done through the power of flipflops, and various gates (minimum amount) to ensure the output is in the correct and in the right sequence. This would be done through a transition table including the current and next states, followed with a K map for each J and K input, which would be color coded. This would then result in the creation of a simulation to ensure the earlier steps were correct and final step before the physical circuit.

Analytical Solution

To solve for my values, I first created a state transition table with the current and following states.

Number	Q1	Q2	Q3	Q4	C5	Next_Q1	Next_Q2	Next_Q3	Next_Q4	Next_C6	J1	K1	J2	K2	J3	K3	J4	K4	C6 --> J6	C6 -->K6
4	0	1	0	0	**0**	0	0	0	0	**0**	0	X	X	1	0	X	0	X	0	X
0	0	0	0	0	**0**	0	0	0	0	**1**	0	X	0	X	0	X	0	X	1	X
0	0	0	0	0	**1**	0	1	0	1	0	0	X	1	X	0	X	1	X	X	1
5	0	1	0	1	0	0	0	0	1	**0**	0	X	X	1	0	X	X	0	0	X
1	0	0	0	1	**0**	1	0	0	1	0	1	X	0	X	0	X	X	0	0	X
9	1	0	0	1	0	0	0	1	0	0	X	1	0	X	1	X	X	1	0	X
2	0	0	1	0	0	0	1	1	0	0	0	X	1	X	X	0	0	X	0	X
6	0	1	1	0	0	0	1	1	1	**0**	0	X	X	0	X	0	1	X	0	X
7	0	1	1	1	**0**	0	1	0	0	**0**	0	X	X	0	X	1	X	1	0	X
	Q1	Q2	Q3	Q4	C5	Next_Q1	Next_Q2	Next_Q3	Next_Q4	Next_C6	J1	K1	J2	K2	J3	K3	J4	K4	C6 --> J6	C6 -->K6

Using this table, I was then able to create a new transition table and k maps which would be color coded per unique position to ensure it is easy to read.

Number	Q1	Q2	Q3	Q4	C5	Next_Q1	Next_Q2	Next_Q3	Next_Q4	Next_C6	J1	K1	J2	K2	J3	K3	J4	K4	C6 --> J6	C6 -->K6
4	0	1	0	0	**0**	0	0	0	0	**0**	0	X	X	1	0	X	0	X	0	X
0	0	0	0	0	**0**	0	0	0	0	**1**	0	X	0	X	0	X	0	X	1	X
0	0	0	0	0	**1**	0	1	0	1	0	0	X	1	X	0	X	1	X	X	1
5	0	1	0	1	0	0	0	0	1	**0**	0	X	X	1	0	X	X	0	0	X
1	0	0	0	1	**0**	1	0	0	1	0	1	X	0	X	0	X	X	0	0	X
9	1	0	0	1	0	0	0	1	0	0	X	1	0	X	1	X	X	1	0	X
2	0	0	1	0	0	0	1	1	0	0	0	X	1	X	X	0	0	X	0	X
6	0	1	1	0	0	0	1	1	1	**0**	0	X	X	0	X	0	1	X	0	X
7	0	1	1	1	**0**	0	1	0	0	**0**	0	X	X	0	X	1	X	1	0	X
	Q1	Q2	Q3	Q4	C5	Next_Q1	Next_Q2	Next_Q3	Next_Q4	Next_C6	J1	K1	J2	K2	J3	K3	J4	K4	C6 --> J6	C6 -->K6

J1		C5 = 0	C5 = 0	C5 = 0	C5 = 0
	Q1 Q2 / Q3 Q4	00	01	11	10
	00	0	1	X	0
	01	0	0	0	0
	11	X	X	X	X
	10	X	X	X	X
SOP SOL:					
J1 = !Q2Q4					

		C5 = 1	C5 = 1	C5 = 1	C5 = 1
	Q1 Q2 / Q3 Q4	00	01	11	10
	00	0	X	X	X
	01	X	X	X	X
	11	X	X	X	X
	10	X	X	X	X

K5		C5 = 0	C5 = 0	C5 = 0	C5 = 0
	Q1 Q2 / Q3 Q4	00	01	11	10
C6 = 0	00	X	X	X	X
C6 = 0	01	X	X	X	X
C6 = 0	11	X	X	X	X
C6 = 0	10	X	X	X	X
SOP SOL:					
K5 = 1					

		C5 = 1	C5 = 1	C5 = 1	C5 = 1
	Q1 Q2 / Q3 Q4	00	01	11	10
C6 = 0	00	1	X	X	X
C6 = 0	01	X	X	X	X
C6 = 0	11	X	X	X	X
C6 = 0	10	X	X	X	X

J5		C5 = 0	C5 = 0	C5 = 0	C5 = 0			C5 = 1	C5 = 1	C5 = 1	C5 = 1
Q1 Q2 / Q3 Q4		00	01	11	10	Q1 Q2 / Q3 Q4		00	01	11	10
C6 = 0	00	1	0	X	0	C6 = 0	00	X	X	X	X
C6 = 0	01	0	0	0	0	C6 = 0	01	X	X	X	X
C6 = 0	11	X	X	X	X	C6 = 0	11	X	X	X	X
C6 = 0	10	X	0	X	X	C6 = 0	10	X	X	X	X
SOP SOL:											
J5 = !Q2!Q3!Q4											

K4		C5 = 0	C5 = 0	C5 = 0	C5 = 0			C5 = 1	C5 = 1	C5 = 1	C5 = 1
Q1 Q2 / Q3 Q4		00	01	11	10	Q1 Q2 / Q3 Q4		00	01	11	10
C6 = 0	00	X	0	X	X	C6 = 0	00	X	X	X	X
C6 = 0	01	X	0	1	X	C6 = 0	01	X	X	X	X
C6 = 0	11	X	X	X	X	C6 = 0	11	X	X	X	X
C6 = 0	10	X	1	X	X	C6 = 0	10	X	X	X	X
SOP SOL:											
K4 = Q1 + Q3											

J4		C5 = 0	C5 = 0	C5 = 0	C5 = 0			C5 = 1	C5 = 1	C5 = 1	C5 = 1
Q1 Q2 / Q3 Q4		00	01	11	10	Q1 Q2 / Q3 Q4		00	01	11	10
C6 = 0	00	0	X	X	0	C6 = 0	00	1	X	X	X
C6 = 0	01	0	X	X	1	C6 = 0	01	X	X	X	X
C6 = 0	11	X	X	X	X	C6 = 0	11	X	X	X	X
C6 = 0	10	X	X	X	X	C6 = 0	10	X	X	X	X
SOP SOL:											
J4 = C5+Q3Q2											

K3		C5 = 0	C5 = 0	C5 = 0	C5 = 0			C5 = 1	C5 = 1	C5 = 1	C5 = 1
Q1 Q2 / Q3 Q4		00	01	11	10	Q1 Q2 / Q3 Q4		00	01	11	10
C6 = 0	00	X	X	X	0	C6 = 0	00	X	X	X	X
C6 = 0	01	X	X	1	0	C6 = 0	01	X	X	X	X
C6 = 0	11	X	X	X	X	C6 = 0	11	X	X	X	X
C6 = 0	10	X	X	X	X	C6 = 0	10	X	X	X	X
SOP SOL:											
K3 = Q4											

J3		C5 = 0	C5 = 0	C5 = 0	C5 = 0			C5 = 1	C5 = 1	C5 = 1	C5 = 1
Q1 Q2 / Q3 Q4		00	01	11	10	Q1 Q2 / Q3 Q4		00	01	11	10
C6 = 0	00	0	0	X	X	C6 = 0	00	0	X	X	X
C6 = 0	01	0	0	X	X	C6 = 0	01	X	X	X	X
C6 = 0	11	X	X	X	X	C6 = 0	11	X	X	X	X
C6 = 0	10	X	1	X	X	C6 = 0	10	X	X	X	X
SOP SOL:											
J3 = Q1											

K2		C5 = 0	C5 = 0	C5 = 0	C5 = 0			C5 = 1	C5 = 1	C5 = 1	C5 = 1
Q1 Q2 / Q3 Q4		00	01	11	10	Q1 Q2 / Q3 Q4		00	01	11	10
C6 = 0	00	X	X	X	X	C6 = 0	00	X	X	X	X
C6 = 0	01	1	1	0	0	C6 = 0	01	X	X	X	X
C6 = 0	11	X	X	X	X	C6 = 0	11	X	X	X	X
C6 = 0	10	X	X	X	X	C6 = 0	10	X	X	X	X
SOP SOL:											
K2 = !Q3											

J2		C5 = 0	C5 = 0	C5 = 0	C5 = 0		C5 = 1	C5 = 1	C5 = 1	C5 = 1
Q1 Q2 / Q3 Q4		00	01	11	10	Q1 Q2 / Q3 Q4	00	01	11	10
C6 = 0	00	0	0	X	1	C6 = 0	00	1	X	X	X
C6 = 0	01	X	X	X	X	C6 = 0	01	X	X	X	X
C6 = 0	11	X	X	X	X	C6 = 0	11	X	X	X	X
C6 = 0	10	X	0	X	X	C6 = 0	10	X	X	X	X
SOP SOL:										
J2 = C5+Q3										

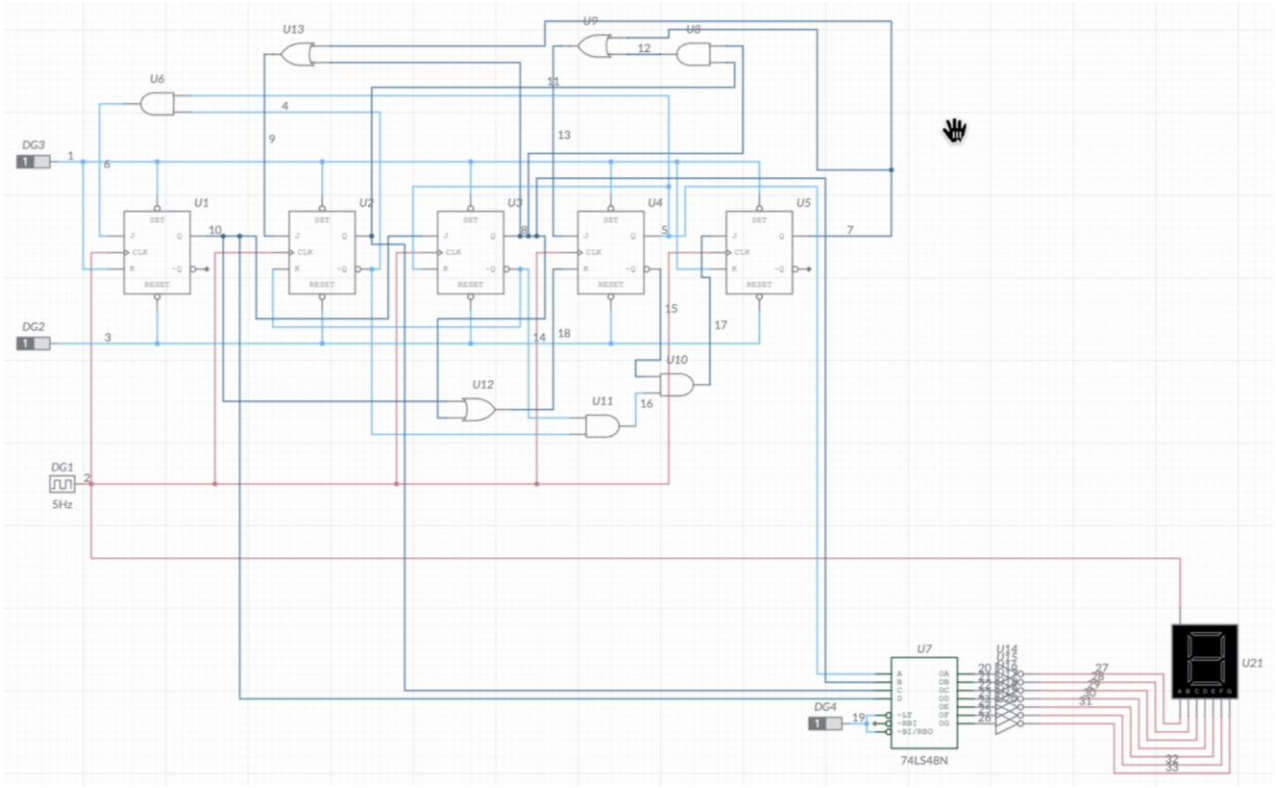
K1		C5 = 0	C5 = 0	C5 = 0	C5 = 0		C5 = 1	C5 = 1	C5 = 1	C5 = 1
Q1 Q2 / Q3 Q4		00	01	11	10	Q1 Q2 / Q3 Q4	00	01	11	10
C6 = 0	00	X	X	X	X	C6 = 0	00	X	X	X	X
C6 = 0	01	X	X	X	X	C6 = 0	01	X	X	X	X
C6 = 0	11	X	X	X	X	C6 = 0	11	X	X	X	X
C6 = 0	10	X	1	X	X	C6 = 0	10	X	X	X	X
SOP SOL:										
K1 = 1										

For the don't cares, they are denoted as X, and portions of the table are so for some reasons. The reasons include unused states, so for when the circuit doesn't reach any certain circuit combinations, which makes the final value a don't care. Thus it doesn't affect the circuits performance, hence creating it as a don’t care. This can later then help optimize k maps and simplification processes.

As for optimizations, I did both SOP and POS solutions for the k maps, and had noted SOP was more optimized for each K-map. I also ensured the blue rectangle was big as possible to ensure an extremely efficient circuit and general SOP solution. Another optimization is using only 5 flipflops as opposed to six, this is a result of realizing that one of the K values for the sixth flipflops having a full columns of For design choices, I looked at the gates, and the flipflops that connect more often than others, such as the pair Q3 and Q1, and the triple Q2 Q4 and Q5, would be on the same side in the circuit to ensure shorter wires and more readability within the physical circuit.

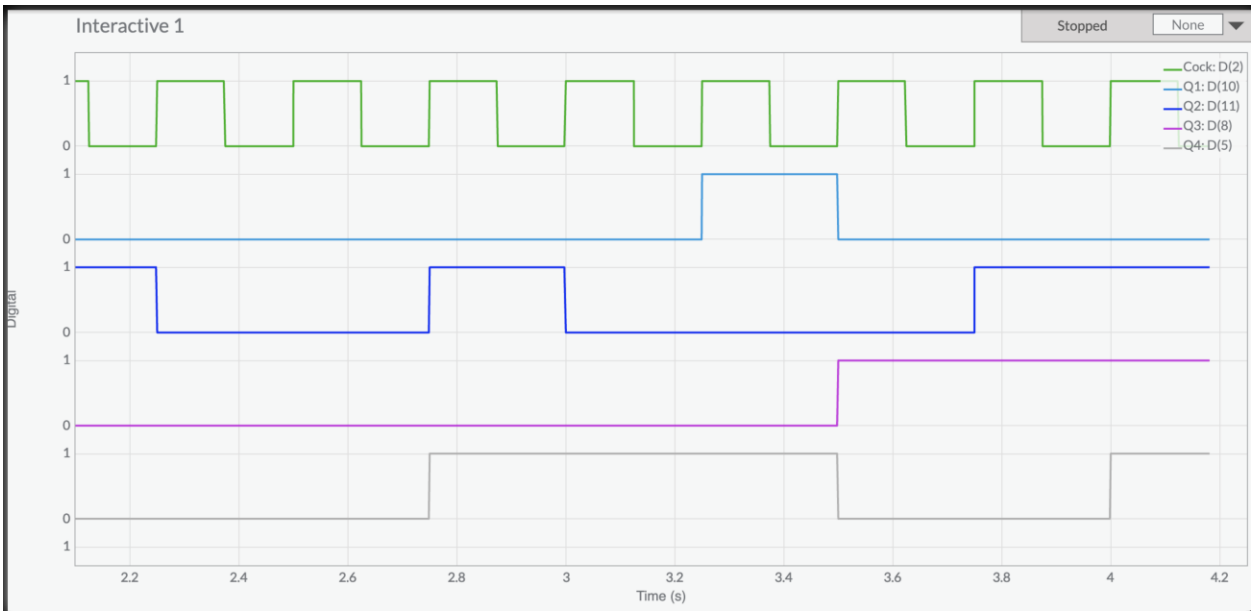
Multisim Solution

The Multisim solution was made using the analytical solution’s information and formed on the Multisim software. This was thoroughly tested and ensured all the output values matched the desired results.



I ended up using a total of 7 or gates, which one OR gate was changed in the physical circuit due to the k not physical implementation, but in total, 4 AND gates, and 3 OR gates. I used a decoder and due to mutism live not having the same decoder, I used a different one. This resulted in the expected outputs and confirmed my Kmaps and previous calculations s to be correct. The flipflops are ordered in acsending order, so Flipflop 1 at the far left and 5 at the far right. All. my binary numbers are set to 1, and clock is at 5Hz.

After building the circuit within Multisim, the results of the circuit happen to match our findings analytically. This can then further be checked through a timing diagram using the Multisim software and compare our results starting off with 4.



We can see through the timing diagram the Multisim go through 4(0100) to 0 twice(000), then 5(0101), to 1(0001), to 9(1001), then to 2(0010), then almost last 6(0110) and finally 7(0111), creating the timing diagram, and final output of 400519267.

Viewing the timing diagram mutism and seeing how it matches my results, I can conclude the results were as expected.

Conclusion

Methods

This circuit was solved for analytically, simulated, and physically, three methods that all resulted in similar values or the exact same for analytical and simulated. This close alignment of the different methods and the outputs matching ensures the experiment was done correctly with minimal errors and within reasonable uncertainty.

Final Thoughts

The lab was really valuable for learning about digital logic design, emphasizing efficient circuit implementation and validation across an analytical, simulated, and physical environment. We designed and tested the transition table, timing diagram, and circuit design. The behavior observed during physical implementation highlighted the challenges and need for precision in real-world applications. I found this to be extremely helpful as it really felt as an impactful project as we didn't have the circuit given to us, and we had to find the circuit in of itself to get our own unique student number!.