MICROPROCESSOR PROGRAMMING AND INTERFACING

OPEN-ENDED PROBLEM

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Question:

Design a Microprocessor based system in which: 1. Two EPROMs 2764 are to be interfaced for Address Space 1 and two RAMs 6116 are to be interfaced for Address Space 2. A single decoder 74139 is to be used. Draw the diagram (by using some application software) and mention binary address space (starting and final addresses) for individual EPROM and RAM devices.

Solution:

EPROMs used are of 27 series, their memory capacity is 64 Kilobytes

Converting 64 Kilobytes which is a byte word into bytes as follows:

64Kb/8Kb=8Kb =2^3. 2^{10} =2^{13} (13 address lines from A0-A12 directly connected to 8088)

Selection pins for decoder A13, A14

Enable pins for decoder are from A15-A19

➢ Address Space 1:

Starting Address – PPPP PP00 0000 0000 0000

Final Address – PPPP PP11 1111 1111 1111

Calculation of PPPP PP:

ROLL # =062 = 3E (hex) =0011 1110b
Binary in reverse order= 0111 1100
Discard 2 least significant bits= 0111 11
PPPP PP= 0111 11

Starting Address – 0111 1100 0000 0000 0000 (7C000 h)

Final Address – 0111 1111 1111 1111 1111 (7FFFF h)

➢ Table for the two 2764 EPROMs:

Enable /fixed | select | Direct address

		A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
EPROM 1	INITIAL ADDRESS	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	FINAL ADRESSD	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
EPROM 2	INITIAL ADDRESS	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	FINAL ADDRESS	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

EPROM 1	EPROM 2
Starting address= 7C000h Final address =7DFFFh	Starting address= 7EFFFh Final address=7FFFFh

RAMs are 6116, which means 61 is name of series, and 16 is memory capacity.

Converting 16 KB into bits as follows:

16 KB/8 KB= 2 =2^1. 2^{10} =2^{11} (11 address lines from A0-A10 directly connected to 8088)

Selection pins for decoder A11, A12

Enable pins for decoder are from A13-A19

➢ Address Space 2:

Starting Address – RRRR RRRR 0000 0000 0000

Final Address – RRRR RRRR 1111 1111 1111

Calculation of RRRR RRRR:

ROLL # =062 = 3E (hex) =0011 1110*

RRRR RRRR= 0011 1110

Starting Address –0011 1110 0000 0000 0000 (3E000h)

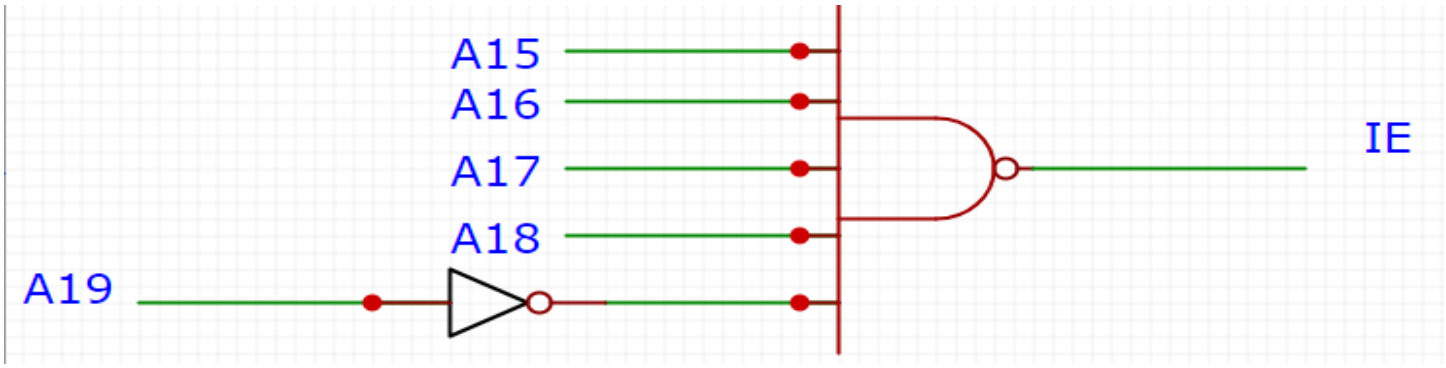
Final Address –0011 1110 1111 1111 1111 (3EFFFh)

➢ Table for the two 6116 RAMs:

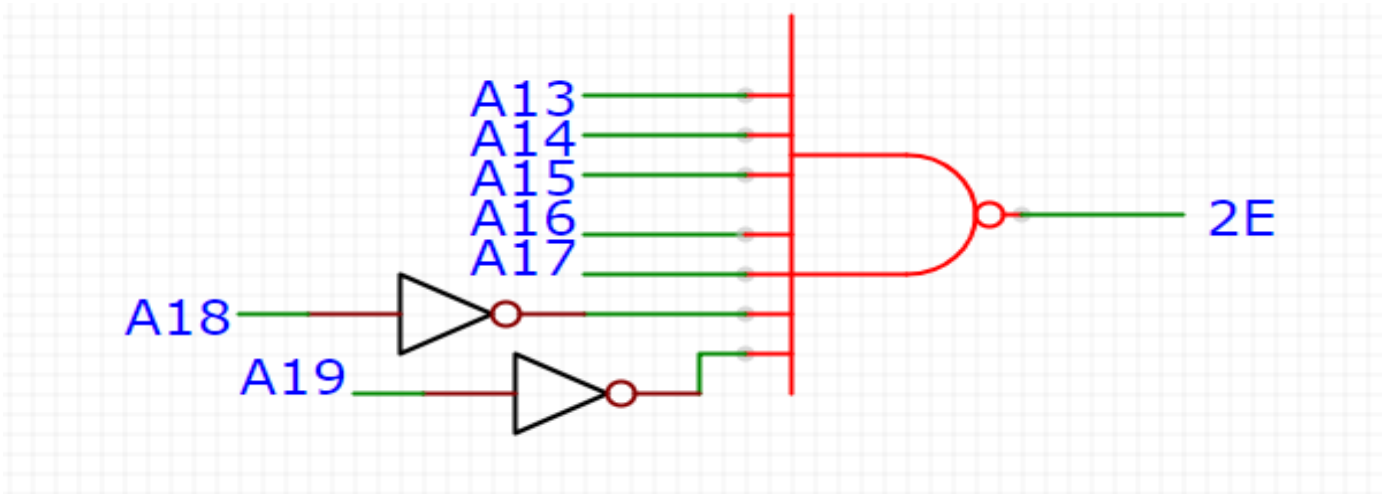
		Enable /fixed							select		Direct address										
		A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
RAM 1	INITIAL ADDRESS	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	FINAL ADRESSD	0	0	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1
RAM 2	INITIAL ADDRESS	0	0	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0
	FINAL ADDRESS	0	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1

RAM 1	RAM 2
Starting address= 3E000h Final address =3E7FFh	Starting address= 3E800h Final address=3EFFFh

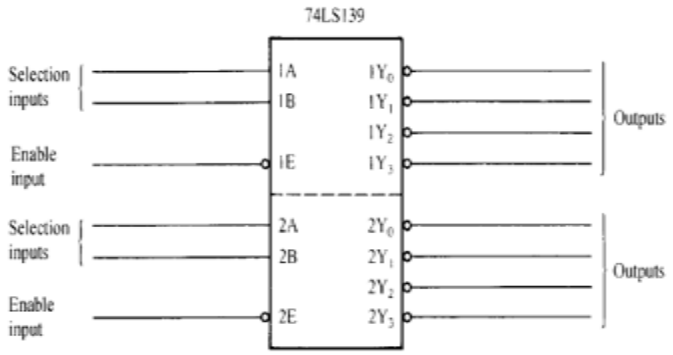
➢ First Enable pin of 74139



➢ Second Enable pin of 74139



➢ Output for 74139



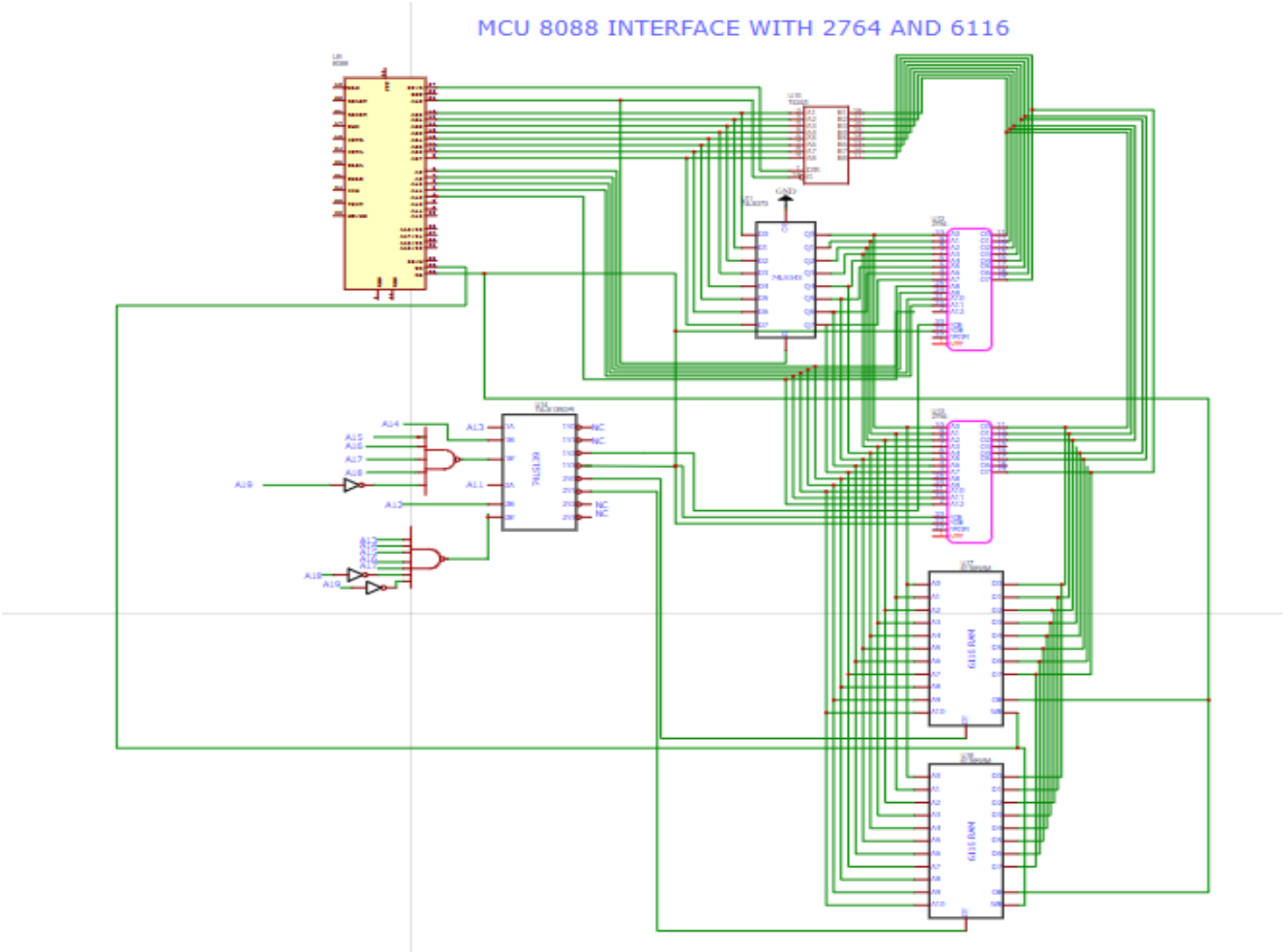
	Inputs		Outputs			
$\overline{E}$	A	B	$\overline{Y_0}$	$\overline{Y_1}$	$\overline{Y_2}$	$\overline{Y_3}$
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0
1	X	X	1	1	1	1

output of Address Space 1

As the selection pins are 10 and 11 so 2764 EPROM will be connected to 1Ȳ2 and Ȳ3 respectively.

output of Address Space 1

As the selection pins are 00 and 01 so 6616 RAM will be connected to 2 Ȳo and 2 Ȳ1 respectively



Question:

Two 8255 PPI and two 8254 PIT/C are to be interfaced for Address Space 3. A single decoder 74138 is to be used. Draw the diagram (by using some application software) and mention binary address space (starting and final addresses) for individual 8255and 8254 devices.

Solution:

➢ Address Space 3: (for both 8255 and 8244)

Starting Address – AAAA 0000

Final Address – AAAA 11111

Roll # =062 =76o = 1111 10

Reverse order of binary = 0111 11

Discard 2 least significant bits= 0111

AAAA= 0111

Starting Address – 0111 0000 (70h)

Final Address – 0111 1111 (7Fh)

➢ Table for the two 8255 PPI:

FIXED

		A7	A6	A5	A4	A3	A2	A1	A0
8255 1	INITIAL ADDRESS	0	1	1	1	0	0	0	0
	FINAL ADRESSD	0	1	1	1	0	0	1	1
8255 2	INITIAL ADDRESS	0	1	1	1	0	1	0	0
	FINAL ADDRESS	0	1	1	1	0	1	1	1

8255 1 Starting address= 70h Final address =73h	8255 2 Starting address= 74h Final address=77h

A0 — A1 Is used to select the port modes for each 8255

➢ Table for the two 8254 PIT/C:

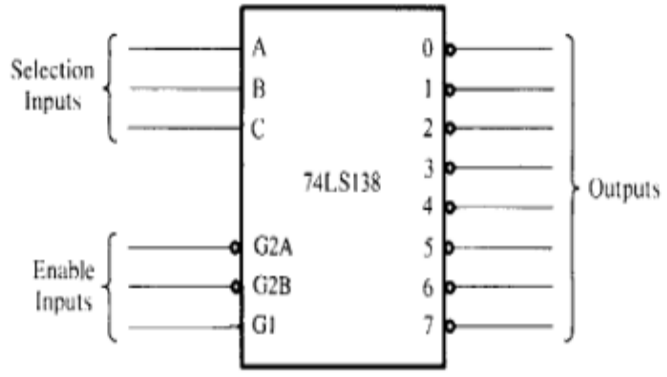
fixed — selection of Counter/timer

		A7	A6	A5	A4	A3	A2	A1	A0
8254 1	INITIAL ADDRESS	0	1	1	1	1	0	0	0
	FINAL ADRESSD	0	1	1	1	1	0	1	1
8254 2	INITIAL ADDRESS	0	1	1	1	1	1	0	0
	FINAL ADDRESS	0	1	1	1	1	1	1	1

8254 1	8254 2
Starting address= 78h Final address =7Bh	Starting address= 7Ch Final address=7Fh

A0 — A1 Is used to select the counter/timer for each 8254.

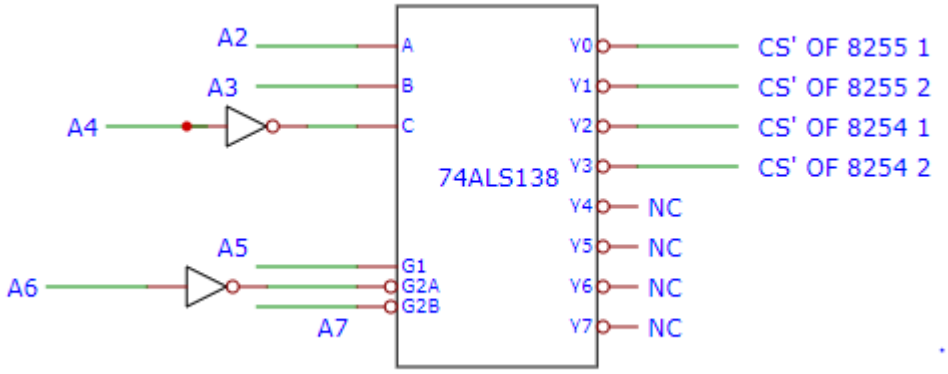
➢ Output for 74138

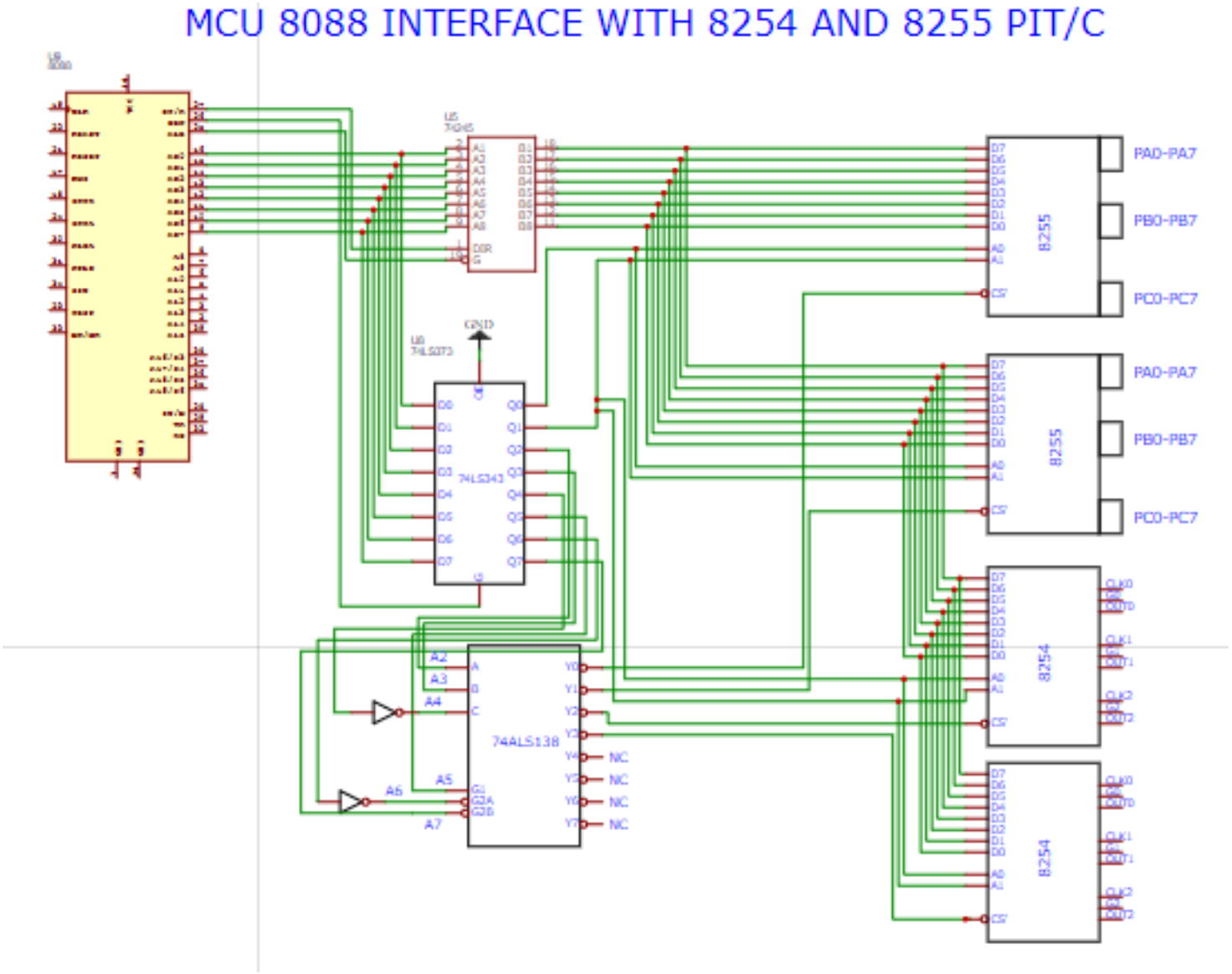


Inputs						Outputs							
Enable			Select										
$\overline{G2A}$	$\overline{G2B}$	G1	C	B	A	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$
1	X	X	X	X	X	1	1	1	1	1	1	1	1
X	1	X	X	X	X	1	1	1	1	1	1	1	1
X	X	0	X	X	X	1	1	1	1	1	1	1	1
0	0	1	0	0	0	0	1	1	1	1	1	1	1
0	0	1	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	0	1	1	0	1	1	1	1	1
0	0	1	0	1	1	1	1	1	0	1	1	1	1
0	0	1	1	0	0	1	1	1	1	0	1	1	1
0	0	1	1	0	1	1	1	1	1	1	0	1	1
0	0	1	1	1	0	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1	1	1	1	0

- A4 is inverted then selections bits become 000,001,010,011 so output will be at $\bar{Y}o$, $\bar{Y}1$, $\bar{Y}2$, $\bar{Y}3$ respectively.

- To enable decoder 138 G1=1, $\overline{G}2A=0$ and $\overline{G}2B=0$





As A0-A7 is multiplexed so first we have to demultiplexed it using **74245** and **74LS373** for separate data and address pin respectively.