DEPARTMENT OF ELECTRONIC ENGINEERING

N.E.D. UNIVERSITY OF ENGINEERING AND TECHNOLOGY

VLSI SYSTEM DESIGN(EL-408)

BATCH 2017-18

LAB SESSION # 12 TO 14

INSTUCTOR NAME: MISS SABA FAKHAR

CLASS: B.E

SECTION: C **GROUP**

MEMBERS:

1. **MUNTAHA SHAMS** (EL-17062)
Cloud id: shams4002093@cloud.neduet.edu.pk

2. **FARYAL ZEHRA** (EL-17065)
Cloud id: zehra4007201@cloud.neduet.edu.pk

3. **WARDAH ARSHAD** (EL-17069)
Cloud id: arshad4004588@cloud.neduet.edu.pk

4. **ZEENAT SHAIKH** (EL-17074)
Cloud id: Shaikh4003776@cloud.neduet.edu.pk

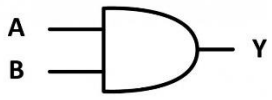
5. **AREEJ ASAD** (EL-17089)
Cloud id: asad4008253@cloud.neduet.edu.pk

LAB 12

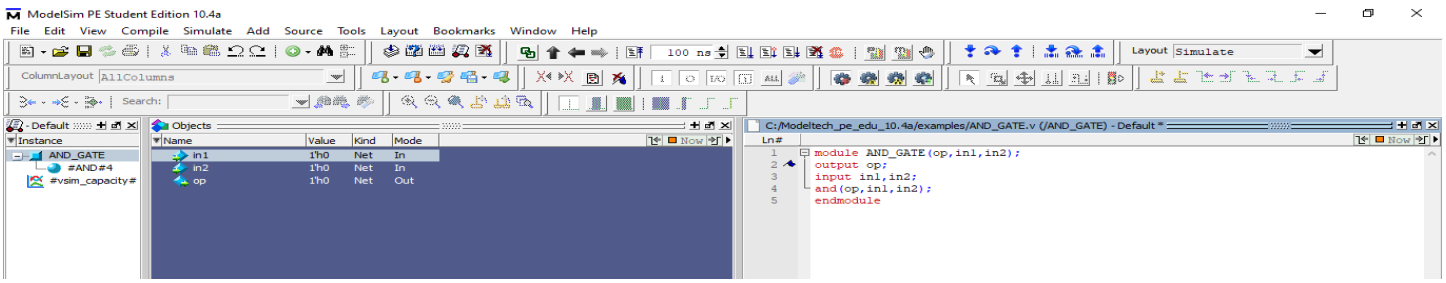
a) Design the modules using all basic gates: AND, OR, XOR, NOR, NAND and XNOR gate and verify the results

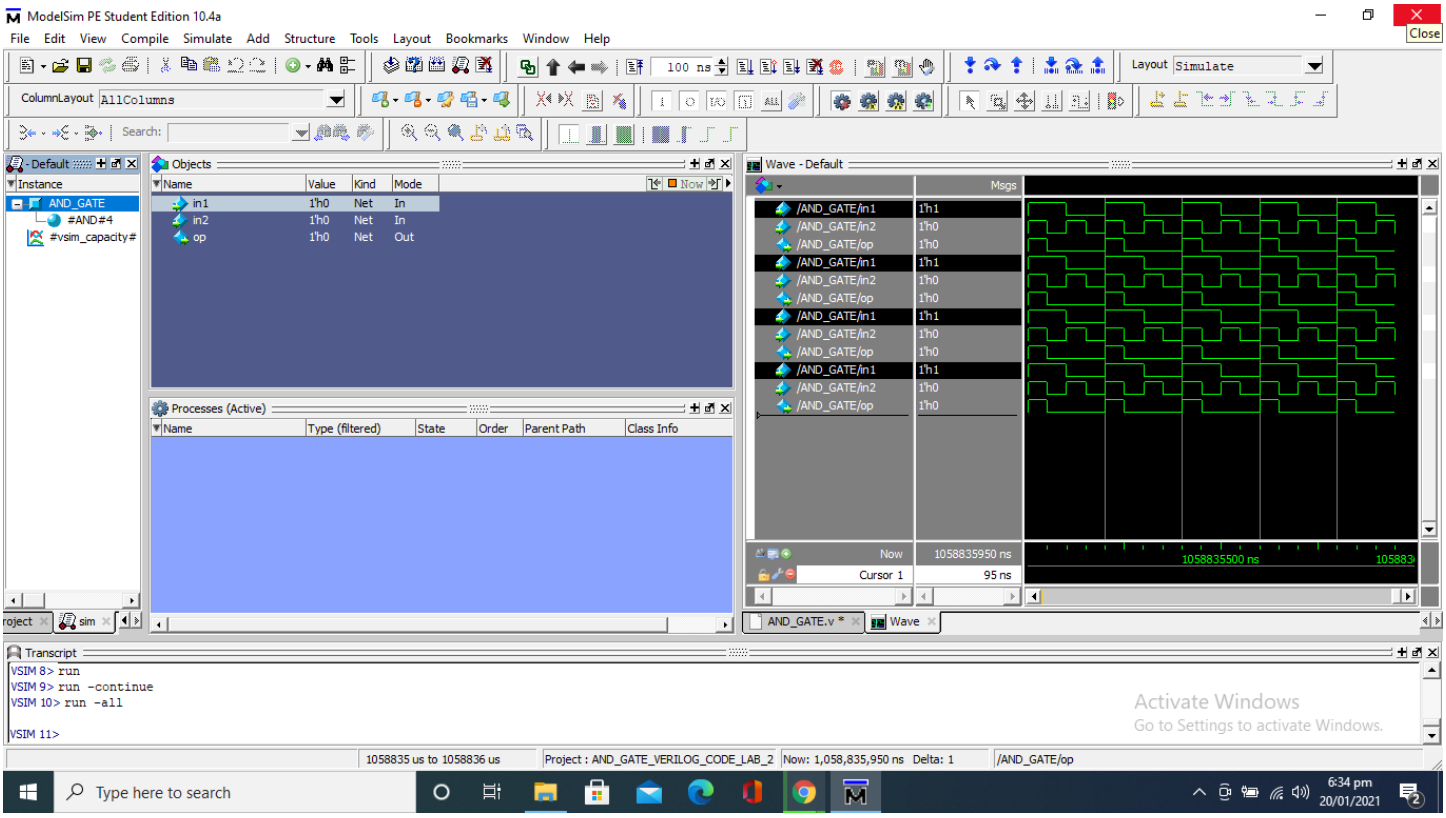
AND GATE

Inputs		Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1



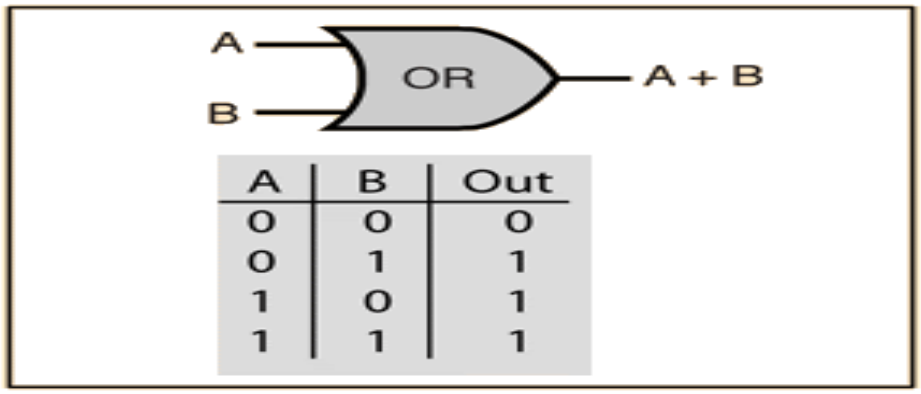
Y = A.B



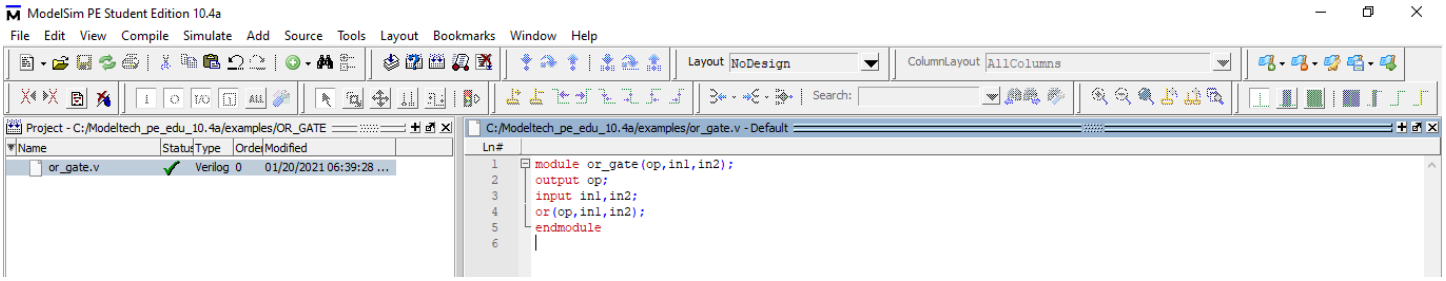


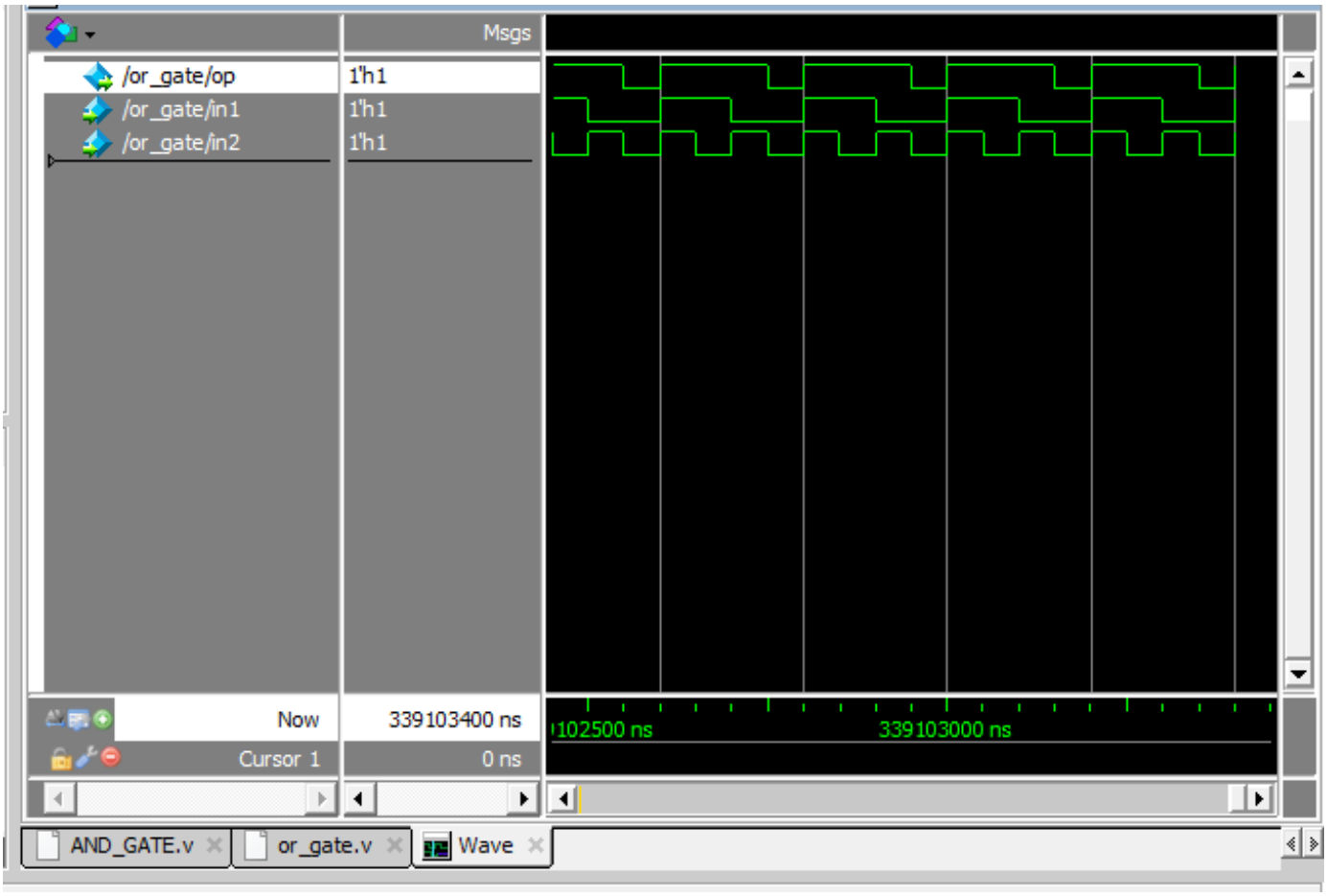
The output waveform is only high when both the inputs I.e., in1 and in2 are high

OR-GATE



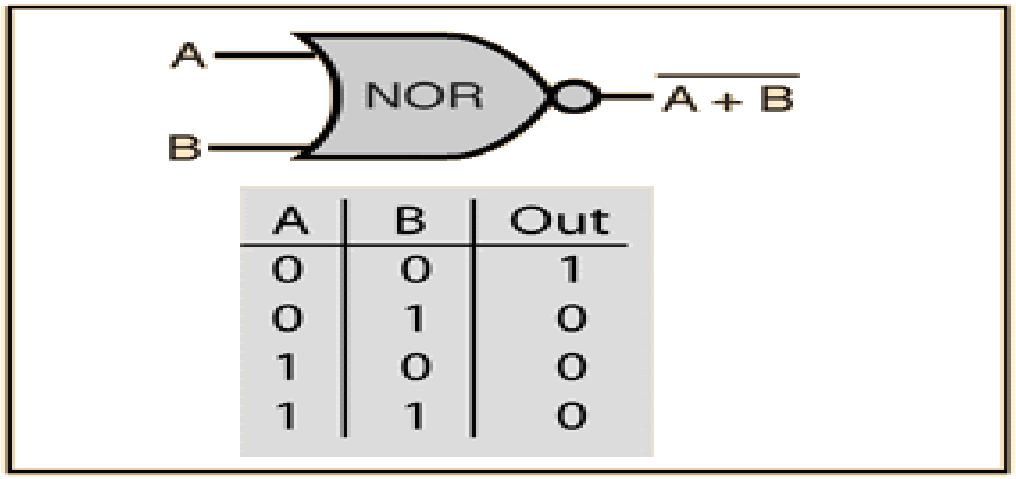
A	B	Out
0	0	0
0	1	1
1	0	1
1	1	1



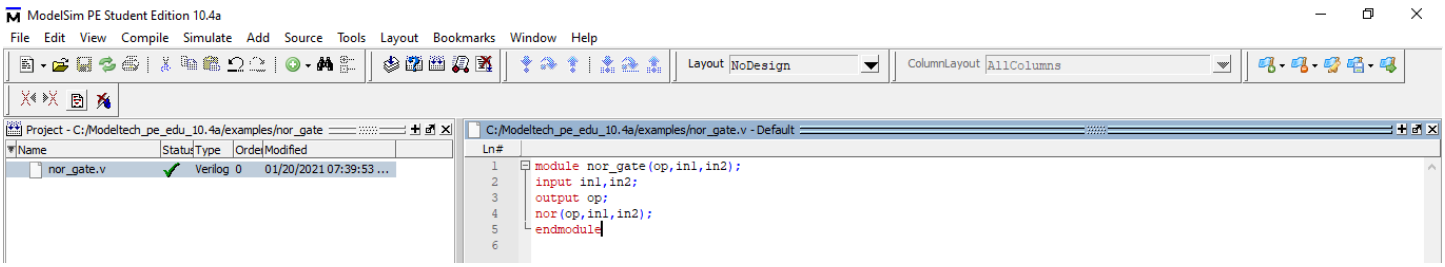


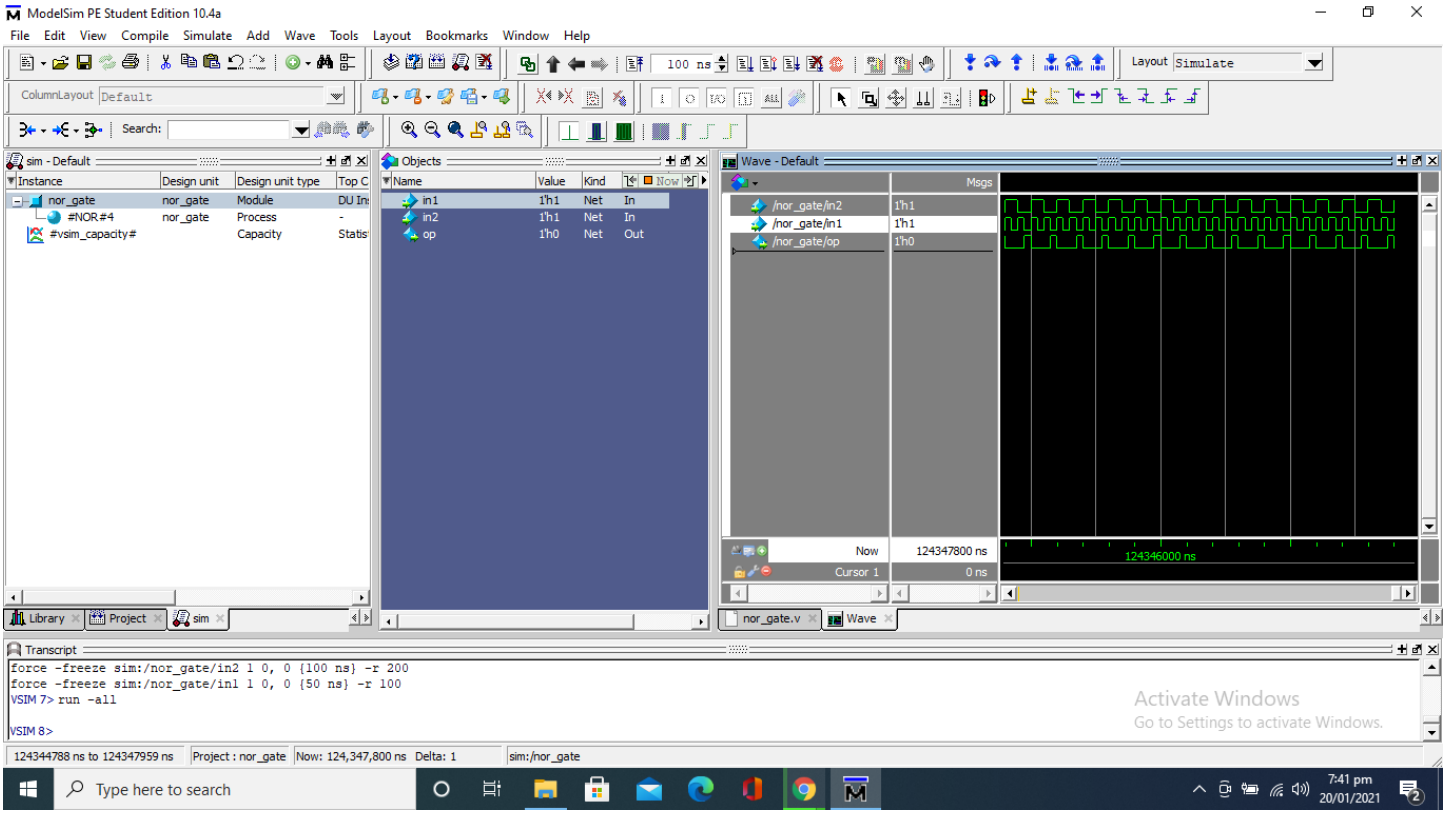
The output waveform is high elsewhere except it is only low when both the inputs I.e., in1 and in2 are low.

NOR-GATE



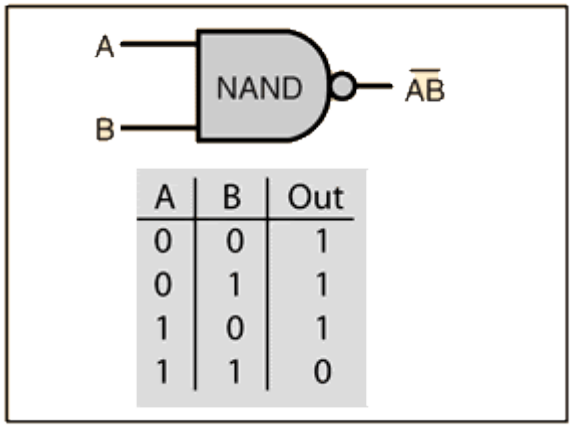
A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0



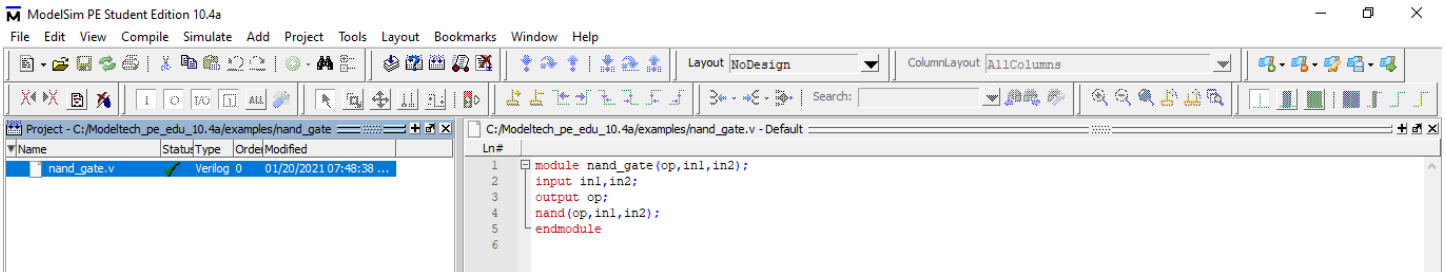


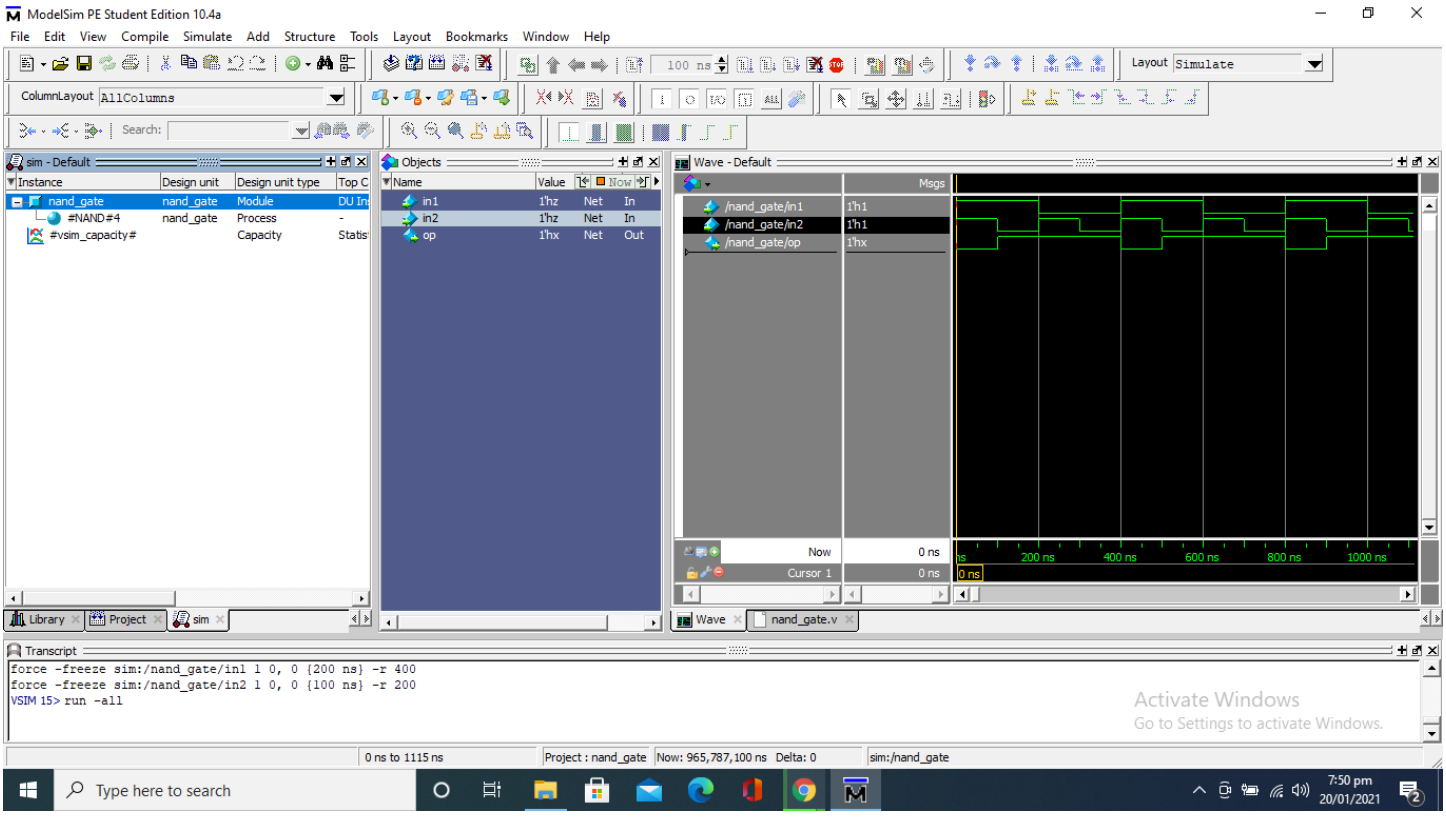
The output waveform is low elsewhere except it is only high when both the inputs I.e., in1 and in2 are low.

NAND-GATE



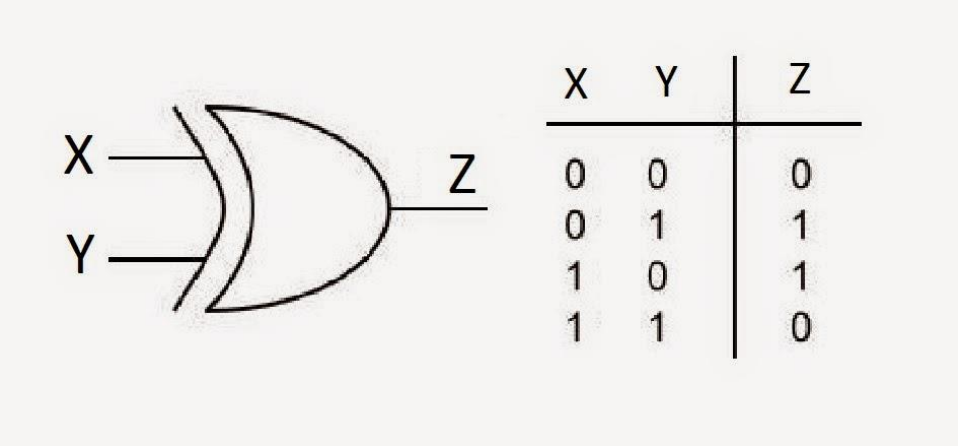
A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0



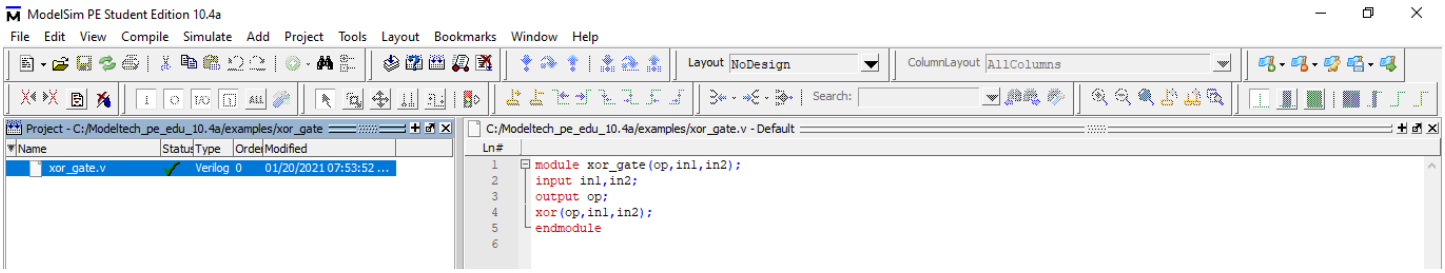


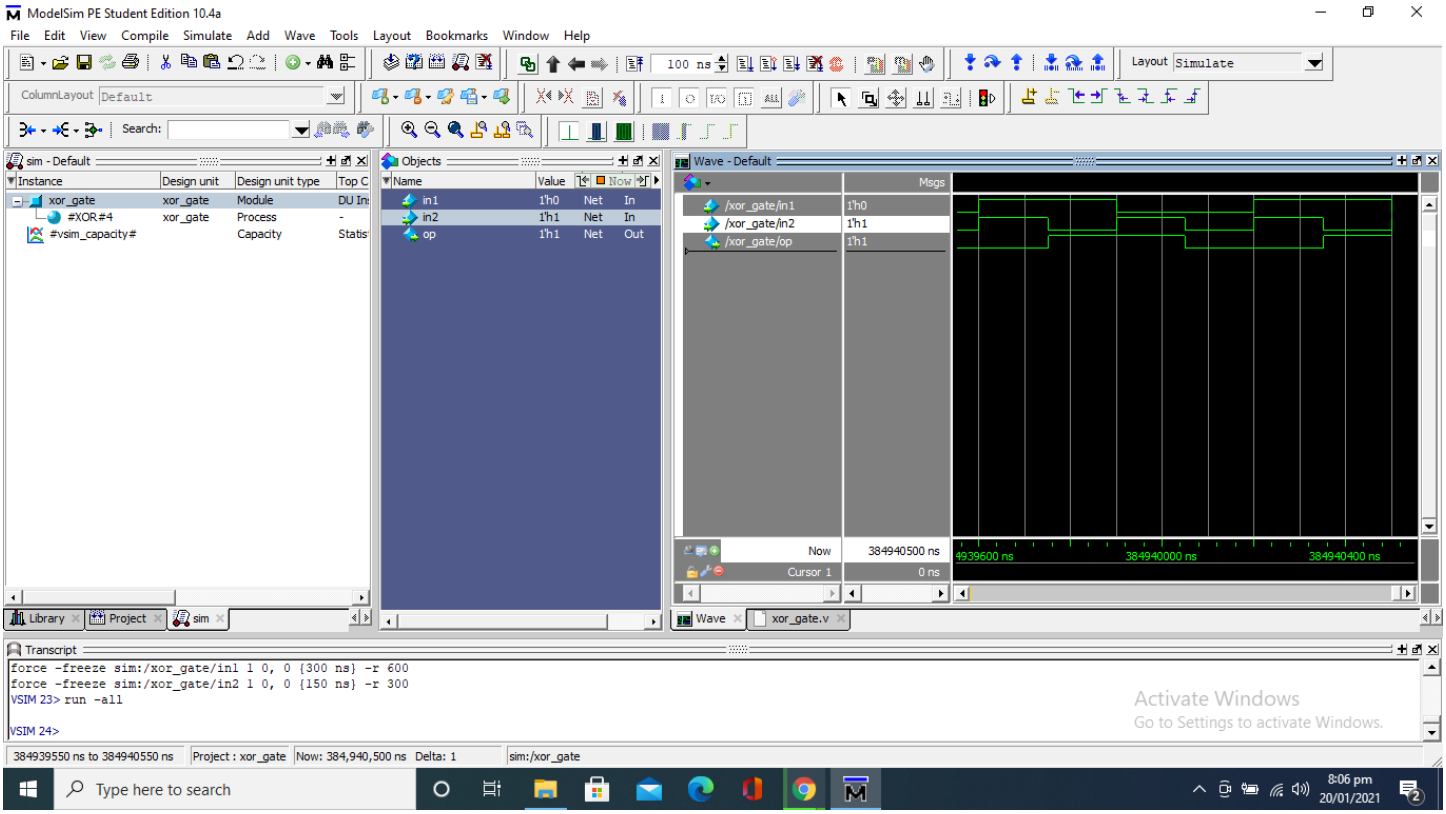
The output waveform is high elsewhere except it is only low when both the inputs I.e., in1 and in2 are high.

XOR-GATE



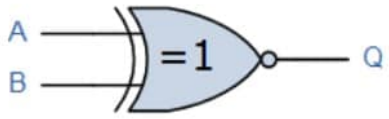
X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	0

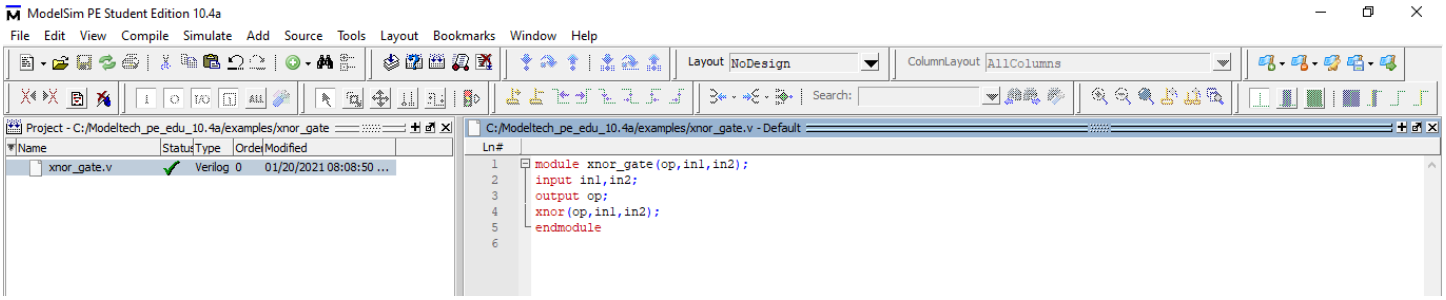


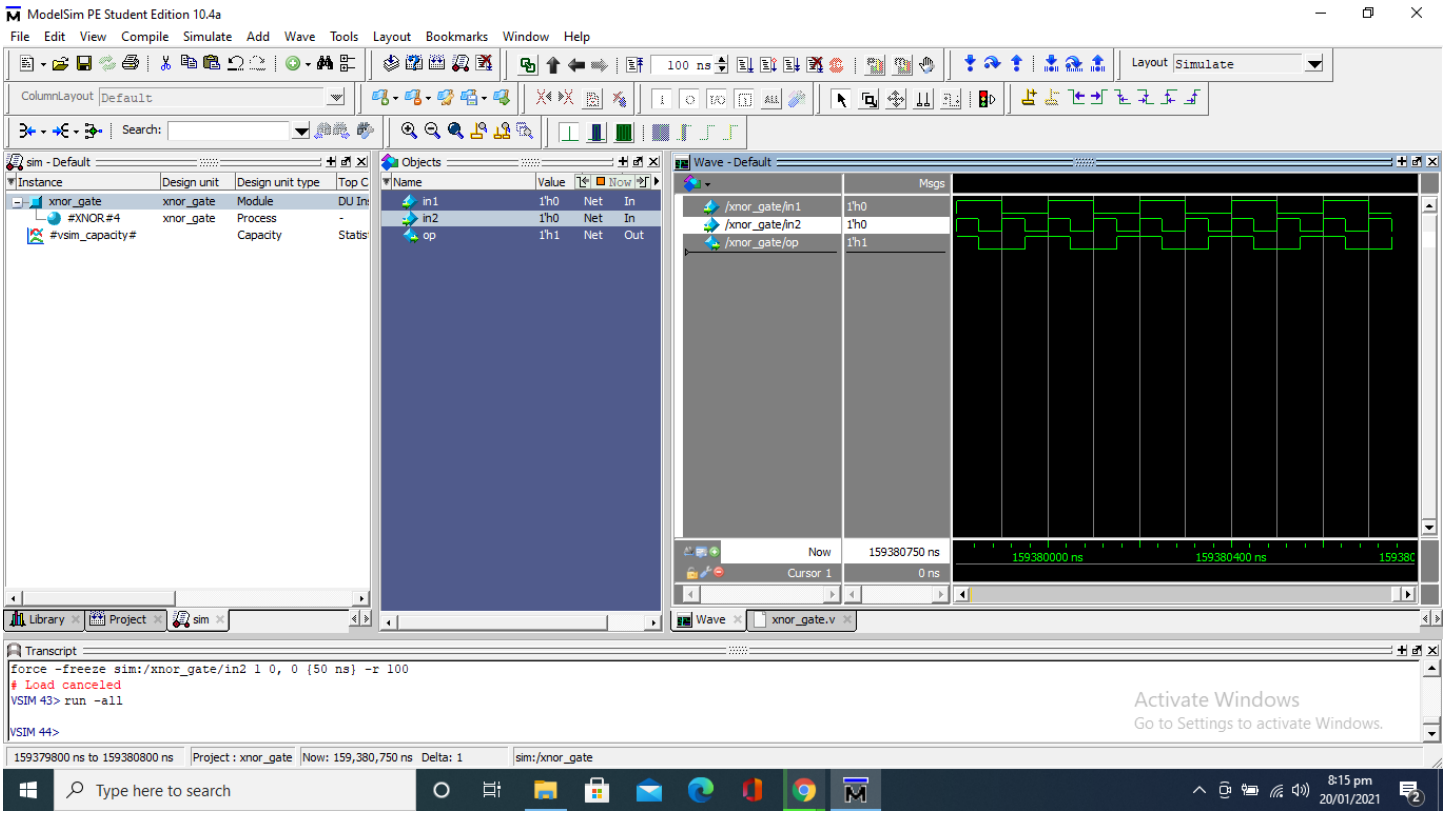


The output waveform is high for dissimilar inputs and low for similar inputs

XNOR-GATE

Symbol	Truth Table		
	A	B	Q
 2-input Ex-NOR Gate	0	0	1
	0	1	0
	1	0	0
	1	1	1
Boolean Expression Q = A XNOR B			



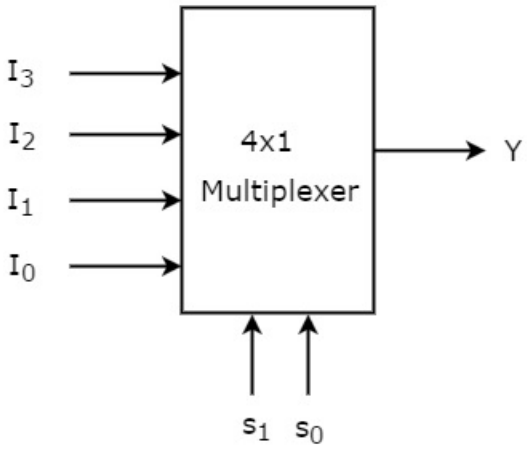


The output of the XNOR gate is high if both the inputs are the same; otherwise, the output is low. An EX-NOR gate is an equality detector. Here's the logical representation of the XNOR gate.

RESULTS : The AND , OR , NAND , NOR , XOR & XNOR gates have been implemented and verified.

Lab 13

Objective : To implement 4 to 1 MUX on Modelsim Software

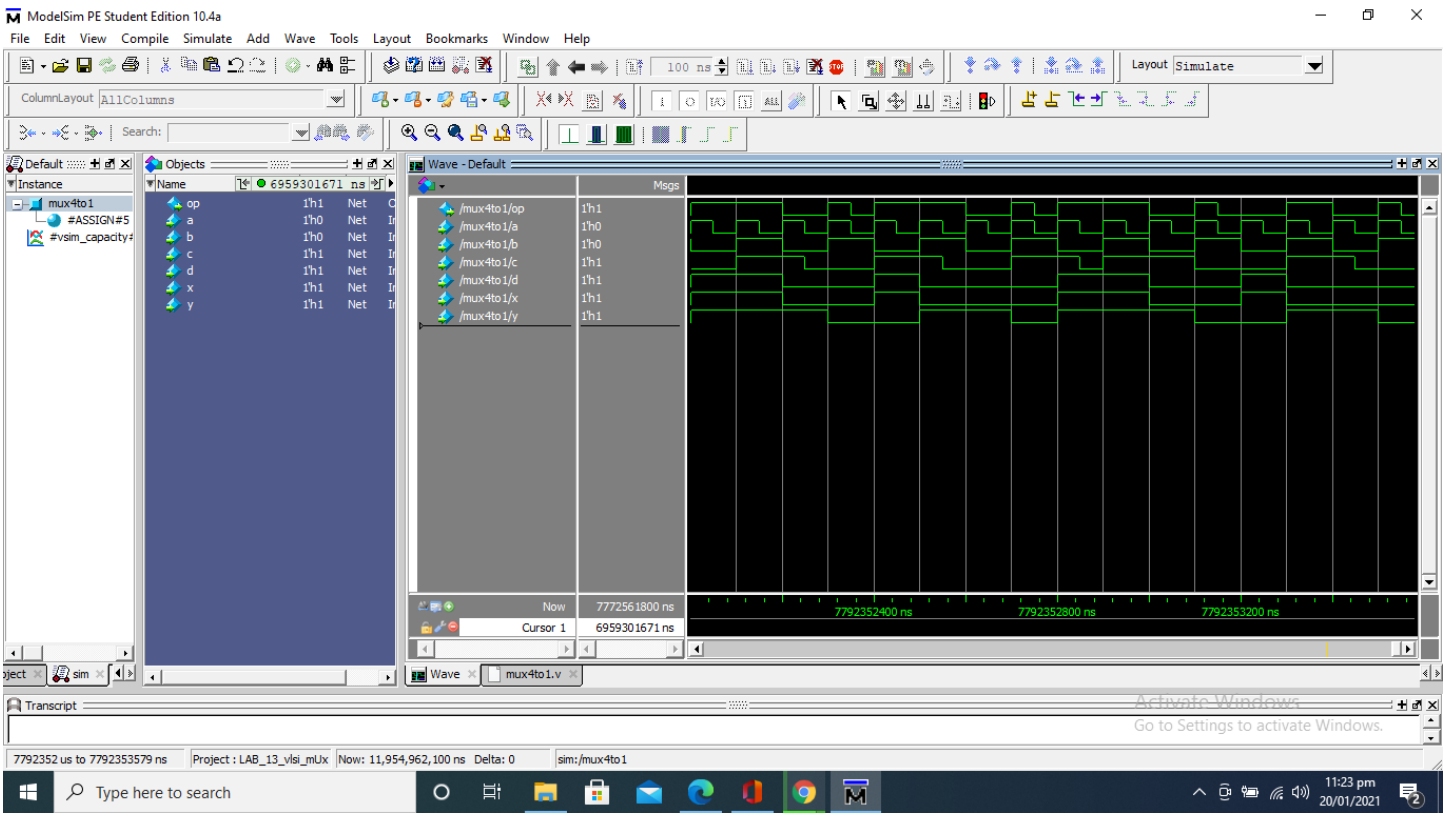


Project - E:/modelsim/examples/vlsi

Name	Status	Type	Order	Modified
mux4.v	✓	Verilog	0	01/23/2021 04:43

E:/modelsim/examples/mux4.v - Default

```
1  module mux4(a,b,c,d,x,y,out);
2   input a,b,c,d;
3   input x,y;
4   output out;
5   assign out= (a&(~x)&(~y))|(b&(~x)&(~y))|(c&(~x)&(~y))|(d&x&y);
6  endmodule
7
```



Outcome: The above waveforms verify the working of a 4:1 multiplexer.

Here when the input to the selector bits is 00 the output is a

When the input to the selector bits is 0 1 the output is b

When the input to the selector bits is 1 0 the output is c

When the input to the selector bits is 1 1 the output is d