

**DEPARTMENT OF ELECTRONIC ENGINEERING
N.E.D. UNIVERSITY OF ENGINEERING
AND TECHNOLOGY**

**VLSI SYSTEM DESIGN(EL-408)
BATCH 2017-18**

LAB SESSION # 8 TO 10

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CLASS: B.E

SECTION: C

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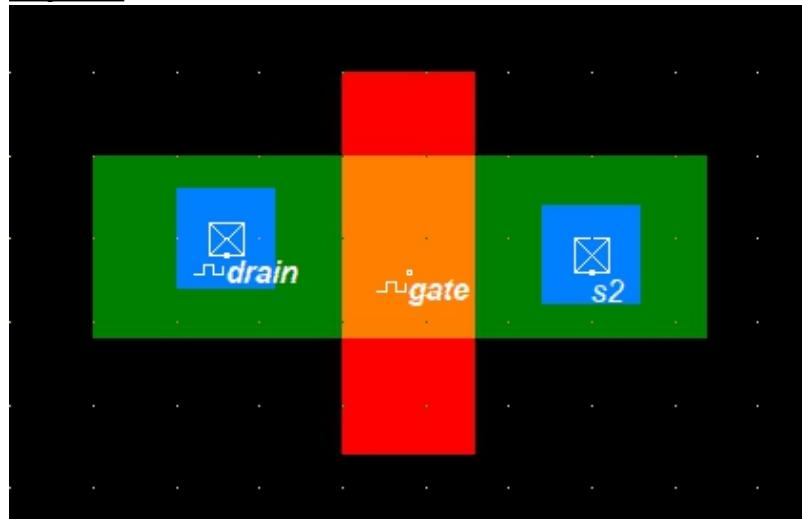
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LAB SESSION #8

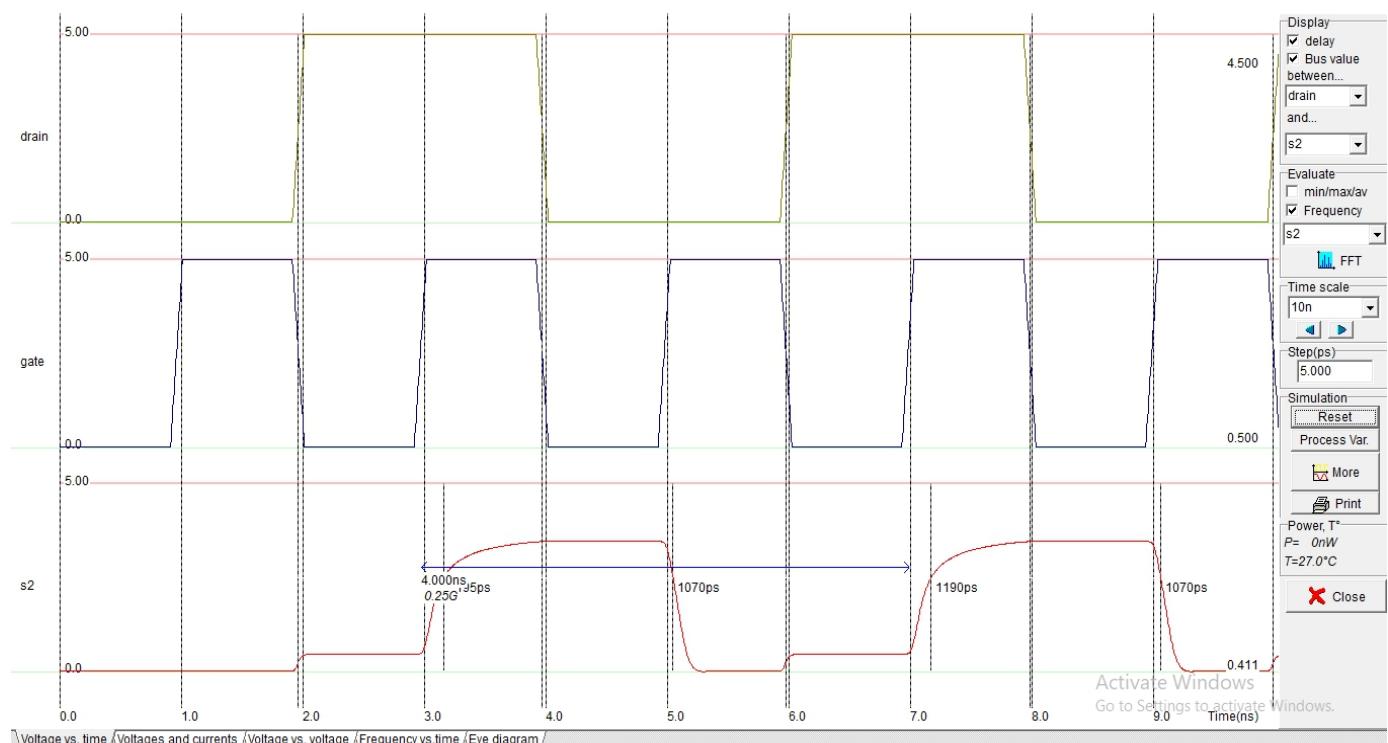
To design and verify the layout of a CMOS inverter using Microwind

TASK#1: NMOS TRANSISTOR

Layout:



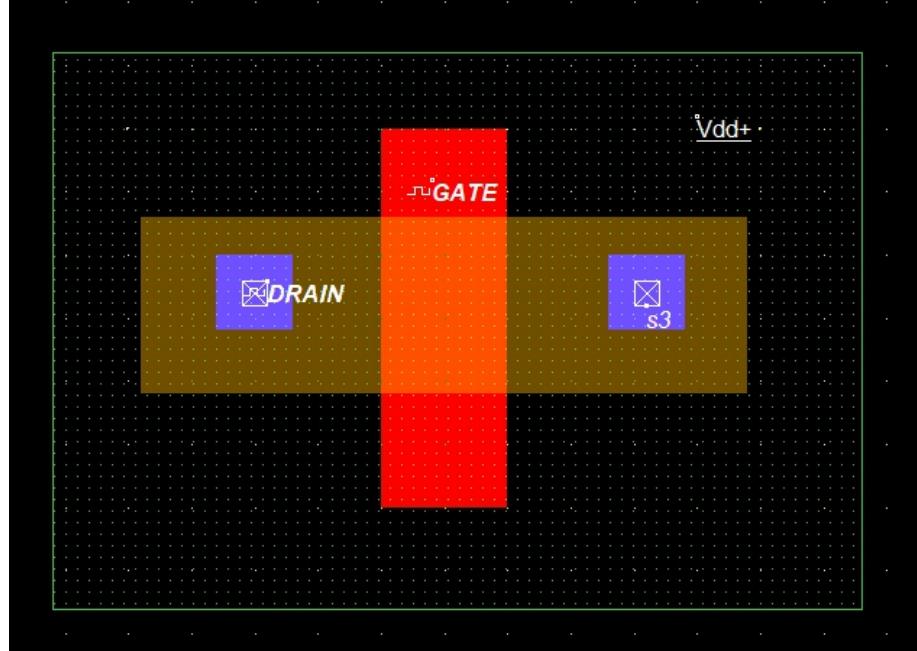
Simulation:



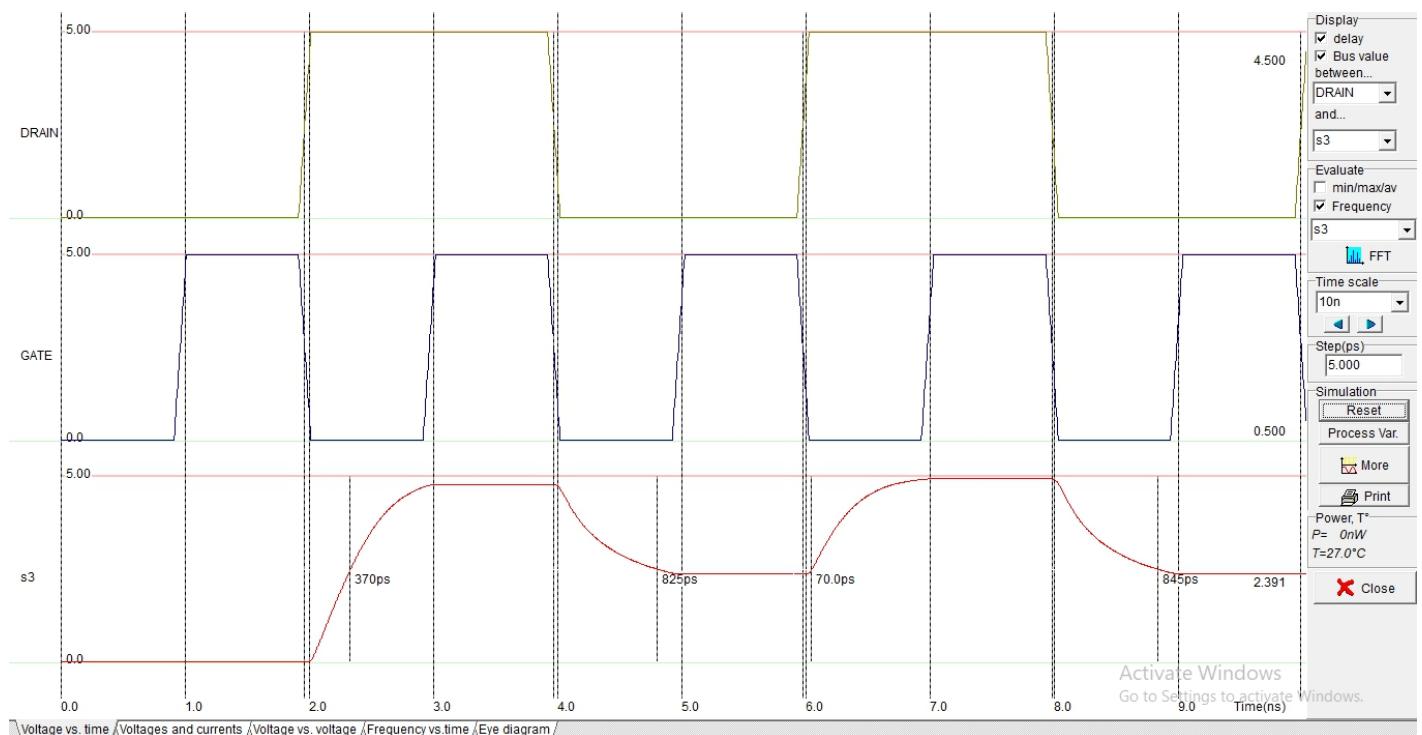
When $V_{gate}=0$ so cutoff (no current flow) and when $V_{gate}=5V$ so saturation (current flow). when $V_{gate}=0-5V$ so pass-through triode region. When signal high so NMOS on.

TASK#2: PMOS TRANSISTOR

Layout:



Simulation:

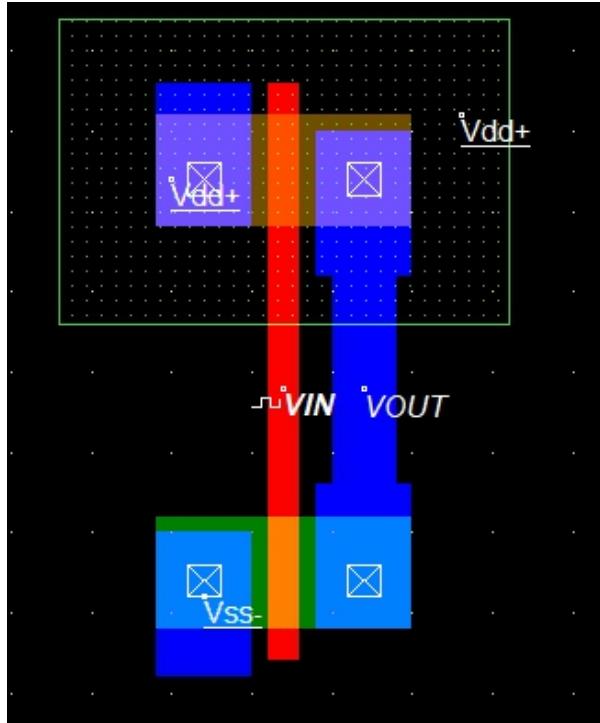


When $V_{gate}=0$ saturation (current flow) and when $V_{gate}=5V$ so cutoff (no current flow). when $V_{gate}=0-5V$ so pass-through triode region. When signal low so PMOS on.

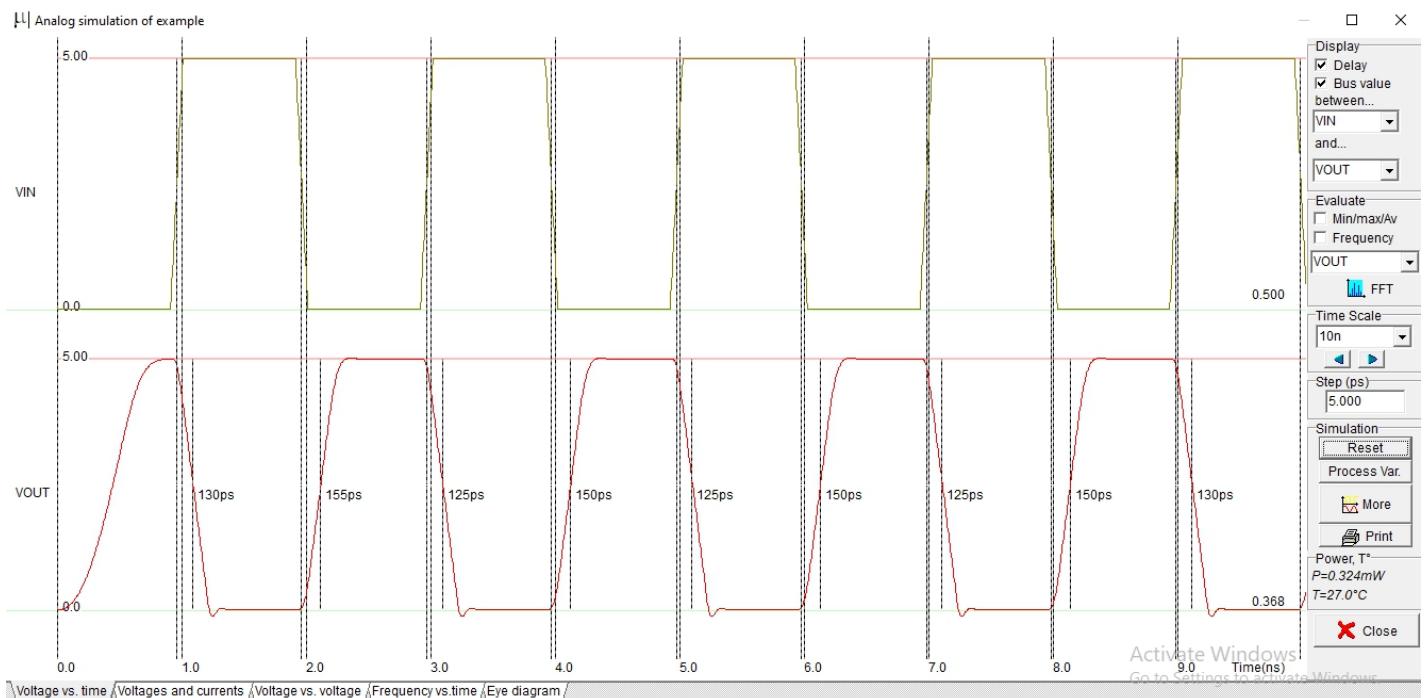
TASK#3: CMOS INVERTER

1) $(W/L)_P = (W/L)_N$ where $W=4\text{um}$ $L=0.8\text{um}$

Layout:

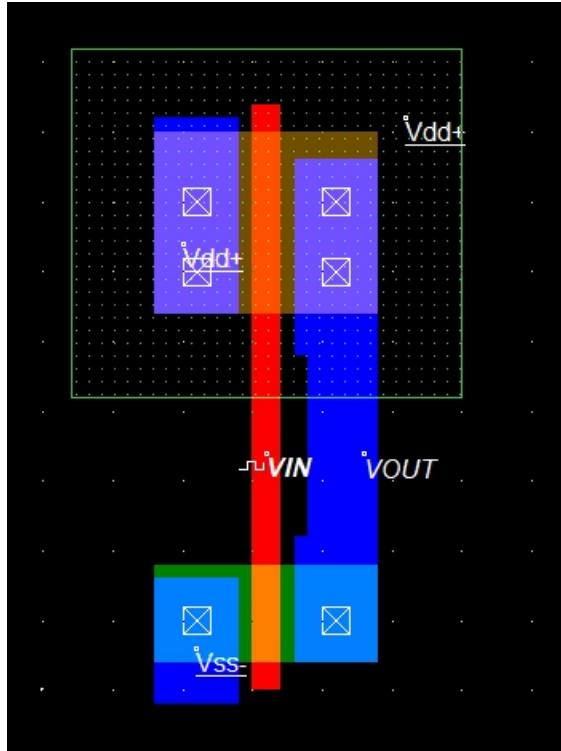


Simulation:

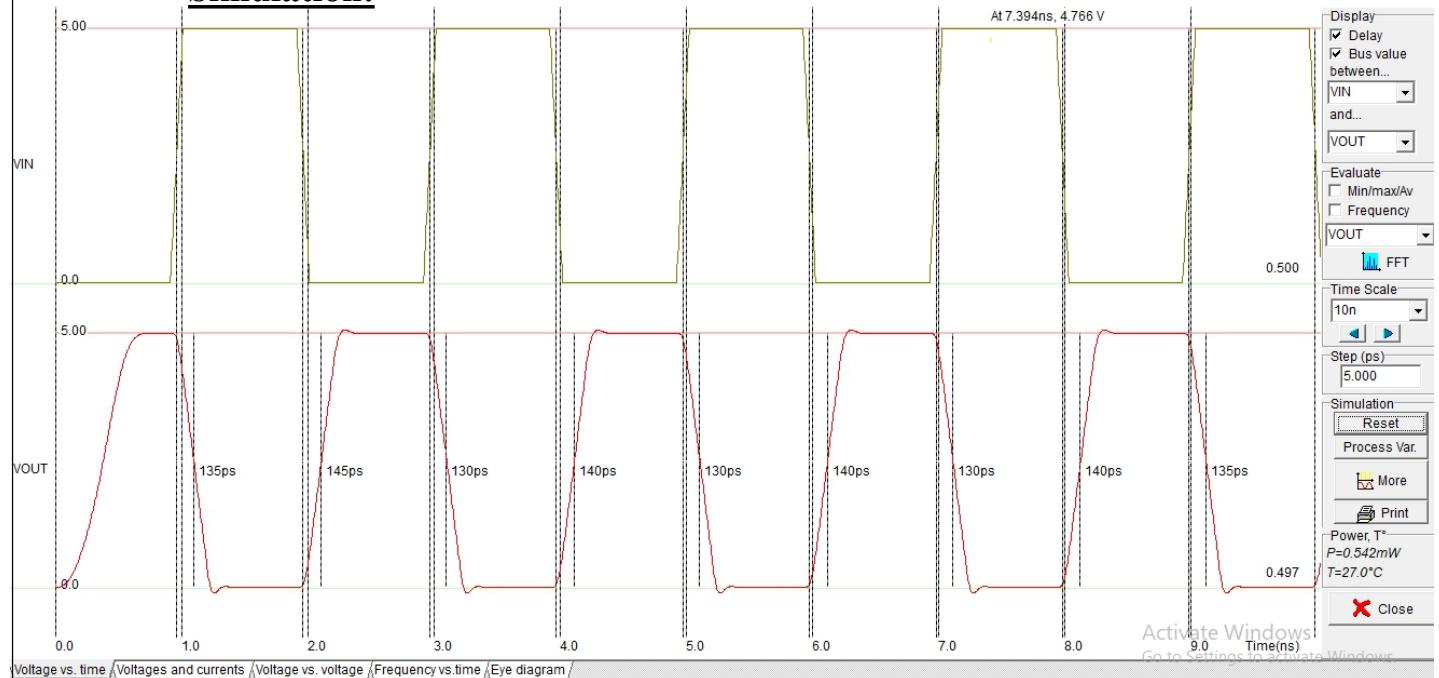


$$2)(W/L)_P = 2x(W/L)_N \text{ where } W=8\mu\text{m} \text{ L}=0.8\mu\text{m}$$

Layout:



Simulation:



In **CMOS INVERTER**, When $V_{IN} = 0V$ so PMOS on and when $V_{IN} = 5V$ so NMOS on. Charging of capacitance takes place when PMOS on and discharging of capacitor takes place when NMOS on. All PMOS transistors network, known as P-network, is responsible for determining rise time of output. While, All NMOS transistors network known as N-network, is responsible for determining fall time of output waveform.

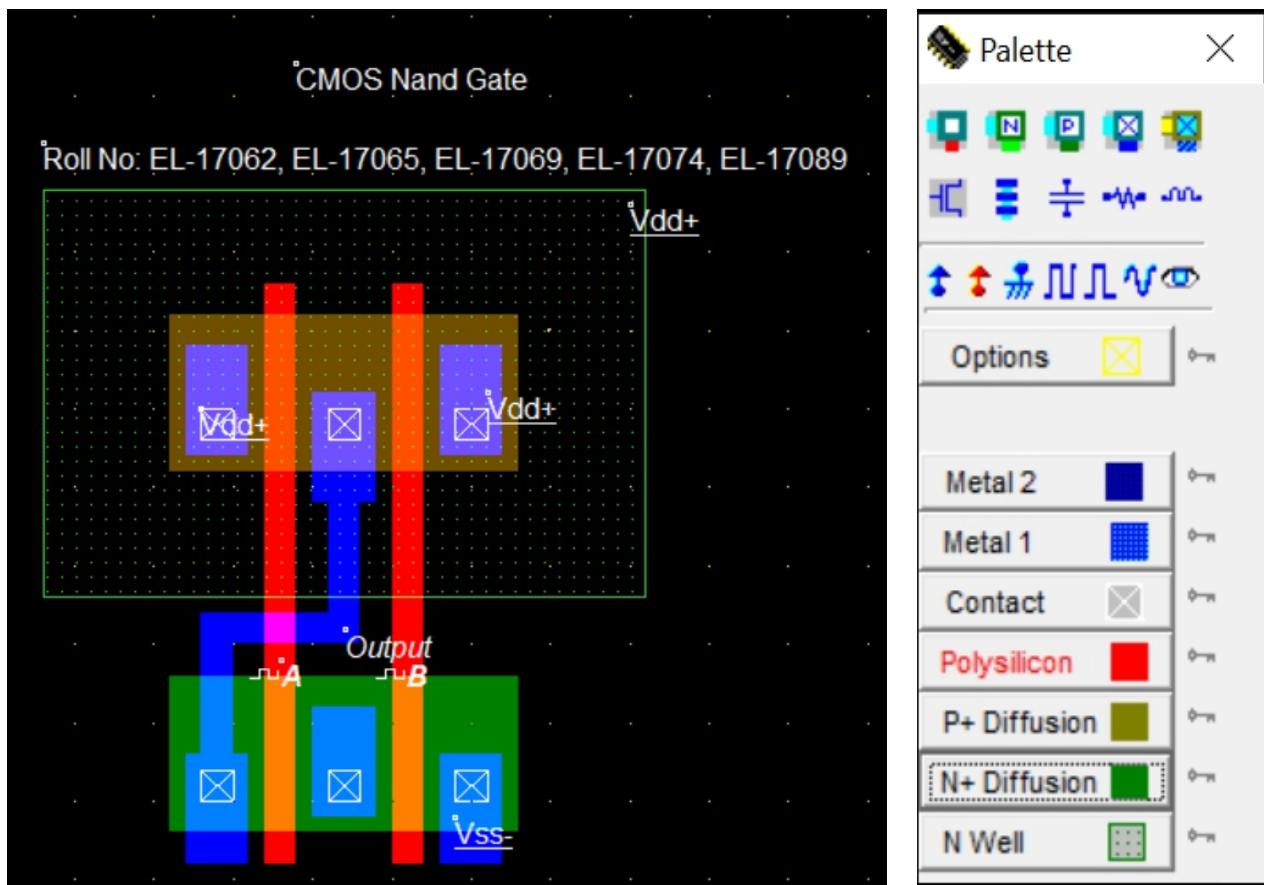
when $(W/L)_P = (W/L)_N$ so rise time is around 155,150ps where fall time is around 125ps

when $(W/L)_P = 2x(W/L)_N$ so rise time is around 145,140ps where fall time is around 135,130ps

LAB 09

TO DESIGN AND VERIFY THE LAYOUT OF A CMOS NAND GATE.

LAYOUT:



DIFFUSION LAYERS:

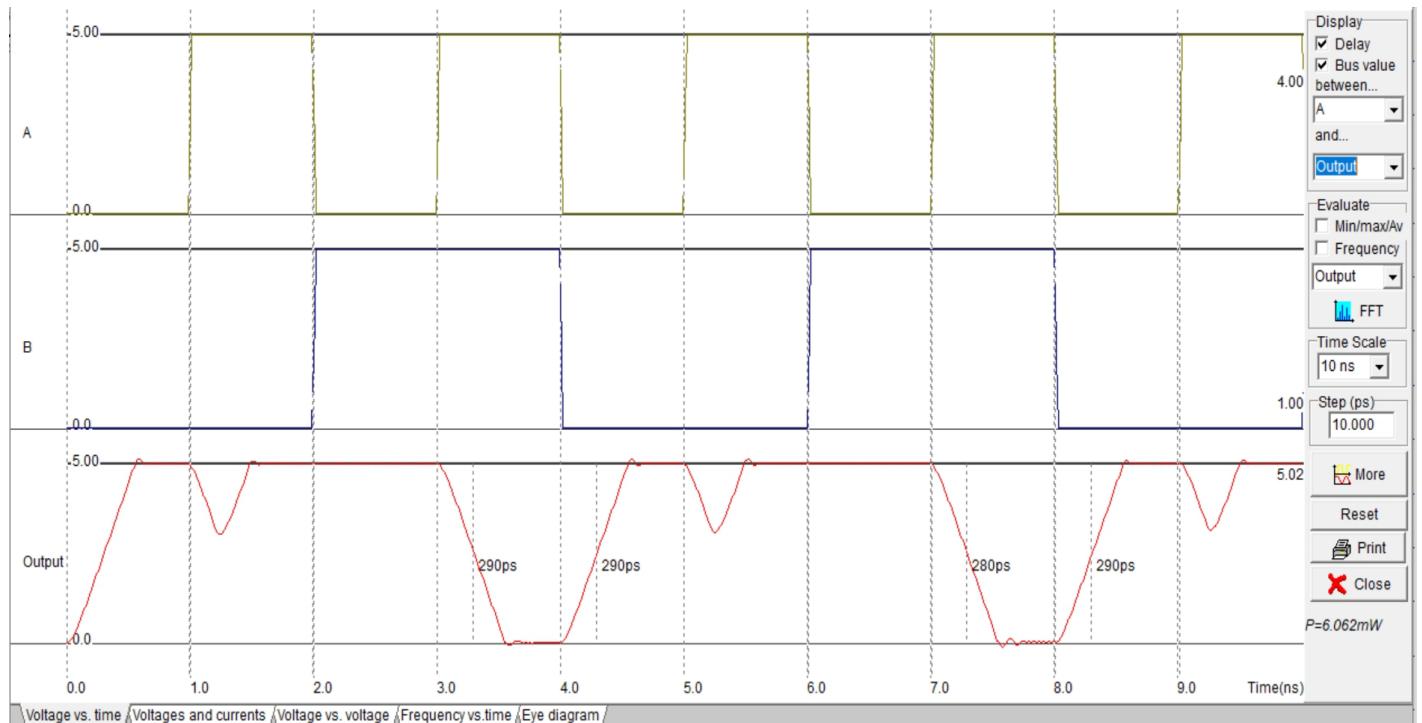
- There should be continuous layer of n+ and p+ diffusion.
- There must be a single rail of Vdd as well as for Vss.
- Width and length of all transistors should be same.

The diffusion layers: p+ diffusion layer, n+ diffusion layer

$$W_{PMOS} = W_{NMOS} = 2.0\text{um}$$

$$L_{PMOS} = L_{NMOS} = 0.6\text{um}$$

SIMULATIONS:



CONCLUSION:

The CMOS NAND gate is verified from the below observations:

| Clock A | Clock B | output |
|---------|---------|--------|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

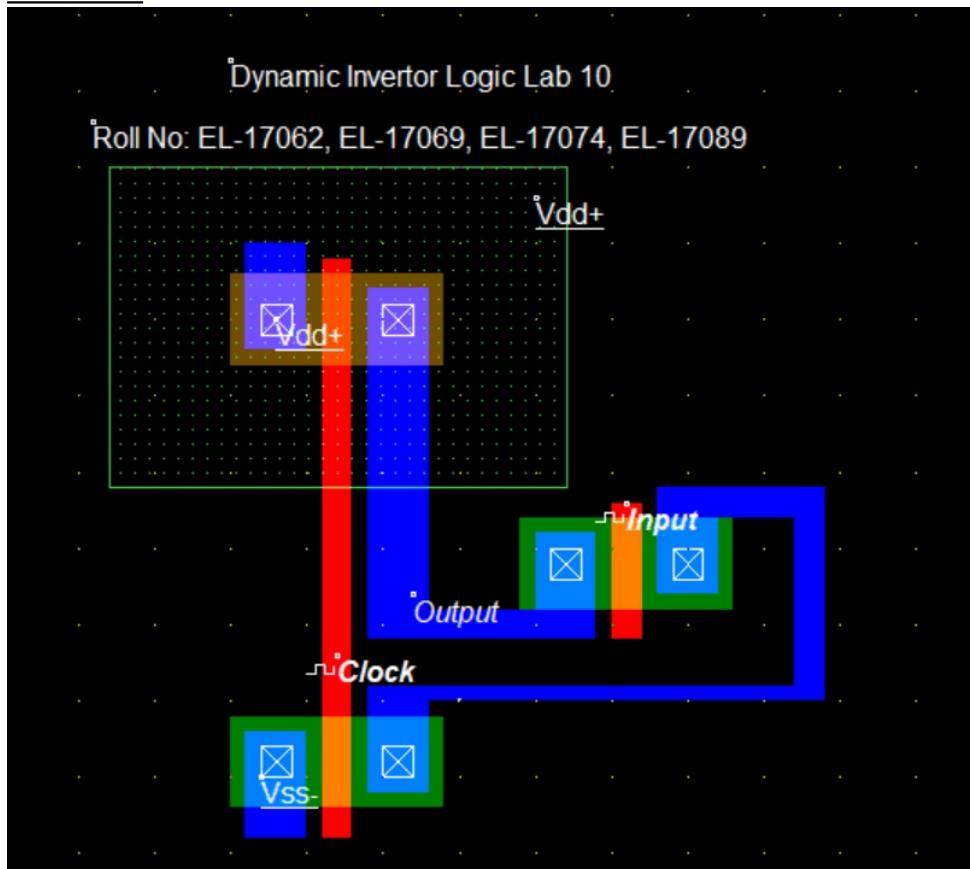
LAB 10

TO DESIGN AND VERIFY THE LAYOUT OF

DYNAMIC INVERTER LOGIC USING MICROWIND

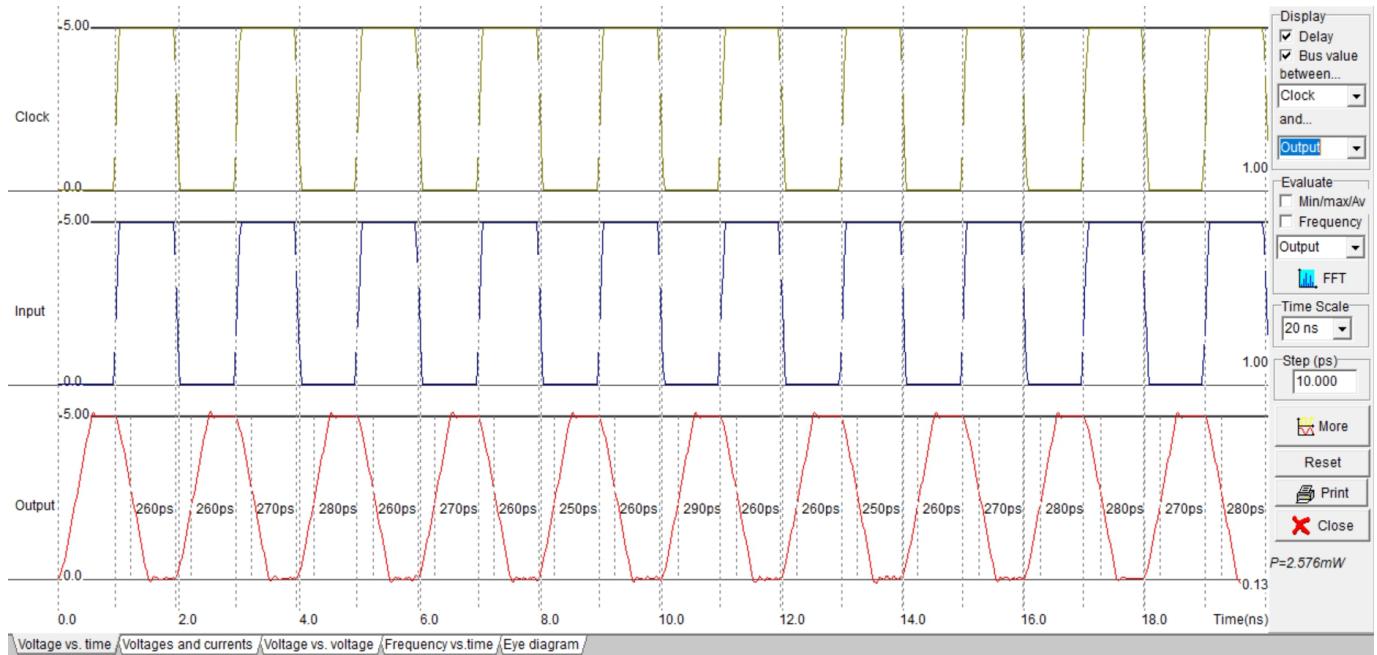
- a) Take frequency of clock signal in comparison to frequency of square wave input signal. Observe and attach the simulation results
- b) Take frequency of clock signal much smaller than frequency of square wave input signal. Observe and attach the simulation results.
- c) Take frequency of clock signal much greater than frequency of square wave input signal. Observe and attach the simulation results.

LAYOUT:



i) Frequency of clock same as that of square wave input.

Clock= Vin(Input)= 2ns time period.

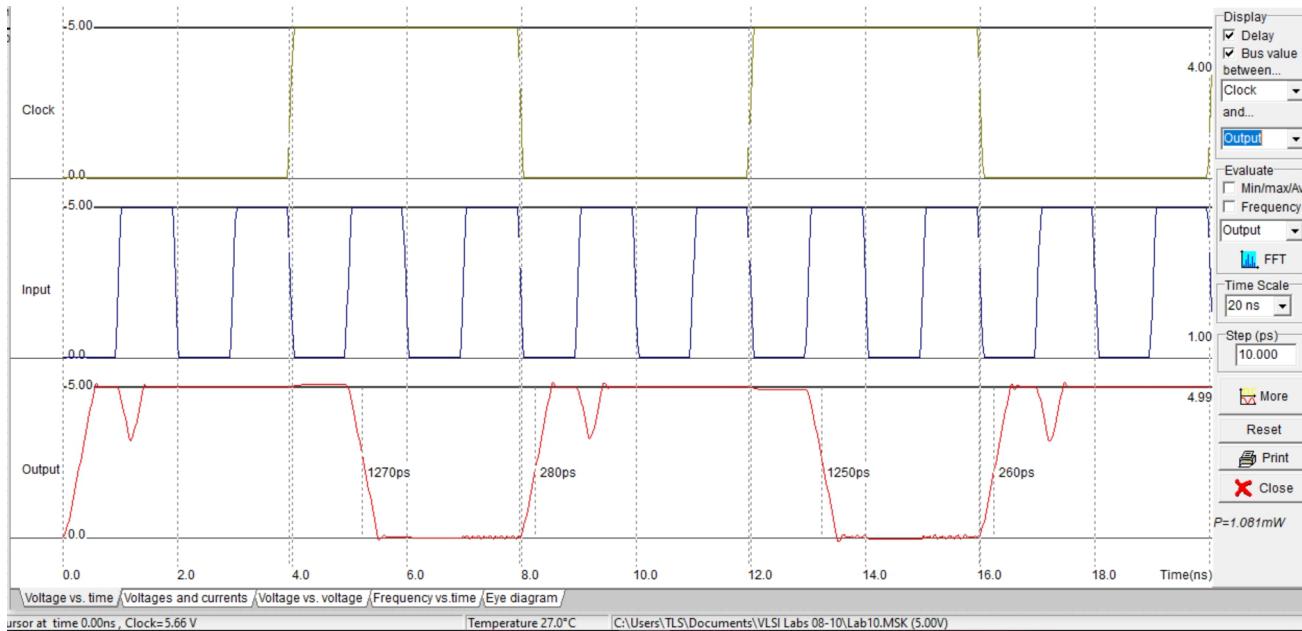


CONCLUSION:

Our first observation is when our V_{in} and clock input frequencies are same. We observed that clock's high and low stages are occurring exactly at the same time when V_{in} changes its level from high to low and low to high. As a result, when clock is low, our circuit is in pre-charged phase because output voltage is equal to $V_{dd}(\text{high})$. Whereas, when clock input is high, our circuit is in evaluation phase and input V_{in} is also high, so that Q1 is off, Q2 and Q3 is on and our capacitor start discharging which results our output voltage to be zero.

ii) Frequency of clock smaller than the frequency of square wave input

Clock= 8ns time period, Vin(input)=2ns time period



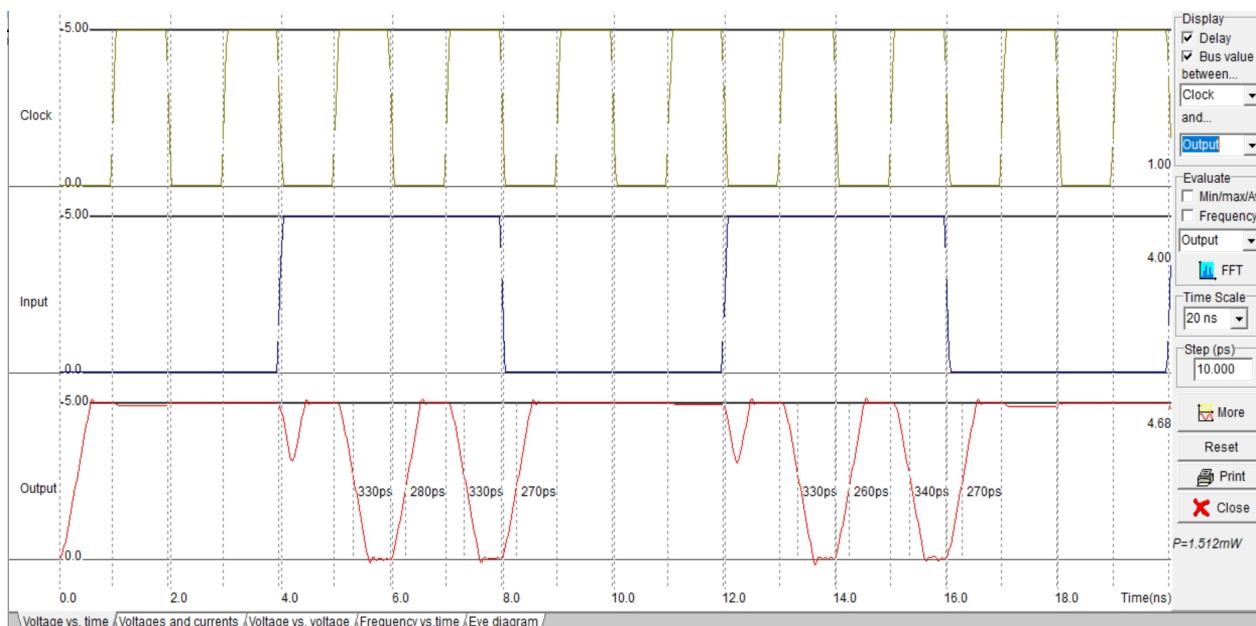
CONCLUSION:

In this observation, we have observed when our clock pulse is smaller than V_{in} and due to which its transition from low to high and high to low goes slowly. Now if we consider high input (V_{in}) pulse, then we observed that our V_{out} decreases and capacitor starts discharging as there is a path available for it to discharge. When our V_{in} becomes low and clock is still high, our V_{out} will hold its previous low state as all Q1(PMOS) and Q2 is open switch and Q3 becomes switched on, but there is no path available for capacitor to get charged.

While if our clock is low, and V_{in} is high, our Q1 and Q2 is switched on and Q3 becomes open switch, capacitor starts charging and V_{out} becomes equal to V_{dd} . When V_{in} gets low, Q2 and Q3 will be open switch and our capacitor retain its charge, thus V_{out} remains equal to V_{dd} .

iii) Frequency of clock greater than frequency of square wave input

Clock= 2ns time period, Vin(Input)=8ns time period



CONCLUSION:

Next observation is when we have frequency of clock greater than V_{in} and we observe that clock pulse coming more faster than V_{in} . Therefore, at some moments when clock is high and V_{in} is low, our V_{out} is high which is one case of evaluation phase. Whereas, when our V_{in} is high and our clock get transition from low to high, then our output voltage (V_{out}) gets abrupt transition from high to low. Similarly, we can observe the pre-charge phase condition there and we can see that our V_{out} pulse contains abrupt transition from high to low and low to high and not smoothly changed as we have observed in case 1.