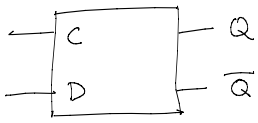
lecture 6

sequential circuits 2

Last lecture

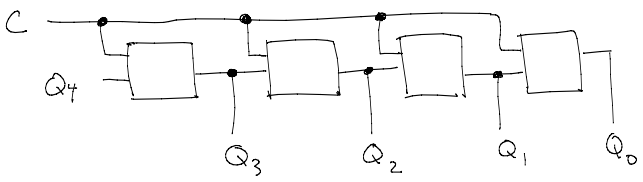
- D flipflop

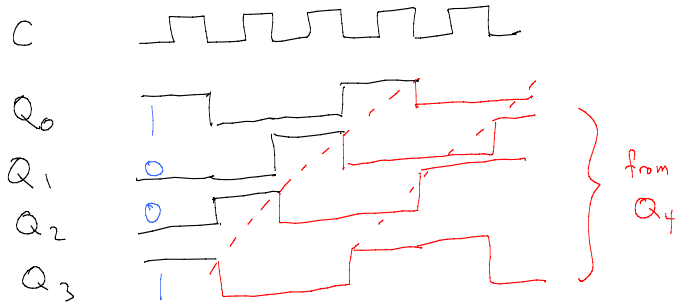


- read / write are synchronized with clock

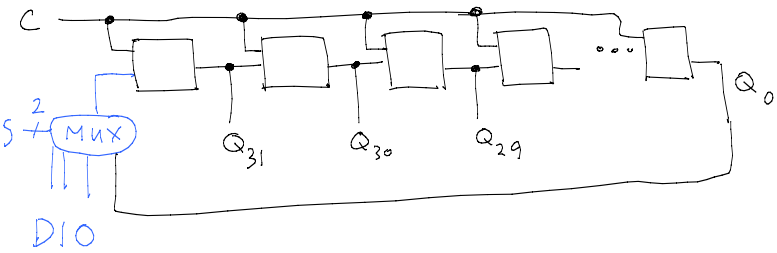
- can be either rising or falling edge

Shift right register (falling edge)

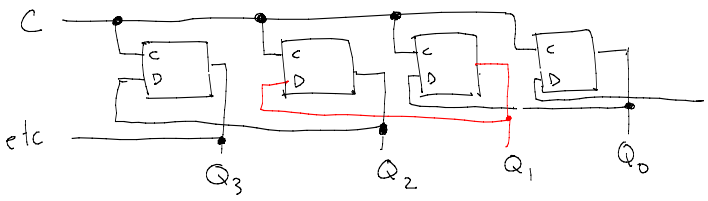




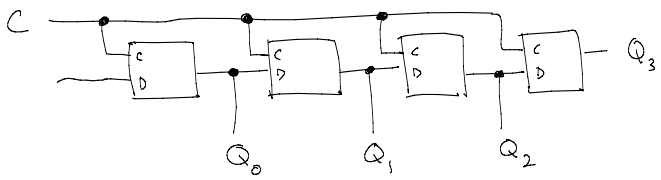
Shift right register



Shift left register

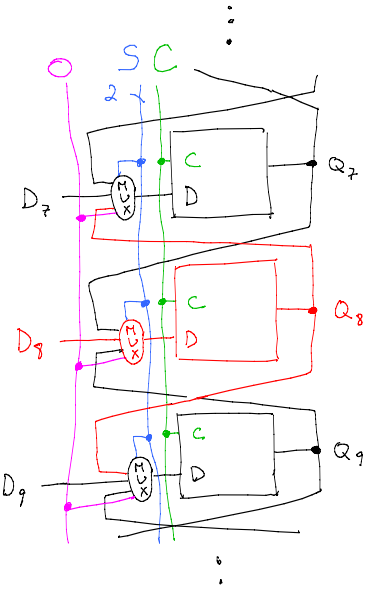


Alternatively ...

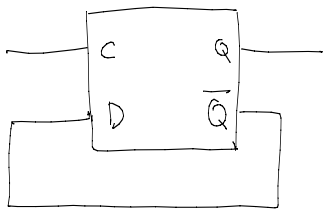


Select from

- shift left (down)
- shift right (up)
- write data
- clear



T flip-flop (toggle)



(falling edge)

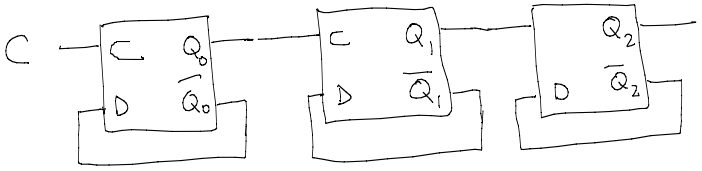
C

Q

$\overline{Q}$

What does this circuit do?

(assume falling edge triggered)



C

Q_0 0 1 0 1 0 1 0 1 0

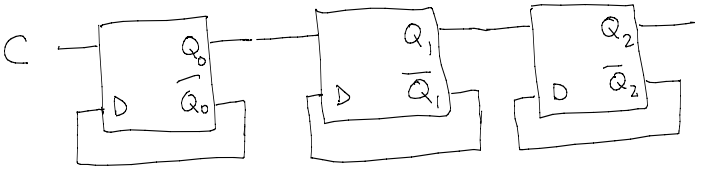
Q_1 0 0 1 1 0 0 1 1 0

Q_2 0 0 0 0 1 1 1 1 0

0 1 2 3 4 5 6 7 8

What does this circuit do?

(assume rising edge triggered)



Timer (count down)

C

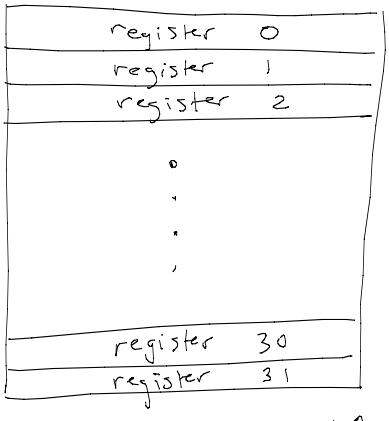
Q_0 0 1 0 1 0 1 0 1 0

Q_1 0 1 1 0 0 1 1 0 0

Q_2 0 1 1 1 1 0 0 0 0

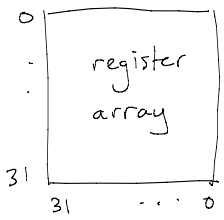
0 1 2 3 4 5 6 7

Register Array



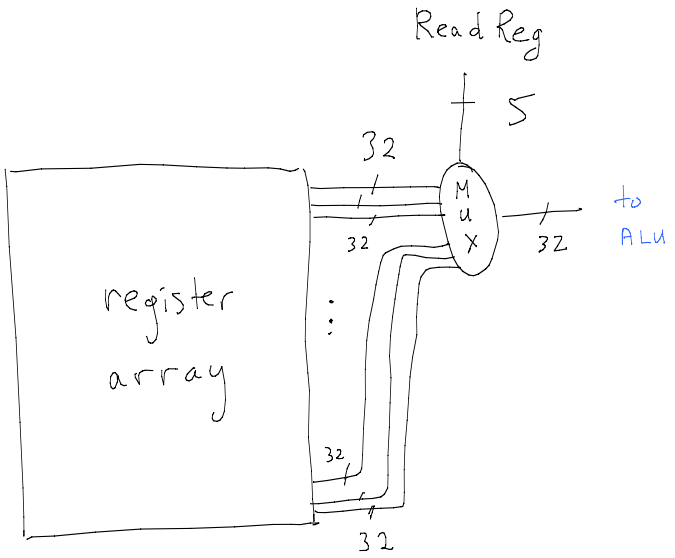
31, 30, ... , 3, 2, 1, 0

$x = y + z$

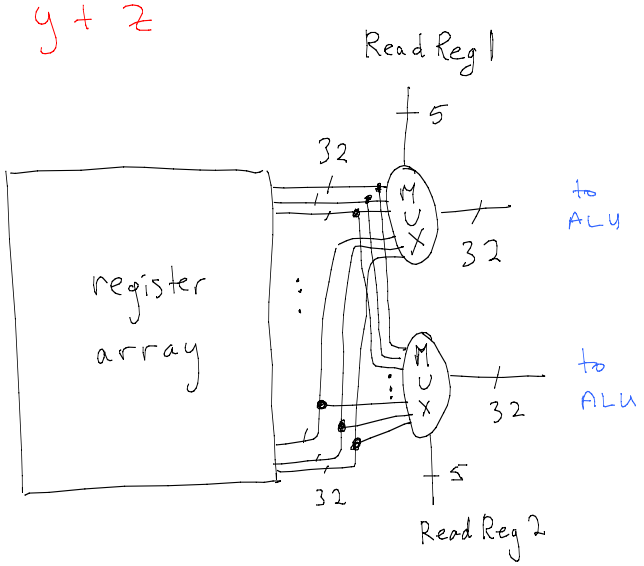


How to read y and z ?

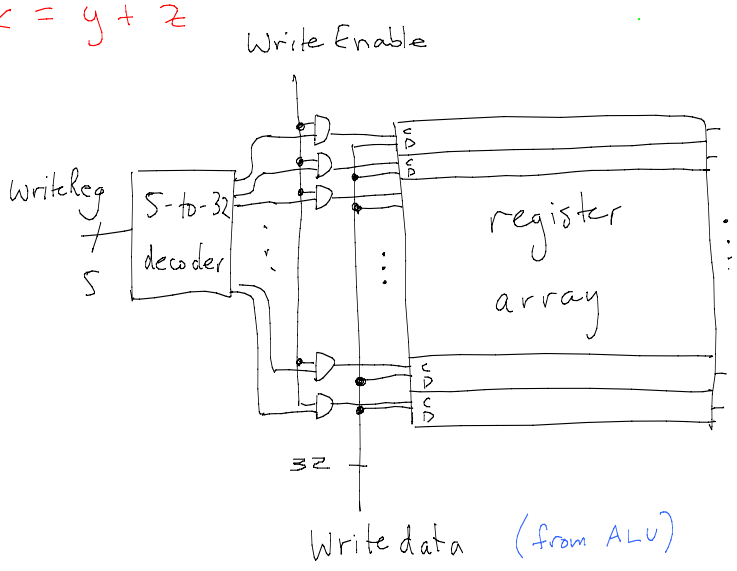
How to write result into x ?

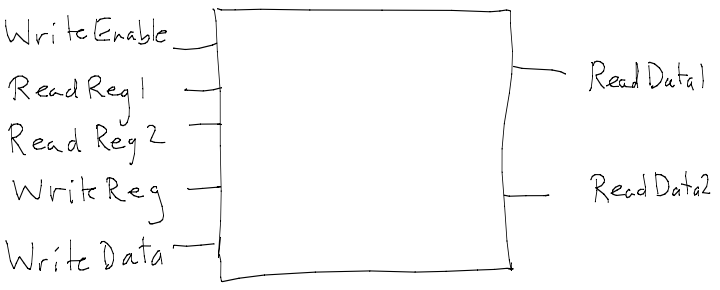


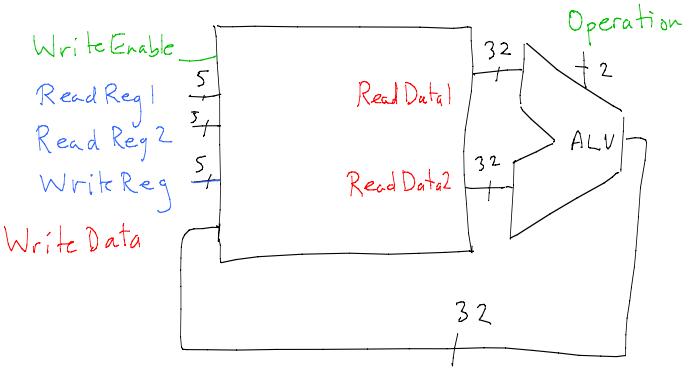
$x = y + z$



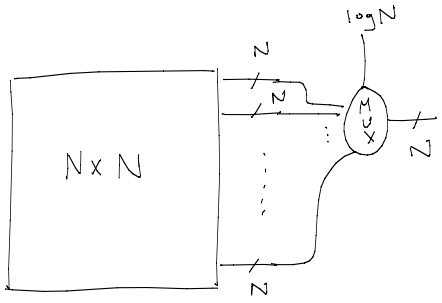
$x = y + z$



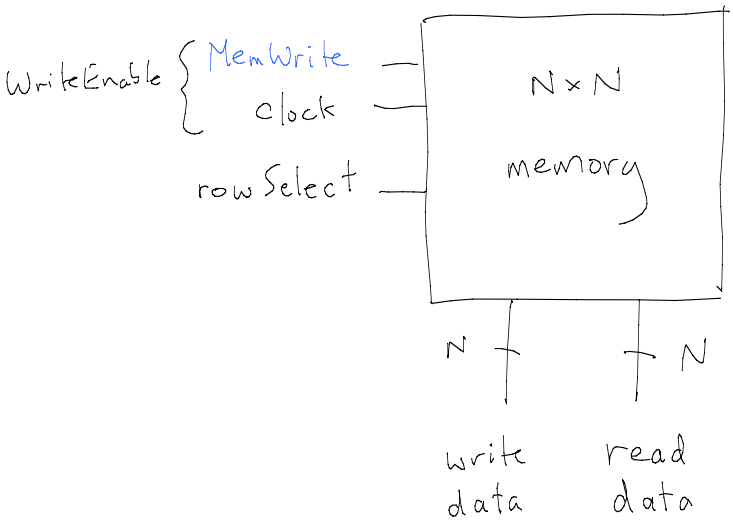


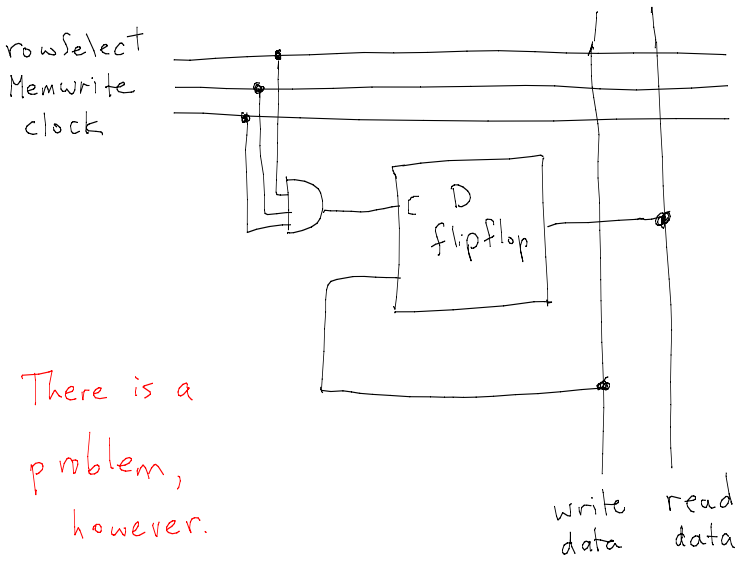


address
data
control
} types of signals



For larger memory arrays, the multiplexor design is not feasible.

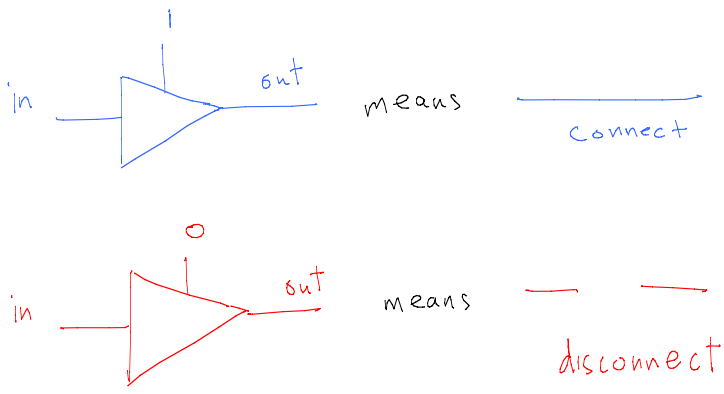


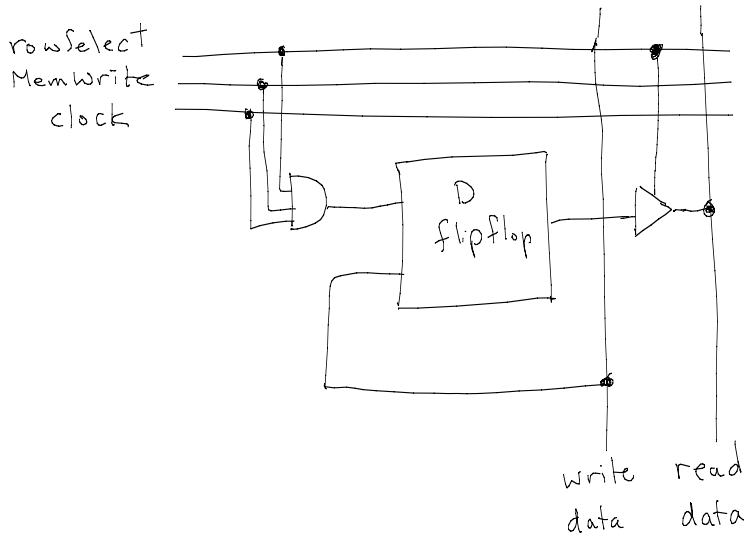


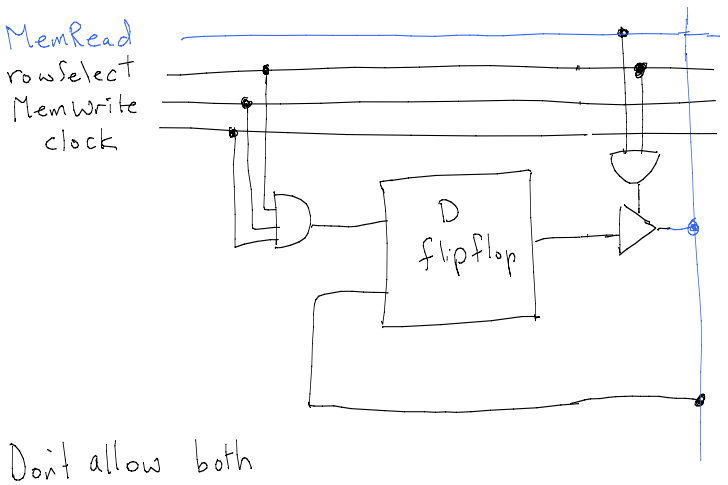
There is a problem, however.

tri-state gate

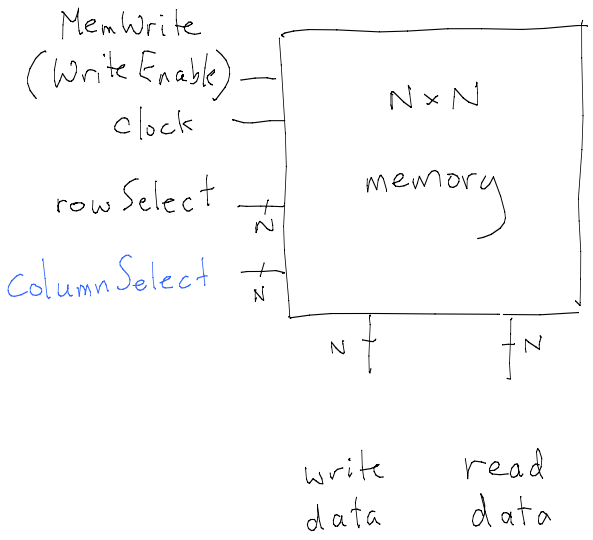
(also known as tristate buffer)

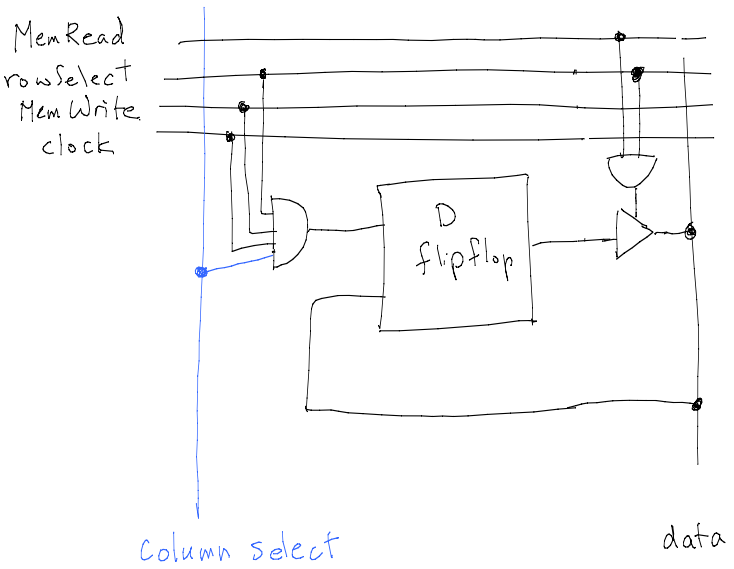




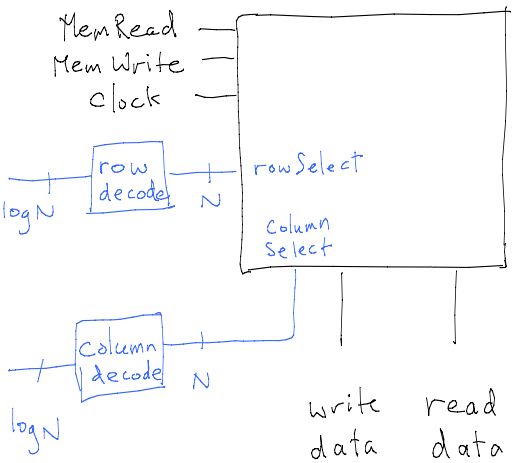


Don't allow both MemRead and MemWrite to be 1.





RAM (N x N memory)

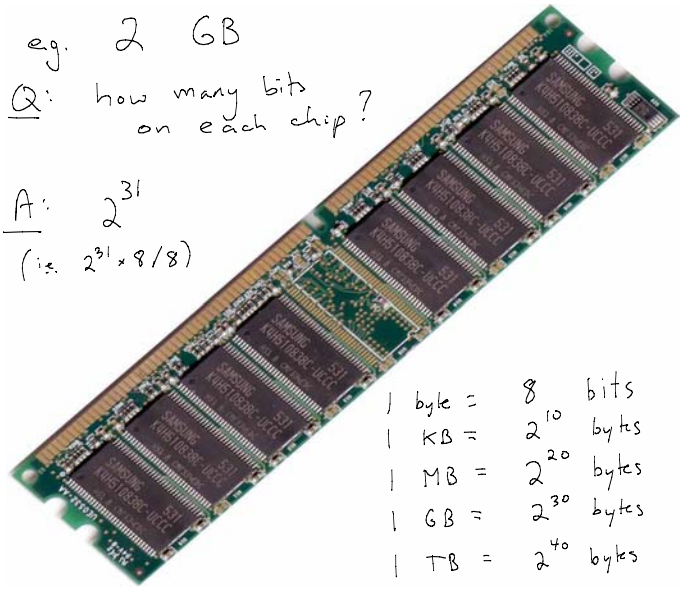


eg. 2 GB

Q: how many bits on each chip?

A: 2^{31}

(i.e. $2^{31} \times 8/8$)



1 byte	=	8	bits
1 KB	=	2^{10}	bytes
1 MB	=	2^{20}	bytes
1 GB	=	2^{30}	bytes
1 TB	=	2^{40}	bytes