Student ID:	
Faculty Initial	

Department of Computer Science and Engineering
FINAL EXAMINATION SUMMER 2015

CSE260: Digital Logic Design

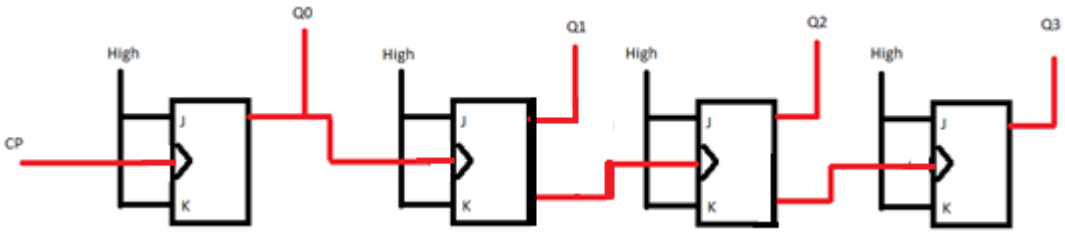
Total Marks: 150 **Time Allowed: 2 hours 15 minutes**

- Answer **ALL** questions
- Fill up Student ID and Faculty initial in the top left corner box of question Paper

Question 1

[6 marks]

a) Draw the timing diagram of clock pulse, Q0, Q1, Q2 and Q3



[4 marks]

b) Design an asynchronous modulo 13 counter where the flip-flop for least significant bit and most significant bit are comprised of negative edge triggered T flip-flop and rest are positive edge triggered T flip-flop.

Question No. 2

a)

[12 marks]

Selection Bits (S_2 S_1 S_0)	Operation
000	Reset (Save 0 in all Flip-flops)
001	Rotate left
010	Invert Stored value
011	Shift left
100	Rotate right
101	Parallel Load
110	No change
111	Shift right

Design a ***6 bit*** bidirectional shift register, using as many 8:1 MUXes, basic gates and D

Flip-flops as you need, to perform according to the following table

b) Determine the essential prime implicants of the following function using Quine Mcclusky method. [8 marks]
$F(A,B,C,D) = \Sigma(3,4,5,7,9,13,14,15)$.

Question 3

a) (i) Implement 64 :1 multiplexer with four 16:1 and one 4 :1 multiplexer. [10 marks]
(ii) Design 1:16 demux using as many '2x4 decoder with enable' as you like and one '2x4 decoder without enable'
(Use only block diagrams)

[6 marks]

b) Perform the following arithmetic using 7 bit two's complement and comment whether overflow has occurred or not?
(i) (+27) + (-61)
(ii) (-27) + (+61)
(iii) (-27) + (-61)

[4 marks]

c) Determine the decimal value of the 7-bit binary number (1001100) when interpreted as:

Unsigned number	Signed-magnitude number	Signed-1's complement number	Signed-2's complement number

Question 4:

a) Design XOR and XNOR gate using one 2:1 MUX [4 marks]

b) [10 marks]

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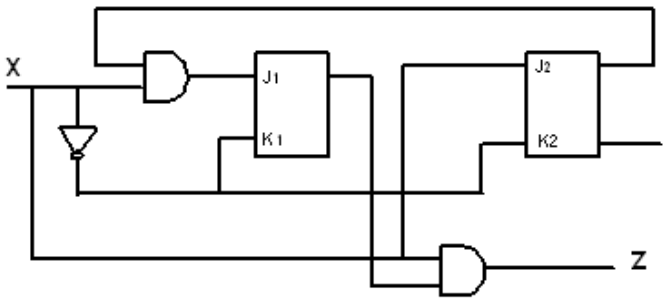

Consider the above synchronous sequential circuit. Determine its state table and state diagram.

c) Minimize the expressions and draw the logic diagram of the following functions [6 marks]

(i) F(X,Y,Z)=XY + X'YZ' + YZ
(ii) G(x,y,z)= x'y' + x'yz + xz + xyz'.

Question No. 5 : *For the love of Coffee*

Gloria's Jeans wants to hire you to design their automated coffee machine. They want their machine to be able to make three of their most popular coffee flavors: 'Shot of espresso', "Latte" and "Mocha". Basic ingredient for any of these flavors are Brewed Coffee, ful cream milk, sugar and coco powder.

Input and output of the automated coffee machine is as follows:

Input (4 variables)

C= 1 indicates presence of Brewed coffee.
M = 1 indicates presence of full cream milk
S = 1 indicates presence of sugar.
K = 1 indicates presence of Cocoa Powder

Output (3 variables)

E = 1 indicates ***Shot of Espresso*** *is ready*
L = 1 indicates ***Latte*** *is ready*
M = 1 indicates ***Mocha*** *is ready.*

Gloria's Jeans authorities has asked you to consider the following points when designing the system:

1. Without brewed coffee it is impossible to make any type of coffee.

2. Brewed coffee and milk are essential for making Latte. Sugar is n optional(may or may not be there) ingredient. You do not need cocoa powder to make Latte.

3. Brewed coffee, cocoa powder and milk are essential for making 'Mocha'. Sugar (may or may not be there) is an optional ingredient.

4. 'Shot of Espresso' is just brewed coffee. Sugar is an optional ingredient. Cocoa powder and milk is not at all needed to make 'Shot of Espresso'.

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a) Using the above specification, prepare a truth table for the automated coffee machine. [15 marks]

b) Using 4 variable Karnaugh-Map method, derive SOP expressions for all of the three flavors of coffee mentioned above. [20 marks]

Question No. 6

Design the sequential circuit specified by the state diagram of the figure shown using T flip-flops. [20 marks]