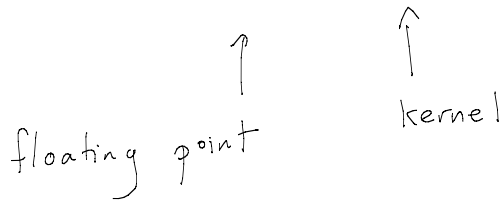
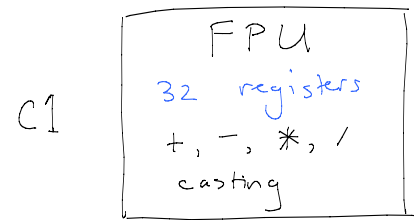


## lecture 12

MIPS coprocessors c1 & c0



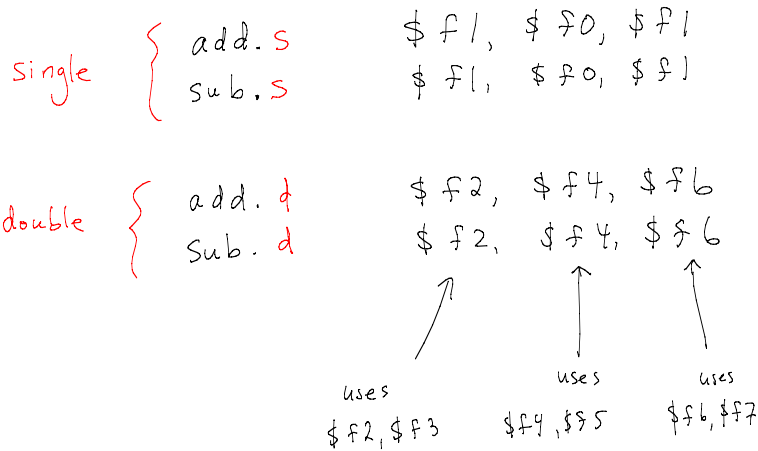
## Floating Point Unit (FPU)



\$f0, \$f1, ..., \$f30, \$f31

double precision uses 2 adjacent words  
\$f0, \$f2, \$f4, ... \$f28, \$f30

## Floating point operations



## NOT ALLOWED

add.s \$s0, \$s1, \$s2

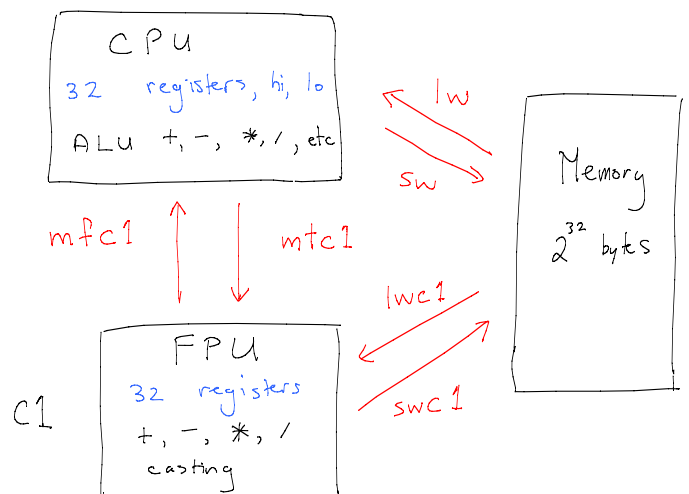
add \$f0, \$f3, \$f7

mul.s \$f1, \$f0, \$f1  
div.s \$f1, \$f0, \$f1

mul.d \$f2, \$f4, \$f6  
div.d \$f2, \$f4, \$f6

Note: hi, lo register not used

## Data Transfer Operations



CPU  $\leftrightarrow$  C1

mtcl \$s0, \$f0

mfcl \$f0, \$s0

Note backwards ordering for these instructions.

Loading and storing

lwcl \$f2, 40(\$s0)

swcl \$f2, 40(\$s0)

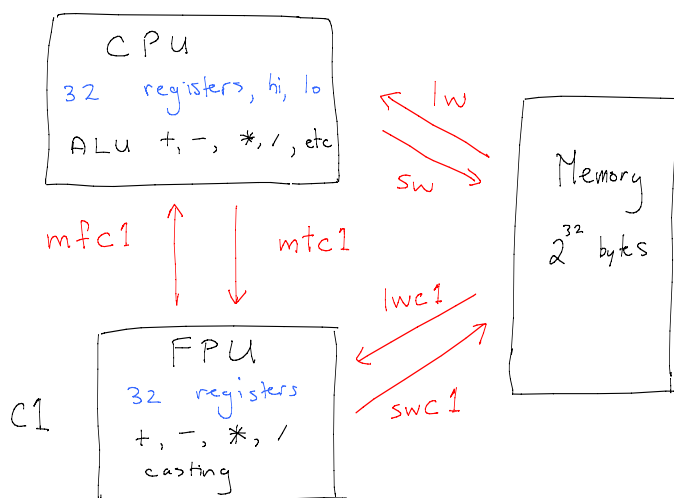
↑  
address held in  
CPU register

l.d \$f2, 40(\$s0)

s.d \$f2, 40(\$s0)

pseudo instruction loads two adjacent words

## Data Transfer Operations



## Casting

int i

float x

double y

i = (int) x

x = (float) i

y = (double) x

x = (float) y

## Casting in MIPS

— performed on C1 (not CPU)

cvt. — —

e.g.

cvt.s.d \$f3, \$f0

cvt.w.s \$f0, \$f1

↑  
int

int i // \$s0

float x // \$f0

i = (int) x

mov.s \$f4, \$f0

cvt.w.s \$f4, \$f4

mfc1 \$f4, \$s0

#\$f4 is temp  
# "w" for int

```
int    i           // $s0
float  x           // $f0
```

$x = (\text{float}) i$

---

```
mtcl    $s0, $f0  # note order
cvt.s.w  $f0, $f0
```

## Example

```
addi    $s0, $0, -8
mtcl    $s0, $f0
```

# Both \$s0, \$f0 have  
# 0x ffffffff8  
# Verify for yourself

# \$f0 = 0x ffffffff8

cvt.s.w \$f1, \$f0

sign exp significand

1 10000010 000000000000000000000000

# \$f1 = 0xc1000000

```
int    i = 841242345
```

//  $2^{23} < i < 2^{31}$

```
int    j = (int)((float)i)
```

//  $i \neq j$

---

```
mtcl    $s0, $f0
cvt.s.w  $f1, $f0
cvt.w.s  $f1, $f1
mfcl    $f1, $s1
```

# \$s0, \$s1 have different values

Single precision

1, 8, 23

Double precision

1, 11, 52

(sign, exponent, significand)

double x, y

$x = -0.3$

$y = (\text{float}) x$  // will be cast back to double

---

double1: .double -0.3

l.d \$f0, double1

cvt.s.d \$f2, \$f0

cvt.d.s \$f4, \$f2



# MIPS Coprocessor 0 registers

Vaddr - where was bad address  
 Status - user? kernel?  
           R/W/ interruptable  
 Cause - overflow? bad address?  
 EPC - return address  
       (after exception resolved)  
 ;

## Example

; 0x00040070 0x00040074 0x00040078	 addiu \$s0, \$0, 1 sll \$s0, \$s0, 31 addu \$t0, \$s0, \$s0
---------------------------------------------	-----------------------------------------------------------------------

⇒ program crashes  
 (overflow error)

	<u>before</u>	<u>after</u>
Vaddr	0	0
Status	0x0000ff11	0x0000ff13
Cause	0	30
EPC	0	0x00400078

Details omitted.

30 means overflow error

```
addi $s0, $0, 8
addi $s1, $0, 0
div $s0, $s1
```

⇒ Same error (in MARS)

```
str: .asciiz "Hello"
      la $s0, str
      j  str
```

⇒ MARS assembler error

```
inst: la $s0, inst
      lw $t0, 0($s0)
```

	<u>before</u>	<u>after</u>
Vaddr	0	0x00400070
Status	0x0000ff11	0x0000ff13
Cause	0	10
EPC	0	0x00400078

## Floating point exceptions ?

- division by zero
- overflow  $2^{127} + 2^{127}$
- underflow  $2^{-127} \cdot 2^{-24}$
- issues with NaN

WHAT DOES MARS DO ?

## RECALL LECTURE 3

exponent code	exponent value
00000000	reserved
00000001	-126
00000010	-125
⋮	⋮
01111111	0
10000000	1
10000001	2
⋮	⋮
11111110	127
11111111	reserved

## RECALL LECTURE 3

Exponent code 11111111

if significant is all 0's

then value is  $\pm \infty$   
depending on sign bit

else value is "not a number"  
(NaN)

e.g. variable declared but  
not yet assigned a value

```
addi    $s0, $0, 1
sll     $s0, $s0, 30
mtc1    $s0, $f0
cvt.s.w $f0, $f0
mul.s   $f0, $f0, $f0
mul.s   $f0, $f0, $f0
mul.s   $f0, $f0, $f0
```

$\Rightarrow$   $\$f0 = +\infty$  (no exception)

## RECALL LECTURE 3

Exponent code 00000000

"denormalized" numbers

$\pm 0. \text{-----} \times 2^{-126}$

- belong to  $(-2^{-126}, 2^{-126})$
- includes 0

IEEE single precision floating  
point representation of 0

0 00000000 000000000000000000000000

```
mtc1    $0, $f0
```

# no need to convert

divide by 0

positive float: .float 13

l.s \$f0, positive float

mtcl \$0, \$f1

div.s \$f2, \$f0, \$f1

$\Rightarrow$  \$f2 =  $+\infty$

0/0

mtcl \$0, \$f1  
div.s \$f2, \$f1, \$f1

$\Rightarrow$  \$f2 = NaN