

[illegible]

Inst	Addr	CC 14	CC 15	CC 16	CC 17	CC 18	CC 19	CC 20	CC 21	CC 22	CC 23	CC 24	CC 25	CC 26	CC 27	CC 28	CC 29	CC 30	CC 31
inst 2	42, 42, 1	IF	ID	EX	MEM	WB													
subi 42, 42, 1			IF	ID	EX	MEM	WB												
lwi 42, 40, 1				IF	ID	EX	MEM	WB											
lwi 45, 40, 5					IF	ID	EX	MEM	WB										
ori 46, 46, 45						IF	ID	EX	MEM	WB									
lwi 42, 40, 6							IF	ID	EX	MEM	WB								
sll 46, 46, 1								IF	ID	EX	MEM	WB							
subi 42, 42, 1									IF	ID	EX	MEM	WB						
beg 42, 40, 1										IF	ID	EX	MEM	WB					
imp 12											IF	ID	EX	MEM	WB				
sll 46, 46, 1												IF	ID	EX	MEM	WB			
ori 42, 42, 1													IF	ID	EX	MEM	WB		
beg 42, 40, 1														IF	ID	EX	MEM	WB	

hmtz Vlk	CC 27	CC 28	CC 29	CC 30	CC 31	CC 32	CC 33	CC 34	CC 35	CC 36	CC 37	CC 38	CC 39	CC 40	CC 41	CC 42	CC 43	CC 44
imp 12	IF	ID	EX	MEM	WB													
sl 96,96,1		IF	ID	EX	MEM	WB												
mbi 92,92,1			IF	ID	EX	MEM	WB											
beg 92,90,1				IF	ID	EX	MEM	WB										
add 97,97,96					IF	ID	EX	MEM	WB									
ov 97,93,1						IF	ID	EX	MEM	WB								
lw 92,90,7							IF	ID	EX	MEM	WB							
HAHA								IF	ID	EX	MEM	WB						
done									IF	ID	EX	MEM	WB					
done										IF	ID	EX	MEM	WB				
done											IF	ID	EX	MEM	WB			
done												IF	ID	EX	MEM	WB		
done													IF	ID	EX	MEM	WB	

3 instructions were in parallel
 a verification was made
 instructions were in parallel

Paralel 2, un paralelismu
 paralelismu

Paralel 1