74LV1T34 Single supply translating buffer Rev. 1 — 28 November 2017

Product data sheet

General description

The 74LV1T34 is a single, level translating buffer. The low threshold inputs support 1.8 V input logic at V_{CC} = 3.3 V and can be used in 1.8 V to 3.3 V level up translation. In addition, the 5 V tolerant input pins enable level down translation (3.3 V to 2.5 V output at V_{CC} = 2.5 V). The output level is referenced to the supply voltage and supports 1.8 V, 2.5 V, 3.3 V and 5.0 V CMOS levels. The wide V_{CC} range permits the generation of output levels to connect to controllers or processors.

Features and benefits 2

- Single supply voltage translator at 1.8 V, 2.5 V, 3.3 V and 5.0 V
- Up translation
 - 1.2 V to 1.8 V at V_{CC} = 1.8 V
 - 1.5 V to 2.5 V at V_{CC} = 2.5 V
 - 1.8 V to 3.3 V at V_{CC} = 3.3 V
 - 3.3 V to 5.0 V at V_{CC} = 5.0 V
- Down translation
 - 3.3 V to 1.8 V at V_{CC} = 1.8 V
 - 3.3 V to 2.5 V at V_{CC} = 2.5 V
 - 5.0 V to 3.3 V at V_{CC} = 3.3 V
- 5 V tolerant inputs
- Latch-up performance exceeds 250 mA per JESD 78 Class II
- · ESD protection:
 - HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 2 kV
 - CDM JESD22-C101F exceeds 1 kV
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

Applications

- Portable applications
- · PC and notebooks
- Automotive
- Industrial controller
- Telecom



4 Ordering information

Table 1. Ordering information

Type number	Package	Package								
	Temperature range Name Description									
74LV1T34GW	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1						
74LV1T34GX	-40 °C to +125 °C	X2SON5	plastic thermal enhanced extremely thin small outline package; no leads; 5 terminals; body 0.8 X 0.8 X 0.35 mm	SOT1226						

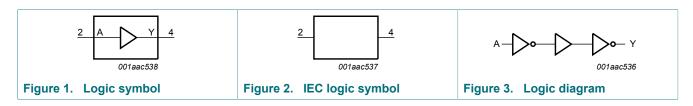
5 Marking

Table 2. Marking

Type number	Marking code ^[1]
74LV1T34GW	SQ
74LV1T34GX	SQ

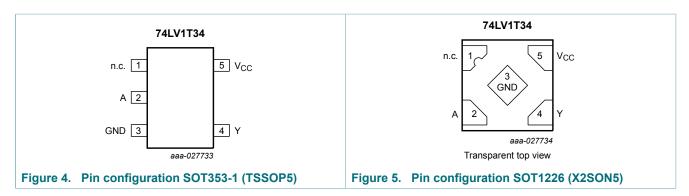
[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

6 Functional diagram



7 Pinning information

7.1 Pinning



7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
n.c.	1	not connected
A	2 data input	
GND	3	ground (0 V)
Υ	4	data output
V _{CC}	5	supply voltage

8 Functional description

Table 4. Function table [1]

Input	Output
A	Υ
L	L
Н	Н

[1] H = HIGH voltage level; L = LOW voltage level

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9 Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
VI	input voltage	[1]	-0.5	+7.0	V
V _O	output voltage	output HIGH or LOW state [2] [3]	-0.5	V _{CC} + 0.5	V
		output in power-off state [2]	-0.5	4.6	V
I _{IK}	input clamping current	V _I < 0 V	-20	-	mA
I _{OK}	output clamping current	$V_O < 0 \text{ V or } V_O > V_{CC}$	-	±20	mA
I _O	output current	V _O = 0 V to V _{CC}	-	±25	mA
I _{CC}	supply current		-	50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [4]	-	250	mW

^[1] If the input current ratings are observed, the minimum input voltage ratings may be exceeded.

10 Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{CC}	supply voltage		1.6	5.0	5.5	V
VI	input voltage		0	-	5.5	V
Vo	output voltage	output HIGH or LOW state	0	-	V_{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.8 V to 5.0 V	-	-	20	ns/V

^[2] If the output current ratings are observed, the output voltage ratings may be exceeded.

^[3] This value is limited to 7 V maximum.

^[4] For TSSOP5 packages: above 75 °C the value of P_{tot} derates linearly with 3.3 mW/K. For X2SON5 package: above 70 °C the value of P_{tot} derates linearly with 3.1 mW/K.

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11 Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °	C	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	Min	Max	
V _{IH}	HIGH-level	V _{CC} = 1.65 V to 1.8 V	0.94	-	1.0	-	1.0	-	V
	input voltage	V _{CC} = 2.0 V	0.99	-	1.03	-	1.03	-	V
		V _{CC} = 2.25 V to 2.5 V	1.135	-	1.18	-	1.18	-	V
		V _{CC} = 2.75 V	1.21	-	1.23	-	1.23	-	V
		V _{CC} = 3.0 V to 3.3 V	1.35	-	1.37	-	1.37	-	V
		V _{CC} = 3.6 V	1.47	-	1.48	-	1.48	-	V
		V _{CC} = 4.5 V to 5.0 V	2.02	-	2.03	-	2.03	-	V
		V _{CC} = 5.5 V	2.10	-	2.11	-	2.11	-	V
V _{IL}	LOW-level	V _{CC} = 1.65 V to 2.0 V	-	0.58	-	0.55	-	0.55	V
	input voltage	V _{CC} = 2.25 V to 2.75 V	-	0.75	-	0.71	-	0.71	V
		V _{CC} = 3.0 V to 3.6 V	-	0.80	-	0.65	-	0.65	V
		V _{CC} = 4.5 V to 5.5 V	-	0.80	-	0.80	-	0.80	V
V _{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL} ;							
		V _{CC} = 1.65 V to 5.5 V; I _O = -20 μA	V _{CC} -0.1	-	V _{CC} -0.1	-	V _{CC} -0.1	-	V
		V_{CC} = 1.65 V; I_{O} = -2 mA	1.28	-	1.21	-	1.21	-	V
		V _{CC} = 1.8 V; I _O = -2 mA	1.5	-	1.45	-	1.45	-	V
		V_{CC} = 2.3 V; I_{O} = -2.3 mA	2.0	-	2.0	-	2.0	-	V
		V_{CC} = 2.3 V; I_{O} = -3 mA	2.0	-	1.93	-	1.93	-	V
		V_{CC} = 2.5 V; I_{O} = -3 mA	2.25	-	2.15	-	2.15	-	V
		$V_{CC} = 3.0 \text{ V}; I_{O} = -3 \text{ mA}$	2.78	-	2.7	-	2.7	-	V
		V_{CC} = 3.0 V; I_{O} = -5.5 mA	2.6	-	2.49	-	2.49	-	V
		V_{CC} = 3.3 V; I_{O} = -5.5 mA	2.9	-	2.8	-	2.8	-	V
		V_{CC} = 4.5 V; I_{O} = -4 mA	4.2	-	4.1	-	4.1	-	V
		V _{CC} = 4.5 V; I _O = -8 mA	4.1	-	3.95	-	3.95	-	V
		V _{CC} = 5.0 V; I _O = -8 mA	4.6	-	4.5	-	4.5	-	V

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Symbol	Parameter	Conditions	25 °C		-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	Min	Max	
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL}							
	output voltage	V_{CC} = 1.65 V to 5.5 V; I_{O} = 20 μ A	-	0.1	-	0.1	-	0.1	V
		V _{CC} = 1.65 V; I _O = 2 mA	-	0.2	-	0.25	-	0.25	V
		V_{CC} = 2.3 V; I_{O} = 2.3 mA	-	0.1	-	0.15	-	0.15	V
		$V_{CC} = 2.3 \text{ V}; I_{O} = 3 \text{ mA}$	-	0.15	-	0.2	-	0.2	V
		$V_{CC} = 3.0 \text{ V}; I_{O} = 3 \text{ mA}$	-	0.1	-	0.15	-	0.15	V
		V_{CC} = 3.0 V; I_{O} = 5.5 mA	-	0.2	-	0.252	-	0.252	V
		V _{CC} = 4.5 V; I _O = 4 mA	-	0.15	-	0.2	-	0.2	V
		V _{CC} = 4.5 V; I _O = 8 mA	-	0.3	-	0.35	-	0.35	V
lı	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 0$ V to 5.5 V	-	±0.1	-	±1	-	±1	μA
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 1.8$ V, 2.5 V, 3.3 V, 5.0 V	-	1	-	10	-	10	μA
ΔI _{CC}	additional supply current	per input pin; V_{CC} = 1.8 V; V_I = 0.3 V or 1.1 V; I_O = 0 A; other pins at V_{CC} or GND	-	10	-	10	-	10	μA
		per input pin; V_{CC} = 5.5 V; V_I = 0.3 V or 3.4 V; I_O = 0 A; other pins at V_{CC} or GND	-	1.35	-	1.5	-	1.5	mA

12 Dynamic characteristics

Table 8. Dynamic characteristics

GND = 0 V. For test circuit, see Figure 7.

Symbol	Parameter	Conditions	-40 °C to +125 °C					
			Min	Typ 25 °C	Max 25 °C	Max 85 °C	Max 125 °C	
t _{pd}	propagation delay	A, B to Y; see Figure 6						
		V _{CC} = 1.8 V; C _L = 15 pF	-	6.3	9.4	10.6	11.4	ns
		V _{CC} = 1.8 V; C _L = 30 pF	-	7.4	10.5	12.0	12.8	ns
		V _{CC} = 2.5 V; C _L = 15 pF	-	4.5	6.4	7.2	7.8	ns
		V _{CC} = 2.5 V; C _L = 30 pF	-	5.3	7.2	8.2	8.9	ns
		V _{CC} = 3.3 V; C _L = 15 pF	-	3.7	5.2	5.9	6.3	ns
		V _{CC} = 3.3 V; C _L = 30 pF	-	4.3	5.9	6.8	7.1	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	3.1	3.9	4.3	4.5	ns
		V _{CC} = 5.0 V; C _L = 30 pF	-	3.6	4.5	4.9	5.2	ns
C _I	input capacitance	$V_I = V_{CC}$ or GND; $V_{CC} = 3.3 \text{ V}$	-	1.5	10	10	10	pF
Co	output capacitance	$V_O = V_{CC}$ or GND; $V_{CC} = 3.3 \text{ V}$	-	2.5	-	-	-	pF

74LV1T34

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Single supply translating buffer

Symbol Parameter		Conditions	-40 °C to +125 °C					
				Typ 25 °C	Max 25 °C	Max 85 °C	Max 125 °C	
C _{PD}	power dissipation capacitance	per buffer; V_I = GND to V_{CC} ; [2] C_L = 30 pF; f = 10 MHz						
		V _{CC} = 1.8 V	-	4.2	-	-	-	pF
		V _{CC} = 2.5 V	-	5.5	-	-	-	pF
		V _{CC} = 3.3 V	-	7.4	-	-	-	pF
		V _{CC} = 5.0 V	-	11.5	-	-	-	pF

 $\begin{tabular}{ll} [1] & t_{pd} is the same as t_{PLH} and t_{PHL}. \\ [2] & C_{PD} is used to determine the dynamic power dissipation (P_D in μW). \\ & $P_D = C_{PD}\,x\,V_{CC}^2\,x\,f_i\,x\,N + \sum(C_L\,x\,V_{CC}^2\,x\,f_o)$ where: } \end{tabular}$

f_i = input frequency in MHz;

fo = output frequency in MHz;

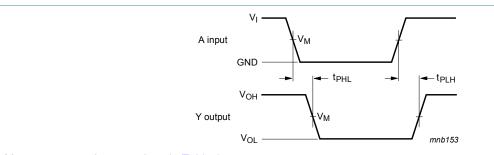
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\sum (C_L \times V_{CC}^2 \times f_0) = \text{sum of the outputs.}$

12.1 Waveforms and test circuit



Measurement points are given in Table 9.

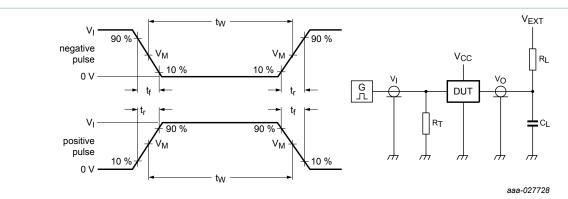
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 6. The input A to output Y propagation delays

Table 9. Measurement points

Input	Output
V _M	V_{M}
0.5V ₁	0.5V _{CC}

Single supply translating buffer



Test data is given in Table 10.

Definitions test circuit:

 R_T = Termination resistance should be equal to output impedance Z_0 of the pulse generator

C_L = Load capacitance including jig and probe capacitance

R_L = Load resistance

V_{EXT} = External voltage for measuring switching times

Figure 7. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	oly voltage Input			oltage Input Load V _E			V _{EXT}		
V _{CC}	VI	Δt/ΔV ^[1]	f _{max}	C _L	R _L	t _{PLH} , t _{PHL}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}	
1.8 V	V _{CC}	≤ 1.0 ns/V	15 MHz	15 pF, 30 pF	1ΜΩ	GND	GND	V _{CC}	
2.5 V	V _{CC}	≤ 1.0 ns/V	25 MHz	15 pF, 30 pF	1ΜΩ	GND	GND	V _{CC}	
3.3 V	3 V	≤ 1.0 ns/V	50 MHz	15 pF, 30 pF	1ΜΩ	GND	GND	V _{CC}	
5.0 V	3 V	≤ 1.0 ns/V	50 MHz	15 pF, 30 pF	1ΜΩ	GND	GND	V _{CC}	

[1] dV/dt ≥ 1.0 V/ns

13 Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm SOT353-1 detail X DIMENSIONS (mm are the original dimensions) D(1) E⁽¹⁾ Z⁽¹⁾ UNIT С ΗЕ Lp θ max. 0.30 0.25 1.35 2.25 0.46 0.60 0.1 1.0 2.25 0.15 0.65 0.425 mm 1.1 0.15 0.08 1.85 1.15

Note

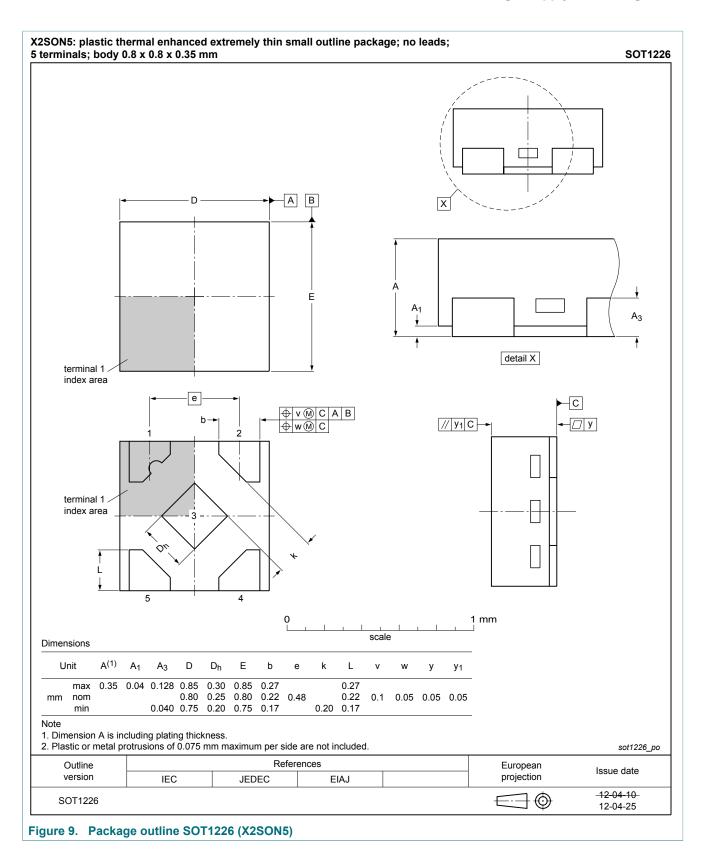
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN	ISSUE DATE
	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT353-1		MO-203	SC-88A			-00-09-01 03-02-19

Figure 8. Package outline SOT353-1 (TSSOP5)

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Single supply translating buffer



14 Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charge Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

15 Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV1T34 v.1	20171128	Product data sheet	-	-

16 Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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