Design of SRAM Cell Using Hybrid VLSI Techniques for Low Leakage and High Speed in Embedded Memories

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***Abstract*—A novel 10T SRAM architecture is proposed in this paper which operates in three modes (active, park, standby or hold). The main objective of the proposed architecture is to provide better stability and reduced delay in active mode, reduced leakage current in standby mode and retaining the logic state in park mode. Simulation results shows that the proposed SRAM is much better than conventional and other SRAM cells designed using hybrid techniques.**

Keywords— CMOS · SRAM cell · Low power · High speed · Subthreshold current

I. INTRODUCTION (*HEADING 1*)

The increasing demand of battery operated high speed portable digital system and implantable devices causes increase in need of supply voltage scaling and device scaling [1]. Supply voltage scaling causes the difference between supply voltage and transistor threshold voltage to be a very low value in modern SoC design [2]. This makes stability to reach a problematic zone and making it to be considered as an important factor during designing. Device scaling causes reduction in channel length, oxide thickness and threshold voltage (Vt) which leads to increase in drain induced barrier lowering (DIBL), Gate induced drain leakage (GIDL), and subthreshold current. When a CMOS circuit is in idle state there is still some leakage or static power dissipation due to the leakage current flowing through nominally OFF transistors [3]. CMOS logic gates have both NMOS and PMOS transistors, both of which dissipate finite reverse leakage and sub threshold currents. There are millions of transistors in a silicon chip and overall power dissipation due to leakage current is comparable to dynamic power dissipation. The main leakage current component in NMOS is the reverse-biased diode [4]. With increase in temperature, leakage current increases. In a chip, millions of transistors are fabricated and every transistor in the chip, constitutes the leakage current. In this case, the sum of all leakage currents then becomes significant. So it is necessary to reduce leakage power dissipation in VLSI circuits [5].

In this paper the proposed SRAM cell operates with less delay and high stability in active mode and with reduced leakage current in standby mode.

II. DESIGN OF PROPOSED SRAM CELL

Proposed SRAM cell was designed by combining TRIMODE MTCMOS power and ground gated techniques. The proposed SRAM cell consist of ten transistors in which four are high Vt transistors and six are low Vt transistors. High Vt transistors are slow, but have a low subthreshold leakage current and low Vt transistors are fast, but have a high subthreshold leakage current. The SRAM cell is implemented using low Vt transistors to perform fast operation and sleepy transistors were implemented using high Vt transistors to have low subthreshold leakage current. The proposed SRAM cell operates in three modes, active, park and standby mode. The schematic diagram of proposed SRAM cell using TRIMODE MTCMOS power and ground gated is shown in Fig. 1.

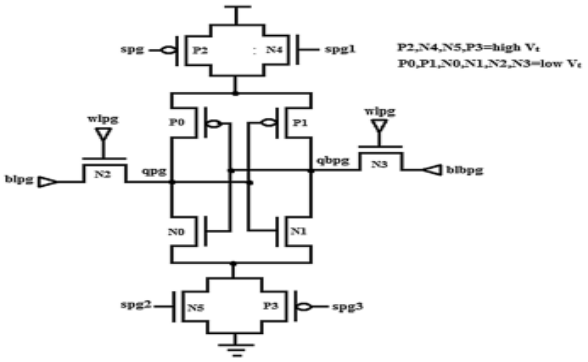

Fig. 1 Schematic diagram of proposed SRAM cell

III. SIMULATION RESULT

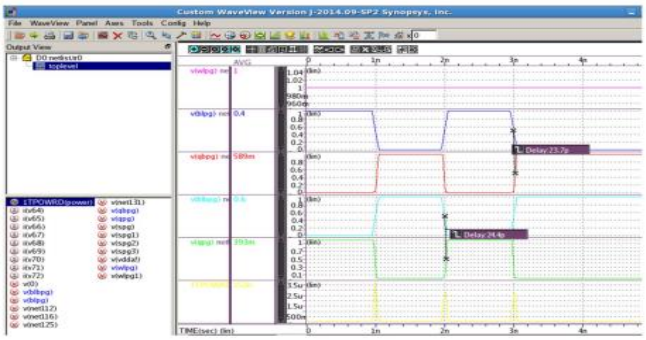

Fig. 2 Simulation result of proposed SRAM cell

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