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A modified bypass circuit for improved hot spot reliability of solar panels subject to partial shading

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ABSTRACT

A new bypass strategy for monocrystalline and polycrystalline solar panels allowing significant hot spot temperature reduction in both partial and full shading conditions is presented. The approach relies on a series-connected power MOSFET that subtracts part of the reverse voltage from the shaded solar cell, thereby acting as a voltage divider. Differently from other active bypass circuits, the proposed solution does not require either a control logic or power supply and can be easily substituted to the standard bypass diode. The operation of the new circuit is described with reference to the shading condition prescribed by the EN 61215 qualification procedure. Experiments performed on two commercial solar panels have shown that the shaded cell can be cooled up to 24 °C with respect to the case in which the standard bypass diode is adopted.

1. Introduction

One of the main concerns for the reliability of silicon solar panels (hereinafter also referred to as modules) is the possible occurrence of localized overheating (hot spot), which may induce accelerated aging (Manganiello et al., 2015) and, in severe cases, even irreversible malfunctioning. Hot spot formation is inherently related to the internal structure of solar panels, which are formed by tens of series-connected individual solar cells, each behaving as an independent current source; it is indeed well known that, when for whatever reason the current supplied by one cell is lower than the others, such a cell operates in reverse-bias mode and dissipates power. This occurrence is extremely frequent since it takes place every time a shadow partially covers the panel, thus reducing the corresponding photogenerated current. Whether or not the reverse biasing of a solar cell can be dangerous depends on the reverse current–voltage (I–V) characteristic of the inherent p–n junction (Moretón et al., 2015), which is impacted by two key parameters, namely, the breakdown voltage BV (assumed positive) and the shunt resistance R_{sh}. The breakdown voltage is the maximum allowed reverse voltage for the safe operation of the junction; approaching this voltage leads to a huge increase of the reverse current and eventually to device destruction. The shunt resistance describes undesired current paths through the inherent cell diode or along the cell edges, that is, it accounts for the non-ideal blocking properties of the junction; the current flow in the shunt resistance produces power dissipation and, consequently, cell heating. In both cases the reverse voltage appearing across the solar cell determines the amount of dissipated power and, hence, the temperature reached by the cell.

As will be recalled in the following sections, the maximum reverse voltage that can be found across one cell depends on the number of series-connected cells; in order to limit the reverse voltage to safe values, bypass diodes are antiparalleled to two or more panel subsections, hereinafter referred to as subpanels. As a common practice, a subpanel comprises about 20 elementary cells so that the maximum reverse voltage across one of them cannot exceed about $19 \times 0.6\ \text{V} = 11.4\ \text{V}$, where 0.6 V is the average voltage drop on forward-biased cells; this value should in principle be low enough to guarantee safe operation in reverse conditions (El Basri et al., 2015).

Before commercialization, the reliability of the solar module design is verified by means of the certification procedure performed according to the European Standard EN 61215 (Crystalline silicon terrestrial photovoltaic modules: design qualification and type approval), which verifies the hot spot tolerance by recreating the worst expected operating conditions (see next section) (Herrmann et al., 1997). In spite of that, hot spot failure is one of the most frequently reported phenomena limiting module lifetime (Review of Failures of Photovoltaic Modules, 2014; DeGraaff et al., 2011). This is due to a twofold reason. First, the actual reverse characteristics of cells embedded in a solar panel – in principle

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sharing identical nominal parameters – exhibit widely spread values for both BV (down to 10 V Kim and Krein, 2015) and shunt resistance (down to 20 Ω d'Alessandro et al., 2011a,b). Second, the qualification procedure EN 61215 is limited to few randomly selected panels; as a consequence, panels including anomalous solar cells are most likely to be present among the thousands often needed to build a solar plant. Moreover, some defects, like microcracks or delamination, occurring either during installation or during the operating life of the panel (Manganiello et al., 2015; Simon and Meyer, 2010) can affect the hot spot tolerance.

In the past, the increase in the number of bypass diodes (up to one diode for each cell) has been proposed as a possible solution (Suryanto Hasym et al., 1986; Chen, 2012); however, this approach has not encountered the favor of crystalline modules producers since it requires a not negligible technological cost and can be even detrimental in terms of power production when many diodes are conducting because of their power consumption (Daliento et al., 2009).

More recently, it has been shown that the distributed MPPT approach (Coppola et al., 2012) is beneficial for mitigating the hot spot in partially shaded modules with a temperature reduction up to 20 °C for small shadows (Solórzano and Egido, 2014); unfortunately, no advantages were found for totally obscured cells. On the other hand, methods to alleviate the hot spot in PV systems adopting centralized conversion schemes, which are still largely prevalent, are still lacking. In a recent paper (Kim and Krein, 2015) showing the "inadequateness" of the standard bypass diode, the insertion of a series-connected switch (also suggested in Guerriero et al. (2013, 2016), Di Napoli et al. (2015)) suited to interrupt the current flow during bypass events has been proposed; however, the this solution requires a quite complex electronic board that needs devised power supply and suitable control logic for activating the device.

This paper presents a simple bypass solution to appreciably reduce the reverse voltage across shaded cells, thus mitigating power dissipation and cell temperature. The approach is based on the adoption of a power MOSFET that sustains part of the reverse voltage, thus dissipating a portion of the power in the place of the shaded cells. Differently from Kim and Krein (2015), the functioning principle of the proposed approach is fully analog to that of a standard bypass diode, since it does not require either power supply or control logic. In the worst-case conditions, as defined by the EN 61215 discussed in the next section, a temperature reduction up to 24 °C has been achieved. The method is particularly suitable for reducing power dissipation in cells with unexpectedly low R_{sh} or BV; moreover, with respect to the results obtained in Solórzano and Egido (2014), it cools down even fully shaded cells.

The paper is organized as follows: Section 2 recalls the operation of the solar panels in partial shading conditions and illustrates the qualification procedure EN 61215; in Section 3, measurements of the reverse *I–V* curves of cells embedded in two commercial solar panels are reported; in Section 4, the new bypass approach is addressed and described; Section 5 illustrates the comparison between experiments carried out on solar panels either equipped with the proposed circuit or making use of the standard bypass diode; conclusions are drawn in Section 6.

2. Theoretical background

As outlined above, the hot spot occurrence is significantly related to the internal structure of a solar panel, the typical arrangement of which is reported in Fig. 1.

A solar panel is made by series-connected elementary cells, usually organized in multiples of about 20, forming subpanels (Silvestre et al., 2009; Guerriero et al., 2015) each equipped with

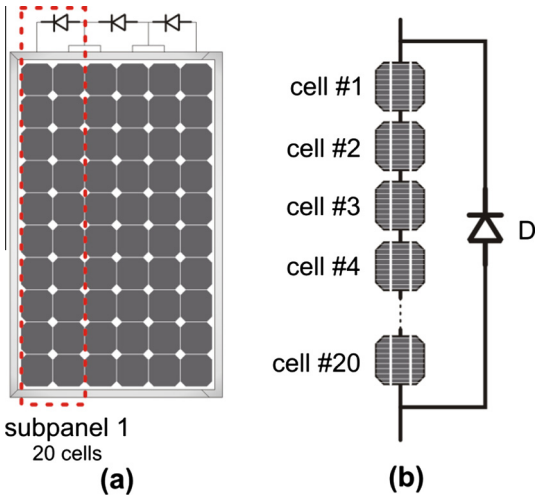

Fig. 1. (a) Sketch of a solar panel partitioned into 3 20-cell subpanels, each equipped with a bypass diode; the section corresponding to the first subpanel is highlighted; (b) simplified representation of an individual subpanel.

an antiparalleled bypass diode. If one or more cells are affected by shading or malfunctioning events that reduce their photogenerated current, these cells are most likely pushed into reverse-bias mode; in this case, the diode (i) plays a protection role, by mitigating the reverse voltage falling on them, and (ii) guarantees an alternative current path, thereby preventing a collapse of the power production. This scenario is schematically illustrated in Fig. 2, which shows the circuit representation of a subpanel, built as the series connection of one-diode cell models (d'Alessandro et al., 2015); the shunt resistances have been taken into account, because they strongly impact the operation in reverse-bias conditions, while, for the sake of simplicity, the series resistances have been neglected.

Whenever for some reason the current photogenerated by a solar cell is less than the others (in the example shown in Fig. 2 the photogenerated current corresponding to cell #1 is assumed zero) the excess current coming from other subpanels (equal to I_{string} in this case, if, in a first-order analysis, the current flow through R_{sh1} is disregarded) is forced to flow through the bypass diode D. As a consequence, the voltage across the whole subpanel coincides with the low voltage drop V_D across the forward-biased diode D (about 0.8–1 V for silicon diodes or 0.3–0.5 V for Schottky diodes depending on the excess current). Meanwhile, the other cells inside the subpanel cannot supply their photogenerated currents, because the series connection is broken by cell #1; hence, these currents are forced to flow through the corresponding intrinsic forward-biased diodes $D_{\#i}$, thus exhibiting a voltage drop V_F. As a consequence, a voltage given by $(N-1)\cdot V_F$ falls from node #1 to node #*N* (see Fig. 2). By applying the KLV, the reverse voltage V_R across the dark cell #1 can be evaluated as

$$V_R = (N-1)V_F + V_D \tag{1}$$

For a reliable design the number *N* should be chosen low enough to prevent V_R from exceeding BV.

The above analysis has been performed by neglecting the current flow through the shunt resistance of the shaded cell; in such a hypothesis the power dissipated by the cell would be zero (the cell does not conduct current) unless V_R approaches BV. In order to quantify the power dissipation occurring in real cells ($R_{sh} > 0\ \Omega$), the simple geometric construction (Manganiello et al., 2015) shown in Fig. 3 can be adopted.

This figure shows the *I–V* characteristic of a shaded cell (the slope in the reverse region depends on the shunt resistance) and

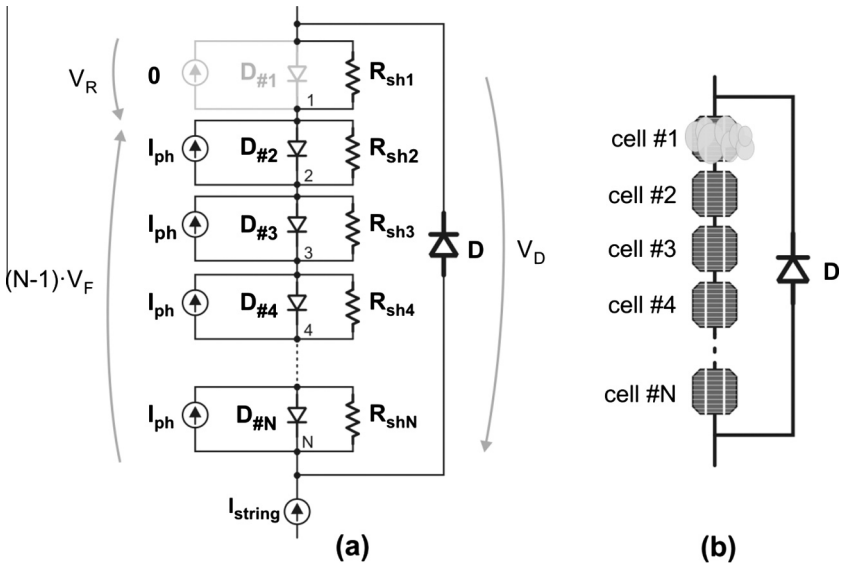

Fig. 2. (a) Equivalent circuit and (b) pictorial description of a subpanel comprising 20 cells. Cell #1 is assumed fully shaded.

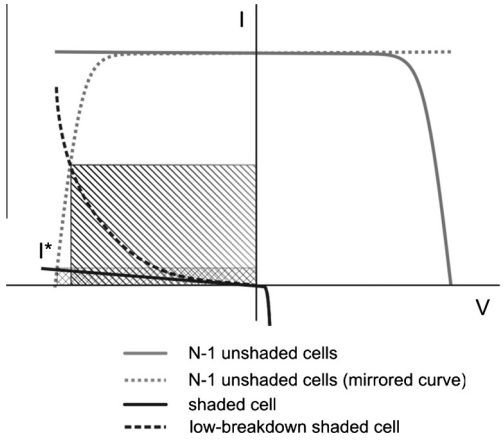

Fig. 3. Geometric approach to determine the power dissipation in a fully shaded cell: the I–V curve of the fully shaded cell (black solid line) is compared to the mirrored version (gray dashed line) of the I–V curve corresponding to the $N-1$ illuminated cells (gray solid line). The I–V curve of a fully shaded cell exhibiting low BV (black dashed line) is also shown to highlight the increase in power dissipation.

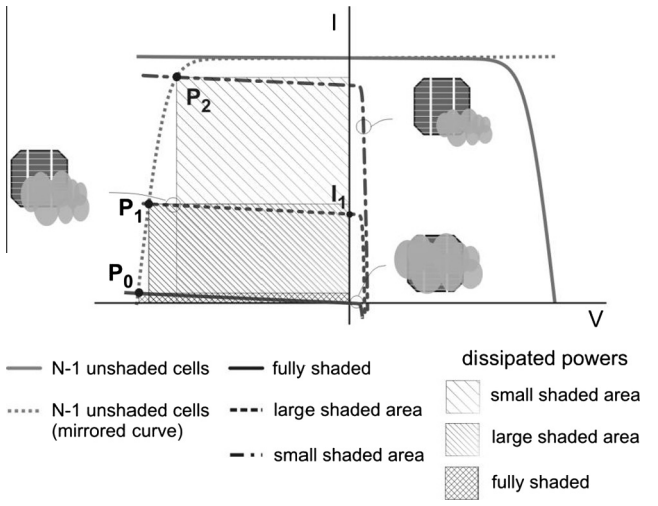

Fig. 4. Power dissipation vs. shaded area: the geometric approach determines the operating point P_1 of a cell with a large shaded area (black dashed line) with respect to point P_0 corresponding to a fully shaded cell (black solid line). The operating point P_1 identifies the power dissipation, while I_1 is the current photogenerated by the shaded cell. By reducing the shaded area (black dash-dotted line), the power dissipation grows up to the maximum value corresponding to the operating point P_2.

the I–V curve describing the series of the $N-1$ illuminated cells, which is also depicted as mirrored in the second quarter because, from the KLV, the positive voltage supplied by the illuminated cells appears as reverse voltage for the shaded one. Thus, the operating current of the system is given by the intercept value I^*, and the power dissipated by the shaded cell corresponds to the shaded area. It can be easily inferred that the power dissipation depends on the shunt resistance (besides depending on the shaded area, as will be shown later); in particular, a lower shunt resistance would entail a higher dissipation. A critical condition takes place when BV is lower than expected; in such a case, the reverse branch of the I–V curve may exhibit a sharp growth (Alonso-García and Ruíz, 2006), thus increasing the power dissipation in fully shaded cells. Given the almost exponential shape of the I–V curve in that region, it is clear that an even small reduction in the reverse voltage could offer great benefits in terms of dissipated power. In Section 3, experiments performed on two solar modules (monocrystalline and polycrystalline, respectively) show that the occurrence of low-R_{sh} cells is not rare.

It is worth recalling that the qualification procedure EN 61215 identifies as "critical" cell the one exhibiting the highest shunt resistance; this definition originates from the fact that the dissipated power also depends on the shaded area, as schematically illustrated in Fig. 4.

This figure shows what happens when the shadow does not cover the entire cell so that partial photogeneration (given by current I_1) occurs. The I–V curve of the partially shaded cell can be obtained by simply translating upward the I–V curve of the dark cell. As I_1 is lower than the current supplied by fully illuminated cells, also the partially shaded cell is reverse biased and its operating point P_1 lies in the second quarter. Although the reduction of the shaded area could in principle be associated to "better" conditions, it is evident that the power dissipation increases with respect to the case of a fully shaded cell. By further reducing the shaded area the operating point of the shaded cell moves toward

higher currents so that power dissipation increases. For each given shunt resistance a specific shaded area exists such that the maximum power producible by illuminated cells is dissipated over the shaded cell (P_2 in Fig. 4); an additional decrease in the shaded area would instead reduce the power dissipation. The above description explains why a high quality cell (very high shunt resistance) can be subject to dramatically high dissipation induced by even small shadows (bird dropping, leafs, etc.). EN 61215 prescribes that in such a condition the solar panel must work for at least five hours without damages.

3. Measurements of the reverse characteristics of solar cells

The previous section showed that the power dissipation over shaded cells depends on the shape of the reverse branch of *I–V* curves. In order to correctly interpret thermal measurements performed on solar panels, the reverse characteristics of individual cells embedded in the solar panels under test were preliminarily measured by means of the following simple procedure (d'Alessandro et al., 2011a). Let us consider a solar panel with only one cell fully obscured (cell #1 in Fig. 5a). In this case, the *I–V* characteristic of the whole panel is shaped as shown in Fig. 5b. The thick portion of the curve almost corresponds to the reverse branch of cell #1, this observation coming from the fact that in such a voltage range all bypass diodes are off and the current supplied by the solar panel is limited by the shaded cell. As a consequence, the shunt resistance of the shaded cell can be extracted from the slope of the thick portion of the *I–V* characteristic of the panel.

This method was applied to extract the shunt resistances of intentionally obscured solar cells embedded in two commercial monocrystalline and polycrystalline solar panels, the nominal parameters of which are summarized in Table 1; such an evaluation was performed with the aim of establishing a "quality ranking" among the cells. The *I–V* curves measured by fully shading one cell at a time are reported in Fig. 6; the insets show the "best" (cell #39 and cell #17) and the "worst" (cell #36 and cell #7) cells in terms of shunt resistance. The main, quite surprising, result is the large spread of R_{sh} among cells belonging to the same panel: the shunt resistances extracted from the slopes of the curves lie in the range 17–250 Ω for the monocrystalline panel and 14–60 Ω for the polycrystalline one. This will lead to important consequences from the point of view of the behavior in reverse bias conditions, as will be shown in Section 5.

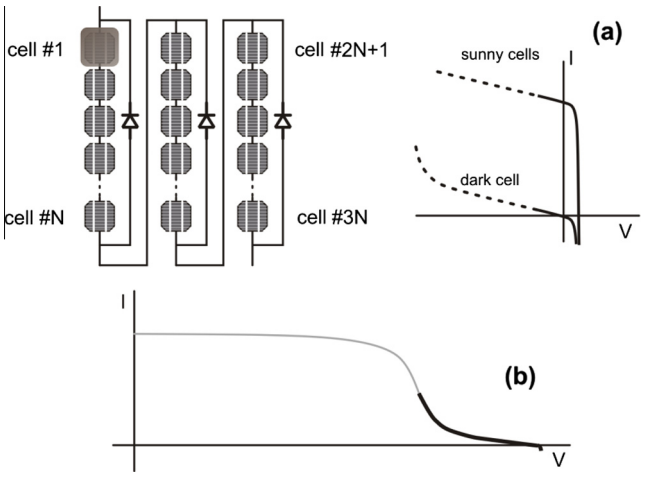

Fig. 5. Shunt resistance extraction method: (a) schematic representation of a PV panel formed by three *N*-cells subpanels, with fully shaded cell #1; (b) comparison between the *I–V* curve of the dark cell #1 with the one of a sunny cell; (c) *I–V* curve of the whole panel, the thick portion of which almost coincides with the reverse branch of the shaded cell.

4. Bypass approach for reverse voltage mitigation

As illustrated in Section 2, the reverse voltage across shaded solar cell(s) is given by the sum of the forward voltages across sunny cells plus the forward voltage across the bypass diode. In order to lower the reverse voltage and, consequently, the dissipated power and the overheating, we propose the improved bypass approach shown in Fig. 7a, which exploits a power MOSFET M connected in series with the subpanel and an ordinary bypass diode connected across the series formed by the subpanel plus M. As will be clarified shortly, the role of M is to share part of the voltage supplied by the sunny cells during bypass conditions, thus lowering the reverse voltage across the shaded cell(s), while negligibly affecting the operation of the solar panel during normal functioning. The key point is that M behaves as an almost ideal short circuit when the gate–source voltage V_{GS} is high, while it exhibits a significant drain–source voltage drop V_{DS} when V_{GS} is low. Fig. 7 witnesses that V_{GS} coincides with the voltage supplied by the subpanel (i.e., $V_{GS} = V_{subpanel}$). Hence, when the subpanel is sunny (Fig. 7b), so that $V_{subpanel}$ is high, M is pushed into deep linear region, and the string current I_{string} ($=I_{subpanel}$) flows through M while the bypass diode D is off. By suitably choosing a low-$R_{DS,on}$ MOSFET, the power reduction of the subpanel due to the increase in the series resistance can be limited to tens of mW. Experiments reported in Section 5 show that a voltage drop V_{DS} as low as 50 mV appears across the MOSFET when the solar panel is in sunny conditions. In the worst case of only one shaded solar cell, D turns on, the current flowing through M decreases and its operating point moves toward a higher voltage V_{DS}, which is in turn subtracted from the reverse voltage across the shaded cell. In other terms, according to Fig. 7c, (1) modifies in

$$V_R = (N-1)V_F + V_D - V_{DS} \quad (2)$$

This implies that the presence of M reduces the power dissipation across the solar cell and, hence, its temperature; obviously the subtracted power is dissipated by M, but the reliability concern is conveniently moved from the panel to an external device particularly suited for high temperature operation, which may in principle survive during the whole lifetime of the panel. The power production of the panel is negligibly impacted by the proposed solution, since an appreciable current reduction might take place only for a panel voltage inducing $V_{subpanel} \approx V_{DS}$ (that is, the series composed by subpanel and MOSFET is almost in short-circuit conditions), which is however far away from the voltage corresponding to the maximum power point.

Table 1
Nominal parameters of the panels under test.

	M54050	MF120EC3
Manufacturer	ET Solar	Mitsubishi El.
Technology	Mono-Si	Poly-Si
V_{MPP}[a]	20.2 V	17.6 V
I_{MPP}[a]	2.48 A	6.84 A
P_{MPP}[a]	50 W	120 W
V_{oc}[a]	24.6 V	22.0 V
I_{sc}[a]	2.81 A	7.36 A
Efficiency[a]	12.5%	13%
FF[a]	72%	74%
Number of cells	40	36
Number of subpanels (bypass diodes)	2	2

[a] Measured @ STC.

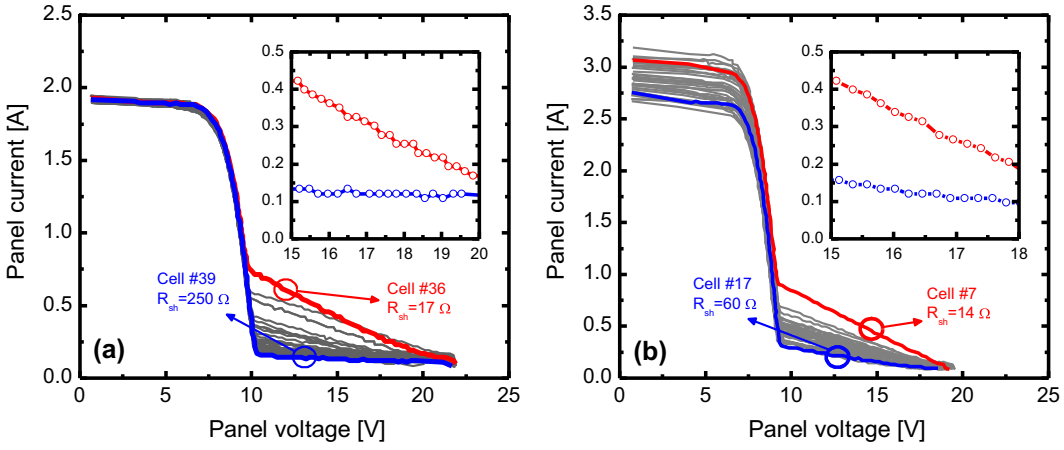

Fig. 6. *I–V* curves corresponding to the (a) monocrystalline and (b) polycrystalline panels under test. The curves were traced by fully obscuring one cell at a time to determine the shunt resistance of the dark cell. The characteristics corresponding to the "best" (blue line) and the "worst" (red line) cell are magnified and reported in the insets. The polycrystalline panel was measured under rapidly changing weather conditions. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

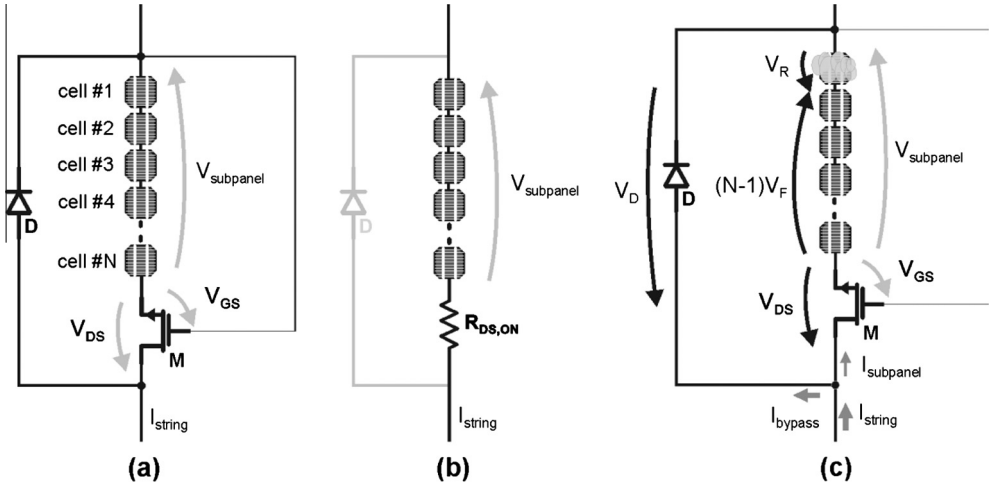

Fig. 7. (a) Schematic diagram of the proposed bypass strategy; operation under (b) sunny and (c) shading (bypass) conditions.

It must be remarked that integrated smart MOSFET-based bypass systems (e.g., Bauwens and Doutreloigne, 2014) ensuring $V_{subpanel} \rightarrow 0$ V in bypass conditions would lead only to $V_R = (N-1) \cdot V_F$, which can be obtained from (1) with $V_D = 0$ V; in addition, they require power supply and control logic.

Lastly, it must be noted that the proposed strategy works properly up to almost zero subpanel current (fully obscured solar cell).

The voltage V_{DS} falling on the power MOSFET can be quantified by resorting to the geometrical construction illustrated in Fig. 8, which shows the I_D–V_{DS} characteristics (I_D is the drain current coinciding with $I_{subpanel}$) of the same transistor exploited for the experiments reported in Section 5.

The working regions of the MOSFET can be identified as follows. The pinch-off curve is reported, which is described by the condition $V_{DS} = V_{GS} - V_{th}$, where V_{th} is the threshold voltage of the device. When the solar panel is fully illuminated (Fig. 7a), the operating point is forced into deep linear region (on the left of the pinch-off curve) and the voltage drop V_{DS} across the MOSFET is very low (tens of mV). In order to understand what happens in shading conditions, where the bypass diode turns on (Fig. 7b), let us first consider the ideal condition of zero voltage drop across the diode ($V_D = 0$ V). In this case, as can be seen from Fig. 7b, V_{DS} coincides with $V_{GS} = V_{subpanel}$; therefore the operating points will

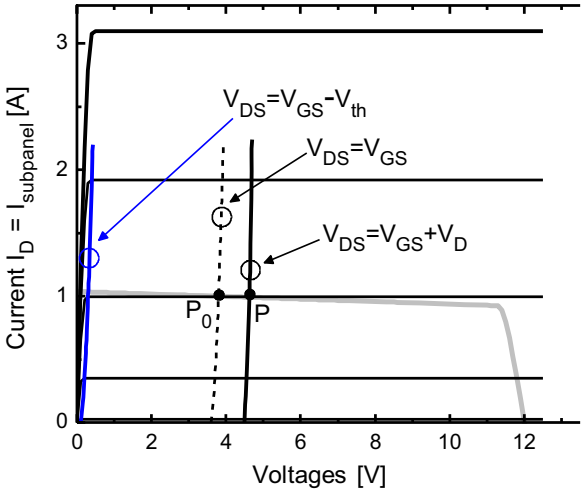

Fig. 8. I_D–V_{DS} curves of the power MOSFET exploited for the experiments. The different *loci* of points corresponding to the operating conditions of the device are reported: the blue line is the pinch-off curve, i.e., the edge between the linear and pinch-off regions; the black dashed line is the *locus* during bypass operation in the assumption of $V_D = 0$ V; the black solid line is the *locus* when the voltage drop across the diode is taken into account; the gray solid line is the *I–V* characteristic of the shaded subpanel.

lie on the $V_{DS} = V_{GS}$ curve, which can be obtained by simply shifting by V_{th} the $V_{DS} = V_{GS} - V_{th}$ curve. By considering that the voltage drop across the diode is not zero, a further rightward shift by V_D of such a curve must be accounted for; thus, the operating points in bypass conditions will lie on the curve $V_{DS} = V_{GS} + V_D$, which can be adjusted by properly choosing the threshold voltage of the MOSFET, and obviously depend on the current supplied by the subpanel that acts as a load for the transistor. Based on such considerations, we conduct a practical analysis by reporting the $I_{subpanel}$–$V_{subpanel}$ characteristic of a shaded subpanel (with short-circuit current $I_{sc} = 1$ A) in the I_D–V_{DS} plane, which can be done in the ideal case of $V_D = 0$ V. The operating point of the MOSFET will be given by the intercept P_0 of the characteristic of the panel with the $V_{DS} = V_{GS}$ curve. In order to restore the voltage drop $V_D > 0$ V, this point is to be translated rightward (for the same current) to P on the $V_{DS} = V_{GS} + V_D$ curve. As V_{DS} is subtracted from the solar cell reverse voltage, a significant reduction of power dissipation can be obtained.

It should be remarked that the proposed approach results in some additional cost compared to a traditional bypass strategy, especially if discrete power MOSFETs are used. In this paper we did not perform a detailed analysis of such costs, which should include re-designing of the junction box. Nevertheless such a mandatory analysis can be well done by potentially interested module manufacturers. On the other hand, an efficient and cheaper solution would involve the adoption of a 3-terminal integrated circuit embedding both the power MOSFET and the bypass diode (the drain and gate being short-circuited with anode and cathode, respectively), simply mounted in place of the standard diode; in this case the additional cost is expected to be negligible.

5. Experiments

Experiments were carried out on the two solar panels already described in Table 1. Power MOSFETs IRFZ44V (Datasheet) were exploited. According to the connections illustrated in Fig. 7, solar panels were equipped with the novel solution by substituting their bypass diodes at a subpanel level. Measurements were conducted either with the traditional bypass diode or with the proposed approach. Similar to Spagnolo et al. (2012), the temperature distribution was monitored through an IR camera HT THT70 with 384×288 pixels resolution; thermographic images were converted into temperature maps by applying a proper RGB-to-Grayscale algorithm. An accuracy test was conducted by comparing the temperature detected through the IR camera to that measured by a thermocouple. Measurements were performed by obscuring either the "best" or the "worst" cell (i.e., the ones with the highest and lowest shunt resistance, respectively) of the panels. Both partial and full shading conditions were considered.

The results of the first experiment concerning the monocrystalline module are reported in Fig. 9. The "best" cell (#39) was partially covered with an adhesive tape. The solar panel was series connected in an 1 kW string, the operating point of which was adjusted by means of an electronic load in order to drive the shaded panel in bypass mode. In such a condition the shaded cell becomes reverse biased and a hot spot arises; the shaded area was chosen to achieve the maximum dissipated power (point P_2 in Fig. 4 corresponding to about 22 W). Fig. 9b shows the thermographic image acquired when the subpanel was protected by the standard bypass diode; in this case, the temperature reached by the cell was about 93 °C. Fig. 9c refers to the same operating conditions but with the proposed bypass approach. It is found that the maximum temperature over the shaded cell reduces to 73 °C, a much safer value. The voltage drop V_{DS} measured across the MOSFET was 4.4 V, which means that about 1/3 of the voltage supplied by the subpanel was subtracted from the reverse biased cell.

An analogous experiment was performed by partially obscuring the "worst" cell (#36) of the panel. Again the shaded area was adjusted to maximize power dissipation (a larger area is needed in this case). Results are reported in Fig. 10, which shows the photo of the shaded panel, the thermographic image achieved by adopting the standard bypass diode, and the image corresponding to the adoption of the new bypass approach. As expected, the maximum temperature reached when the subpanel is protected by the standard diode is almost equal (92 °C) to the previous case since the same power was dissipated by the cell. Conveniently, the proposed solution allowed a slightly higher reduction of the maximum cell temperature, which was measured to be about 68 °C. This result is a consequence of the higher slope of the reverse I–V curve, which leads to a stronger reduction of the current when the reverse voltage is reduced by the same amount.

A further experiment was performed by fully obscuring cell #36 (cell #39 was tested as well, yet results very similar as #36 were obtained and are omitted here for the sake of brevity). As shown in Fig. 11, unlike the previous cases, thermographic images are taken from the backside of the solar panel since the front is covered by the shield. The obtained image is really interesting (Geisemeyer et al., 2014) because it shows that the temperature increase

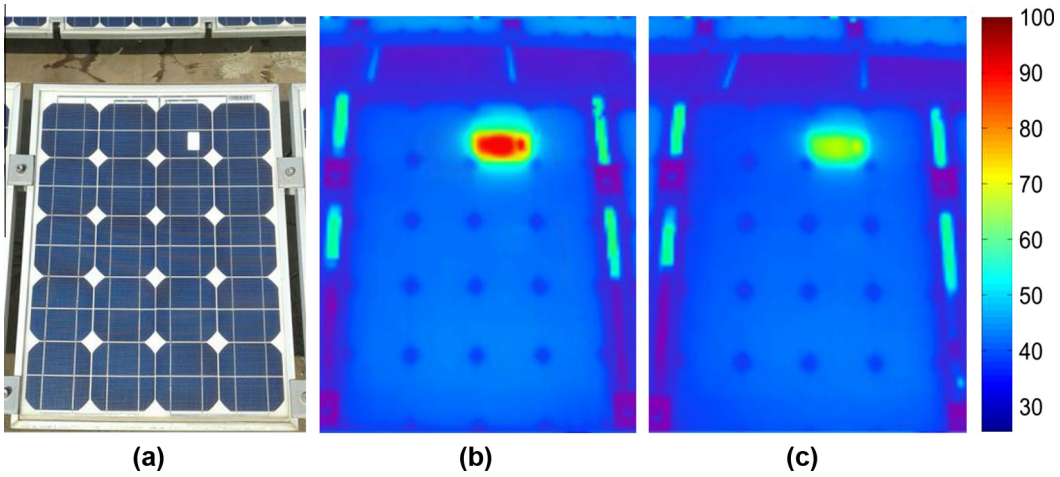

Fig. 9. (a) Photo of the monocrystalline panel under test; the "best" cell #39 (higher shunt resistance) is shaded with a tape with area suited to maximize the power dissipation; thermographic images corresponding to (b) the traditional bypass diode and (c) the proposed bypass circuit.

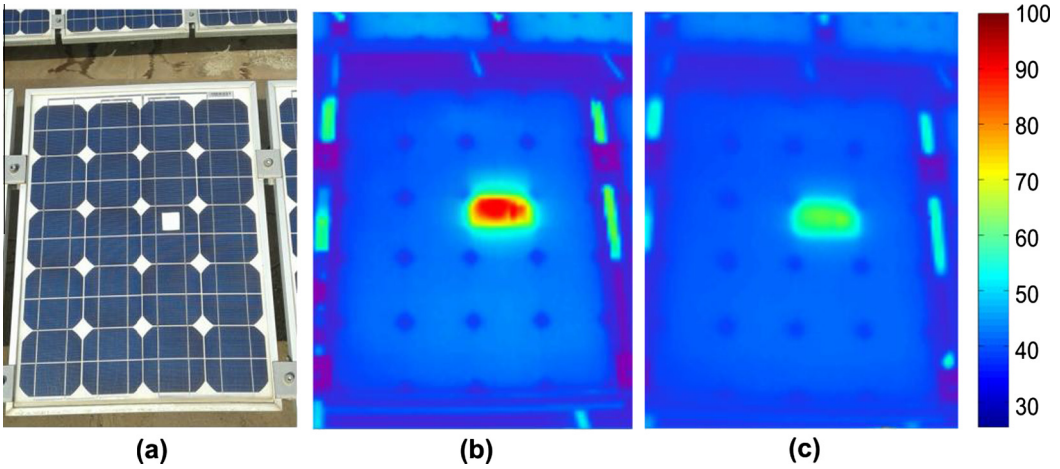

Fig. 10. (a) Photo of the monocrystalline panel; the "worst" cell #36 (lowest shunt resistance) is shaded with a tape with a proper area that maximizes the power dissipation; thermographic images corresponding to (b) the traditional bypass diode and (c) the proposed bypass circuit.

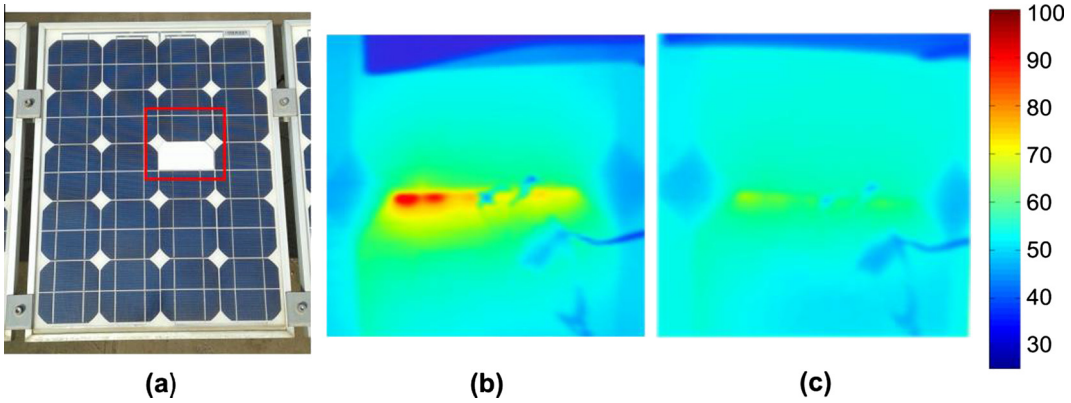

Fig. 11. (a) Photo of the monocrystalline module with the "worst" cell #36 fully shaded; (b) thermographic images or the panel rear corresponding to (b) the standard bypass diode and (c) the proposed bypass solution.

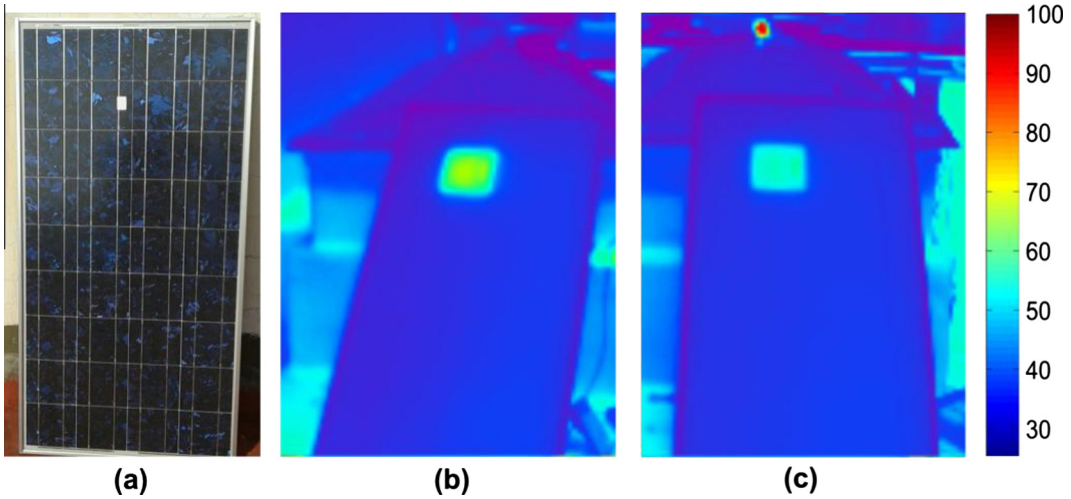

Fig. 12. (a) Photo of the polycrystalline panel; the "best" cell #17 (highest shunt resistance) is shaded with the same tape used for the analysis described in Fig. 9; thermographic images taken for the panel equipped with (b) the traditional bypass diode and (c) the proposed bypass approach.

focalizes in a small region along the edge of cell, thus indicating the presence of a well defined shunt current path, likely related to the surface recombination velocity (Daliento et al., 2007). Again the effectiveness of the proposed approach is evident, since the maximum temperature is reduced from 93 °C to 61 °C.

The same measurements were repeated for the polycrystalline module described by the *I–V* curves shown in Fig. 6b. Here we report only one set of images, which clearly highlights the essence of the novel approach. The experiment shown in Fig. 12 was performed by partially obscuring the "best" cell #17 with the same

tape adopted for the analysis in Fig. 9. The novel bypass solution allows a temperature reduction from 69 °C to 52 °C. It must be remarked that the temperature corresponding to the traditional bypass (69 °C) was lower than the one obtained for the monocrystalline module (93 °C) for a twofold reason: (i) the shunt resistance of the "best" cell is much lower than the monocrystalline counterpart (R_{sh} = 60 Ω instead of 250 Ω), while the shaded area was identical; consequently, this area is too small compared to the one that forces the maximum dissipated power; (ii) to a lesser extent, the number of sunny cells in the subpanel is lower (17 instead of 19). What it is interesting to note is the red[1] spot in the upper part of Fig. 12c, which corresponds to the MOSFET dissipating the excess power subtracted from the solar cell; this emphasizes that, as outlined before, the power dissipation is partially brought outside the panel, thus transferring reliability issues from the solar panel to a specifically designed device.

6. Conclusions

In this paper, an improved bypass approach based on a power MOSFET and a diode has been proposed, which can be applied to any solar module partitioned into subpanels composed by series-connected cells. The solution allows a significant reduction of the hot spot temperature when a solar panel is subject to partial shading by transferring part of the reverse voltage supplied by well-illuminated cells to the MOSFET, which is connected in series with each subpanel. The approach has been experimentally verified by comparing its performance with a standard bypass diode. Thermographic images acquired on monocrystalline and polycrystalline solar panels impacted by heavily-stressing partial shading conditions have showed a temperature reduction up to about 24 °C and 20 °C in shaded solar cells characterized by low and high shunt resistances, respectively. In experiments performed by fully obscuring a solar cell, the temperature has instead been lowered by 32 °C.

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[1] For interpretation of color in 'Figs. 9–12', the reader is referred to the web version of this article.