

REGRESSION ANALYSIS AND COVERAGE CLOSURE

Running Regression and Mapping Coverage Results to Cadence vPlanner

vManager					Regression	Analysis	Planning	Tracking
vPlan Hierarchy					Analyze			
CSCE 714 Project Spring2025					Runs			
Item Name	Overall Average Grade	Overall Covered	Assertion Status					
CSCE 714 Project Spring2025	97.74%	11945 / 15443 (77.35%)	100%					
1 Multi-Core Design	97.74%	11945 / 15443 (77.35%)	100%					
1.1 CPU to LVI Cache interface	98.84%	202 / 222 (90.99%)	100%					
1.1.1 Assertions_slash_Checkers for CPU Interface	100%	24 / 24 (100%)	100%					
1.1.2 Assertions for CPU APB Interface	88.37%	152 / 172 (88.37%)	100%					
1.1.3 Five_trans_test	100%	1 / 1 (100%)	n/a					
1.1.4 read_hit_shared	100%	1 / 1 (100%)	n/a					
1.1.5 Assertion_no_simultaneous_cpu_rd_wr	100%	4 / 4 (100%)	100%					
1.1.6 Assert_cpu_wr_done	100%	4 / 4 (100%)	100%					
1.1.7 Assert_read_hit_produces_data	100%	4 / 4 (100%)	100%					
1.1.8 Assert_data_in_bus_cpu_rd	100%	4 / 4 (100%)	100%					
1.1.9 Assert_data_bus_legal	100%	4 / 4 (100%)	100%					
1.1.10 Assert_addr_bus_legal	100%	4 / 4 (100%)	100%					
1.2 LVI Cache to BUS_slash_LV2_slash_Mem interface	100%	17 / 17 (100%)	100%					
1.2.1 write_hit_me_dcache	100%	1 / 1 (100%)	n/a					
1.2.2 write_hit_shared_pass	100%	1 / 1 (100%)	n/a					
1.2.3 Assert_proc_req_before_gnt	100%	4 / 4 (100%)	100%					
1.2.4 Assert_snoop_req_before_gnt	100%	4 / 4 (100%)	100%					
1.2.5 Assert_bus_req_for_lv2_rd	100%	4 / 4 (100%)	100%					
1.2.6 Assert_snoop_response_must_set_shared_or_wb	100%	1 / 1 (100%)	100%					
1.2.7 Assert_lv2_req_before_gnt	100%	1 / 1 (100%)	100%					
1.2.8 Assert_read_response	100%	1 / 1 (100%)	100%					
1.3 LVI dcache as a R_slash_W memory	100%	4 / 4 (100%)	n/a					
1.3.1 Read_hit_shared	100%	1 / 1 (100%)	n/a					
1.3.2 sequential_rw_dcache	100%	1 / 1 (100%)	n/a					
1.3.3 write_hit_me_dcache	100%	1 / 1 (100%)	n/a					
1.3.4 Random_stress_test	100%	1 / 1 (100%)	n/a					
1.4 LVI icache as a R-only memory	100%	2 / 2 (100%)	n/a					
1.4.1 Read_miss_icache	100%	1 / 1 (100%)	n/a					
1.4.2 Read_miss_dcache	100%	1 / 1 (100%)	n/a					
1.5 LVI dcache LRU functionality	100%	5 / 5 (100%)	n/a					
1.5.1 Fill_cache_way	100%	1 / 1 (100%)	n/a					
1.5.2 Lru_random_reads	100%	1 / 1 (100%)	n/a					
1.5.3 Lru_eviction	100%	1 / 1 (100%)	n/a					
1.5.4 Lru_shared_conflict	100%	1 / 1 (100%)	n/a					
1.5.5 Fill_all_way_all_core	100%	1 / 1 (100%)	n/a					
1.6 LVI icache LRU functionality	100%	1 / 1 (100%)	n/a					
1.6.1 Fill_cache_set_il	100%	1 / 1 (100%)	n/a					
1.7 LVI dcache MESI FSM	100%	11 / 11 (100%)	100%					
1.7.1 Assert_invalidate_on_shared_write_hit	100%	1 / 1 (100%)	100%					
1.7.2 Read_hit_shared	100%	1 / 1 (100%)	n/a					
1.7.3 modified_to_shared	100%	1 / 1 (100%)	n/a					
1.7.4 write_hit_me_dcache	100%	1 / 1 (100%)	n/a					
1.7.5 write_hit_shared	100%	1 / 1 (100%)	n/a					
1.7.6 MESI_Transition_IEM	100%	1 / 1 (100%)	n/a					
1.7.7 MESI_Downgrade	100%	1 / 1 (100%)	n/a					
1.7.8 MESI_Shared_invalidation	100%	1 / 1 (100%)	n/a					
1.7.9 Assert_invalidation_done_after_invalidate	100%	1 / 1 (100%)	100%					
1.7.10 assert_invalidation_done_after_invalidate	100%	1 / 1 (100%)	100%					
1.7.11 Multicore_stress_test	100%	1 / 1 (100%)	n/a					

vManager				Regression	Analysis	Planning	Tracking
<div> <div>All Vplan</div> <div> <div>Run</div> <div>Run Query</div> <div>Metrics</div> <div>Tests</div> <div>vPlan</div> <div>Relax vPlan</div> <div>Relax Coverage</div> <div>Refresh Run</div> <div>New vPlan</div> <div>Edit vPlan</div> <div>Save</div> <div>Expression</div> <div>Toggle</div> <div>Statement</div> <div>File</div> <div>Code View</div> <div>Assertion</div> <div>Instance</div> <div>Analyze Run</div> <div>Correlate Run</div> <div>Run</div> <div>Save Coverage Run</div> <div>Run</div> <div>Re-run</div> <div>Exclude</div> <div>Exclude Covered</div> <div>Exclude Uncovered</div> </div> </div>							
Views				Context Operations			
vPlan Hierarchy				Analyze			
CSCE 714 Project Spring2025							
Id	Name	Overall Average Grade	Overall Covered	Assertion Status			
	1.2.8 Assert_read_response	100%	1 / 1 (100%)	100%			
	1.3 L1 dcache as a R_slash_W memory	100%	4 / 4 (100%)	n/a			
	1.3.1 Read_hit_shared	100%	1 / 1 (100%)	n/a			
	1.3.2 sequential_rw_dcache	100%	1 / 1 (100%)	n/a			
	1.3.3 write_hit_me_dcache	100%	1 / 1 (100%)	n/a			
	1.3.4 Random_stress_test	100%	1 / 1 (100%)	n/a			
	1.4 L1 icache as a R-only memory	100%	2 / 2 (100%)	n/a			
	1.4.1 Read_miss_icache	100%	1 / 1 (100%)	n/a			
	1.4.2 Read_miss_dcache	100%	1 / 1 (100%)	n/a			
	1.5 L1 dcache LRU functionality	100%	5 / 5 (100%)	n/a			
	1.5.1 Fill_cache_way	100%	1 / 1 (100%)	n/a			
	1.5.2 Lru_random_reads	100%	1 / 1 (100%)	n/a			
	1.5.3 Lru_eviction	100%	1 / 1 (100%)	n/a			
	1.5.4 Lru_shared_conflict	100%	1 / 1 (100%)	n/a			
	1.5.5 fill_all_way_all_core	100%	1 / 1 (100%)	n/a			
	1.6 L1 icache LRU functionality	100%	1 / 1 (100%)	n/a			
	1.6.1 fill_cache_set_i	100%	1 / 1 (100%)	n/a			
	1.7 L1 dcache MESI FSM	100%	11 / 11 (100%)	100%			
	1.7.1 Assert_invalidate_on_shared_write_hit	100%	1 / 1 (100%)	100%			
	1.7.2 Read_hit_shared	100%	1 / 1 (100%)	n/a			
	1.7.3 modified_to_shared	100%	1 / 1 (100%)	n/a			
	1.7.4 write_hit_me_dcache	100%	1 / 1 (100%)	n/a			
	1.7.5 write_hit_shared	100%	1 / 1 (100%)	n/a			
	1.7.6 MESI_Transition_IEM	100%	1 / 1 (100%)	n/a			
	1.7.7 MESI_Downgrade	100%	1 / 1 (100%)	n/a			
	1.7.8 MESI_Shared_invalidation	100%	1 / 1 (100%)	n/a			
	1.7.9 Assert_invalidation_done_after_invalidate	100%	1 / 1 (100%)	100%			
	1.7.10 assert_invalidation_done_after_invalidate	100%	1 / 1 (100%)	100%			
	1.7.11 Multicore_stress_test	100%	1 / 1 (100%)	n/a			
	1.8 L2 LRU functionality	100%	1 / 1 (100%)	n/a			
	1.8.1 L2_Lru_replacement	100%	1 / 1 (100%)	n/a			
	1.9 L2 Cache Functionality	100%	5 / 5 (100%)	100%			
	1.9.1 L2_Read_hit	100%	1 / 1 (100%)	n/a			
	1.9.2 Assert_L2_write_data_validity	100%	1 / 1 (100%)	100%			
	1.9.3 Assert_L2_write_hit_completion	100%	1 / 1 (100%)	100%			
	1.9.4 Assert_L2_wr_done	100%	1 / 1 (100%)	100%			
	1.9.5 L2_write_hit_eviction	100%	1 / 1 (100%)	n/a			
	1.10 Functional Coverage	88.4%	648 / 793 (81.72%)	n/a			
	1.10.1 Arbiter	97.62%	72 / 74 (97.3%)	n/a			
	1.10.2 LRU	100%	32 / 32 (100%)	n/a			
	1.10.3 MESI	83.04%	62 / 88 (70.45%)	n/a			
	1.10.4 CPU_L_slash_O	90.25%	145 / 164 (76.8%)	n/a			
	1.10.5 CPU APB	79.17%	36 / 48 (75%)	n/a			
	1.10.6 BUS	89.53%	292 / 355 (82.25%)	n/a			
	1.10.7 L2 APB	79.17%	9 / 12 (75%)	n/a			
	1.11 Code Coverage	87.94%	11049 / 14382 (76.83%)	n/a			
	1.11.1 Block	91.63%	910 / 1028 (88.52%)	n/a			
	1.11.2 Expression	84.34%	325 / 356 (91.29%)	n/a			
	1.11.3 Toggle	87.85%	9814 / 12998 (75.5%)	n/a			