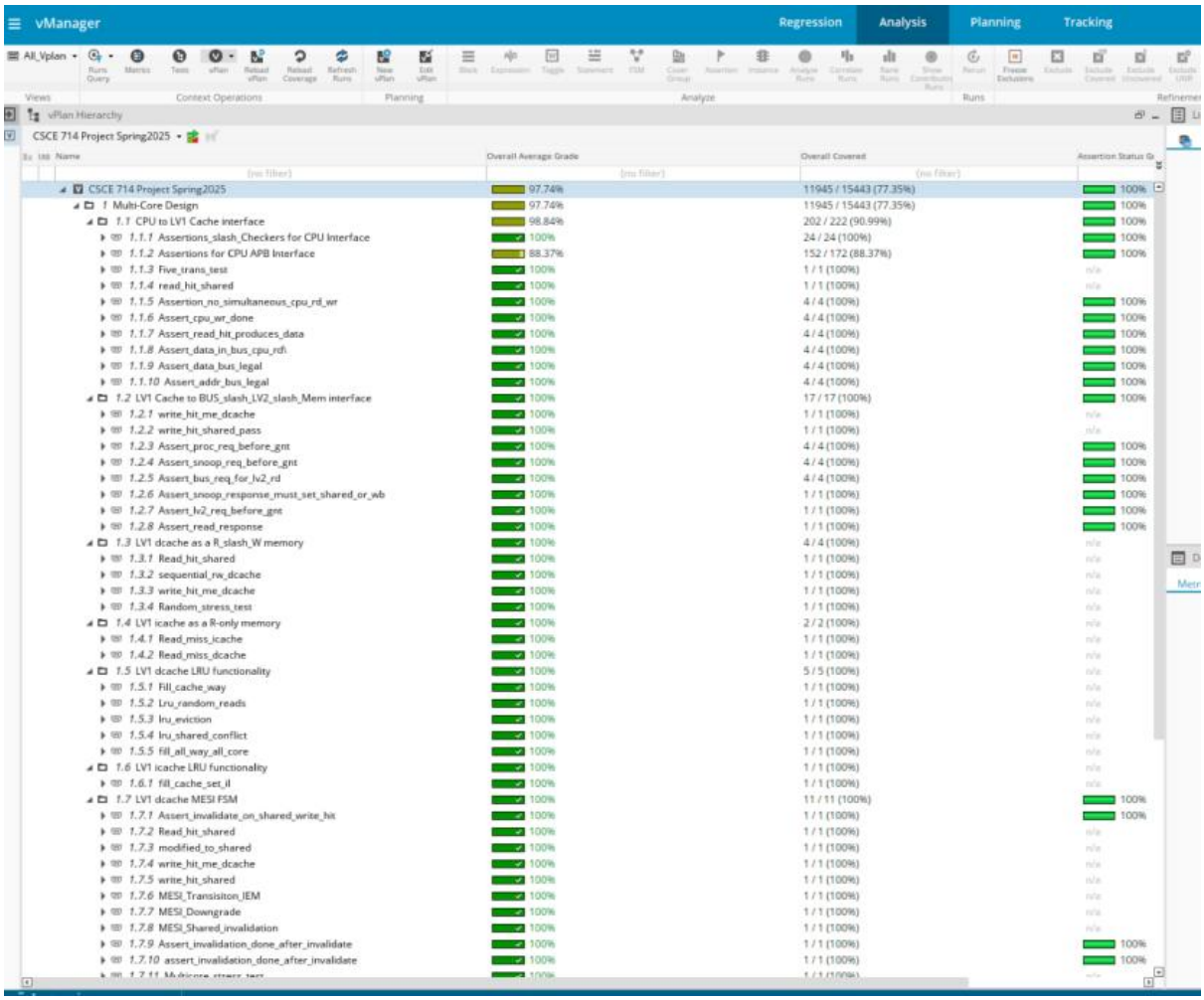
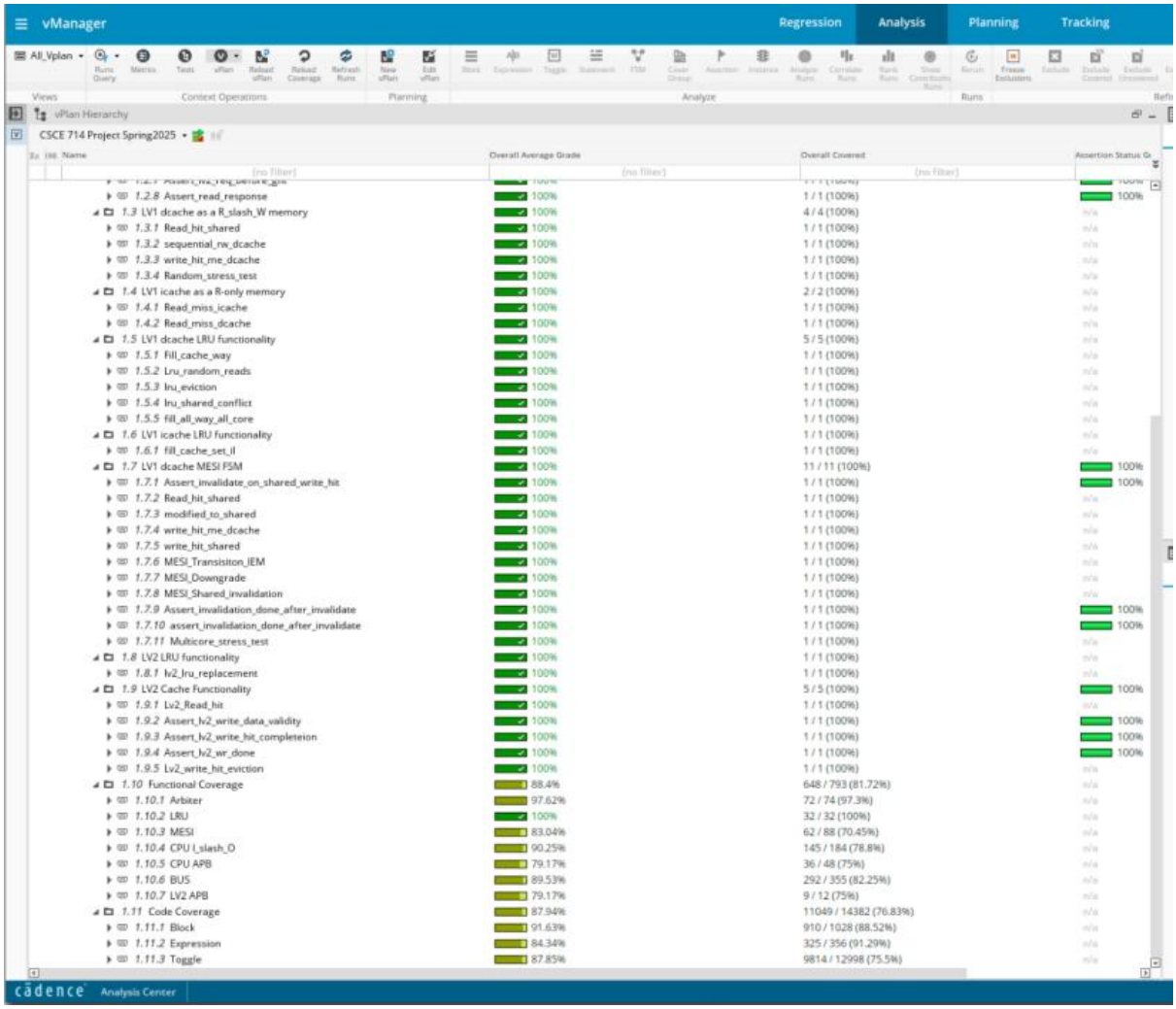
REGRESSION ANALYSIS AND COVERAGE CLOSURE

Running Regression and Mapping Coverage Results to Cadence vPlanner




vManager
Regression
Analysis
Planning
Tracking
All_Vplan
Views
Context Operations
Planning
Analyze
Runs
vPlan Hierarchy
CSCE 714 Project Spring2025
Name
Overall Average Grade
Overall Covered
Assertion Status Gr
1.2.8 Assert_read_response 100% 1 / 1 (100%) 100%
1.3 LV1 dcache as a R_slash_W memory 100% 4 / 4 (100%) n/a
1.3.1 Read_hit_shared 100% 1 / 1 (100%) n/a
1.3.2 sequential_rw_dcache 100% 1 / 1 (100%) n/a
1.3.3 write_hit_me_dcache 100% 1 / 1 (100%) n/a
1.3.4 Random_stress_test 100% 1 / 1 (100%) n/a
1.4 LV1 icache as a R-only memory 100% 2 / 2 (100%) n/a
1.4.1 Read_miss_icache 100% 1 / 1 (100%) n/a
1.4.2 Read_miss_dcache 100% 1 / 1 (100%) n/a
1.5 LV1 dcache LRU functionality 100% 5 / 5 (100%) n/a
1.5.1 Fill_cache_way 100% 1 / 1 (100%) n/a
1.5.2 Lru_random_reads 100% 1 / 1 (100%) n/a
1.5.3 lru_eviction 100% 1 / 1 (100%) n/a
1.5.4 lru_shared_conflict 100% 1 / 1 (100%) n/a
1.5.5 fill_all_way_all_core 100% 1 / 1 (100%) n/a
1.6 LV1 icache LRU functionality 100% 1 / 1 (100%) n/a
1.6.1 fill_cache_set_il 100% 1 / 1 (100%) n/a
1.7 LV1 dcache MESI FSM 100% 11 / 11 (100%) 100%
1.7.1 Assert_invalidate_on_shared_write_hit 100% 1 / 1 (100%) 100%
1.7.2 Read_hit_shared 100% 1 / 1 (100%) n/a
1.7.3 modified_to_shared 100% 1 / 1 (100%) n/a
1.7.4 write_hit_me_dcache 100% 1 / 1 (100%) n/a
1.7.5 write_hit_shared 100% 1 / 1 (100%) n/a
1.7.6 MESI_Transisiton_IEM 100% 1 / 1 (100%) n/a
1.7.7 MESI_Downgrade 100% 1 / 1 (100%) n/a
1.7.8 MESI_Shared_invalidation 100% 1 / 1 (100%) n/a
1.7.9 Assert_invalidation_done_after_invalidate 100% 1 / 1 (100%) 100%
1.7.10 assert_invalidation_done_after_invalidate 100% 1 / 1 (100%) 100%
1.7.11 Multicore_stress_test 100% 1 / 1 (100%) n/a
1.8 LV2 LRU functionality 100% 1 / 1 (100%) n/a
1.8.1 lv2_lru_replacement 100% 1 / 1 (100%) n/a
1.9 LV2 Cache Functionality 100% 5 / 5 (100%) 100%
1.9.1 Lv2_Read_hit 100% 1 / 1 (100%) n/a
1.9.2 Assert_lv2_write_data_validity 100% 1 / 1 (100%) 100%
1.9.3 Assert_lv2_write_hit_completeion 100% 1 / 1 (100%) 100%
1.9.4 Assert_lv2_wr_done 100% 1 / 1 (100%) 100%
1.9.5 Lv2_write_hit_eviction 100% 1 / 1 (100%) n/a
1.10 Functional Coverage 88.4% 648 / 793 (81.72%) n/a
1.10.1 Arbiter 97.62% 72 / 74 (97.3%) n/a
1.10.2 LRU 100% 32 / 32 (100%) n/a
1.10.3 MESI 83.04% 62 / 88 (70.45%) n/a
1.10.4 CPU I_slash_D 90.25% 145 / 184 (78.8%) n/a
1.10.5 CPU APB 79.17% 36 / 48 (75%) n/a
1.10.6 BUS 89.53% 292 / 355 (82.25%) n/a
1.10.7 LV2 APB 79.17% 9 / 12 (75%) n/a
1.11 Code Coverage 87.94% 11049 / 14382 (76.83%) n/a
1.11.1 Block 91.63% 910 / 1028 (88.52%) n/a
1.11.2 Expression 84.34% 325 / 356 (91.29%) n/a
1.11.3 Toggle 87.85% 9814 / 12998 (75.5%) n/a
cadence
Analysis Center