

# Vedant Vishwakarma

Keen to pursue hands-on research in semiconductor device modeling and design at the graduate level.

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## EDUCATION

<b>Bachelor of Technology in Electronics and Communication Engineering</b> <i>Vellore Institute of Technology, Vellore, India</i>	<b>2021-2025</b> CGPA: <b>8.97 / 10</b>
<b>Higher Secondary Certificate (HSC)</b> <i>Indian School DaresSalaam, Dar es Salaam, Tanzania</i>	<b>2020-2021</b> Percentage: <b>90.2%</b>
<b>Secondary School Certificate (SSC)</b> <i>Indian School DaresSalaam, Dar es Salaam, Tanzania</i>	<b>2018-2019</b> Percentage: <b>95.2%</b>

## Experience

- **SSPL DRDO** Nov 2023  
*Internship Trainee* New Delhi, India
  - **Implemented** C++ image processing algorithms, enhancing face and edge detection efficiency across multiple test scenarios.
  - **Strengthened** debugging skills, independently resolving issues faster in verification environments.
- **Maven Silicon** June - July 2024  
*Project Intern* Remote
  - **Developed** a 32-bit pipelined processor using Verilog HDL; involved analyzing signal propagation delays, timing margins, and logic-level behavior relevant to digital IC design.
  - **Utilized** UVM testbench, streamlining verification processes, enhancing test coverage, and accelerating debugging for complex designs.

## Projects

- **MIMO Patch Antenna Design** 2023  
Microwave Studio Suite
  - **Designed** a 4-element MIMO patch antenna with optimized  $\lambda/4$  spacing for minimal coupling.
  - **Achieved** gains of 6.1 and 6.8 dBi with effective impedance matching and low return loss.
  - **Simulated** radiation patterns and S-parameters, confirming improved signal integrity.
- **RISC-V RV32I Processor Design** 2024  
Verilog, UVM, Digital Design
  - **Implemented** a 5-stage pipelined RV32I processor core in Verilog.
  - **Verified** design using UVM testbench to ensure functional correctness.
  - **Focused** on timing optimization and stable execution of ISA-compliant instructions.
- **CAN-Based Accident Avoidance System** 2024  
Arduino, MCP2515
  - **Designed** a sensor-based collision avoidance prototype using ultrasonic sensors and CAN protocol.
  - **Integrated** servo-controlled braking with real-time distance feedback and status display.
- **Deep Learning for Channel Estimation in UV MIMO Systems** 2025  
Python, TensorFlow, MATLAB
  - **Trained** DL models to improve channel estimation in ultraviolet MIMO communication.
  - **Compared** performance with traditional estimation under noise and signal distortion.
  - **Validated** improvements through reconstruction metrics and error rate reduction.

## SKILLS

**Programming:** Embedded C, C, Python, Verilog  
**Tools & Platforms:** STM32CubeIDE, Keil uVision, Proteus, LTspice, Vivado, Cadence Virtuoso, Git  
**Domain Knowledge:** Microcontrollers, GPIOs, Embedded Protocols, Digital Electronics, Analog IC Design

## Certifications

Certification	Institution & Date
Hands-on Analog and Digital IC Design using Cadence Tools	VIT Vellore, Sep 2024
RISC-V ISA RV32I RTL Design	Maven Silicon, Jun - Jul 2024
VSD - Static Timing Analysis I	Udemy, Nov 2024
VLSI Design	Internshala Trainings, Dec 2024