Traction Motor Drive Design and Control

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***Abstract*— This paper reports a detailed description of a Drive and Control system for Traction Motors. The hardware and software configurations, details and the working principles of each stage are explained in detail.**

Keywords*— *AC Motors, Drive and Control Systems, PI Control, F28379D, PCB Design.

1. INTRODUCTION

Motor drivers act as an interface between the power source and the motor and mainly adjust the speed of the employed motor. These devices provide the users with process control and energy conservation. The aim of an AC Motor Drive is to drive a 3-Phase AC motor. To drive 3-phase motors, "Variable Frequency Drives (VFD)" are employed. VFDs convert an incoming 3 Phase voltage into a variable frequency 3 Phase output and drive AC Motors. The block diagram of a VFD is shown in Figure 1.1.

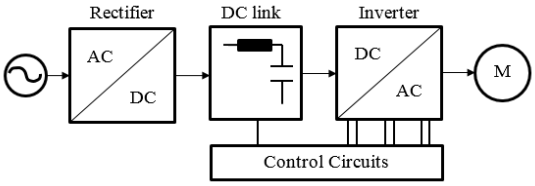

Figure 1. 1: VFD Block Diagram

In such systems, the first step is to make the AC/DC conversion. The rectifier fulfills this duty. Then, the DC link further filters the rectified voltage and delivers a pure DC voltage to the inverter stage. The inverter converts the DC voltage in to a controlled AC voltage to provide the user with the control of the AC motor torque, speed and position.

In this particular project, the input power is directly a DC voltage. It can be thought of an electric vehicle battery pack. Thus, the rectifier stage in Figure 1.1 is not populated. The particular block diagram of the "Traction Motor Drive Design and Control" project is shown in Figure 1.2.

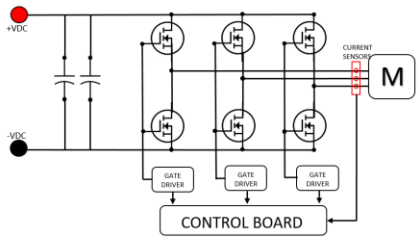

Figure 1. 2: Block Diagram of the Project

As can be seen from the block diagram, the incoming DC voltage is filtered, and then converted into variable frequency AC voltage at the inverter stage. The inverter is designed using IXFH42N60P3 N-Channel high power MOSFETs. Each phase is controlled by two MOSFETs, and AC output is produced based on the switching of these devices. The switching application of the MOSFETs is controlled by Gate Driver circuits. These circuits take PWM signals from the Control Board and provide the MOSFETs with required switching signals. Thus, the control of the motor is completed with the control signals coming from the control board.

There are Current Sensors (LEM-25) at the input of the motor to check the amount of current that motor uses. The current values for phase A and C are fed back to the control circuit, and the required precautions are calculated and carried out.

The aforementioned process is divided into two PCB boards: Power Board and Control Board. These boards consists of the circuits in Table 1.1. Each of these circuits is explained thoroughly in the following sections.

Control Board	Drive Board
1) Fault Circuit	1) Bus Voltage Filter
2) Power Supply Interface	2) Bus Voltage Sense Circuit
3) Current Sensor Interface	3) Gate Driver Fault Circuit
4) Voltage Sensor Interface	4) Isolated DCDC Converter Stage for Gate Drivers
5) Temperature Interface	5) Gate Driver Circuit
6) CAN Interface	6) Mosfet Connections
7) F28379D Launchpad	
8) Gate Driver Interface	
9) Resolver Interface	

Table 1.1: The contents of each PCB

2. Control Board Circuit Explanations

2.1. Fault Circuit

This circuit is implemented to shut the operation of the Motor Driver in case of a Over Current or Over Voltage failure. This circuit is used as an external fault detection application in which the current measurements from the current sensors and the DC Bus voltage are checked. This operation is carried out using quadrature comparators, particularly LM339.

The current sensor (LEM LES25-NP) will output a voltage between 0.25V and 4.75V, which represent -85A and +85A respectively. For instance, if the amplitude of the current output is desired to be between -20A and +20A, the output voltages should be in the range of 2V and 3V. The Voltage/Current output graph of the current sensor (LES 25 NP) is depicted in Figure 2.1.1.

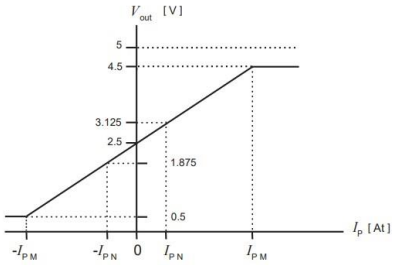

Figure 2.1. 1: Voltage/Current relationship of LES 25NP

I_{PN}: Primary Nominal RMS Current (25A)
I_{PM}: Primary Current Measuring Range (-85A to 85A)

Based on the requirement (the currents should not exceed -20A to 20A range) that the output of LES25 should be between ~2V and ~3V, a circuit was built that produces a FAULT signal if the voltage is not in the aforementioned range. To build this circuit, LM339, a low-power comparator is selected. With this device, four different conditions can be analyzed simultaneously. The pin diagram of LM339 is shown in Figure 2.1.2.

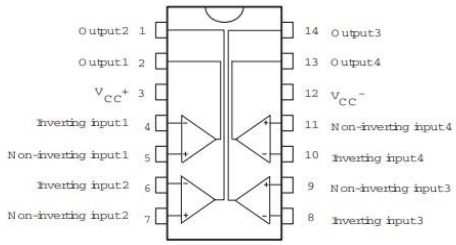

Figure 2.1. 2: Pin Diagram of LM339

Comparator circuits simply compare two voltages. The output of such a device is digital (either HIGH or LOW) depending on the voltage values of the inverting and non-inverting inputs. The principle of the operation is that if the voltage value at the inverting input (-) is greater than the non-inverting(+) input, the output is LOW, and vice versa.
The output of the comparator circuit results in a $\overline{FAULT}$ signal, meaning that FAULT = LOW, NO-FAULT = HIGH.
The cases are as follows: (Refer to Figure 1.1.5 for the schematic)

- If the output voltage of a Current Sensor (IX_Filtered) is less than LowLimit (2V), which is a faulty case, the output of that condition will be LOW. If IX_Filtered is higher than the LowLimit, which is a non-faulty case, the output will be HIGH.
- If the output voltage of a Current Sensor (IX_Filtered) is less than HighLimit (3V), which is a non-faulty case, the output of that condition will be HIGH. If IX_Filtered is higher than the HighLimit, which is a faulty case, the output will be LOW.

The desired input/output table is shown in Table 2.1. To simulate this operation, the circuit shown in Figure 2.1.3 was set on Proteus, and simulated. The simulation result is shown in Figure 2.1.4.

IX_Filtered (V)	Fault
2< V < 3	No
3 < V	Yes
V < 2	Yes

Table 2.1: Desired Current Fault Cases

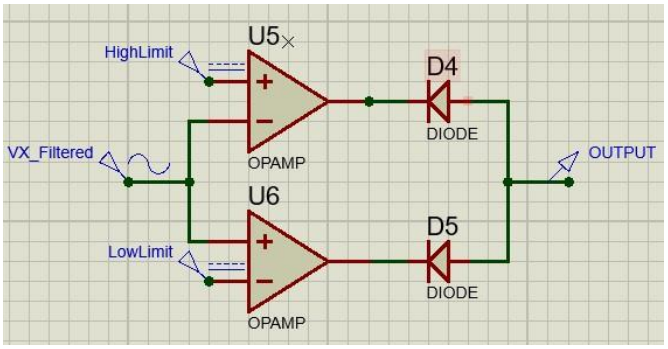

Figure 2.1. 3: The simulated circuit

Figure 2.1. 4: Simulation Results

When IX_Filtered (Green) is in the range of non-faulty voltages, the output (Yellow) is HIGH, else it is LOW.
Following this logic, the circuit shown in Figure 2.1.5 and Figure 2.1.6 are designed. In case either one of the fault

checks is not needed, the DNP resistors will be populated to create automatically non-fault (HIGH) output.

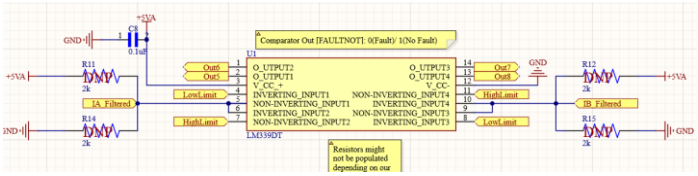

Figure 2.1. 5: A and B phase Fault Circuit

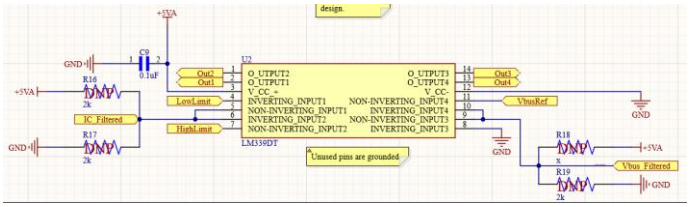

Figure 2.1. 6: C Phase and Bus Voltage Fault Circuit

In case the control is not required, the resistors must be populated to generate a DC voltage (Voltage divider) in high and low limits so that a non-faulty case will be automatically obtained.

If a VBUS fault check is not required, populating R19 will be enough to disable this function. On the design, the VBUS error limit is 280V. This limit can be arranged.

The reference voltages for the comparator circuit are obtained using the following voltage divider circuitry shown in Figure 2.1.7. The values are only for example, not for the current design. The voltage level must be adjusted to satisfy the need.

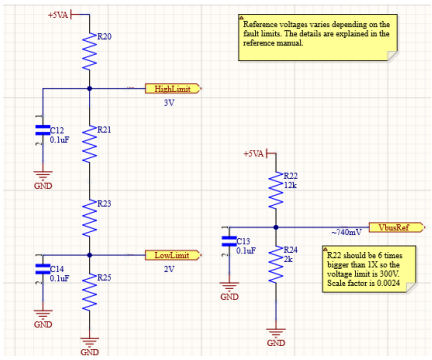

Figure 2.1. 7: Reference Voltage Divider Stage

The outputs of the comparator circuits must be connected to Diodes. The reason for that is, when there is a FAULT case, the main fault signal will be tied to the ground. If there is a no-fault case, there will not be a voltage drop on the pull-up resistor shown in Figure 2.1.8 and the input to the inverter will be high. Moreover, since the output of the comparator circuit is $\overline{FAULT}$, an inverter is required for the SR-Latch input. SR-Latch is required for shutting down the PWM signals, and keeping them shut down until the reset signal (SR-Reset) is sent.

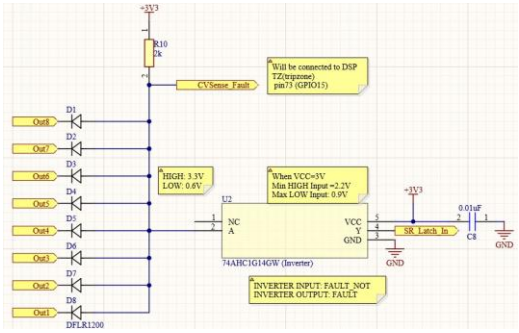

Figure 2.1. 8: Comparator Outputs and Inverter Circuit

At the output of the inverter is a FAULT signal, which is connected to the SR Latch (HEF4043BT). The SR Latch output is connected to Differential Line Driver Enable input for the PWM signals to shut down the operation in case of a failure. The SR Latch Connections are shown in Figure 2.1.9.

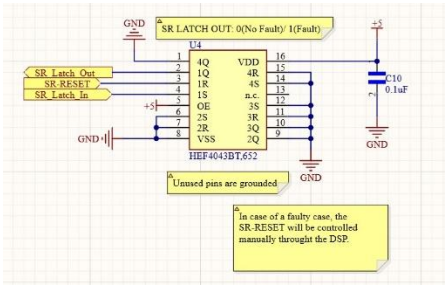

Figure 2.1. 9: SR Latch Connections

The reset signal is controlled through DSP, and the system is restarted after the fault is eliminated.

To sum up, Fault Circuit is used to control the operation conditions based on the current sensor outputs and VBUS voltage. In case of an overvoltage or undervoltage, the operation will be shut down for protecting rest of the circuits.

2.1.1. Functionality Tests of the Fault Circuit

To test this circuit, the Current Sensor control for phase C is eliminated, meaning that the voltage divider resistors are populated and a 2.5V regulated voltage, which is a non-faulty case, is sent to comparators. The functionality test is run for phase A and B current sensor outputs. As mentioned above, the circuit should yield a faulty output if the current sensor outputs a voltage outside the range of 2V-3V. A sinusoidal wave that has the below features is applied to the circuit, and output is examined. The input is Channel 1 (yellow), and the fault circuit output is Channel 2 (blue). The result is depicted in Figure 2.1.10.

Figure 2.1. 10: Oscilloscope View of the Test Setup

As can be seen, when the input voltage is greater than 3V and less than 2V, the output is low. Otherwise, the output is high. The output is connected to an inverter, and connected to the SR-Latch input. Whenever the fault is generated, SR-Latch remains HIGH untill reset.

2.2. Power Supply Interface

This circuit aims to provide the rest of the circuitry with clean and sufficient power. The input to the supply circuit is 12V battery connections. This voltage should be filtered and converted into 3.3V and 5V to provide the ICs with sufficient power.

Firstly, a common mode choke (CMC) is applied to the battery voltage. Common Mode Noise is present on the circuits mainly due to high-frequency switching applications. High-frequency results in a high di/dt ratio which results in higher Electromagnetic Noise. This noise is present on the signal traces and common ground planes, which affects the signals. The contribution of a CMC to the circuit is that it attenuates the common-mode noise. It adds inductance to the power traces to minimize the current ripples. It is used to reduce the EMI components on the power supply. In addition, to reduce the common-mode noise, power traces are kept as close as possible on the layout. The common-mode choke (ACM7060-701-2PL-TL01) connection is shown in Figure 2.2.1.

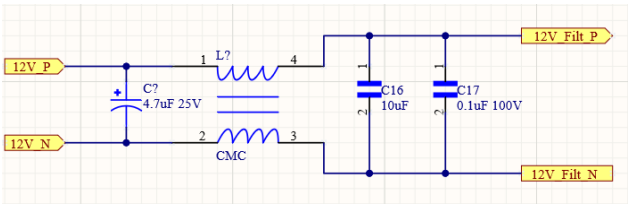

Figure 2.2. 1: Common Mode Choke Connections

After filtering the battery power, the 12V should be converted into 3.3V and 5V. First, 12V is converted to 5V with a buck converter (R-78E5.0-1.0), then the 3.3V is obtained by an LDO that has the input from the 5V. Here, a great care is paid for the noise on analog and digital circuits on the Control Board. Analog circuits are more susceptible to noise. Thus, an LC filter is applied and the power lines of analog and digital circuits are separated. Voltage conversion and filter circuits are shown in Figure 2.2.2 and Figure 2.2.3.

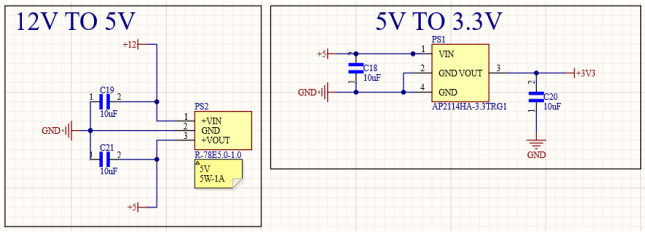

Figure 2.2. 2: 5V and 3.3V Conversion

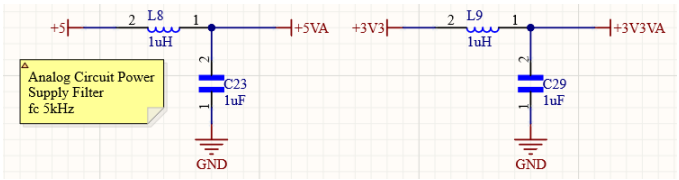

Figure 2.2. 3: LC Filter for the Analog Circuits

2.3. Current Sensor Interface

This circuit processes the Current Sensor outputs and sends them to the Fault circuit and DSP. IX_CSensor refers to the output of the current sensor for the associated phase. IX_Filtered is connected to the Fault Circuit for external fault control, and Current-X is connected to DSP. Notice the voltage divider before the Current-X for the protection of the DSP. The current sensor interface circuit is shown in Figure 2.3.1.

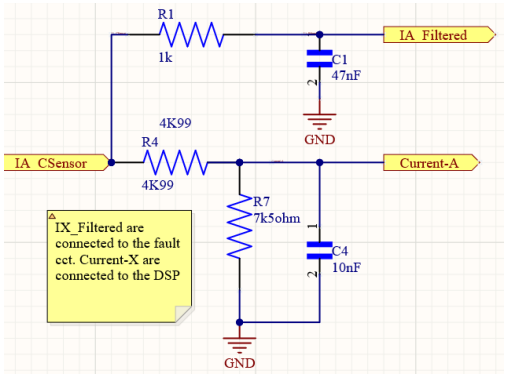

Figure 2.3. 1: Current Sensor Interface Circuit

In this part, taking the measurements of two currents will be enough because of Kirchoff's law. The law ponits out that the sum of the currents entering a node should be zero. Thus:

$$i_A + i_B + i_C = 0$$

If the current value for phase A and C is measured, phase B can be reconstructed. Therefore, two current sensors will be enough.

2.4. Voltage Sensor Interface

Voltage values will be found using estimation method from the PWM signals. The XHS_PWM is a modulated signal, and it is demodulated for DSP to read it using the low-pass filter. This circuit is shown in Figure 2.4.1.

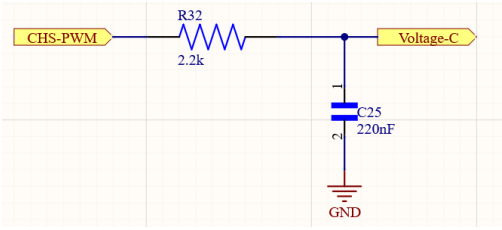

Figure 2.4. 1: Voltage Sensor Interface Circuit

2.5. Temperature Sensor Interface

This circuit is used to obtain the temperature of Bus capacitors, Bus Bar, and three IGBTs. The output of the thermistor is filtered in the interface circuit and sent to DSP for control. The connector connections of the temperature sensor interface are shown in Figure 2.5.1, and the circuit is shown in Figure 2.5.2.

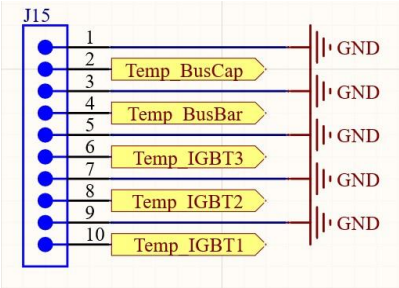

Figure 2.5. 1: The External Connectors

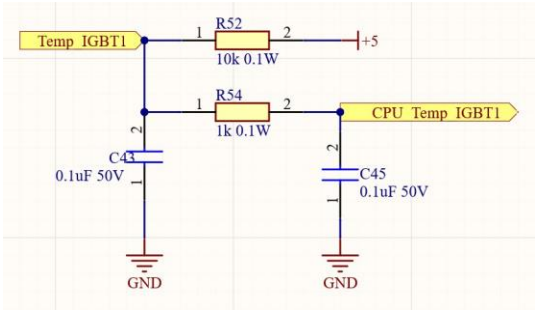

Figure 2.5. 2: Temperature Sensor Interface Circuit

2.6. CAN Bus Interface

This circuit is used for CAN Bus lines (CANH and CANL) to be converted to TX and RX signals via a CAN Transceiver. The CAN Transceiver connections are shown in Figure 2.6.1.

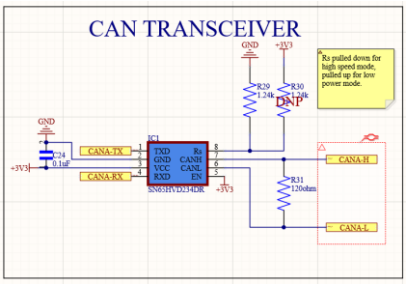

Figure 2.6. 1: CAN Bus Interface Circuit

CAN Transceivers convert the differential CAN pair (CANH and CANL) into TX (transmit) and RX (receive) signals. CANH and CANL signals are separated from each other by a terminating resistor, 120-ohms. There can not be a direct connection between CANH-L pair and an MCU. Transceivers converts them into TX and RX. TX and RX signals are connected to MCUs (TX to RX/ RX to TX).

2.7. F28379D Connections

The main controller board that sends the control signals to the controller is F28379D Launchpad. The software provides the system with the required signals. It has several connectors on the Launchpad, and requires a couple of hardware configurations.

2.7.1. Global Fault Signal

There are two FAULT circuits in this controller board. The first one is the fault circuit for the current sensor and bus voltage (refer to section 2). The output of this circuit is CVSense_Fault ($\overline{FAULT}$).

The second one is the Gate Driver fault outputs (X-FAULT). These signals are also $\overline{FAULT}$. In case of faulty case, the corresponding LEDs will turn ON.

In order to manage all the FAULT signals as one output, a quadrature AND Gate is employed. If any of CVSense_Fault or X-FAULT are faulty (LOW), the AND gate will have LOW signal at the output. This brings us to the conclusion that the AND Gate output is also $\overline{FAULT}$. A HIGH signal is generated only if all the Fault signals are HIGH. The Global Fault circuit is shown in Figure 2.7.1.1.

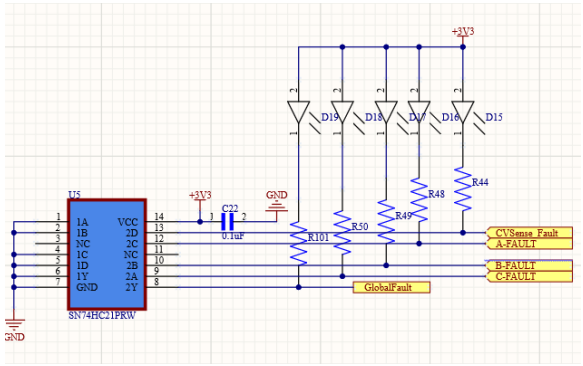

Figure 2.7.1. 1: Global Fault AND Gate Circuit

2.7.2. DSP Connectors

The Connector designators on Altium Schematics and the actual designators on Launchpad do not match. See the notes next to the connectors to locate the actual connectors on the DSP. In Figure 2.7.2.1, the connectors for Quadrature encoders, ground, and CAN-B Bus connections are presented. For all the power connections (3.3V, 5V), 0-ohm DNP resistors are placed. The reason for these DNP resistors is that the DSP will be either powered by the USB cable provided in the package or the power line from the power circuit. When the DSP is powered by the USB cable, the power from an external circuit is not necessary, thus the DNP resistors shall not be populated. In case it is desired to power the DSP by the power supply existing on the board, the 0-ohm resistors must be populated.

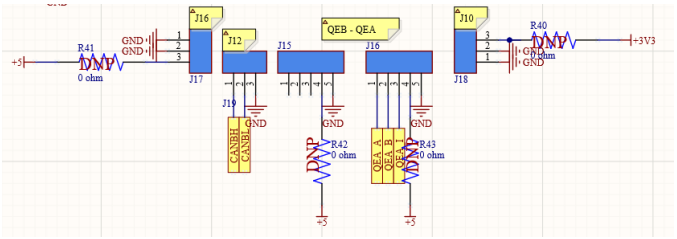

Figure 2.7.2. 1: QEX and Power Connections

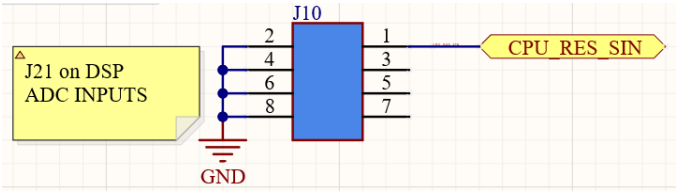

Figure 2.7.2. 2: ADC Connector on DSP

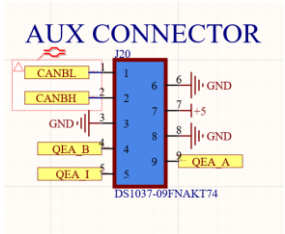

Figure 2.7.2. 3: AUX Connector

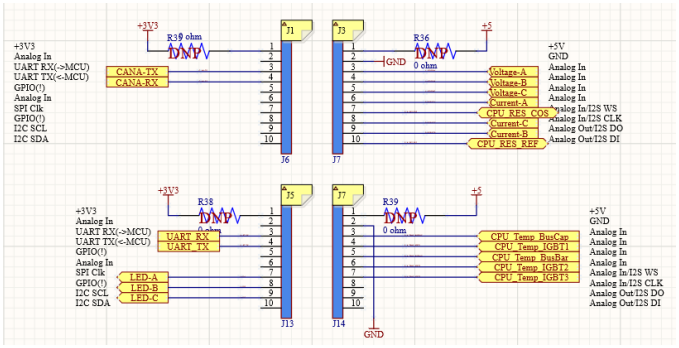

Figure 2.7.2. 4: J1, J3, J5 and J7 on the DSP

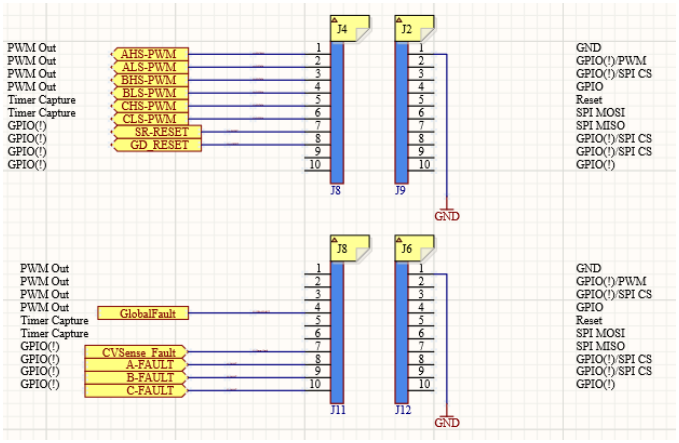

Figure 2.7.2. 5: J4, J2, J8 and J6 on the DSP

2.8. Gate Driver Interface Circuit

Signal integrity has the utmost importance when controlling power devices with a gate driver. Gate drivers are susceptible to EMI or any noise generated by power devices. Power devices have extremely high switching frequencies and create dense EMI which can easily couple on gate control signals. To prevent any interference, differential signals are used for this gate driver design.

Differential signals reduce the effect of the noise that is created during the switching events. A single-ended signal can be converted into a differential pair by transmitting both the original signal and its complement in two closely coupled wires. Thereafter, these two signals are compared to reconstruct the original signal. In Figure 2.8.1, the noise immunity of differential signals and reconstruction of the original signal from the differential pair is depicted.

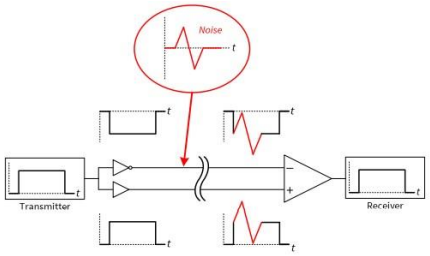

Figure 2.8. 1: Noise Cancellation of Differential Signals

In the circuit, the differential pairs for XHS-PWM, XLS-PWM are constructed using AM26LV31EIPWR quadruple differential line drivers. The associated circuit is shown in Figure 2.8.2 and Figure 2.8.3.

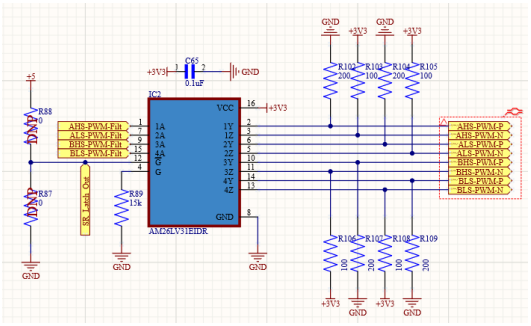

Figure 2.8. 2: Differential Signal Construction (Phase A and B)

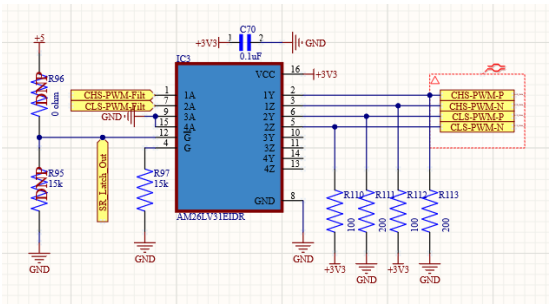

Figure 2.8. 3: Differential Signal Construction (Phase C)

SR Latch Output is connected to these differential line driver ICs. In a faulty situation, SR Latch Out will be HIGH. G' will be controlled by SR Signal. If Faulty Signal comes (SR HIGH), G' will go High and the IC will be disabled.

Also, differential FAULT signals are coming from the Gate Drivers via the connectors. These X-FAULT-P and X-FAULT-N signals are connected from the gate driver circuit (Power Board) to the gate driver interface circuit (Control Board). Connector diagrams are shown in Figure 2.8.4.

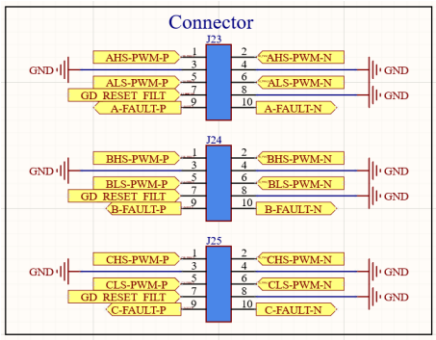

Figure 2.8. 4: Gate Driver Interface Connector

As such, the differential fault signals are reconstructed using a differential line receiver. The operation is shown in Figure 2.8.5.

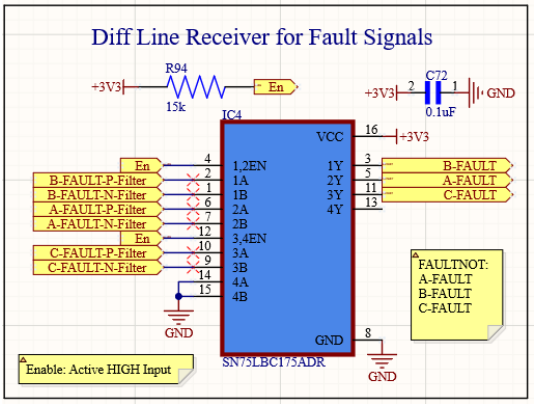

Figure 2.8. 5: Differential Line Receiver Circuit

2.8. Resolver Interface

Resolvers and encoders are devices that measure the rotary position of a shaft by converting the mechanical motion into an electrical signal.
Resolvers have a primary winding on the rotor, and two secondary windings on the stator. Simple structure of a resolver is shown in Figure 2.9.1.

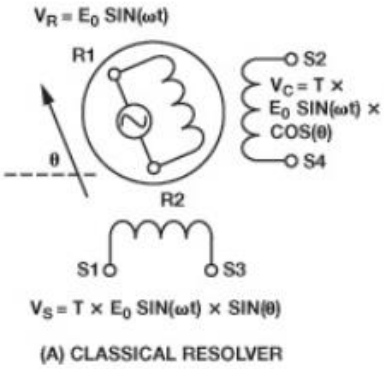

Figure 2.9. 1: Resolver Structure

When the primary winding is excited (RES_REF_OUT on control board), a signal is induced to the secondary windings. The amount of coupling is a function of the rotor position and the resolver attenuation factor. The secondary windings are mechanically 90 degree apart from each other. This yields a 90 degree phase shift between the secondary windings. To have a better understanding, the mathematical formulas below shall be analysed:

$$R_1 - R_2 = E_0 \sin(wt)$$
$$S_3 - S_1 = T\ x\ E_0 \sin(wt)\ x\ sin\theta$$
$$S_4 - S_2 = T\ x\ E_0 \sin(wt)\ x\ cos\theta$$
$$\theta: shaft\ angle$$

$$w: excitation\ signal\ frequency\ (f = 10kHz)$$
$$E_0: Exciation\ signal\ amplitude$$
$$T = Resolver\ transformation\ ratio$$

As mentioned above, a sine wave excites the primary winding and two output signals are induced on the secondary windings. To read these output signals, a Resolver to Digital Converter (RDC) is needed. RDC uses the modulated sine and cosine signals to decode the rotor position.
However, the resolver attenuates the output voltage and it is hard to perform the conversion on such a signal. The signal should be amplified first. Also, resolvers are used in noisy environments, and the environment may induce high-frequency noise to the output signal. Thus, the signal should be filtered as well. The circuitry used to amplify cosine and sine feedbacks are shown in Figure 2.9.2. The same circuit is also populated for Sin output.

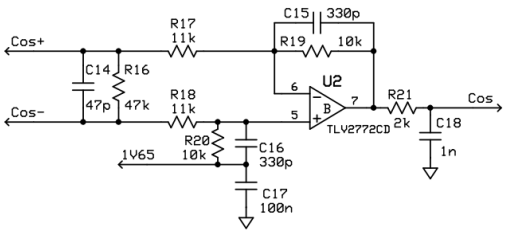

Figure 2.9. 2: Resolver Cosine Feedback Interface Circuit

A similar procedure is also applied for the excitation signal. This signal is generated by F28379D, and needs to be amplified. The circuit that fulfills this duty is shown in Figure 2.9.3. Also, the DC offset is eliminated at the output.

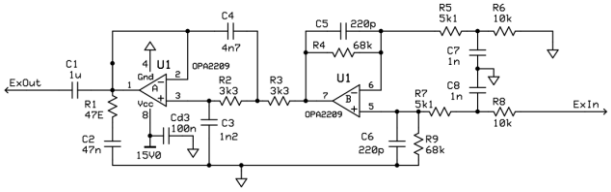

Figure 2.9. 3: Resolver Excitation Signal Interface Circuit

As mentioned above, the Resolver returns two outputs back. One is sine and other is cosine signal outputs. These two outputs are modulated by the excitation signal. The excitation signal and the modulated signal are shown in Figure 2.9.4.

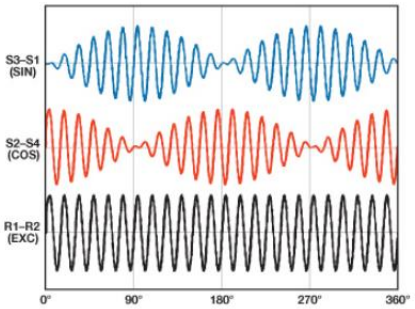

Figure 2.9. 4: Excitation and Feedback Signals

The experiment result of the working principle above is shown in Figure 2.9.5.

Figure 2.9. 5: Experiment Result of the Resolver (CH1: Sine Feedback, CH2: Excitation Signal, CH3: Cosine Feedback)

The position of the motor can be extracted by finding the amplitude of the sine and cosine envelops. The amplitude changes as the motor turns, and there is a 90 degree shift between sine and cosine feedbacks.
Also, the reference speed and the measured speed is verified using Figure 2.9.6.

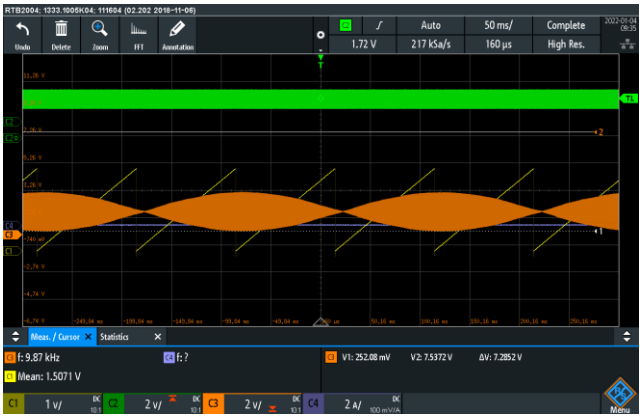

Figure 2.9. 6: CH1: Reference Speed, CH3: Resolver Sine Feedback

When the motor turns a full turn (2π radian or 360 degrees), sine feedback completes a period. And each triangular shape in CH1 (reference speed) represents 90 degrees of rotation, meaning that four repetitions respresent a complete turn of the rotor. There is a small phase shift between them, yet it still verifies that the resolver feeds back the rotor position correctly.

One of the benefits of a resolver is their lack of sensitive optics, which allows them to withstand higher vibrations and shock loads than encoders. They are also resistant to the electrical disturbances, can withstand higher temperatures.

3. Power Board Circuit explanations

3.1. DC Bus Filter

EMI filters are placed after the DC Power supply (B+, B-)in order the filter out the EMI and other interferences that are present on the power. This stage is crucial for the accuracy and precision of all the circuitry on the board. The filtering stage is shown in Figure 3.1.1.

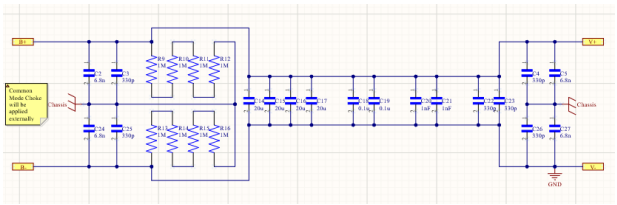

Figure 3.1. 1: Bus Voltage Filter

At the start and the end of the Filtering are Y Caps. Y Caps are designed to filter out the common-mode noise and are connected between the line and chassis. These caps filter the coupling between the ground and the power line. It is extremely critical for these caps not to be short-circuited since it will create a shock risk for the users.
It is important to note that the voltage limits for these CAPS should be high enough to withstand the amount of power (+400DC). All the capacitors in the EMI circuit are film caps, which often have higher voltage limits.
The resistors after the first Y-Caps stage are placed there to absorb the high energy. When the high voltage is charged to the film caps, it does not discharge immediately and keeps the voltage there. The populated resistors help the discharge application.

The 20uF caps are employed to filter out the lower frequency ripples. After that, there are pairs of 0.1uF, 1nF, and 330pF capacitors for precise high-frequency filtering. Three different capacitance values are used for filtering the higher frequencies better. Capacitors have different impedances depending on the frequency, and their filtering capacity varies. The Impedance-Frequency graph of capacitors based on different capacitance values is shown in Figure 2.1.2. The impedance of a capacitor is calculated as follows:

$$X_C = \frac{1}{2\pi f C}$$

Thus, placing different capacitors provides the system with enhanced filtering capacity. There are two caps in the system. These caps will be put at the sides of the board symmetrically.
The capacitors actually include a series LCR branch in them. At certain frequencies, the impedance of the inductor and the capacitor is equal and the total impedance of the capacitor is minimum. This point is called the resonance point, where the capacitor has the highest filtering capability. By applying different capacitors, the filtering capacity of the system is enhanced.

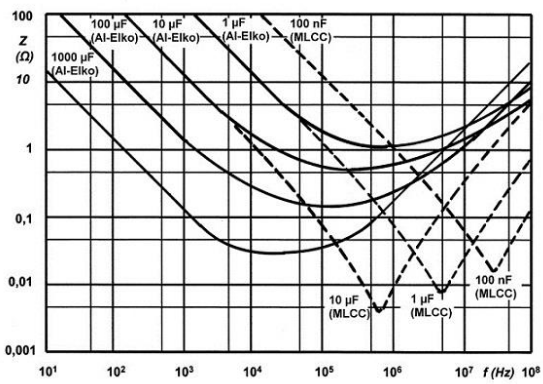

Figure 3.1. 2: Impedance vs Frequency of Different Capacitor Values

3.2. DC Bus Voltage Sense Circuit

V Bus voltage measurement is important to track the operation conditions of the system. A high voltage is first scaled down to a 0-3V band and then sent to the DSP. For this operation, there are two options in the design. These options are shown in Figure 3.3.1 and Figure 3.3.2.

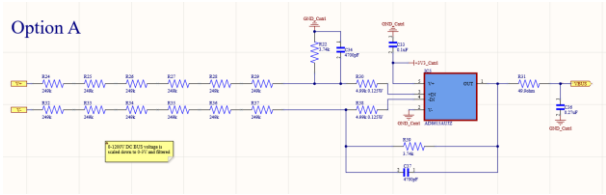

Figure 3.2. 1: Option A for VBUS Measurement

In this option, the high voltage is scaled down to a low voltage using the resistors and then the filtering is applied. VBUS port is connected to the fault circuit interface. If the VBUS is greater than the VBUS reference, a fault is indicated.

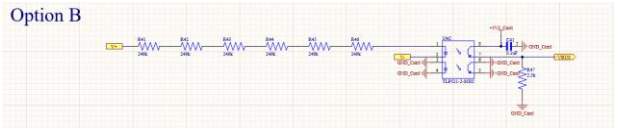

Figure 3.2. 2: Option B for VBUS Measurement

In this option, the same voltage scaling method was applied, yet this time the voltage measurement is isolated from the incoming voltage side.

Currently, option A is populated on the PCBs. In this option, the voltage is scaled using the following voltage division formula:

$$V_{measurement} = V_{BUS} x \frac{3.75k\Omega}{249k\Omega \; x \; 6}$$

This formula is verified on the system by taking measurements at different VBUS levels up to 60V. The scaled VBUS versus the actual VBUS voltage plot is shown in Figure 3.3.3.

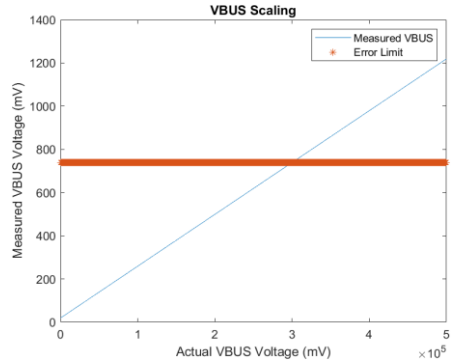

Figure 3.2. 3: Scaled and Actual VBUS Voltages

In this design, the maximum allowed VBUS is, say, 280V. It is equivalent to 716mV in the scaled basis. Thus, the VBUS REF voltage in the FAULT circuit must be set to 716mV. If another VBUS limit is desired, the reference voltage must be arranged accordingly. In this design, the VBUS REF is set to 716mV.

3.3. Gate Driver Fault Circuit

The $\overline{FAULT}$ is generated based on the RDY and /FLT outputs of the Gate Drivers. Each Gate Driver produces a RDY and a /FLT output.

RDY: Open-drain output to report the correct operation of the device (RDY = high if both chips are above the UVLO level and the internal chip transmission is faultless). ***Meaning that, 0 is Faulty and 1 is Non-faulty case.***
/FLT: Open-drain output to report a desaturation error of the MOSFET *(/FLT is low if desaturation occurs).* ***Meaning that, 0 is Faulty and 1 is Non-faulty case.***

For each phase, two gate drivers are employed (High Side and Low Side). Thus, there will be four fault signals to generate a main fault signal for each phase. These signals are connected to a quadrature AND Gate to produce a main $\overline{FAULT}$ signal. The AND Gate stage for Phase-C is shown in Figure 3.2.1.

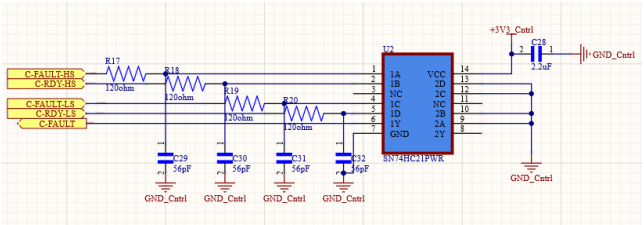

Figure 3.3. 1: And Gate for Fault Signals

The output signal is X-FAULT, which is then connected to a differential line driver to produce X-FAULT-P and X-FAULT-N differential pair. This differential pair is tied up to the connector to be sent to Controller Board Gate Driver Interface. The differential pair in the control board is then connected to a Differential Line receiver to reconstruct the original $\overline{FAULT}$ signals. These $\overline{FAULT}$ signals are sent to Global Fault generator circuit. This process is repeated for all three phases (A, B, C). At the end, Fault signals are named as A-FAULT, B-FAULT and C-FAULT. On the Gate driver Circuit, a different type of IC is used for differential line driver and receiver application. SN75179BDR functions as both driver and receiver. Its functional block diagram is shown in Figure 3.2.2.

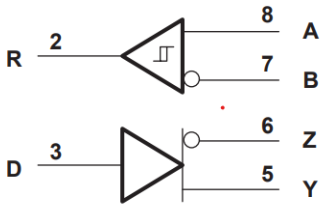

Figure 3.3. 2: Functional Block Diagram of SN75179DR

Differential HS and LS PWM signal are coming from the controller board via the connector, and differential FAULT signal is sent to controller board via the same connector. To suit this application, SN75179BDR is employed with the following circuit in Figure 3.2.3.

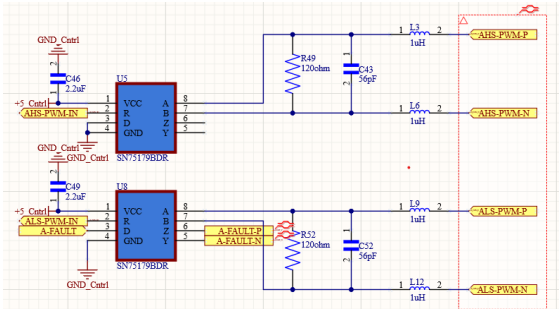

Figure 3.3. 3: Differential Line Driver/ Receiver Circuit

As can be seen, High Side and Low Side PWM differential signals are connected to the receiver inputs after an LCR filter to reconstruct the original PWM signals. These PWM signals are connected to Gate Drivers. Single ended FAULT signal is connected to line driver to produce a differential FAULT signal to be sent to the controller board.

3.4. Gate Driver Fault Circuit

A gate driver is a buffer circuit that amplifies a low voltage low current control signal into a high voltage high current signal. The amplification is necessary since a power transistor would not efficiently work under low voltage. The power transistor requires a certain amount of voltage amplitude at its gate to perform switching. Thus, gate driver circuit is used to amplify a control signal from a microcontroller to make it

suitable for efficient and effective operation of semcionductor switchers. Also, gate drivers provide the isolation for switching devices. The operation can be seen in Figure 3.5.1.

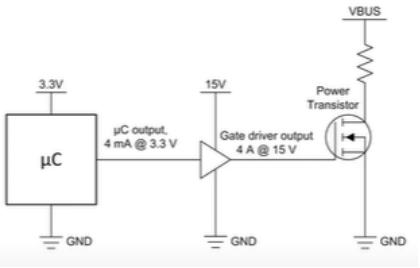

Figure 3.5. 1: Gate Driver Operation

In this aplication, an isolated gate driver IC (1ED020I12-F2) is empoyed. This IC is a single channel driver for 600/1200V MOSFETs, capable of providing the rail to rail current output with 2A, having Vcesat detection and active miller clamp. Keep in mind that the selected MOSFET for this design is IXFH42N60P3, which can work upto 600V and 42A. 1ED020I12-F2 provides several protection features including MOSFET desaturation protection and active miller clamping. Due to the aforementioned features, 1ED020I12-F2 is suitable for this AC Motor drives. The pin configuration of 1ED020I12-F2 is shown in Figure 3.5.2.

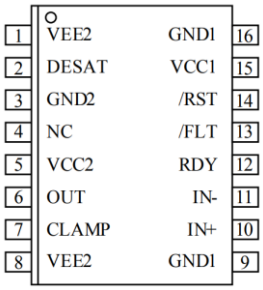

Figure 3.5. 2: Pin Configuration of 1ED020I12-F2

GND1 is the ground of input side.

IN+ is the non-inverting driver input. It controls the driver output if IN- is set LOW. In this design IN- is set LOW to control the output with IN+. An internal pull-down resisor ensures the MOSFET's Off-State.

IN- is the inverting driver input. It is tied to GND1 to make use of IN+.

/RST is the reset input. It has two functions:

1. Enable/ Shutdown of the input chip. The MOSFET is off if /RST is low.
2. Resets the fault states if /RST is low for a time T_{RST}.

/FLT is the fault output. It reports the MOSFET desaturation error. If an error is present, the /FLT goes LOW (Active Low signal). This pin is connected to Fault circuitry.

RDY is the ready status output to report the correct operation of the 1ED020I12-F2. The RDY goes HIGH if the device operates witout errors (Active high signal).

VCC1 is 5V power supply for the input side.

VCC2 is postivie power supply for output side.

VEE2 is the negative power supply or the output side. In this design, it is connected to -2.7V.

GND2 is the ground for the output side. In this design, it is connected to the negative VBUS voltage.

DESAT is the desaturation detection input. Desaturation is a voltage buildup across the Drain/ Source or Collector/ Emitter while the device is on. It can be caused by power supply short circuits due to faulty wiring, control signal failures, overloads induced by the load and failures in the gate driver circuitry. During desaturation, the current and power dissipation drastically increases. This situation yields a high temperature resulting in the failure of the device. To prevent this, DESAT pin turns off the MOSFETs.
If OUT is high, Vds is above a defined value and the certain blanking time is expired, the desaturation protection is activated and the MOSFET is turned off. When the DESAT voltage reaches 9V, the output is driven low, /FLT is driven low after DEAT to FAULT off delay. This delay can be controlled by an external capacitor.

CLAMP is the miller effect prevention pin. Miller effect is the situation where a parasitic turn-on occurs. During turn-on, the parasitic capacitance between Gate and Drain is charged. When the mosfet is in off state, this capacitor discharges. If the voltage drop across the gate resistor is above a certain value, the parasitic turn-on occurs. This might yield a control error, which can cause short ciruits. During turn-off, the gate voltage is monitored, and the clamp output is activated if the gate voltage drops 2V below the VEE2. If an appropriate negative supply is used, connecting CLAMP to gate it redundant. Therefore, miller clamp feature is disabled in this design. If the unipolar supply is used instead of bipolar supply, the CLAMP should be directly connected to gate of the mosfet.
OUT is the driver output to drive the mosfets. The voltage is switched between VCC2 and VEE2. In normal operation mode, the output is controlled by IN+, and /RST. During error mode (Under voltage lock out (UVLO), internall error or DESAT), output is set to VEE2 independent of IN+.

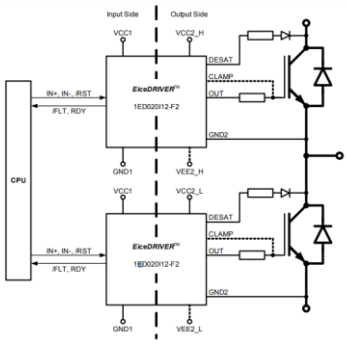

Figure 3.5. 3: Typical Application of 1ED020I12-F2

Gate driver circuits for High Side and Low side are shown in Figure 3.5.3 and Figure 3.5.4. Refer to the datasheet for the pin functionality. The Gate Driver IC is capable of supplying 2A to the driving MOSFETS. With the built push-pull BJT circuit, this current capacity is increased to 4A. The NPN and PNP BJTs are used for amplifying the MOSFET driving currents in case a higher current is required for the power mosfets.

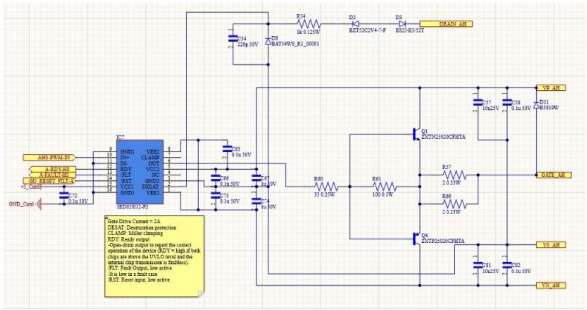

Figure 3.5. 4: High Side Driver Connections

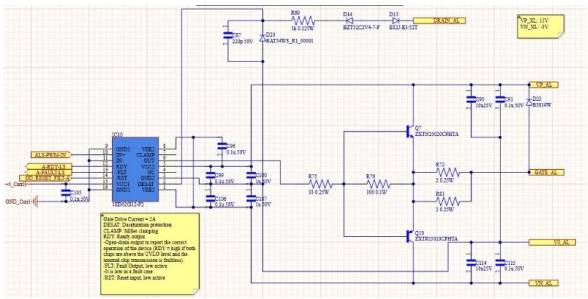

Figure 3.5. 5: Low Side Gate Driver Connections

3.6. Mosfet and Current Sensor Connections

The driving MOSFET connections for Phase A is shown in Figure 3.6.1. The same process is applied for other Phases as well. There are 3 MOSFETs in parallel to provide higher current if required. However, additional MOSFETs might not be populated if max 42A is enough.

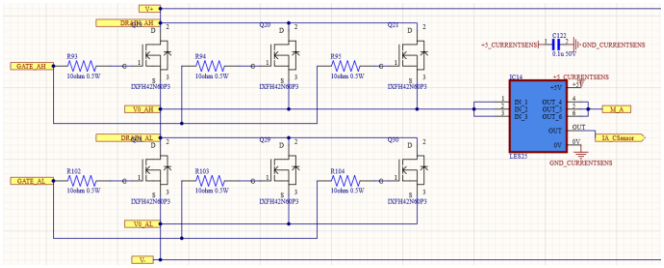

Figure 3.6. 1: Mosfet and Current Sensor Connections

The selected current sensor for this application is LES 25-NP. This sensor allows user to measure the amount of current that flows into the motor. This component will be populated for two of the phases, allowing two current measurements. The third phase current will be estimated based on the other two measurements.

LES 25-NP is capable of measuring -85A and 85A range. The output voltage is between 0.25V and 4.75V, having 0A at 2.5V. Output voltage of LES 25-NP is shown in Figure 3.6.2. Two current sensors will be populated, and the other phase current will be calculated through Kirchoff's Law.

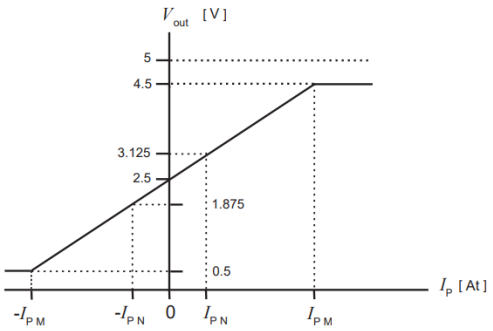

Figure 3.6. 2: Input/ Output Relationship of LES 25-P

4. Field Oriented Control Algorithm

The ultimate aim of the vector control is to control the flux producing and torque producing currents separately as in DC motor. These parameters are decoupled so that they can be controlled independently. To fulfill the decoupling, a couple of mathematical transformations are performed by a Digital Signal Processor (DSP). The particular DSP used in this project is TI-LAUNCHXLF28379D which can perform such mathematical conversion fast enough to provide the precise control of a PMSM.

Torque is defined as the cross-product of the stator current and the rotor flux.

$$T_{em} = \vec{I}_{stator} x \vec{B}_{rotor}$$

As mentioned in the introduction of this section, if these two parameters are kept orthogonal at all times, the produced torque is kept at a maximum. To perform this task, the rotor

position is measured by a resolver. The detailed hardware description of the vector control is explained in Control Board Circuit Explanations.

This project takes the “Sensored Field Oriented Control of 3-Phase Permanent Magnet Synchronous Motors using F28379x” as the reference and follows the same control algorithm and descriptions made in their reference manual. The remaining details should be read carefully from this document for a better understanding of the Vector Control. The incremental build in the aforementioned report is followed step by step to realize the closed-loop control.

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[1] Akin, B., & Bhardwaj, M. (2013). *Sensorless Field Oriented Control of 3-Phase Permanent Magnet Synchronous Motors.* Texas Instruments.

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[3] Texas Instruments, (2015). *Design Drive Development Kit IDDK v2.2.1 Hardware.* Texas Instruments.

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