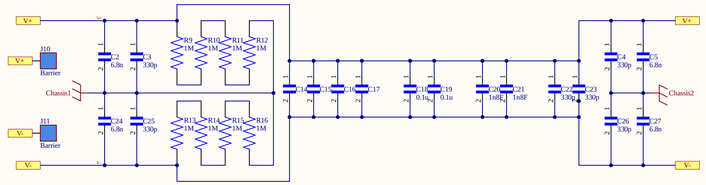
V BUS Filtering Stage



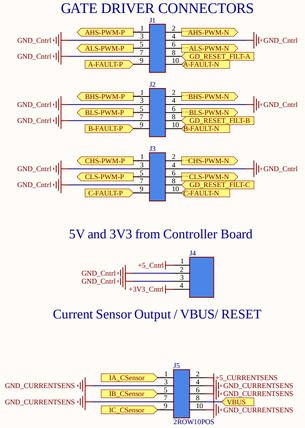
Common Mode Choke will be applied externally

CHASSIS1 and CHASSIS2 will be connected together externally, not on board. The more space chassis has, the more noisy the board gets.

Filtered DC BUS Voltage Side

SHARED CONNECTORS WITH CNTRL BOARD

GATE DRIVER CONNECTORS

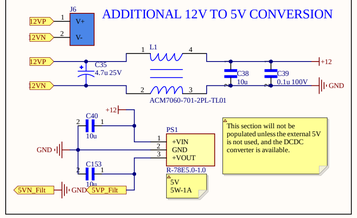


5V and 3V3 from Controller Board

Current Sensor Output / VBUS/ RESET

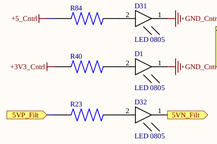
GND_CURRENTSENS and GND_CTRL are not connected to each other on Power Board. They are connected on the CNTRL Board

ADDITIONAL 12V TO 5V CONVERSION



This section will not be populated unless the external 5V is not used, and the DCDC converter is available.

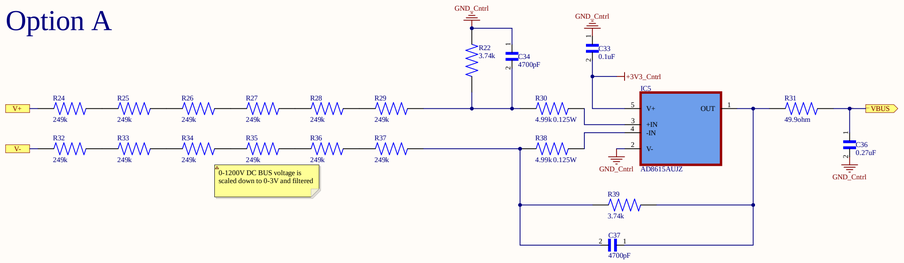
POWER ON LEDs



The LEDs in the LAB will be used.
The resistance value will be determined.

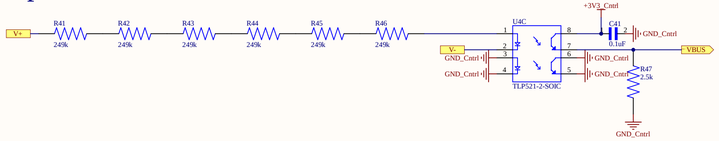
V BUS Voltage Sensing Stage

Option A

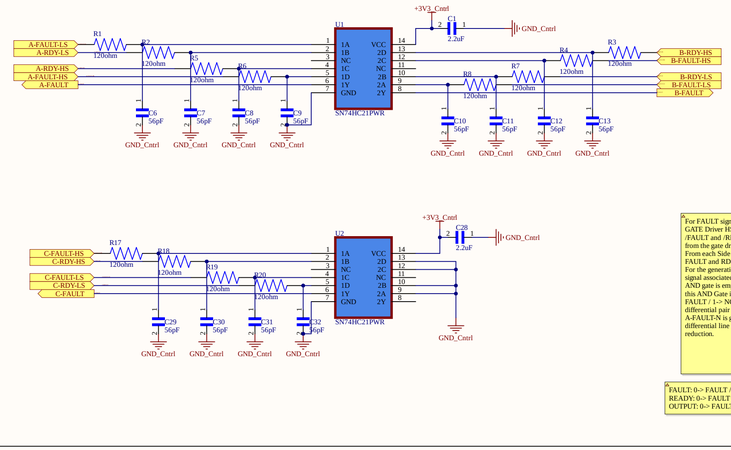


0-1200V DC BUS voltage is scaled down to 0-3V and filtered

Option B



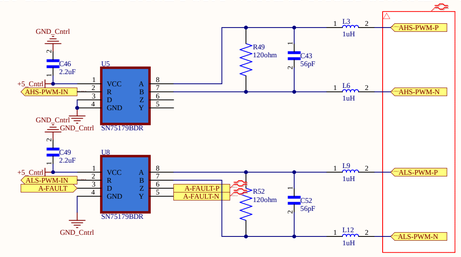
GATE DRIVER FAULT SIGNAL GENERATION STAGE (A, B, C)



For FAULT signals coming from each GATE Driver HS LS pair, the /FAULT and /RDY output signals from the gate drivers are processed. From each Side (HS and LS), a FAULT and RDY signal is produced. For the generation of ONE FAULT signal associated to each PHASE, an AND gate is employed. The output of this AND Gate is NOT-FAULT (0-> FAULT / 1-> NOT-FAULT). Then, a differential pair of A-FAULT-P and A-FAULT-N is generated from the differential line drivers for noise reduction.

FAULT: 0-> FAULT / 1-> NOT-FAULT
READY: 0-> FAULT / 1-> NOT-FAULT
OUTPUT: 0-> FAULT / 1-> NOT-FAULT

DRIVER/ RECEIVER STAGE FOR PWM AND FAULT SIGNALS - PHASE A

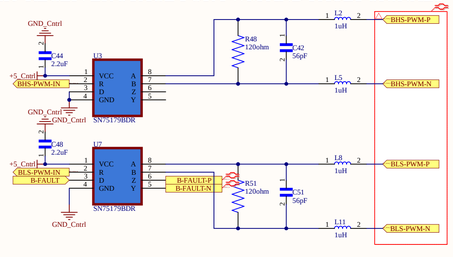


Outputs from the differential line receivers should be as close as possible to the connected IC.

Line Receivers are used to reconstruct the original HS and LS PWM signals coming from the CPU. The traces should travel togthether for less noise susceptibility.

Line Drivers are used to construct a differential FAULT signal to be sent to the controller board via the connector.

DRIVER/ RECEIVER STAGE FOR PWM AND FAULT SIGNALS - PHASE B

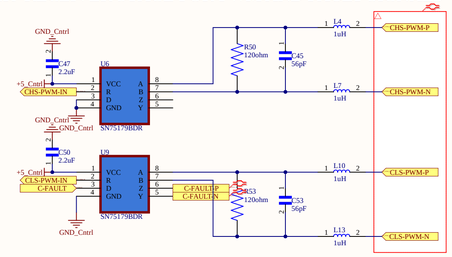


Outputs from the differential line receivers should be as close as possible to the connected IC.

Line Receivers are used to reconstruct the original HS and LS PWM signals coming from the CPU. The traces should travel togthether for less noise susceptibility.

Line Drivers are used to construct a differential FAULT signal to be sent to the controller board via the connector.

DRIVER/ RECEIVER STAGE FOR PWM AND FAULT SIGNALS - PHASE C



Outputs from the differential line receivers should be as close as possible to the connected IC.

Line Receivers are used to reconstruct the original HS and LS PWM signals coming from the CPU. The traces should travel togthether for less noise susceptibility.

Line Drivers are used to construct a differential FAULT signal to be sent to the controller board via the connector.

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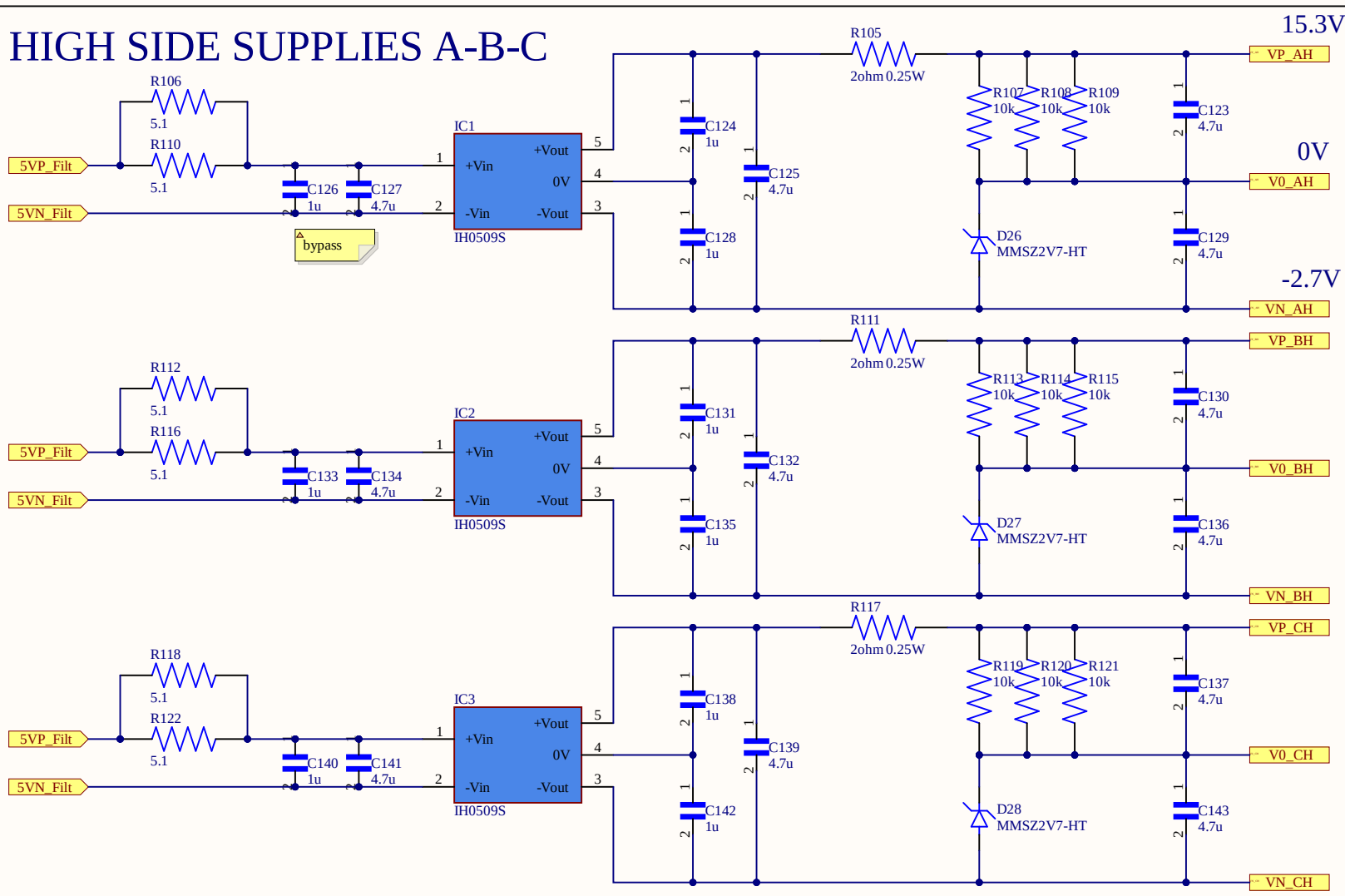
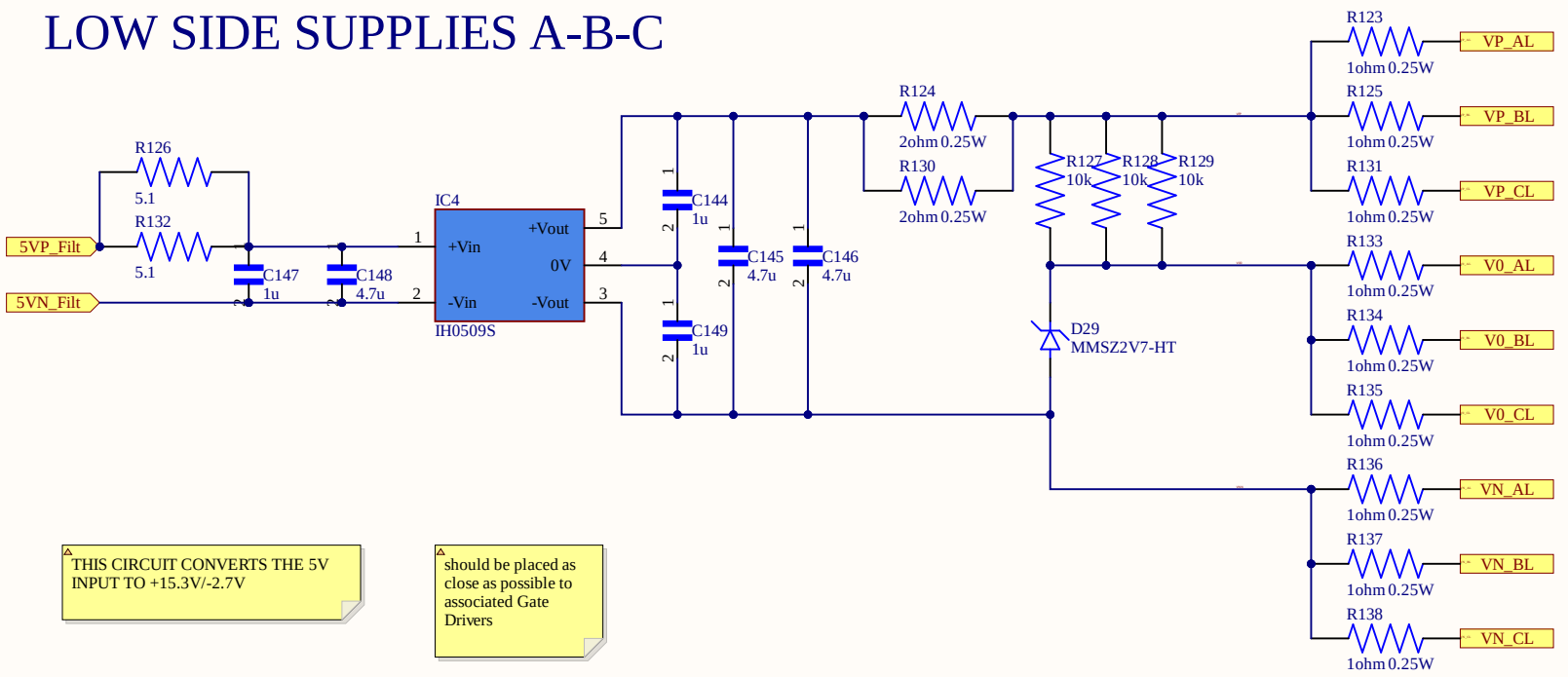
HIGH SIDE SUPPLIES A-B-C



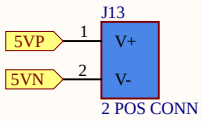
LOW SIDE SUPPLIES A-B-C



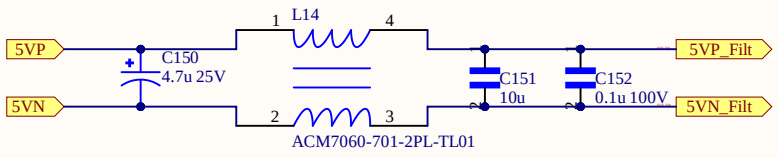
THIS CIRCUIT CONVERTS THE 5V INPUT TO +15.3V/-2.7V

should be placed as close as possible to associated Gate Drivers

5V SUPPLY



CMC for 5V



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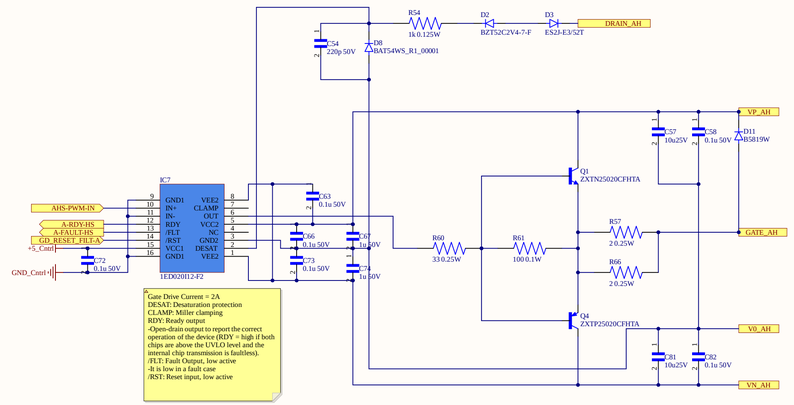
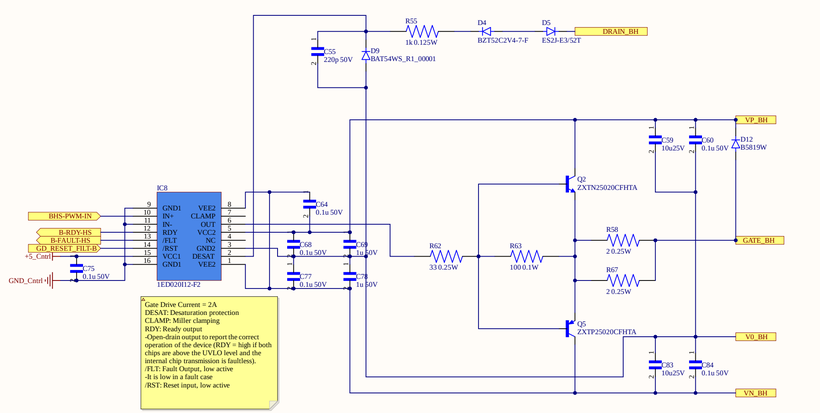
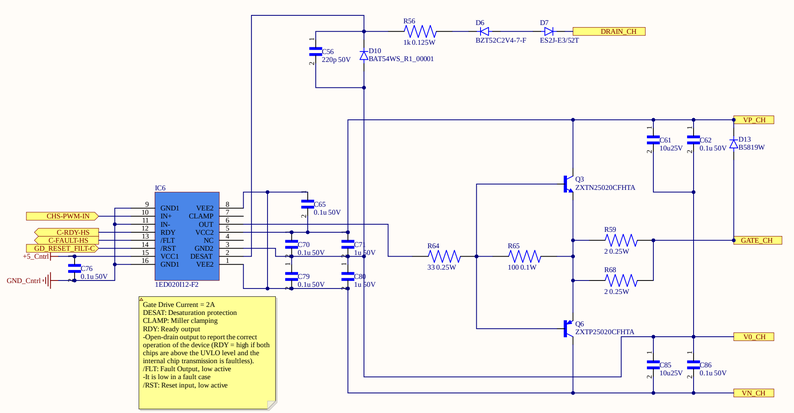
HIGH SIDE DRIVER- PHASE A



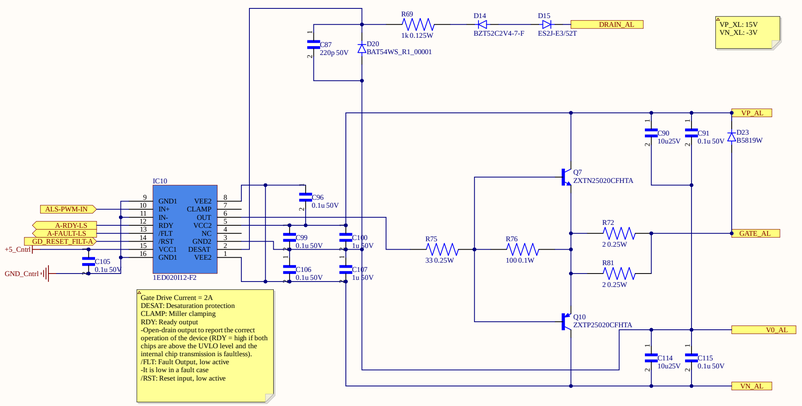
HIGH SIDE DRIVER- PHASE B



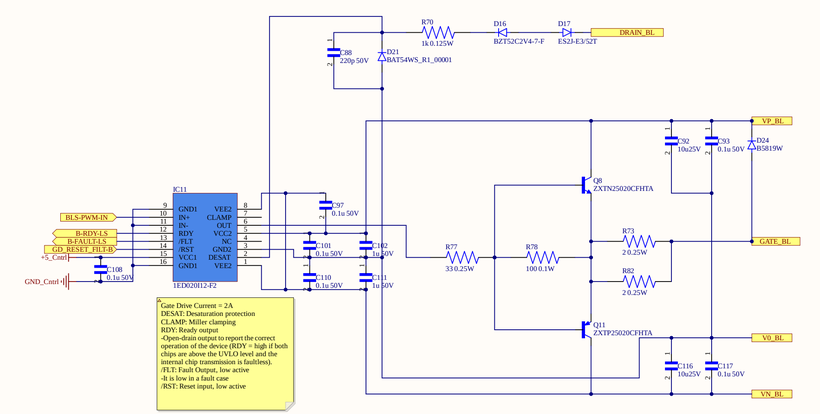
HIGH SIDE DRIVER- PHASE C



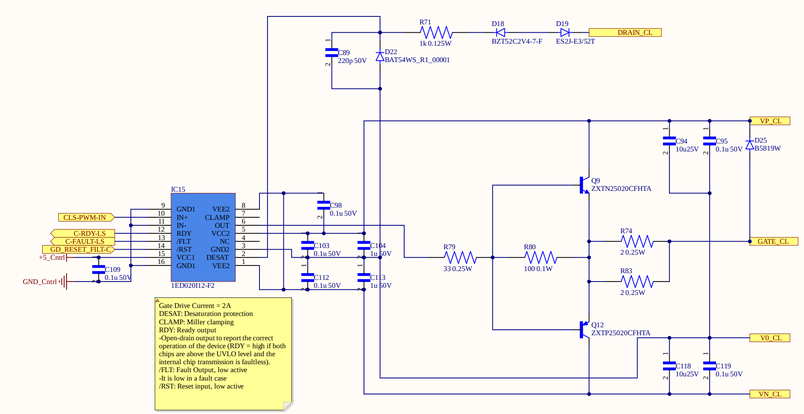
LOW SIDE DRIVER- PHASE A



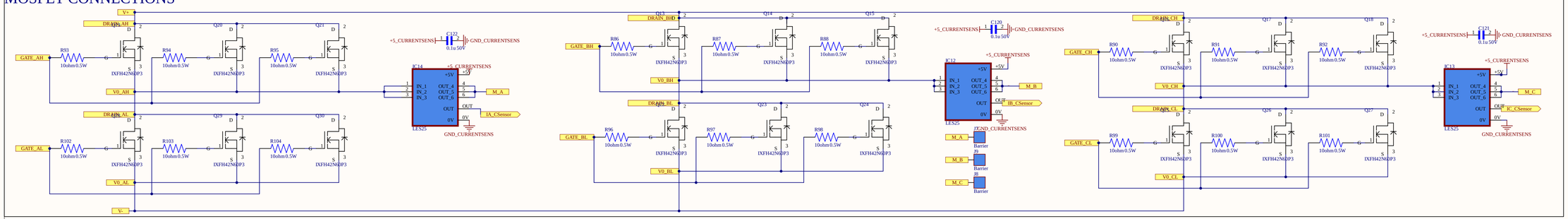
LOW SIDE DRIVER- PHASE B



LOW SIDE DRIVER- PHASE C



MOSFET CONNECTIONS



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