TRACTION MOTOR DRIVE DESIGN AND CONTROL

Motor drivers act as an interface between the power source and the motor, and mainly adjusts the speed of the employed motor. These devices provide the users with process control and energy conservation. The aim of an AC Motor Drive is to drive a 3-Phase Induction motor. To drive 3-phase motors, “Variable Frequency Drives (VFD)” are employed. VFDs convert an incoming 3 Phase voltage into a variable frequency 3 Phase output, and drive AC Motors. The block diagram of a VFD is shown in Figure 1.

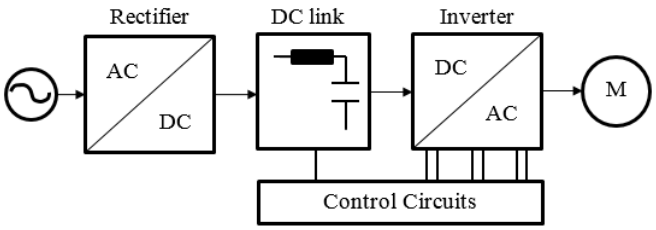


Figure 1: VFD Block Diagram

First, the negatvie components of the AC voltage is converted into positive voltage.Then, the ripples are filtered out in the DC Link stage. At the input of the inverter, there is a fixed DC voltage, which will then be converted into 3 Phase AC output of desired frequency and amplitude to drive the motor.
In this project, the input power is a high DC voltage. Thus, the rectifier stage in Figure 1 is not populated. The particular block diagram of “Traction Motor Drive Design and Control” project is shown in Figure 2.

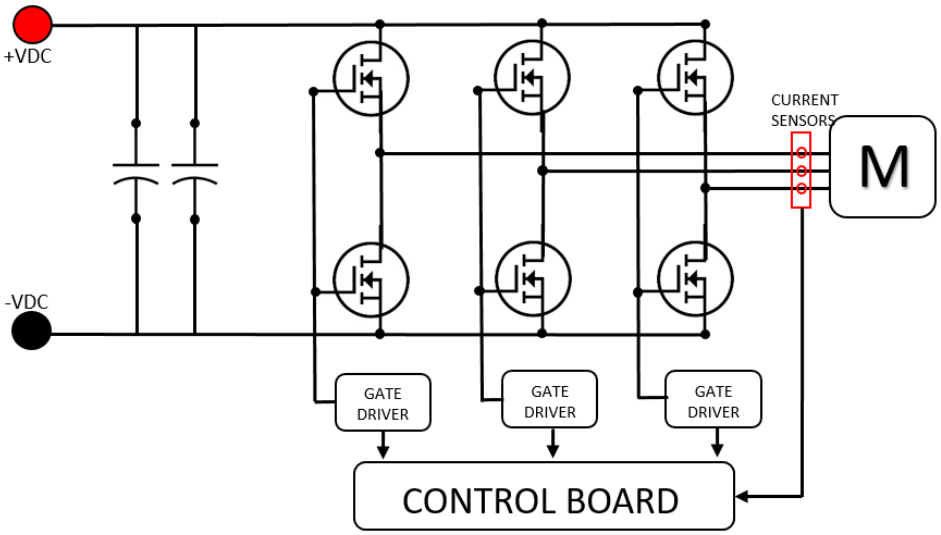


Figure 2: Block Diagram of the Project

As can be seen from the block diagram, the incoming DC voltage is filtered, and then converted into variable frequency AC voltage at the inverter stage. Inverter is designed using IXFH42N60P3 N-Channel high power MOSFETs. Each phase is controlled by two MOSFETs, and AC output is produced based on the switching of these devices. The switching application of the MOSFETs is controlled by Gate Driver circuits. These circuits take PWM signals from the Control Board and provide the MOSFETs with required switching signals. Thus, the speed of the motor is controlled by the PWM signals coming from the Control Board.
There are Current Sensors (LEM-25) at the input of the motor to check the amount of current the motor uses. The current values for each phase are fed back to the control circuit, and the required precautions are calculated and carried out.
The aforementioned process is divied into two PCB boards: Power Board and Control Board. These boards host the circuits in Table 1. Each of these circuits are explained thoroughly in the following sections.

CONTROL BOARD	POWER BOARD
1) Fault Circuit 2) Power Supply Interface 3) Current Sensor Interface 4) Voltage Sensor Interface 5) Temperature Sensor Interface 6) CAN Interface 7) F28379D-LAUNCHPAD 8) Gate Driver Interface 10) Resolver	1) V-BUS EMI Filter 2) Gate Driver Fault Circuit 3) V-BUS Voltage Sensing Circuit 4) DCDC Converter Stage for The Power Supply of Gate Drives 5) Gate Driver Circuits 6) Driving MOSFET Connections

Table 1: The Contents of Boards

1) Controller Board Circuit Explanations

1.1) FAULT CIRCUIT

This circuit is impelemented to shut the operation of the Motor Driver by generating a fault signal. This circuit is used as an external fault detection application in which the current measurements from the Current sensors and the DC Bus voltage are controlled. This operation is carried out using Comparators, particularly LM339.

Fault scenarios based on the Current Sensors

The current sensor (LEM LES25-NP) will output a voltage between 0.5V and 4.5V, which represent -25A and +25A respectivelly. For instance, if the amplitude of the current output is desired to be between -12.5A and +12.5A, the output voltages should be in the range of 1.25V and 3.75V. The Voltage/Current output graph of the current sensor (LES 25 NP) is shown in Figure 1.1.1.

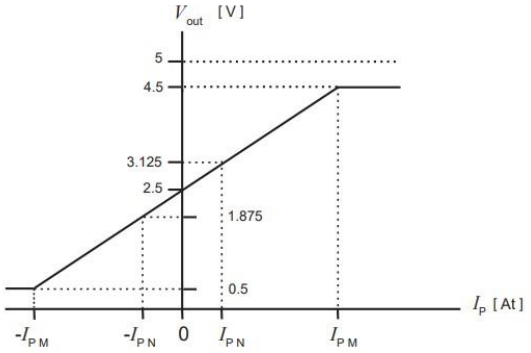


Figure 1.1.1: Voltage/Current graph of the Current Sensor
Retreived from LES 25 NP Datasheet

I_{PN}: Primary Nominal RMS Current (25A)
I_{PM}: Primary Current Measuring Range (-80A to 80A)

Based on the requirement that the output of LES25 should be between 1.25V and 3.75V, we shall build a circuit that produces a FAULT signal if the voltage is NOT in the aforementioned range. To build this circuit, LM339, a low power comparator is selected. With this device, four different conditions can be analyzed simultaneously. The pin diagram of LM339 is shown in Figure 1.1.2.

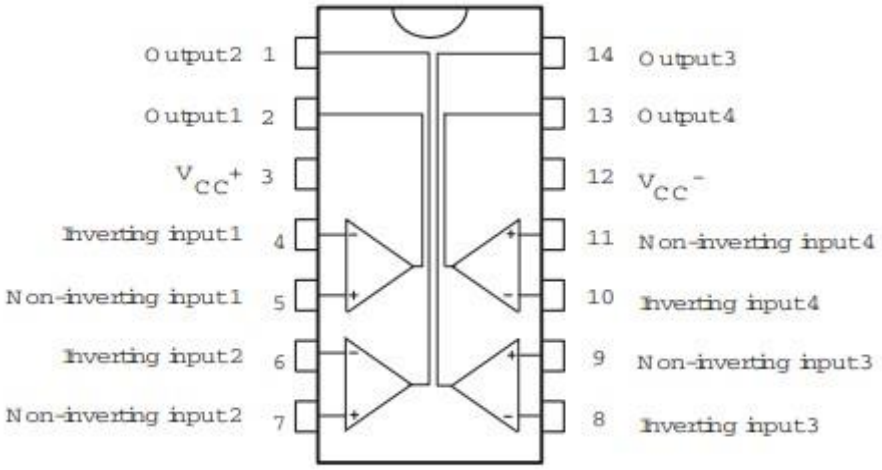


Figure 1.1.2: Pin diagram of LM339

Comparator circuits simply compare two voltages. The output of such a device is digital (either HIGH or LOW) depending on the voltage values of the inverting and non-inverting inputs. The principle of the operation is that if the voltage value at the inverting input (-) is greater than the non-inverting(+) input, the output is LOW, and vice versa.

The output of the comparator circuit results in a $\overline{FAULT}$ signal, meaning that FAULT = LOW, NO-FAULT = HIGH. The cases are as follows: (Refer to Figure 1.5 for the schematic)

- If the output voltage of a Current Sensor (VX_Filtered) is less than LowLimit (1.25V), which is a faulty case, the output of that condition will be LOW. If VX_Filtered is higher than the LowLimit, which is a non-faulty case, the output will be HIGH.
- If the output voltage of a Current Sensor (VX_Filtered) is less than HighLimit (3.75V), which is a non-faulty case, the output of that condition will be HIGH. If VX_Filtered is higher than the HighLimit, which is a faulty case, the output will be LOW.

To simulate this operation, the circuit shown in Figure 1.1.3 was set on Proteus, and simulated. The simulation result is shown in Figure 1.1.4. The desired input/output table is shown in Table 1.

VX_Filtered (V)	FAULT
1.25V < V < 3.75	NO (HIGH)
3.75V < V	YES (LOW)
V < 1.25V	YES (LOW)

Table 1: Desired Fault Cases

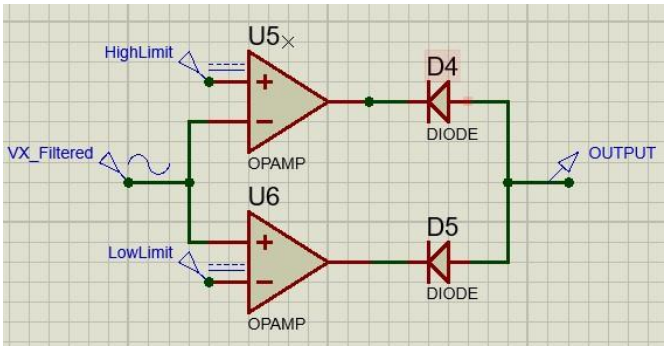


Figure 1.1.3: The simulated circuit

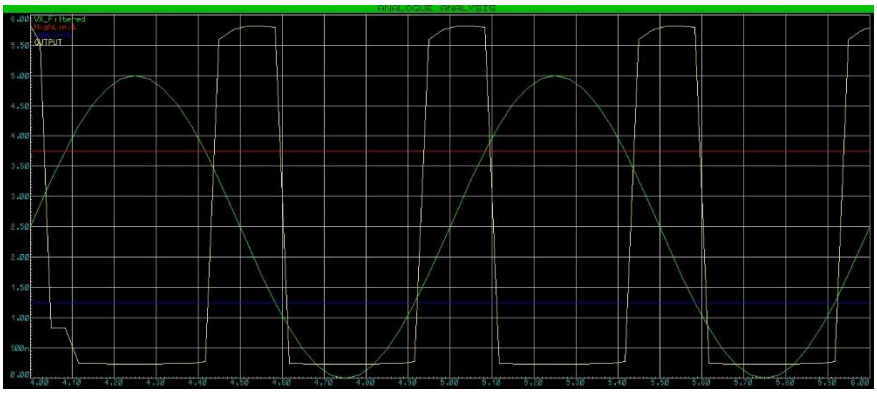


Figure 1.1.4: Simulation results

When VX_Filtered (Green) is in the range of non-faulty voltages, the output (Yellow) is HIGH, else it is LOW. Following this logic, the circuit shown in Figure 1.1.5 and Figure 1.1.6 are designed. In case either one of the fault checks are not needed, the DNP resistors will be populated to create automatically non-fault (HIGH) output.

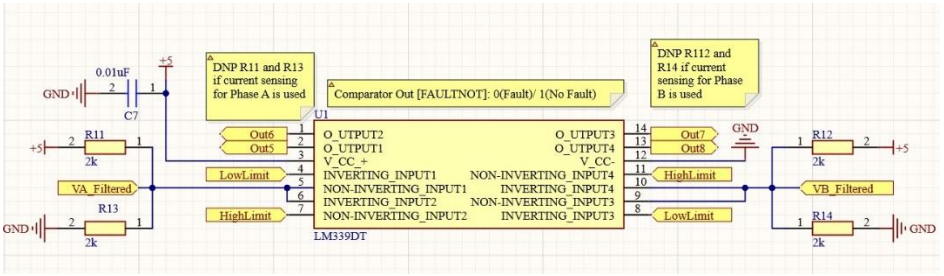


Figure 1.1.5: A and B phase current sensors fault check.

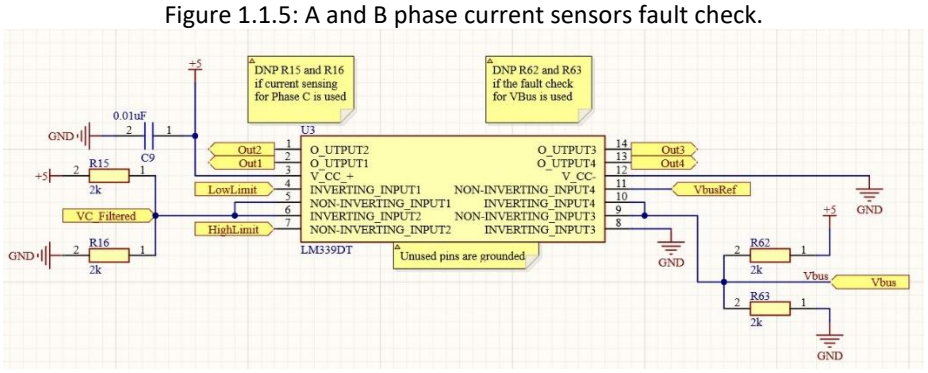


Figure 1.1.6: C phase and VBus fault check.

The reference voltages for the comparator circuit are obtained using the following voltage divider circuitry shown in Figure 1.1.7.

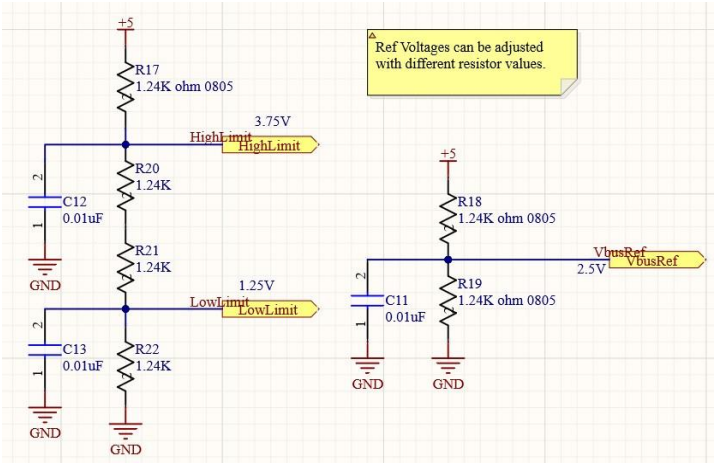


Figure 1.1.7: Voltage Divider circuits for reference voltages

The outputs of the comparator circuits must be connected to Diodes. The reason for that is, when there is a FAULT case, meaning that when the OutX is LOW (0V), CVSense_Fault (Another fault signal that is connected to DSP) will be tied to the LOW voltage. If there is a NO-FAULT case, OutX is HIGH (5V), and there will not be a voltage drop on the pull-up resistor and the input to the inverter will be HIGH (3.3V). Moreover, since the output of the comparator circuit is $\overline{FAULT}$, an inverter is required for the SR-Latch input. SR-Latch is required for shutting down the PWM signals, and keeping them shut down untill the reset signal (SR-Reset) is sent. The circuitis shown in Figure 1.1.8.

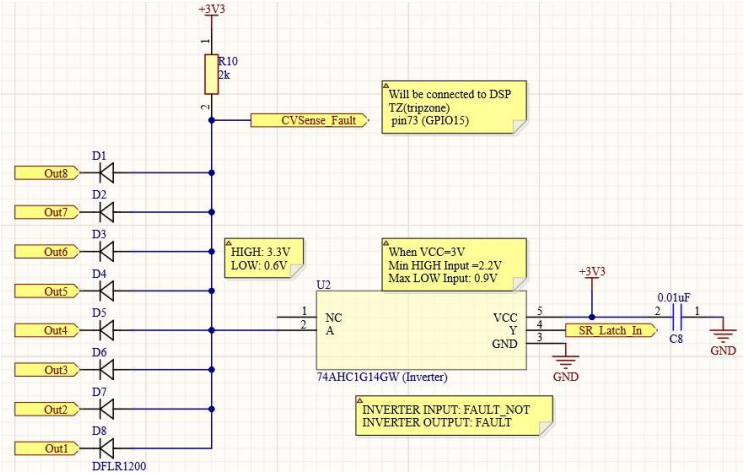


Figure 1.1.8: Diodes and Inverter connections

At the output of the inverter is FAULT signal, which is connected to the SR Latch (HEF4043BT). The SR Latch output is connected to Differential Line Driver Enable input for the PWM signals to shut down the operation in case of a failure. The SR Latch Connections are shown in Figure 1.1.9.

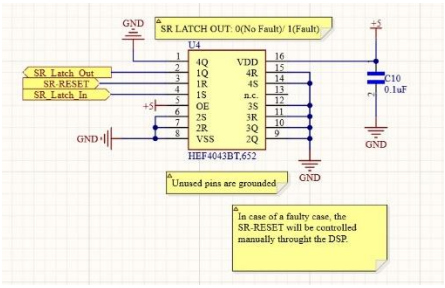


Figure 1.1.9: SR Latch connections

SR Latch reset is connected to a GPIO output of the DSP. In an erronous case, the SR-Latch out will be HIGH, and then the SR-RESET input will be controlled manually through the DSP, and the process will be restarted.

To sum up, Fault Circuit is used to control the operation conditions based on the current sensor outpus and VBUS voltage. In case of an overvoltage or undervoltage, the operation will be shut down for protecting rest of the circuits.

1.2) Power Supply Interface

This circuit aims to provide the rest of the circuitry with clean and sufficient power. The input to the supply circuit is 12V battery connections. This voltage should be filtered and converted into 3.3V and 5V to provide the ICs with sufficient power.
Firstly, a common mode choke (CMC) is applied to the battery voltage. The contribution of a CMC to the circuit is that it attenuates the common mode noise. It is used to reduce the EMI components on the power supply. The common mode choke connections are shown in Figure 1.2.1.

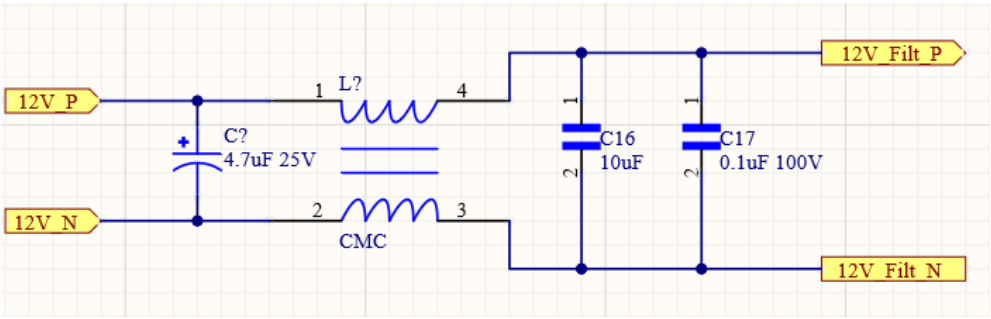


Figure 1.2.1: Common Mode Choke Connections
Part Number: ACM7060-701-2PL-TL01

After filtering the battery power, the 12V should be converted into the other voltages. Voltage regulaters are used to convert it to 3.3V and 5V. The voltage requlator circuits are shown in Figure 1.2.2.

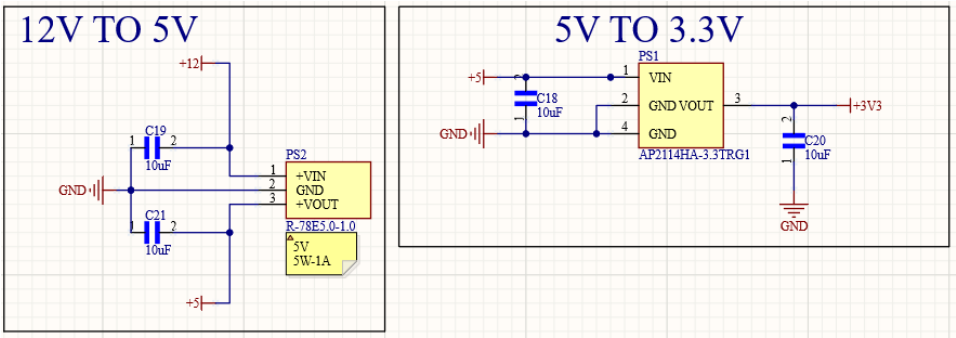


Figure 1.2.2: The voltage requlator circuits for 3.3V and 5V conversion.

R-78E5.0-1.0 is employed for 12V to 5V conversion, and AP2114HA-3.3TRG1 is employed for 5V to 3V3 conversion.

1.3) Current Sensor Interface

This circuit processes the Current Sensor outputs and sends them to Fault circuit and DSP. IX_CSensor refers to the output of the current sensor for the associated phase. IX_Filtered is connected to the Fault Circuit for external fault control, and Current-X iss connected to DSP. The connector that connects to the Power Board current sensor outputs is shown in Figure 1.13.1, and the anti-aliasing filter circuit is shown in Figure 1.3.2. Anti-aliasing filters are populated to attenuate the high frequency noise so that the DSP will operate more accurate.

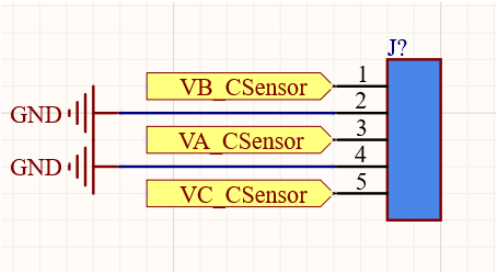


Figure 1.3.1: Connector connections

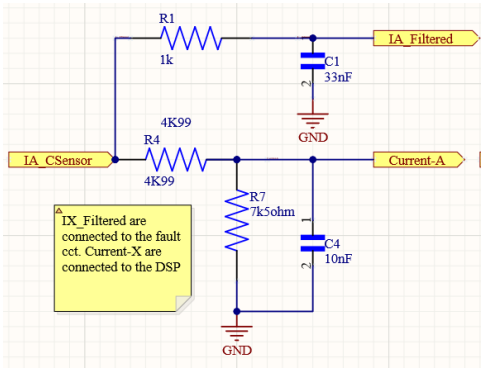


Figure 1.3.2: Current Sensor Interface Circuit

1.4) Voltage Sensor Interface

Voltage values will be found using estimation methof with the PWM signals. Thus, only an anti-aliasing filter is placed between the XHS-PWM and Voltage-X. This circuit is shown in Figure 1.4.1.

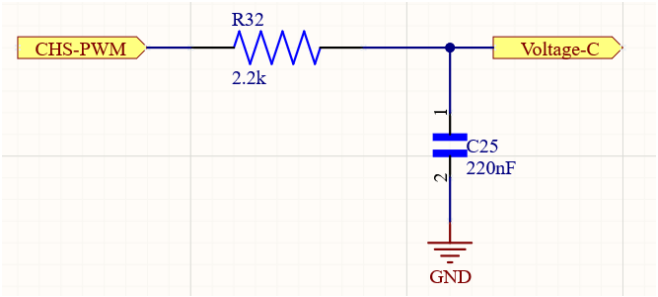


Figure 4.1: Voltage Sensor Interface Circuit

1.5) Temperature Sensor Interface

This circuit is used to obtain the temperature of Bus capacitors, Bus Bar and three IGBTs. The output of the thermisor is filtered in the interface circuit and sent to DSP for control. The connector connections of the temperature sensor interface is shown in Figure 1.5.1, and the circuit is shown in Figure 1.5.2.

Termocouple: https://urun.n11.com/arduino-urunleri-ve-setleri/k-tipi-termokupl-0-800c-P426199755?utm_source=comp_cimri&utm_medium=cpc&utm_campaign=cimri_genel

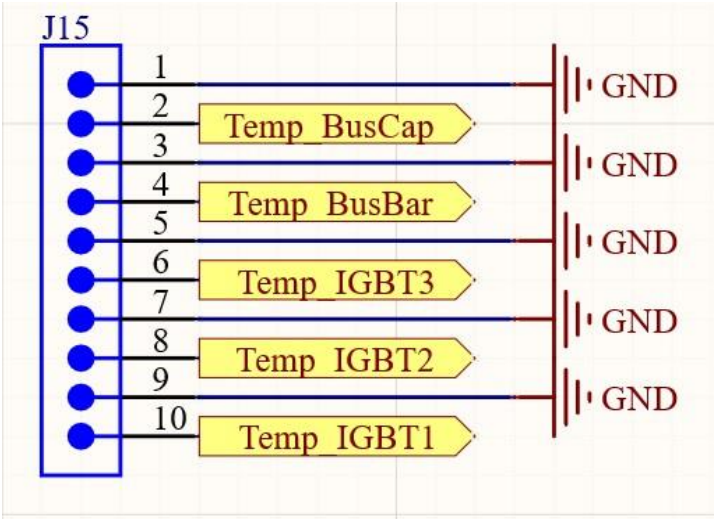


Figure 1.5.1: The connector connections

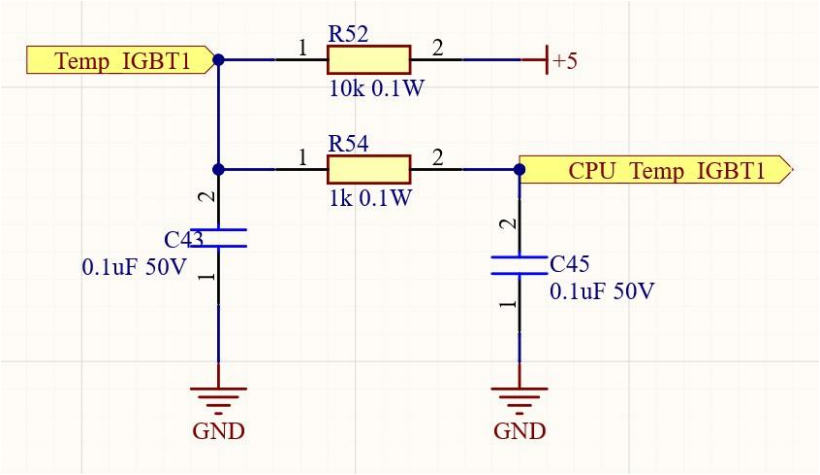


Figure 1.5.2: Temperature sensor interface circuit

1.6) CAN BUS Circuit

This circuit is used for CAN Bus lines (CANH and CANL) to be converted to TX and RX signals via a CAN Transceiver. The CAN Transceiver connections are shown in Figure 1.6.1.

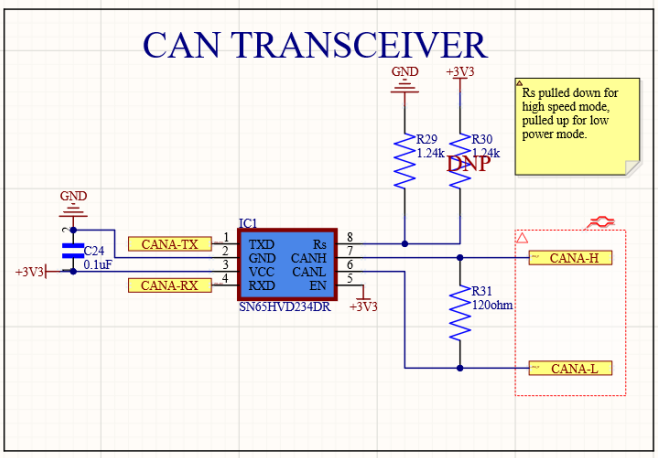


Figure 1.6.1: CAN Transceiver Conections
Part Number: SN65HVD234DR

CAN Transceivers convert the differential CAN pair (CANH and CANL) into TX (transmit) and RX (receive) signals. CANH and CANL signals are separated from each other by a terminating resistor, 120-ohms. There can not be a direct connection between CANH-L pair and an MCU. Transceivers converts them into TX and RX. TX and RX signals are connected to MCUs (TX to RX/ RX to TX).
CAN Port pinout is shown in Figure 1.6.3. CAN Bus differential signals (CANH/CANL) are transferred via J3A. Also, a UART differential signal was interated to this circuir in case of a further need. The UART pair is also connected to DSP.

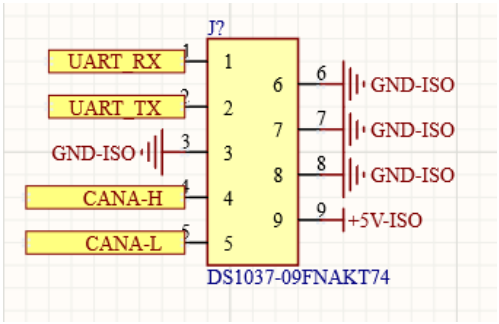


Figure 1.6.3: CAN port pinout

1.7) DSP Connections- TI LAUNCHXL F28379D

Global Fault

There are two FAULT circuits in this controller board. First one is the fault circuit for the current sensor and bus voltage (refer to section 1). The output of this circuit is CVSense_Fault ($\overline{FAULT}$).
Second one is the Gate Driver fault outputs (X-FAULT). These signals are also $\overline{FAULT}$. In case of faulty case, the corresponding LEDs will turn ON.

In order to manage all the FAULT signals at one output, a quadrature AND Gate is employed. If any of CVSense_Fault or X-FAULT are faulty (LOW), the AND gate will have LOW signal at the output. This brings us to the conclusion that the AND Gate output is also $\overline{FAULT}$. A HIGH signal is generated only if all the Fault signals are HIGH. The Global Fault circuit is shown in Figure 1.7.1.

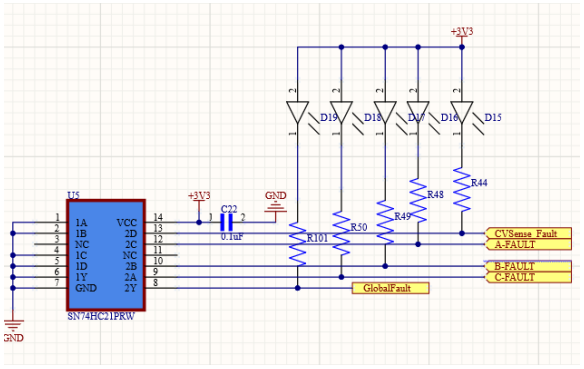


Figure 1.7.1: Global Fault Circuit

DSP Connectors

The Connector designators on Altium Schematics and the actual designators on Launchpad do not match. See the notes next to the connectors to locate the actual connectors on the DSP. In Figure 1.7.2, the connectors for Quadrature encoders, ground and CAN-B Bus connections (There are two CAN Bus on this board. CAN-A and CAN-B) are presented. For all the power connections (3.3V, 5V), a 0-ohm DNP resistors are placed. The reason for these DNP resistors is that the DSP will be either powered by the USB cable provided in the package or the power line from the power circuit. When the DSP is powered by the USB cable, the power from an external circuit is not necessary, thus the DNP resistors shall not be populated.

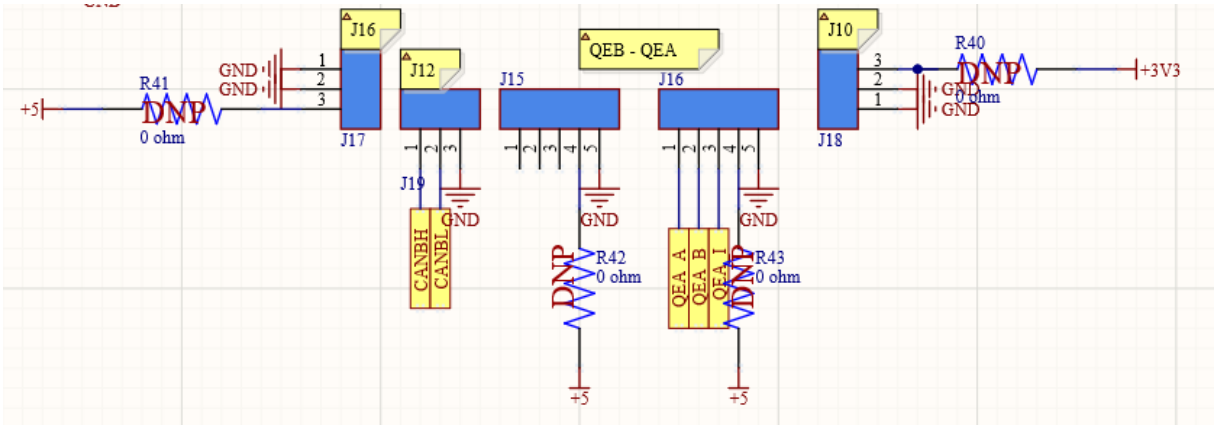


Figure 1.7.2: DSP Connector connections

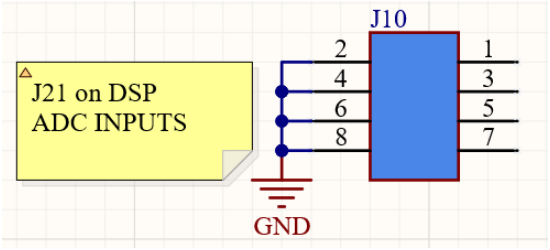


Figure 1.7.3: J21 on DSP

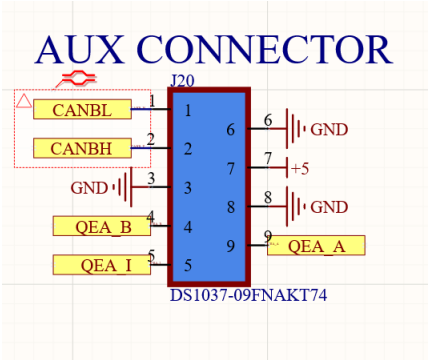


Figure 1.7.4: AUX connector for QEX and CANB

Case LEDs

These LEDs are connected to DSP GPIO. These indicators will be used if a certain activity needs to be pointed out on the Controller Board. The built circuit is shown in Figure 1.7.5.

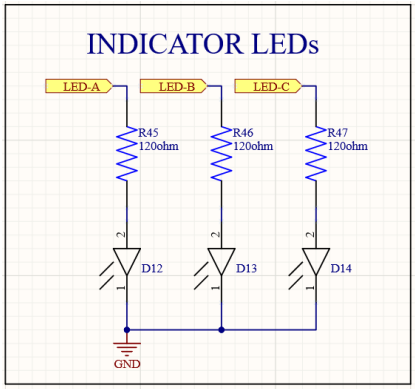


Figure 1.7.5: CASE LED connections

DSP Main Connectors

The connection diagram for the main connectors are shown in Figure 1.7.6 and Figure 1.7.7. The actual connector designators are indicated in the notebox next to each connector.

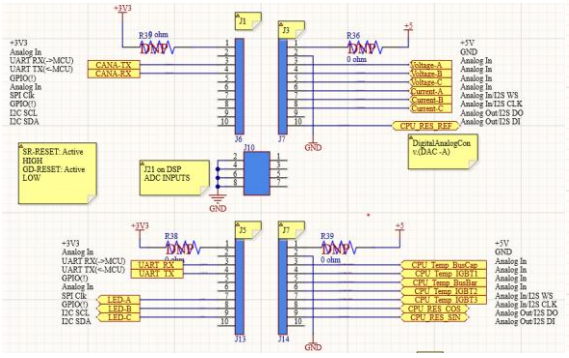


Figure 1.7.6

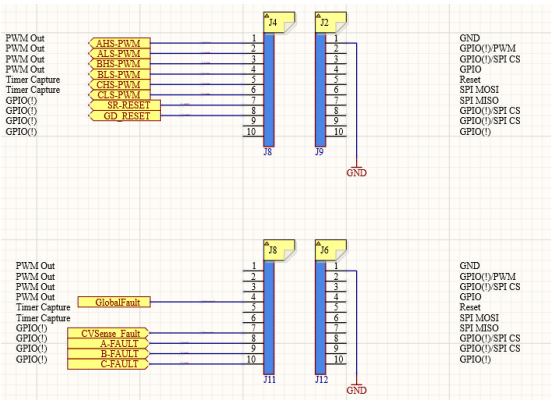


Figure 1.7.7

1.8) Gater Driver Interface Circuit

Signal integrity has an upmost importance when controlling power devices with a gate driver. Gate drivers are susceptible to EMI or any noise generated by power devices. Power devices has extremely high switching frequencies and create dense EMI which can easily couple on gate control signals. To prevent any interference, differential signals are used for this gate driver design.

Differential signals reduce the effect of the noise that is created during the switching events. A single ended signal can be converted into a differential pair by transmitting both the original signal and its complement in two closely coupled wires. Then, these two signals are compared to reconstruct the original signal. In Figure

1.8.1, the noise immunity of differential signals and reconstruction of the original signal from the differential pair is shown.

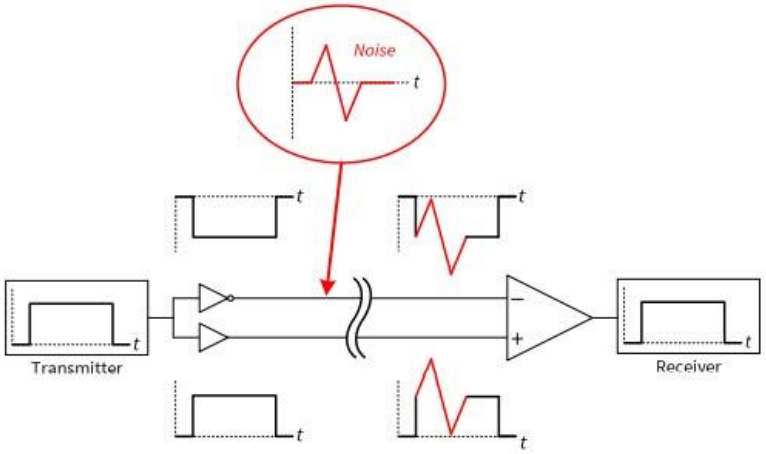


Figure 1.8.1: Noise immunity and reconstruction

In this design, HS-PWM, LS-PWM and FAULT outputs are differential signals. It is recommended to keep a ground plane under the signals.

In the circuit, the differential pairs for XHS-PWM, XLS-PWM are created using AM26LV31EIPWR quadruple differential line drivers. The associated circuit is shown in Figure 1.8.2 and Figure 1.8.3.

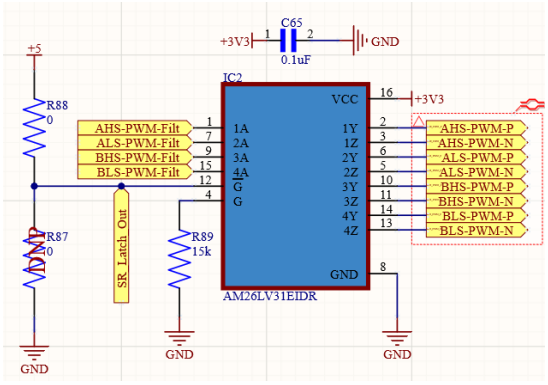


Figure 1.8.2: Differential signal generation for AHS, ALS, BHS, BLS PWM signals.

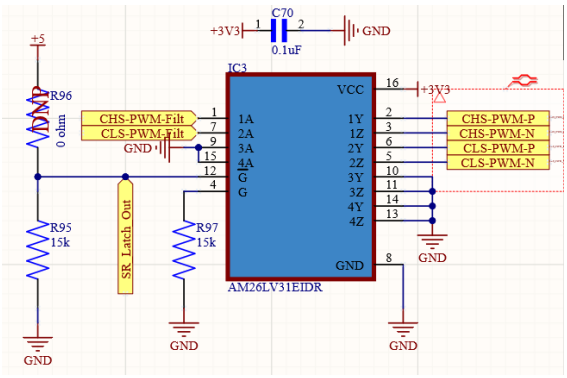


Figure 1.8.3: Differential signal generation for CHS and CLS PWM signals.

SR Latch Output is connected to these differential line driver ICs. In a faulty situation, SR Latch Out will be HIGH. G' will be controlled by SR Signal. If Faulty Signal comes (SR HIGH), G' will go High and the IC will be disabled.

Enable Mechanism of AM26LV31EIDR: The transmitter outputs are enabled when either G is set to logic HIGH or G' is set to logic LOW.The reverse disables the outputs (G = LOW, G' = HIGH). G will be always pulled down.

Also, there are differential FAULT signals comming from the Gate Drivers via the connectors. These X-FAULT-P and X-FAULT-N signals are connected from the gate driver circuit (Power Board) to gate driver interface circuit (Control Board). Connector diagrams are shown in Figure 1.8.4.

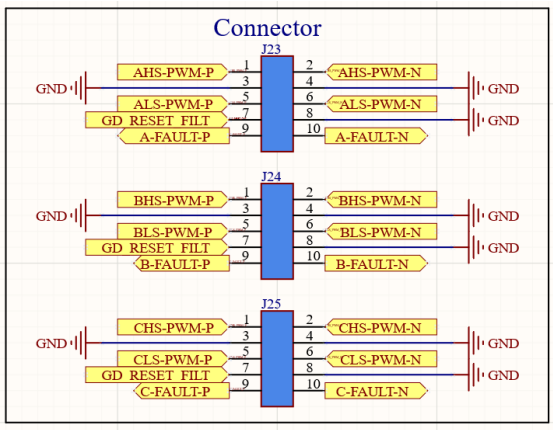


Figure 1.8.4: Gate Driver Interface Connector Diagrams

Then, the FAULT differential pairs are filtered with an LCR filter to be sent to quadruple differential line receiver (SN75LBC175ADR) for the reconstruction of original FAULT signals. The filters are shown in Figure 1.8.5 and the frequency characteristics of the filter is shown in Figure 1.8.6.

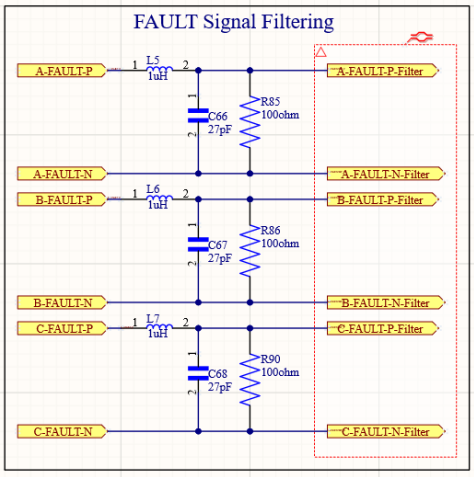


Figure 1.8.5: LCR Filters

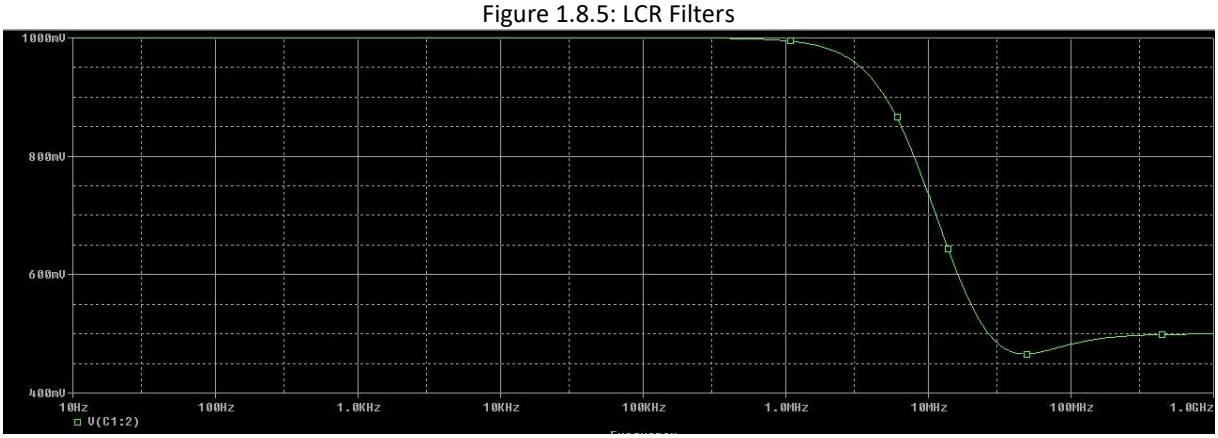


Figure 1.8.6: Frequency characteristics of the filter (Cut-off ~= 10MHz)

After filtering, the signals are sent to the quadruple differential line receiver. This circuit is shown in Figure 1.8.7.

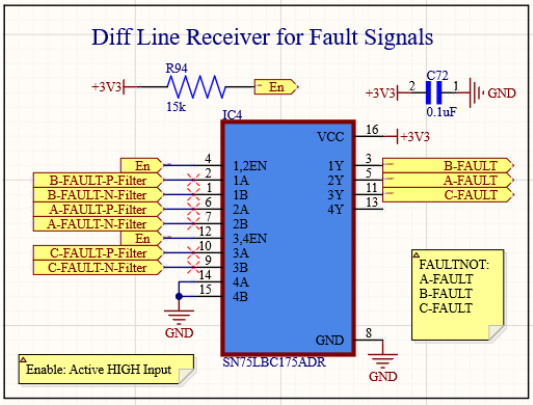


Figure 1.8.7: Quadruple Differential Line Receiver

At the Line Receiver, the FAULT signals are reconstructed from their differential pairs. The principle of this operation is in Figure 1.8.1.

1.9 Resolver

A resolver is a type of rotary electrical transformer used for measuring degrees of rotation. It is considered an analog device, and has a digital counterpart, the rotary (or pulse) encoder.

2) Power Board Circuit Explanations

2.1) DC BUS EMI filter

EMI filters are placed after the DC Power supply (B+, B-)in order the filter out the EMI and other interferences that are present on the power. This stage is crucial for the accuracy and precision of all the circuitry on the board. The filtering stage is shown in Figure 2.1.1.

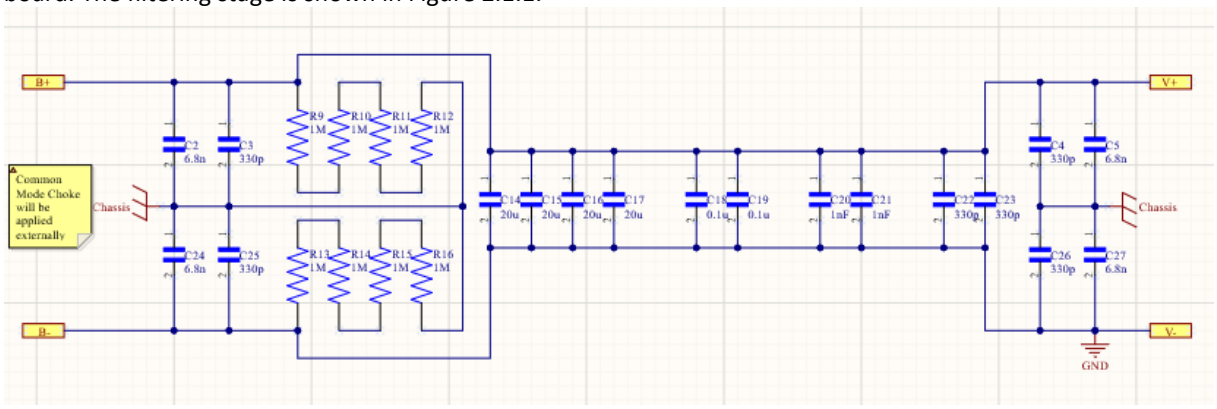


Figure 2.1.1: V BUS Stage (EMI Filtering)

At the start and the end of the Filtering are Y Caps. Y Caps are designed to filter out the common-mode noise, and are connected between the line and chassis. These caps filter the coupling between the ground and the power line. It is extremely critical for these caps not to be short circuitted since it will create a shock risk for the users.

It is important to note that the voltage limits for these CAPS should be high enough to withstand the amount of power (+400DC). All the capacitors in the EMI circuit are film caps, which often have higher voltage limits.

The resistors after the first Y-Caps stage are placed there to absorb the high energy. When the high voltage is charged to the film caps, it does not discharge immediatelly and keeps the voltage there. The populated resistors help the discharge application.

The 20uF caps are employed to filter out the lower frequency ripples. After that, there are pairs of 0.1uF, 1nF and 100pF capacitors for precise high frequency filtering. Three different capacitance values are used for filtering the higher frequencies better. Capacitors have different impedances depending on the signal frequency, and their filtering capacity changes. The Impedance-Frequency graph of capacitors based on different capacitence values are shown in Figure 2.1.2. Impedance of a capacitor is calculated as follows:

$$X_C = \frac{1}{2\pi f C}$$

Thus, placing different capacitors provides the system with enhanced filtering capacity. There are two of each caps in the system. These caps will be put at the sides of the board symmetrically.
The capacitors actually include an LCR circuit in them. At certain frequencies, the capapcitors enter the resonance. By applying various capacitors, the filtering capacity of the system is enhanced.

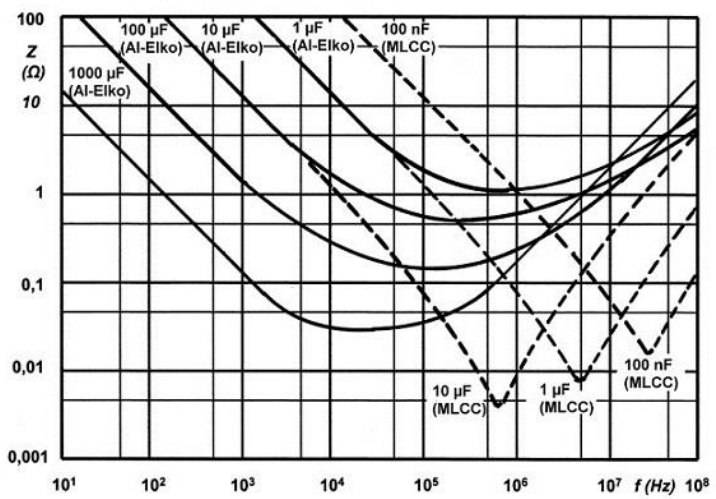


Figure 2.1.2: Impedance vs Frequency for various capacitances

2.2) Gate Driver $\overline{FAULT}$ Circuit

The $\overline{FAULT}$ is generated based on the RDY and /FLT outputs of the Gate Drivers. Each Gate Driver produces a RDY and a /FLT output.
RDY: Open-drain output to report the correct operation of the device (RDY = high if both chips are above the UVLO level and the internal chip transmission is faultless). ***Meaning that, 0 is Faulty and 1 is Non-faulty case.***
/FLT: Open-drain output to report a desaturation error of the IGBT (/FLT is low if desaturation occurs). ***Meaning that, 0 is Faulty and 1 is Non-faulty case.***
For each phase, two gate drivers are employed (For High Side and Low Side). Thus, there will be four fault signals to generate a main fault signal for each phase. These signals are connected to a quadrature AND Gate to produce a main $\overline{FAULT}$ signal.
The AND Gate stage for Phase-C is shown in Figure 2.2.1.

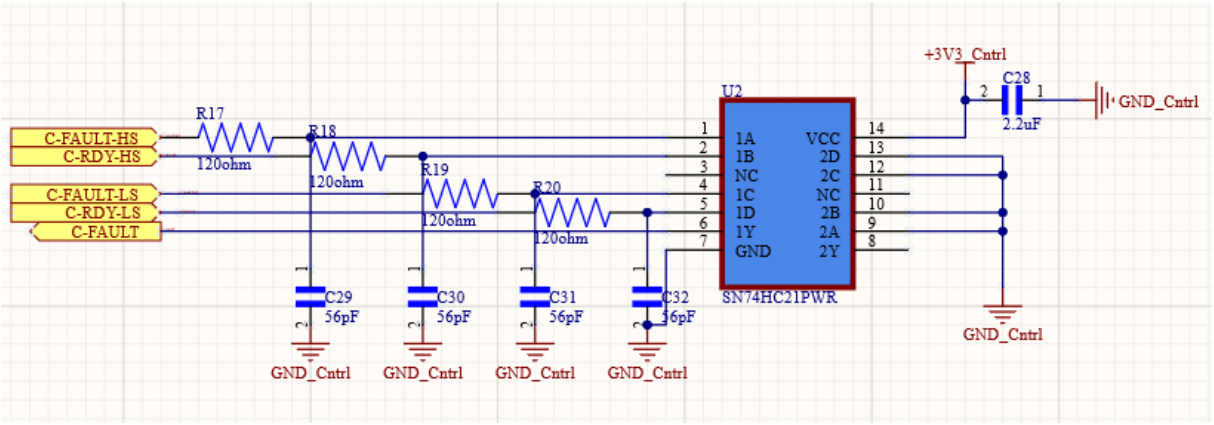


Figure 2.2.1: AND Gate Fault signal stage

The output signal is X-FAULT, which is then connected to a differential line driver to produce X-FAULT-P and X-FAULT-N differential pair. This differential pair is tied up to the connector to be sent to Controller Board Gate Driver Interface. The differential pair in the control borad is then connected to a Differential Line receiver to reconstruct the original $\overline{FAULT}$ signals. This $\overline{FAULT}$ signals are sent to Global Fault generator circuit. This process is repeated for all three phases (A, B, C). At the end, Fault signals are named as A-FAULT, B-FAULT and C-FAULT. On the Gate driver Circuit, a different type of IC is used for differential line driver and receiver application. SN75179BDR functions as both driver and receiver. Its functional block diagram is shown in Figure 2.2.2.

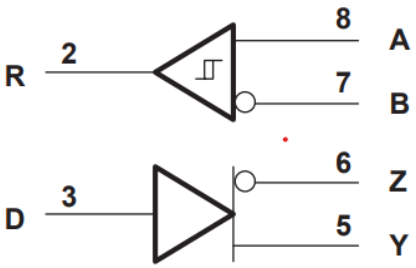


Figure 2.2.2: Functional Block Diagram of SN75179BDR

Differential HS and LS PWM signal are coming from the controller board via the connector, and differential FAULT signal is sent to controller board via the same connector. To suit this application, SN75179BDR is employed with the following circuit in Figure 2.2.3.

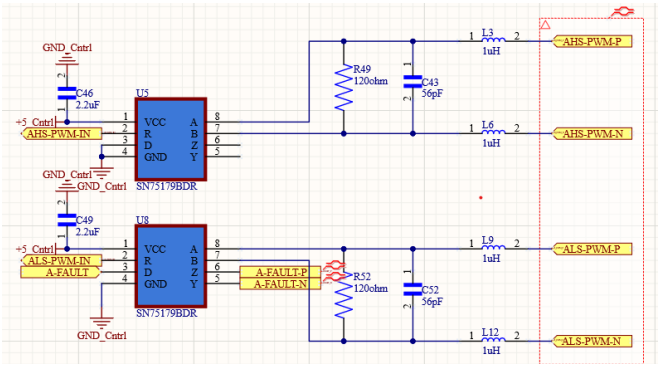


Figure 2.2.3: Differential Line Driver/Receiver Circuit

As can be seen, High Side and Low Side PWM differential signals are connected to the receiver inputs after an LCR filter to reconstruct the original PWM signals. These PWM signals are connected to Gate Drivers. Single ended FAULT signal is connected to line driver to produce a differential FAULT signal to be sent to the controller board.

2.3) VBUS Voltage Sensing Circuit

V Bus voltage measurement is important to track the operation conditions of the system. A high voltage is first scaled down to 0-3V band, and then sent to the DSP. Fort his operation, there are two options in the design. These options are shown in Figure 2.3.1 and Figure 2.3.2.

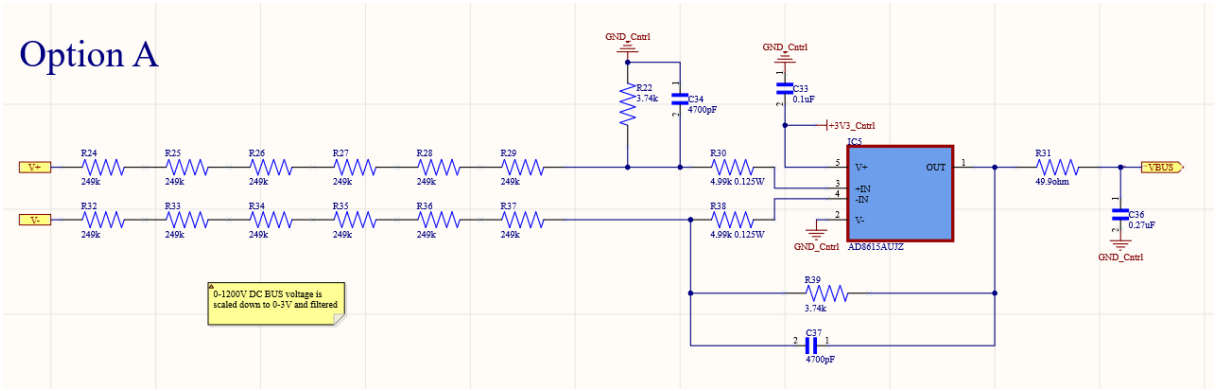


Figure 2.3.1: Option A for VBUS Measurement

In this option, the high voltage is scaled down to a low voltage using the resistors and then the filtering is applied.

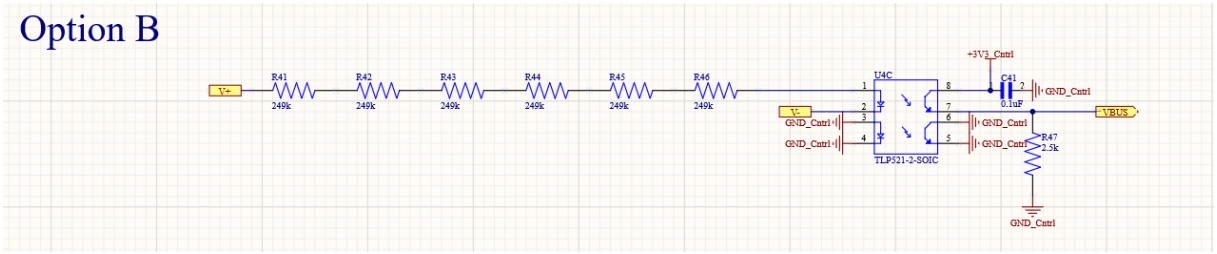


Figure 2.3.2: Option B for VBUS Measurement

In this option, the same voltage scaling method was applied, yet this time the voltage measurement is isolated from the incoming voltage side.

One of these options will not be populated on the PCB.

2.4) DCDC Converter Stage for The Power Supply of Gate Drives

The DCDC power supplies for the gate drives will be VP_XH= 15.3V and VN_XH= -2.7V. This procedure will be carried out by IH0509S, a 5V to +9V/-9V DCDC converter. The power distribution for the High Side Drives are shown in Figure 2.4.1.

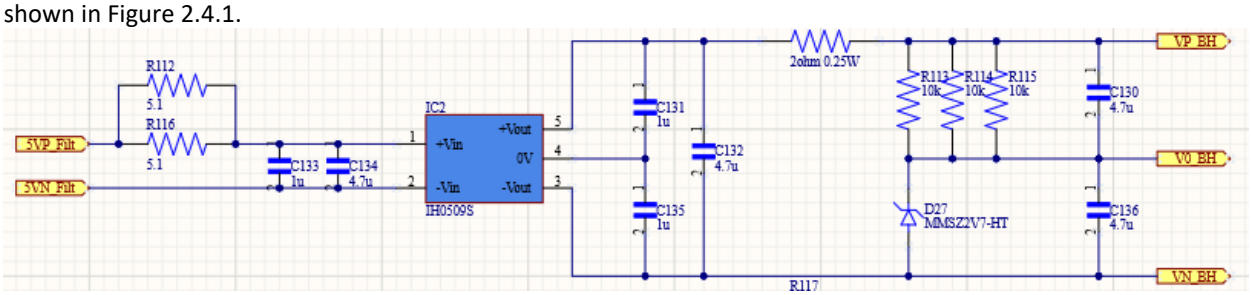


Figure 2.4.1: Power conversion for High Side Gate Drivers

The capacitors on the left side are bypasss caps for IH0509S. In the next stage, there are caps and resistors to eliminate the ripples, and a Zener Diode (V=2.7V) to keep the difference between 0V and VN_XH at 2.7V. This way, VN_XH will be -2.7V and the VP_XH will be 15.3V. This circuitry will be populated three times for A, B, and C phases. Then, these will be connected to Gate Drives. A similar logic is applied for the Low Side Drives, however there will be only one circuit for all the phases as shown in Figure 2.4.2.

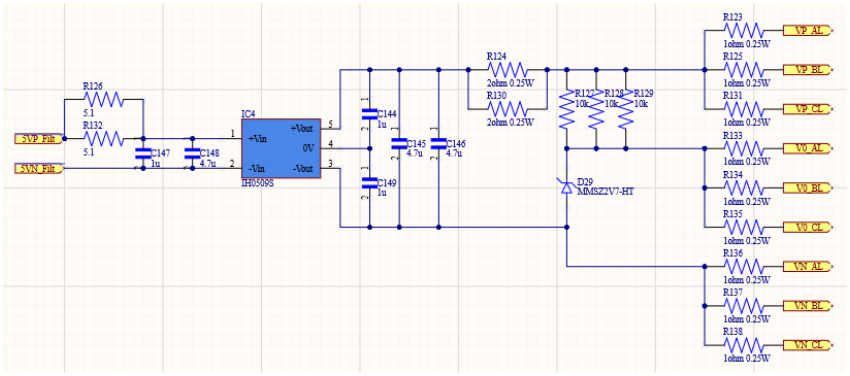


Figure 2.4.2: Power conversion for Low Side Gate Drivers

2.5) GATE DRIVERS

Gate driver circuits for High Side and Low side are shown in Figure 2.5.1 and Figure 2.5.2. The Gate Driver IC is capable of supplying 2A to the driving MOSFETS. With the build BJT circuit, this current capacity is increased to 4A. The NPN and PNP BJTs are used for amplifying the MOSFET driving currents.

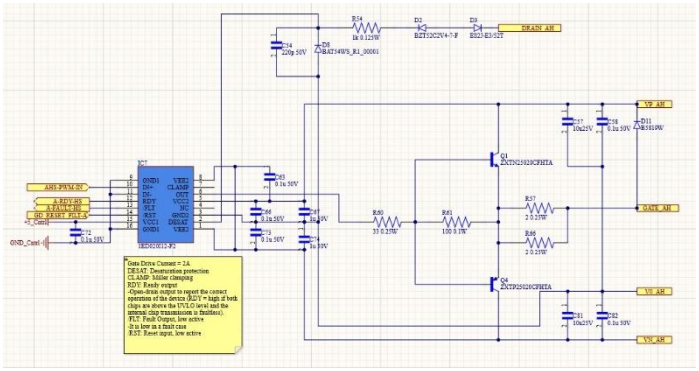


Figure 2.5.1: High Side Gate Driver Connections

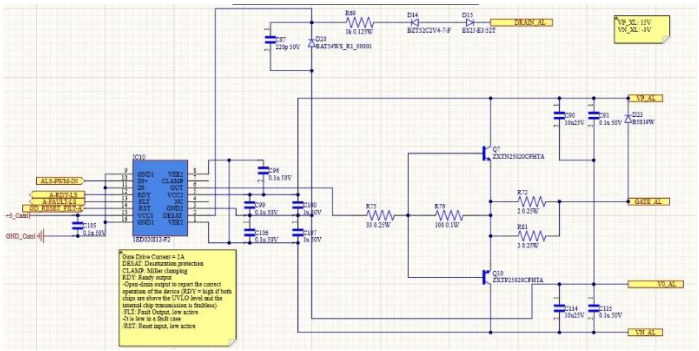
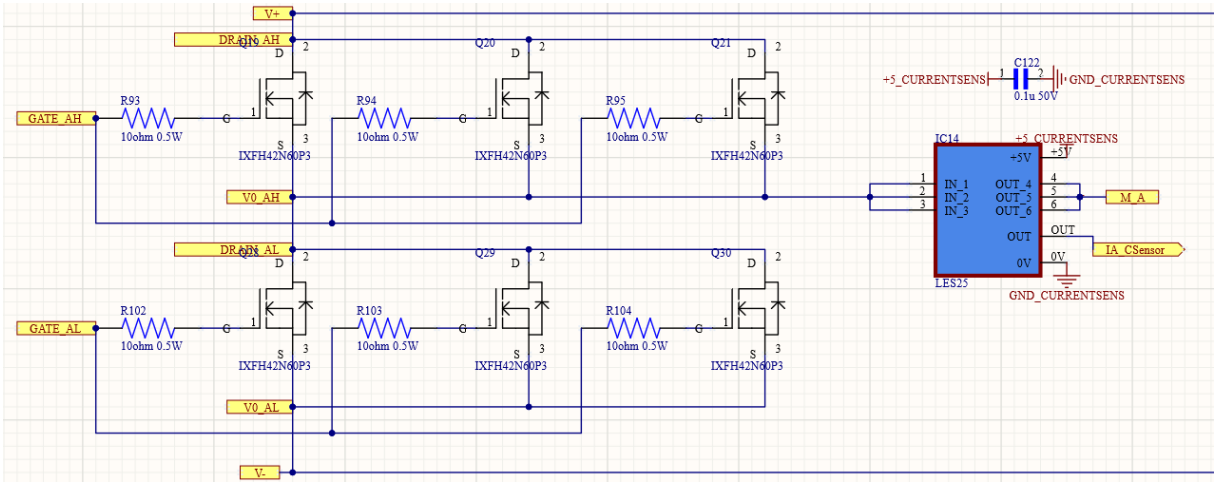


Figure 2.5.2: Low Side Gate Driver Connections

2.6) Mosfet Connections and Current Senor

The driving MOSFET connections for Phase A is shown in Figure 2.6.1. The same process is applied for other Phases as well. There are 3 MOSFETs in parallel to provide more accurate control by increasing the drain to source current. However, additional MOSFETs might noe be populated.


V+
DRAIN_AH
GATE_AH
R93
10ohm 0.5W
Q19
IXFH42N60P3
R94
10ohm 0.5W
Q20
IXFH42N60P3
R95
10ohm 0.5W
Q21
IXFH42N60P3
V0_AH
DRAIN_AL
GATE_AL
R102
10ohm 0.5W
Q28
IXFH42N60P3
R103
10ohm 0.5W
Q29
IXFH42N60P3
R104
10ohm 0.5W
Q30
IXFH42N60P3
V0_AL
V-
+5_CURRENTSENS
C122
0.1u 50V
GND_CURRENTSENS
IC14
+5_CURRENTSENS
+5V
IN_1
IN_2
IN_3
OUT_4
OUT_5
OUT_6
M_A
OUT
0V
IA_CSensor
LES25
GND_CURRENTSENS