everyday genius

MT7603E DATASHEET

Version: 1.2
Release date: 2014-10-1212

Document Revision History

Revision	Date	Author	Description
0.0	2012-09-14	AlexCC Lin	Initial Draft
0.1	2013-09-28	AlexCC Lin	Update Preliminary Data
0.2	2013-10-01	AlexCC Lin	Modify feature list
0.3	2013-10-09	AlexCC Lin	Update thermal information
0.4	2014-04-07	AlexCC Lin	Correct power-on-sequence timing Update theda Ja number
0.5	2014-04-10	AlexCC Lin	Fix typo
1.0	2014-06-08	AlexCC Lin	Formal released
1.1	2014-07-10	AlexCC Lin	Update Max junction temperature
1.2	2014-10-12	AlexCC Lin	1. Update 1.6 voltage spec 2. Correct typo of PCIe VRT value

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1 System Overview

1.1 General Descriptions

The MT7603E is a highly integrated Wi-Fi single chip which supports 300 Mbps PHY rate. It fully complies with IEEE 802.11n and IEEE 802.11 b/g standards, offering feature-rich wireless connectivity at high standards, and delivering reliable, cost-effective throughput from an extended distance.
Optimized RF architecture and baseband algorithms provide superb performance and low power consumption. Intelligent MAC design deploys a high efficient DMA engine and hardware data processing accelerators which offloads the host processor.
The MT7603E is designed to support standard based features in the areas of security, quality of service and international regulations, giving end users the greatest performance any time and in any circumstance.

1.2 Features

1.2.1 Platform

- Embedded high-performance 32-bit RISC microprocessor
- Highly integrated RF with 55nm CMOS technology
- Integrate high efficiency switching regulator
- Best-in-class active and idle power consumption performance
- Compact 7mm x 7mm QFN56L package
- LTE Coexistence(UART)
- Antenna Detection
- Buffered clock output for co-clock with other SOC chipset
- Integrate EFUSE to eliminate the requirement for external EEPROM
- 16 programmable general purpose Input / Output
- 2 configurable LED pins
- Auto-calibration
- Calibration Free(save MP cost)

1.2.2 WLAN

- IEEE 802.11 b/g/n compliant
- 2T2R mode with support of 300Mbps PHY rate
- Greenfield, mixed mode, legacy modes support
- Support MCC(multi channel concurrent)
- Frame aggregation
- BW5/10 narrow band(Rx +2.5dBm), extending coverage
- WoWLAN via GPIO(client mode), Support Host Sleep(AP mode)
- Airtime Fairness(QoS)

- Meet ETSI EN 300 328 V1.8.1 test plan(mandatory for EU in 2014/E)
- Integrated LNA, PA, and T/R switch
- IEEE 802.11 d/h/k support
- Security support for WFA WPA/WPA2 personal, WPS2.0, WAPI
- Supports 802.11w protected managed frames
- QoS support of WFA WMM, WMM PS
- Supports Wi-Fi Direct
- Per packet transmit power control

1.3 Applications

MT7603E is designed for a compact PCB design for PCIE interface. It is suitable for the following applications.

- Broadband platform(xDSL/xPON/Cable..etc)
- AP router
- DTV
- BDP

1.4 Block Diagram

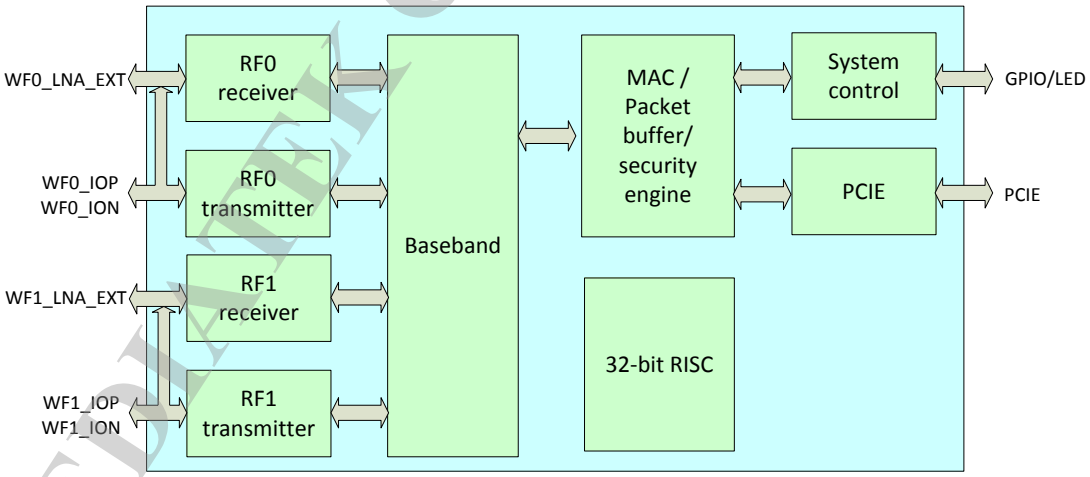


Figure 1 MT7603E block diagram

2 Product Descriptions

2.1 Pin Layout

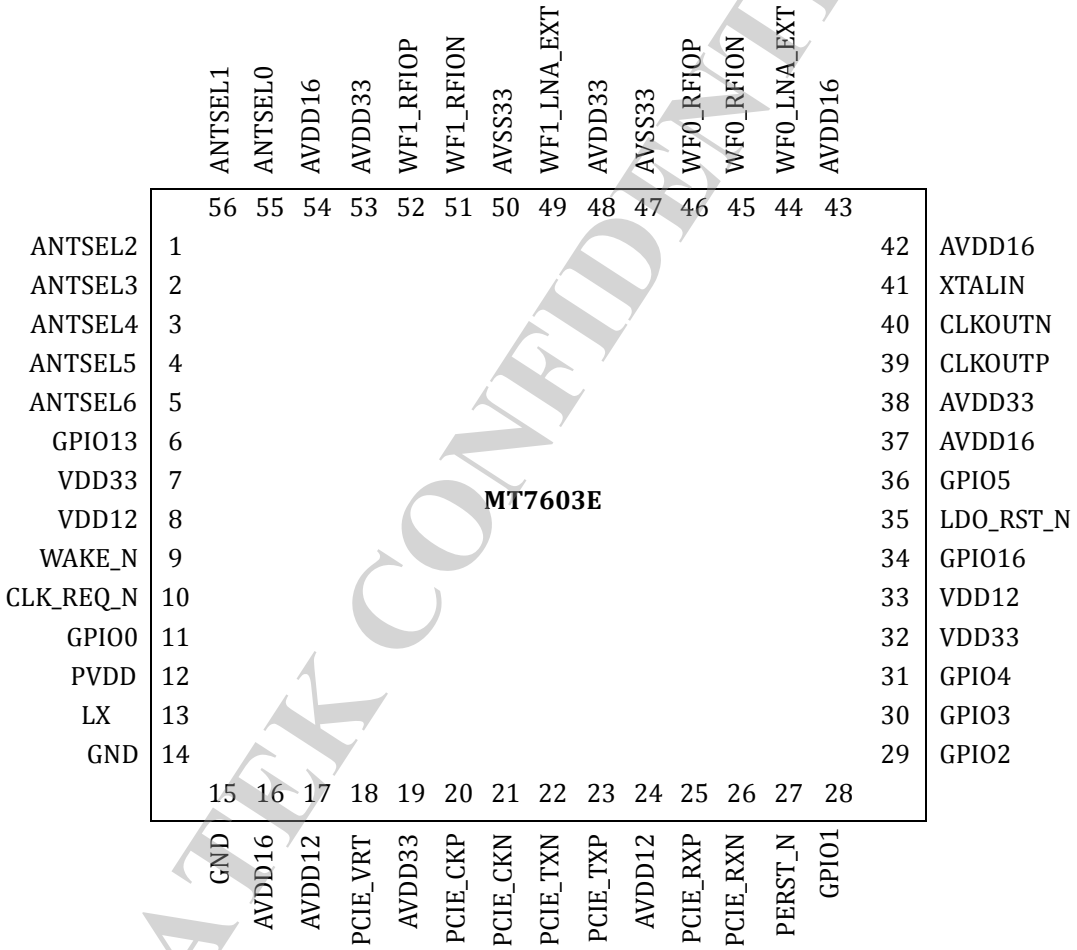


Figure 2 Top view of MT7603E QFN56 pin-out.

2.2 PIN Description

QFN56	Pin Name	Pin description	Default PU/PD	I/O	Supply domain
Reset and clocks					
35	LDO_RST_N	External system reset active low	PU	Input	VDD33
27	PERST_N	PCIE reset , active low	PU	Input	VDD33
41	XTALIN	Crystal input or external clock input	N/A	Input	
39	CLKOUTP	Crystal co-clock output	N/A	Output	
40	CLKOUTN	Crystal co-clock output	N/A	Output	
PCIE interface					
19	AVDD33	PCIE 33V	N/A	Input	AVDD33
24	AVDD12	PCIE12V	N/A	Input	AVDD12
18	PCIE_VRT	Connect to external 5.1K ohm resister	N/A	In/out	
20	PCIE_CKP	PCIE reference clock	N/A	Input	
21	PCIE_CKN	PCIE reference clock	N/A	Input	
22	PCIE_TXN	PCIE TX	N/A	Output	
23	PCIE_TXP	PCIE TX	N/A	Output	
25	PCIE_RXP	PCIE RX	N/A	Input	
26	PCIE_RXN	PCIR RX	N/A	Input	
Programmable I/O					
11	GPIO0	Programmable input/output	PU	In/out	VDD33
28	GPIO1	Programmable input/output	PD	In/out	VDD33
29	GPIO2	Programmable input/output	PD	In/out	VDD33
30	GPIO3	Programmable input/output	PD	In/out	VDD33
31	GPIO4	Programmable input/output	PD	In/out	VDD33
36	GPIO5	Programmable input/output	PD	In/out	VDD33
3	ANTSEL4	Antenna selection control pin / Programmable input/output(GPIO6)	PD	In/out	VDD33
4	ANTSEL5	Antenna selection control pin / Programmable input/output(GPIO7)	PD	In/out	VDD33
5	ANTSEL6	Antenna selection control pin / Programmable input/output(GPIO8)	PD	In/out	VDD33
1	ANTSEL2	Antenna selection control pin / Programmable input/output(GPIO9)	PD	In/out	VDD33
2	ANTSEL3	Antenna selection control pin / Programmable input/output(GPIO10)	PD	In/out	VDD33
55	ANTSEL0	Antenna selection control pin / Programmable input/output(GPIO11)	PD	In/out	VDD33
56	ANTSEL1	Antenna selection control pin / Programmable input/output(GPIO12)	PD	In/out	VDD33

6	GPIO13	Programmable input/output	PU	In/out	VDD33
9	WAKE_N	PCIE WAKE_N / Programmable input/output(GPIO14)	PU	In/out	VDD33
10	CLK_REQ_N	PCIE CLK_REQ_N / Programmable input/output(GPIO15)	PD	In/out	VDD33
34	GPIO16	Programmable input/output	PD	In/out	VDD33
WIFI radio interface					
44	WF0_LNA_EXT	WF0 auxiliary RX input	N/A	Input	
45	WF0_RFION	WF0 main TRX inout	N/A	In/out	
46	WF0_RFIOP	WF0 main TRX inout	N/A	In/out	
49	WF1_LNA_EXT	WF1 auxiliary RX input	N/A	Input	
51	WF1_RFION	WF1 main TRX inout	N/A	In/out	
52	WF1_RFIOP	WF1 main TRX inout	N/A	In/out	
PMU/SMPS					
17	AVDD12	LDO 1.2V output	N/A	Output	
16	AVDD16	SMPS 1.6V input	N/A	Iutput	
12	PVDO	SMPS 3.3V power supply	N/A	Input	
13	LX	SMPS control	N/A	In/out	
14	PGND	SMPS analog groung	N/A	In/out	
15	AGND	PMU analog ground	N/A	In/out	
Power supplies					
7,32	VDD33	Digital I/O power supply	N/A	Input	VDD33
8,33	VDD12	Digital core power supply	N/A	Input	
53, 48, 38	AVDD33	RF 3.3V power supply	N/A	Input	
50, 47	AVSS33	RF 3.3V power ground	N/A	Input	
54, 43, 42, 37	AVDD16	RF 1.6V power supply	N/A	Input	
E-PAD	DVSS	Digital ground	N/A		

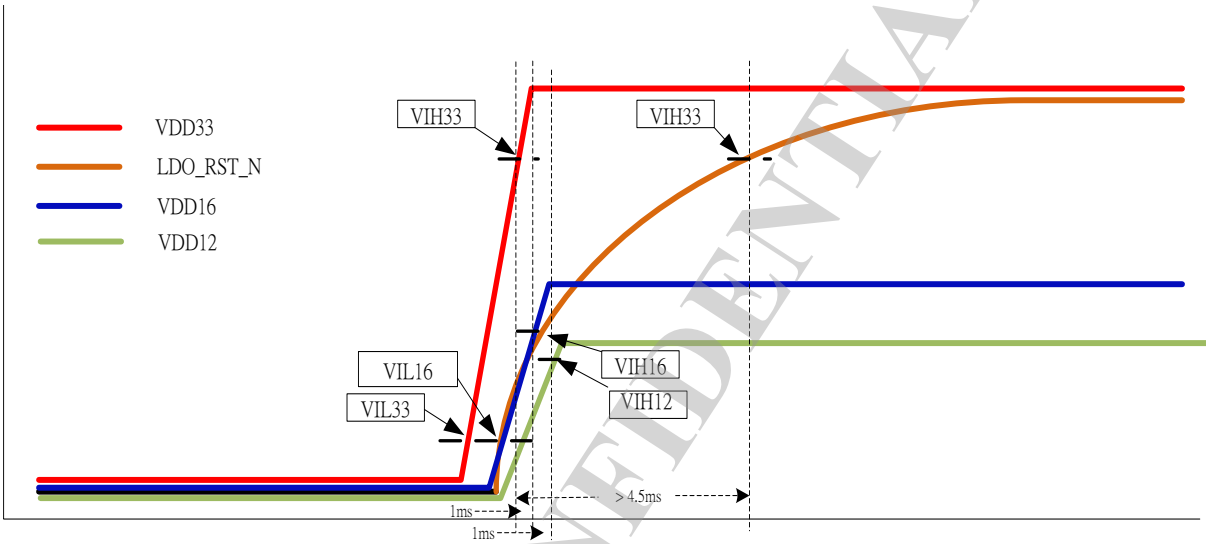
Table 1 Pin descriptions

2.3 Strapping option

QFN56	Pin Name	Pin description	
3	ANTSEL4	XTAL_SEL0	PD
4	ANTSEL5	XTAL_SEL1 25HMz DIP : {XTAL_SEL1 = PU, XTAL_SEL0 = PD} 40Mhz SMD : {XTAL_SEL1 = PU, XTAL_SEL0 = PU}	PU
5	ANTSEL6	EXT_EE_SEL: Pull down	PD
11	GPIO0	Co-clock selection Current mode: Pull down Voltage mode : Pull up	PD

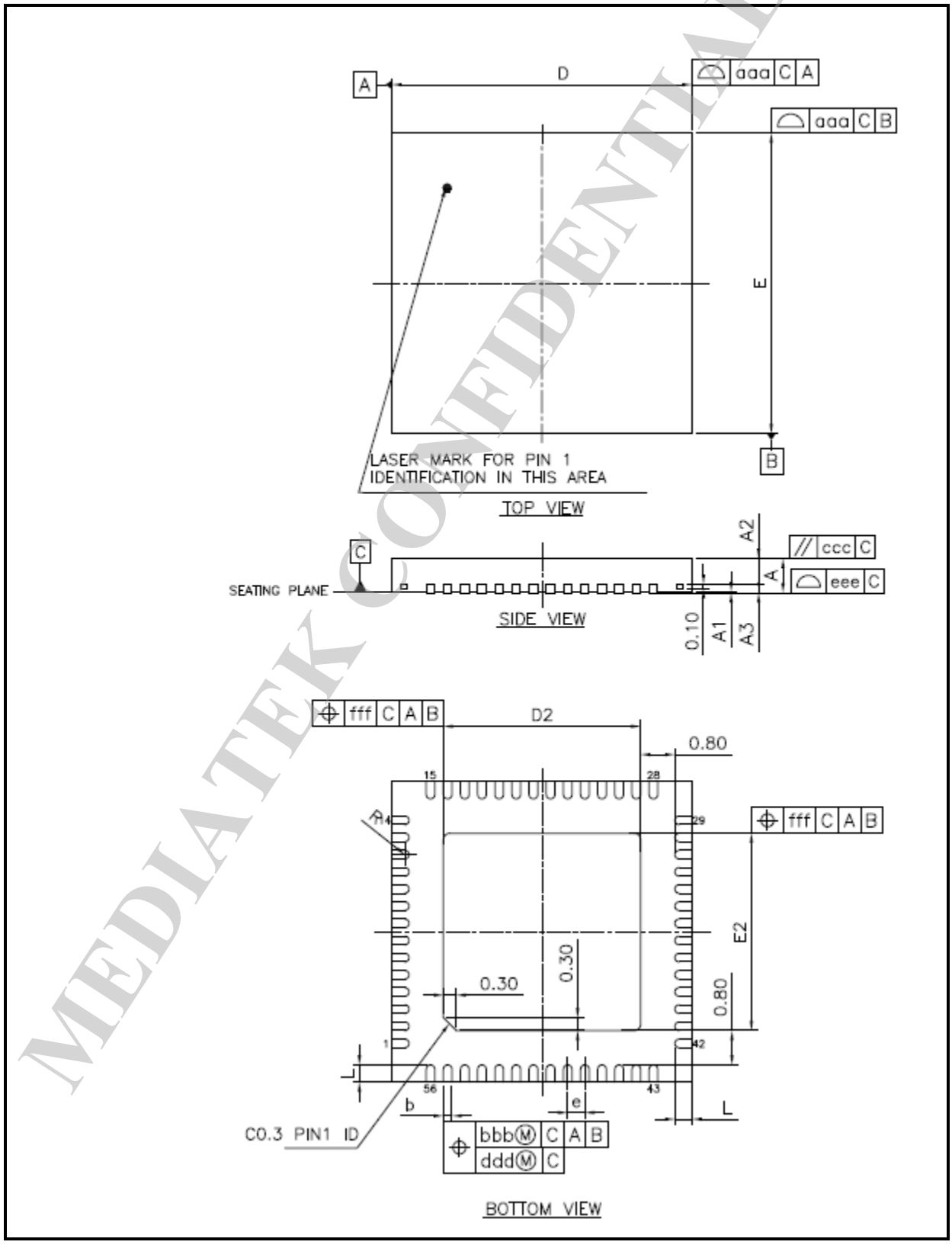
Table 2 Strapping option

2.4 Power on sequence/reset



Note :
1. 1.6V can be ready before 3.3V ready. Generally, 1.6V would be ready after 3.3V ready (around 1ms)
2. 1.2V would be ready after 1.6V ready (around 1ms)
3. LDO_RST_N must be 4.5 ms delay at least after 3.3V ready.

2.5 Package information



Item		Symbol	MIN.	NOM.	MAX.
total height		A	0.70	0.75	0.80
stand off		A1	0.00	0.02	0.05
mold thickness		A2	0.50	0.55	0.60
leadframe thickness		A3		0.20 REF.	
lead width		b	0.15	0.20	0.25
package size	X	D	6.90	7.00	7.10
	Y	E	6.90	7.00	7.10
E-PAD size	X	D2	4.50	4.60	4.70
	Y	E2	4.50	4.60	4.70
lead length		L	0.30	0.40	0.50
lead pitch		e		0.40 bsc	
lead arc		R	0.075	---	---
Package profile of a surface		aaa		0.10	
Lead position		bbb		0.07	
Paralleliam		ccc		0.10	
Lead position		ddd		0.05	
Lead profile of a surface		eee		0.08	
Epad position		fff		0.10	

Figure 3 Package outline drawing

2.6 Ordering Information

Part number	Package	Operational temperature range
MT7603EN	7x7x0.8 mm 56-QFN	-10~55°C

Table 3 Ordering information

2.7 TOP Marking Information

MT7603EN : Part number
DDDD : Date code
: Internal control code
BBBBBBB : Lot number

Figure 4 Top marking

3 Electrical characteristics

3.1 Absolute maximum rating

Symbol	Parameters	Maximum rating	Unit
VDD33	3.3V Supply Voltage	-0.3 to 3.6	V
VDD12	1.2V Supply Voltage	-0.3 to 1.5	V
VDD16	1.6V Supply Voltage	-0.3 to 1.8	V
T_{STG}	Storage Temperature	-40 to +125	°C
VESD	ESD protection (HBM)	2000	V

Table 4 Absolute maximum ratings

3.2 Recommended operating range

Symbol	Rating	MIN	TYP	MAX	Unit
VDD33	3.3V Supply Voltage	2.97	3.3	3.63	V
VDD12	1.2V Supply Voltage	1.14	1.2	1.26	V
VDD16	1.6V Supply Voltage	1.5	1.6	1.76	V
$T_{AMBIENT}$	Ambient Temperature	-10	-	55	°C

Table 5 Recommended operating range

3.3 DC characteristics

Symbol	Parameter	Conditions	MIN	MAX	Unit
V_{IL}	Input Low Voltage	LVTTL	-0.28	0.6	V
V_{IH}	Input High Voltage		2.0	3.63	V
V_{T-}	Schmitt Trigger Negative Going Threshold Voltage	LVTTL	0.68	1.36	V
V_{T+}	Schmitt Trigger Positive Going Threshold Voltage		1.36	1.7	V
V_{OL}	Output Low Voltage	$\|I_{OL}\|$ = 1.6~14 mA	-0.28	0.4	V
V_{OH}	Output High Voltage	$\|I_{OH}\|$ = 1.6~14 mA	2.4	VDD33+0.33	V
R_{PU}	Input Pull-Up Resistance	PU=high, PD=low	40	190	KΩ
R_{PD}	Input Pull-Down Resistance	PU=low, PD=high	40	190	KΩ

Table 6 DC description

3.4 Thermal characteristics

Max junction temp = 125'C

Thermal characteristics when stationary, without an external heat sink in an air-conditioned environment:

Thermal Resistance θ JA (°C/W) for JEDEC 2L system PCB .....32.18 °C /W

Thermal Resistance θ JA (°C/W) for JEDEC 4L system PCB .....21.19 °C /W

Thermal Resistance θ JC (°C/W) for JEDEC system PCB .....8.81 °C /W

Thermal Resistance θ JB (°C/W) for JEDEC system PCB .....3.44 °C /W

Thermal Characterization parameter ΨJt (°C/W) for JEDEC 2L system PCB .....2.78 °C /W

Thermal Characterization parameter ΨJt (°C/W) for JEDEC 4L system PCB .....1.72 °C /W

NOTE: JEDEC 51-7 system FR4 PCB size: 76.2x114.3mm (3"x4.5")

Table 7 Thermal information

ESD CAUTION

MT7603E is ESD (electrostatic discharge) sensitive device and may be damaged with ESD or spike voltage. Although MT7603E is with built-in ESD protection circuitry, please handle with care to avoid the permanent malfunction or the performance degradation.