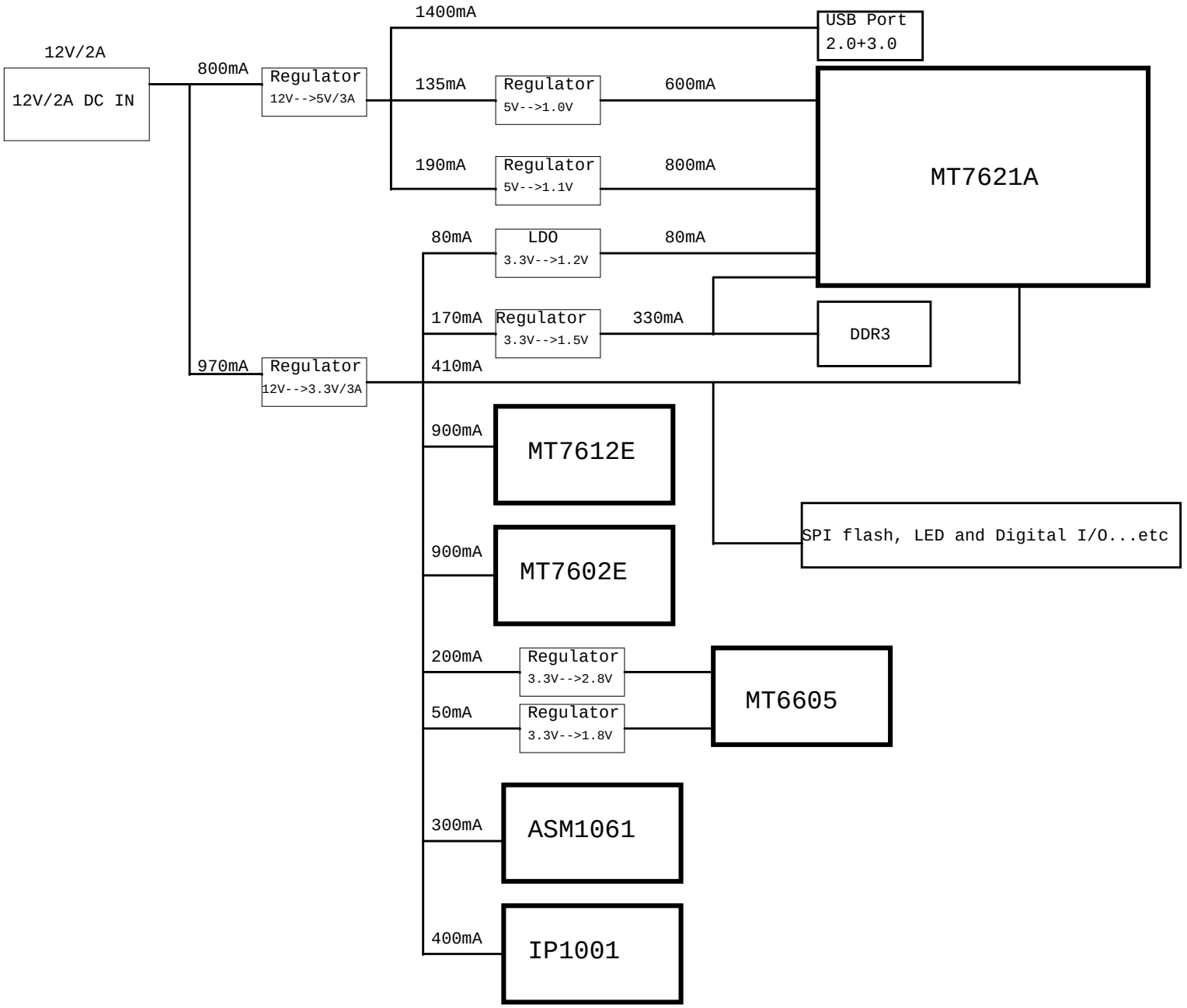
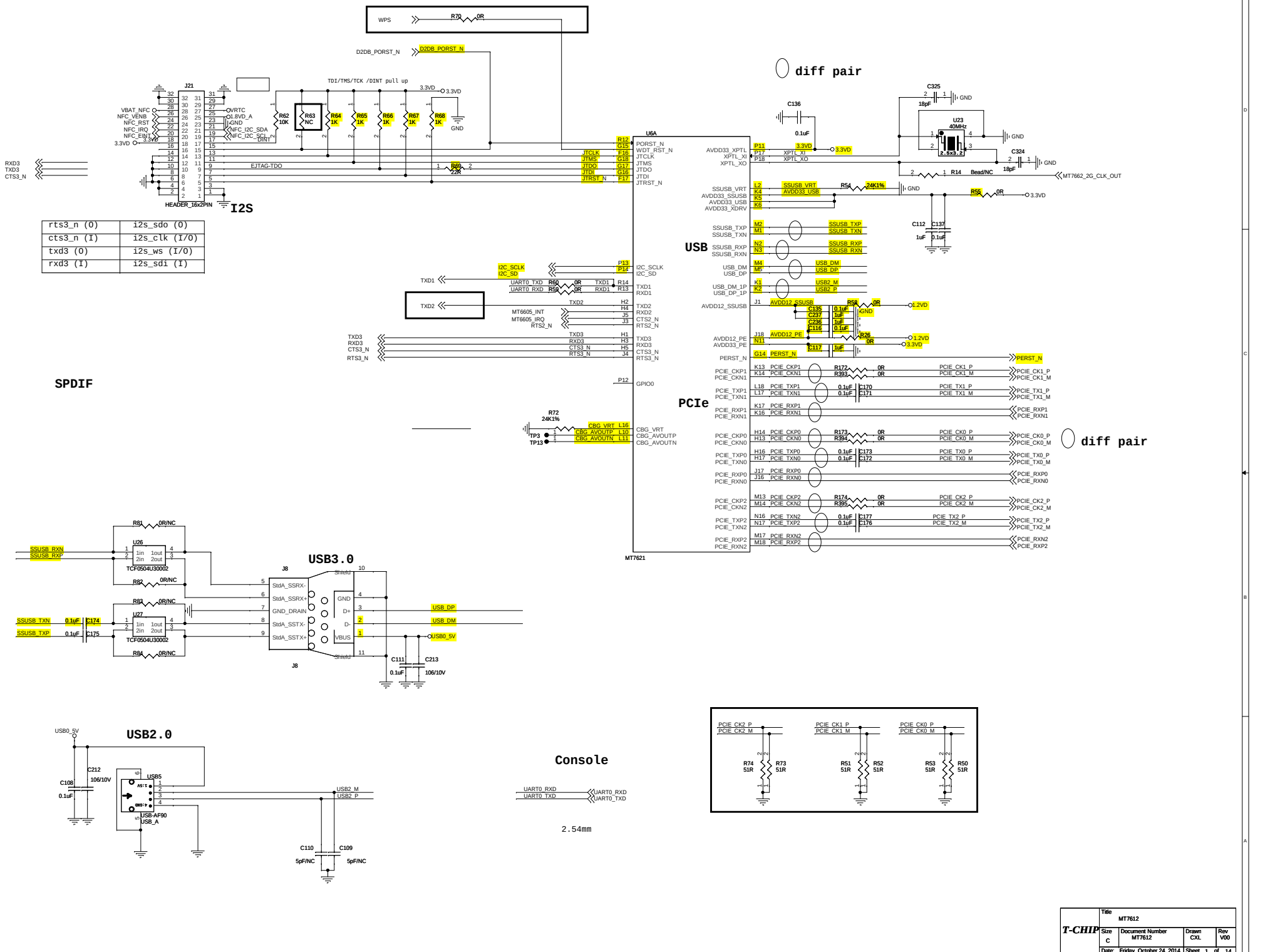

12V/2A
12V/2A DC IN
800mA
Regulator
12V-->5V/3A
1400mA
USB Port
2.0+3.0
135mA
Regulator
5V-->1.0V
600mA
190mA
Regulator
5V-->1.1V
800mA
MT7621A
80mA
LDO
3.3V-->1.2V
80mA
170mA
Regulator
3.3V-->1.5V
330mA
DDR3
970mA
Regulator
12V-->3.3V/3A
410mA
900mA
MT7612E
SPI flash, LED and Digital I/O...etc
900mA
MT7602E
200mA
Regulator
3.3V-->2.8V
50mA
Regulator
3.3V-->1.8V
MT6605
300mA
ASM1061
400mA
IP1001



rts3_n (O)	i2s_sdo (O)
cts3_n (I)	i2s_clk (I/O)
txd3 (O)	i2s_ws (I/O)
rxd3 (I)	i2s_sdi (I)

T-CHIP	Title: MT7612		
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DDR3/DDR2 Interface
The pinout is differenet
when use DDR3 and DDR2

diff pair

Test Pad for signal measurement

RDQM0	1	TP4
RDQM1	1	TP5
RDQS0	1	TP6
RDQS0_	1	TP7
RDQS1	1	TP31
RDQS1_	1	TP8
RRAS_	1	TP9
RCS_	1	TP10
RCAS_	1	TP29
RWE_	1	TP30
RDQ2	1	TP32
RDQ7	1	TP33
RDQ9	1	TP34
RDQ12	1	TP35
RA4	1	TP37
RODT	1	TP36
RDQ15	1	TP38
RA6	1	TP39
RA8	1	TP40

U6B

MT7621

TF/SPI Flash

spi_cs0 (I/O)	nd_cs_n (O)
spi_cs1 (I/O)	nd_we_n (O)
spi_clk (I/O)	nd_re_n (O)
spi_miso (I/O)	nd_d[4] (I/O)
spi_mosi (I/O)	nd_d[5] (I/O)
spi_wp (I/O)	nd_d[6] (I/O)
spi_hold (I/O)	nd_d[7] (I/O)

SPI Flash

MX25L6406EM2I

TF_wp (I)	nd_wp (O)
TF_clk (I/O)	nd_rb_n (I)
TF_cd (I)	nd_cle (O)
TF_cmd (I/O)	nd_ale (O)
TF_data[0] (I/O)	nd_d[0] (I/O)
TF_data[1] (I/O)	nd_d[1] (I/O)
TF_data[2] (I/O)	nd_d[2] (I/O)
TF_data[3] (I/O)	nd_d[3] (I/O)

TF_SOCKET
MICRO-SD-YST

OPTION

ED6	NC/ESD9B5V	E0402N
ED7	NC/ESD9B5V	E0402N
ED8	NC/ESD9B5V	E0402N
ED9	NC/ESD9B5V	E0402N
ED10	NC/ESD9B5V	E0402N
ED11	NC/ESD9B5V	E0402N
ED12	NC/ESD9B5V	E0402N

T-CHIP	Title: MT7612		
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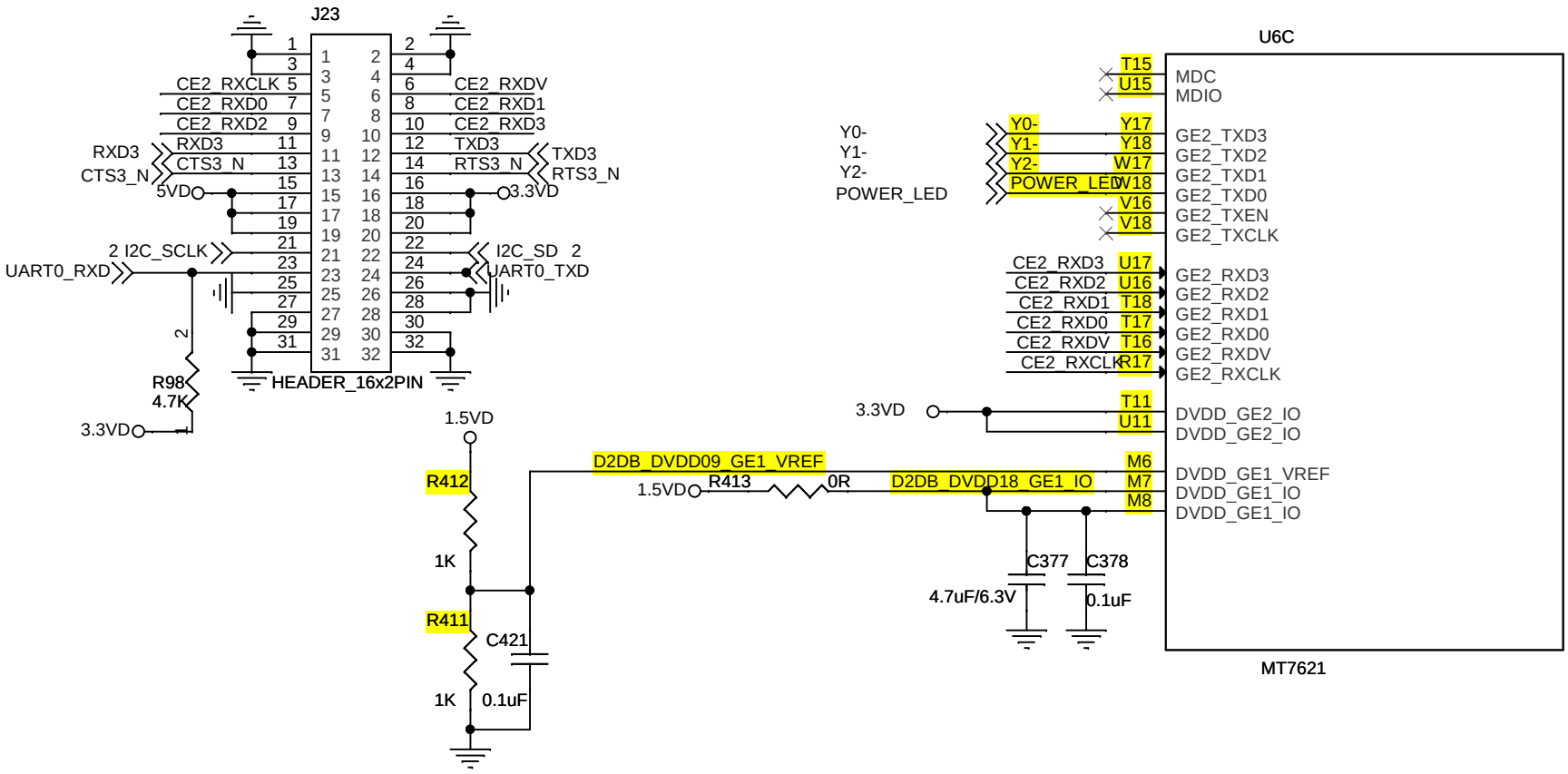
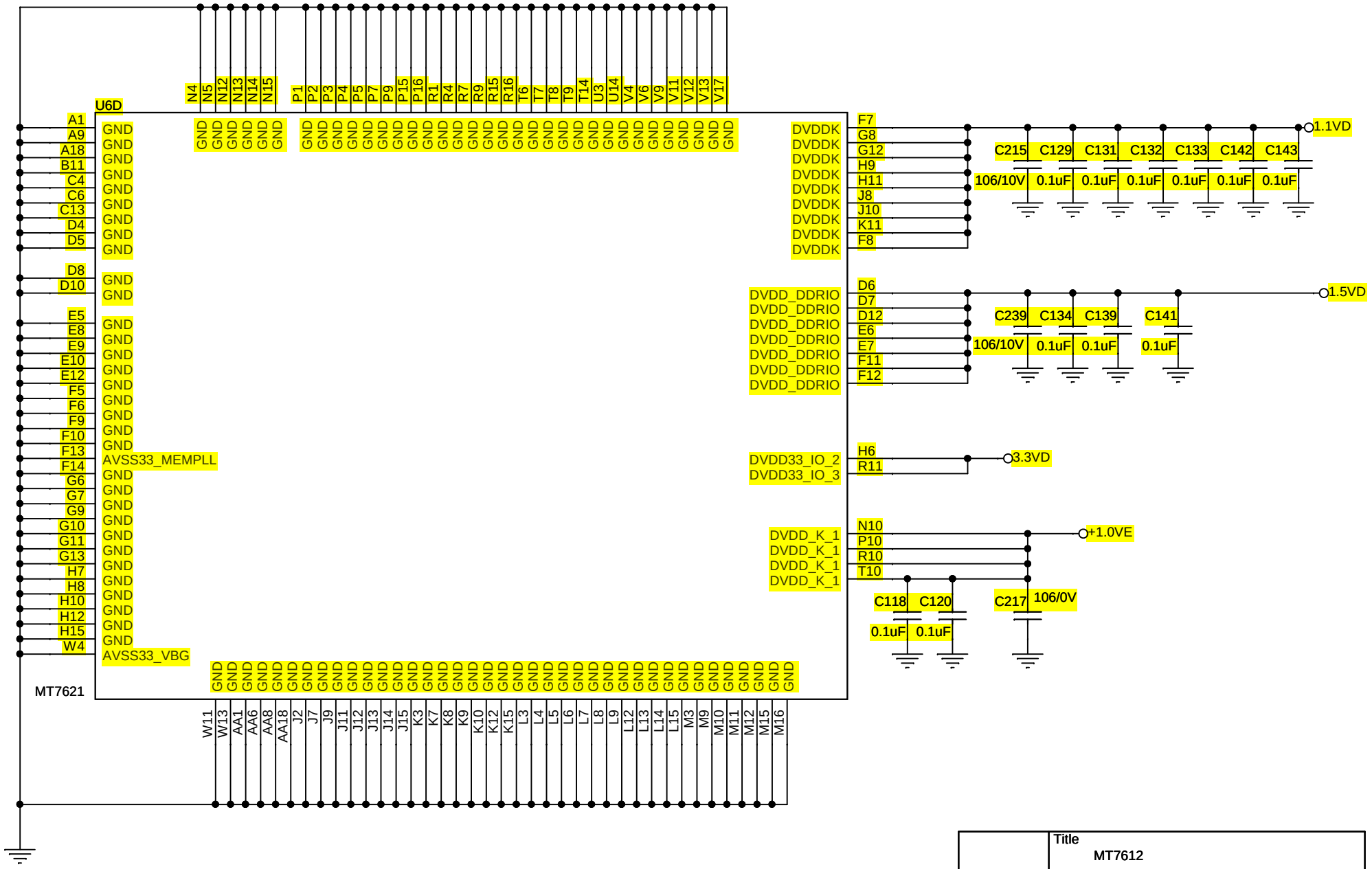
RGMII Interface



T-CHIP	Title: MT7612			
	Size: C	Document Number: MT7612	Drawn: CXL	Rev: V00
	Date: Friday, October 24, 2014	Sheet 3 of 14		

MT7621 Power



T-CHIP	Title: MT7612		
	Size: C	Document Number: MT7612	Drawn: CXL / Rev: V00
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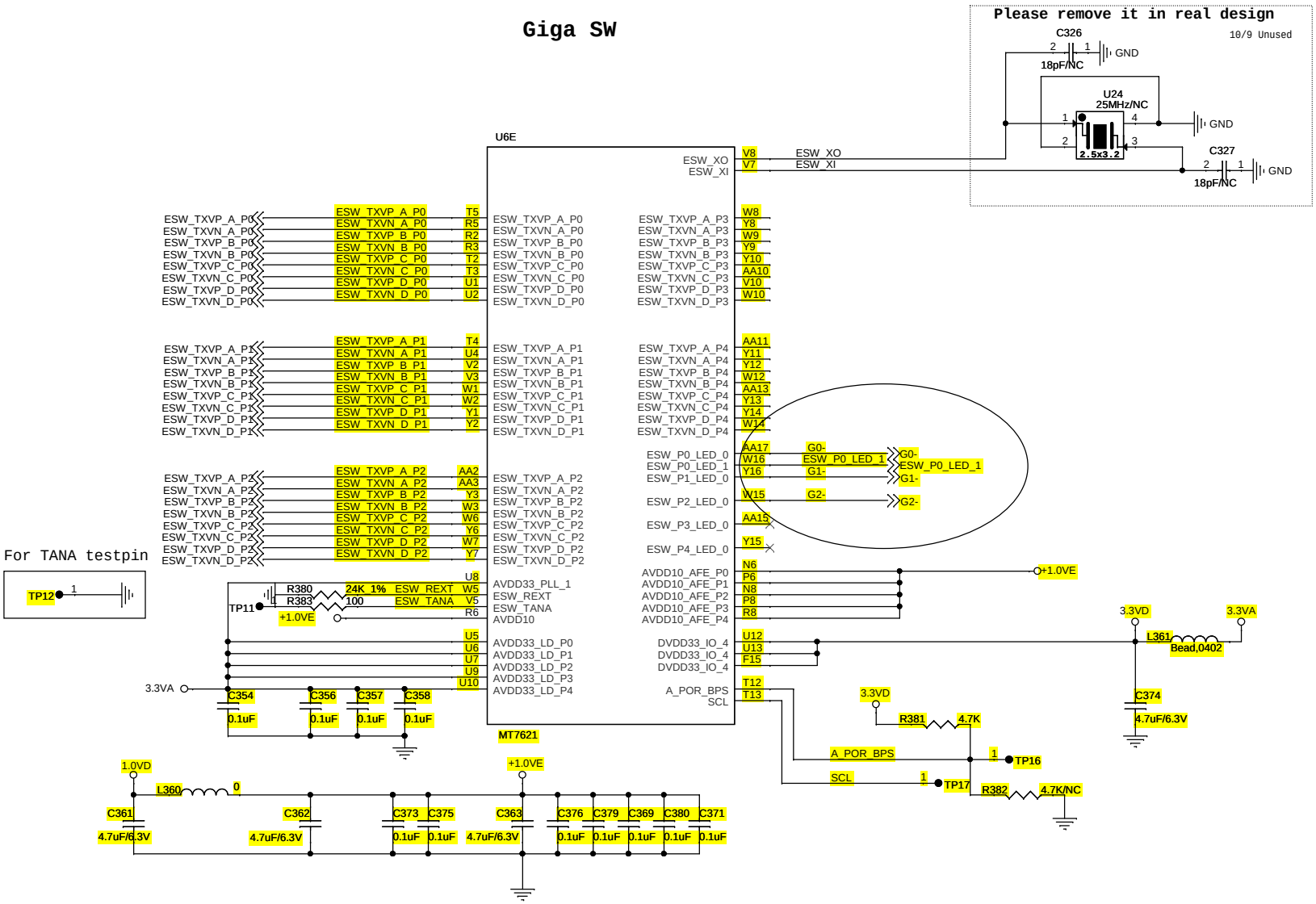
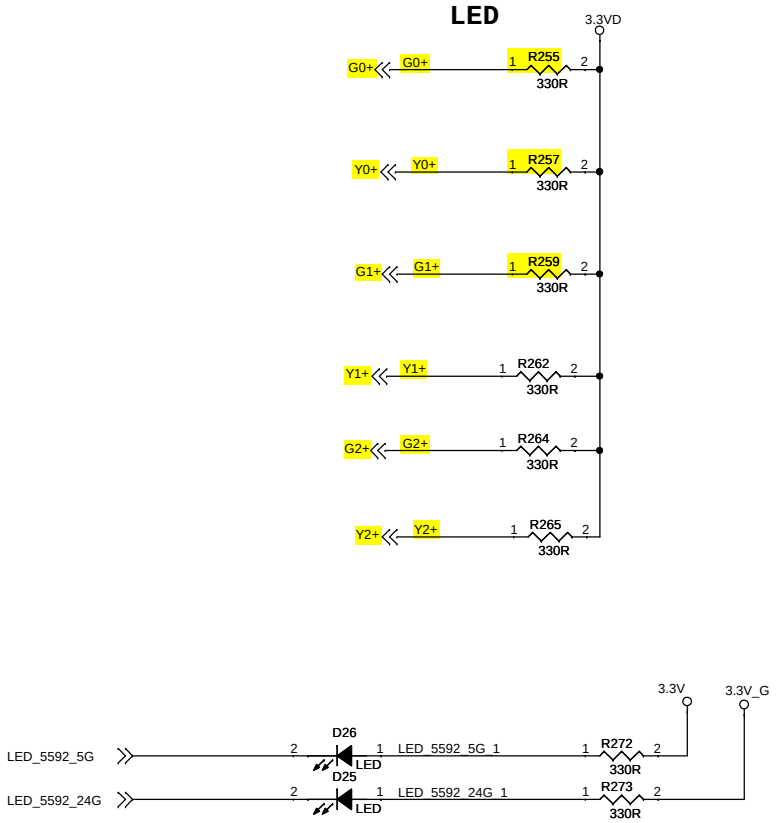
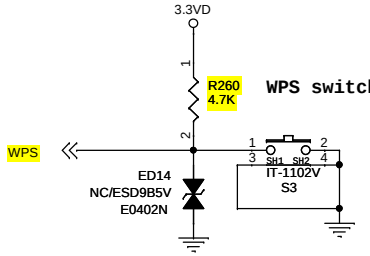
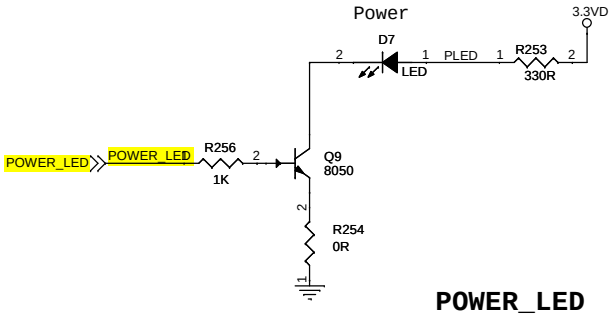
Giga SW



T-CHIP	Title: MT7612			
	Size: C	Document Number: MT7612	Drawn: CXL	Rev: V00
	Date: Friday, October 24, 2014	Sheet 5 of 14		







T-CHIP	Title: MT7612			
	Size: C	Document Number: MT7612	Drawn: CXL	Rev: V00
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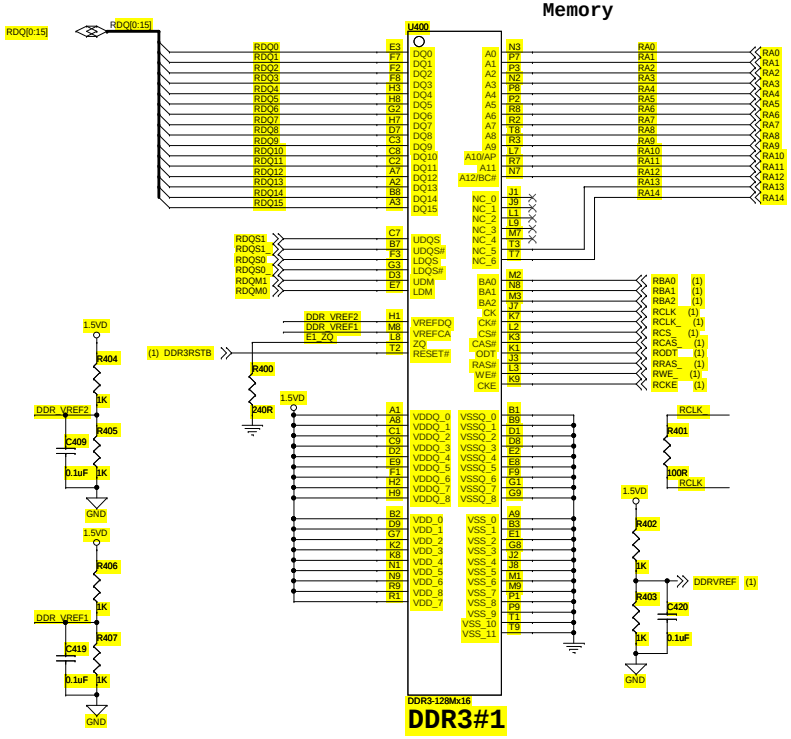
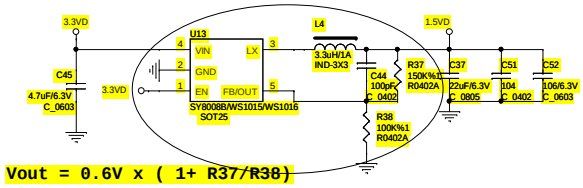
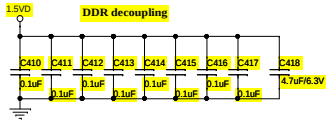
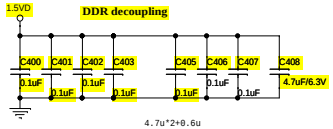
Memory





Vout = 0.6V x (1+ R37/R38)





4.7u*2+0.6u

T-CHIP	Title: MT7612			
	Size: C	Document Number: MT7612	Drawn: CXL	Rev: V00
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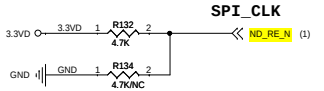
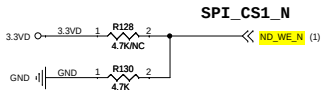
Boot Strapping

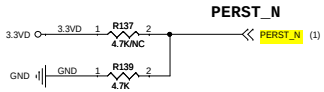
Pin Name	Description	Value	
SPI_CLK	DRAM_FROM_EE	For non scan mode: 0: DRAM/PLL configuration from EEPROM **1: DRAM configuration from Auto Detect**	For FT mode: 0: SUTIF 1: 3-wire SPI
{SPI_CS1_N, SPI_CS0_N, MDC }	XTAL_MODE	000: 20 MHz, Self Oscillation mode 001: 20 MHz, Single end input 010: 20 MHz, differential input **011: 40 MHz, Self Oscillation mode**	100: 40 MHz, Single end input 101: 40 MHz, differential input 110: 25 MHz, Self Oscillation mode 111: 25 MHz, Single end input
PERST_N	OCP_RATIO	**0: 1:3** 1: 1:4	
TXD2	DRAM_TYPE	**0: DDR3** 1: DDR2	
{RTS2_N, RTS3_N, TXD1, GPIO0}	CHIP_MODE[3:0]	0000: Normal / Boot from SPI 4-byte address and XTAL clock 0001: Normal / Boot from ROM (NAND page 2k+64 bytes) **0010: Normal / Boot from SPI 3-byte address** 0011: Normal / Boot from SPI 4-byte address 0100: iNIC RGMI / Boot from ROM 0101: iNIC MII / Boot from ROM 0110: iNIC RVMII / Boot from ROM 0111: iNIC PHY / Boot from ROM 1000: iNIC RGMII / Boot from ROM and XTAL clock 1001: Normal / Boot from internal SRAM 1010: Normal / Boot from ROM (NAND page 2k+128 bytes) 1011: Normal / Boot from ROM (NAND page 4k+128 bytes) 1100: Normal / Boot from ROM (NAND page 4k+224 bytes) 1101: Debug mode 1110: Scan mode 1111: Final Test	

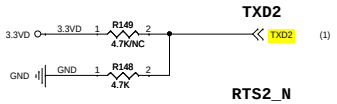
Giga Switch Hardware Trap

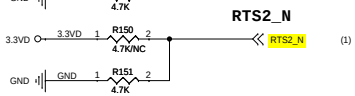
Pin Name	Trap	Fuction	Description	Default
P0_LED_0	HWTRAP[0]	HT_CHIP_MODE[0]	chip_mode[3:0] 4'b0000: IDDQ mode 4'b0001: IOTEST mode 4'b0010: NANDTREE mode 4'b0011: RING mode (both IO and std-cell) 4'b0100: MBIST 4'b0101: SCAN mode (internal) 4'b0110: SCAN-COMP mode (compression) 4'b0111: SCAN-MBIST-OLT mode 4'b1000: AFE-OLT mode 4'b1001: GPHY ATE mode 4'b1010: GPHY ADUMP mode 4'b1011: GPHY ADUMP probe mode 4'b1100: Reserved 4'b1101: Reserved 4'b1110: bootup probe mode 4'b1111: normal mode	4'b1111
P1_LED_0	HWTRAP[1]	HT_CHIP_MODE[1]		
P2_LED_0	HWTRAP[2]	HT_CHIP_MODE[2]		
P0_LED_1	HWTRAP[3]	HT_CHIP_MODE[3]		
P3_LED_0	HWTRAP[9]	HT_XTAL_FSEL[0]	External Crystal Frequency Selection xtal_freq_sel[1:0] 2'b01: 20MHz 2'b10: 40MHz 2'b11: 25MHz	2'b10
P4_LED_0	HWTRAP[10]	HT_XTAL_FSEL[1]		

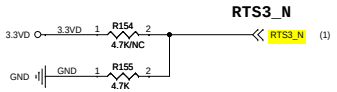


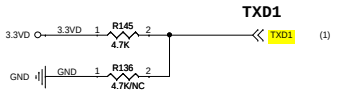


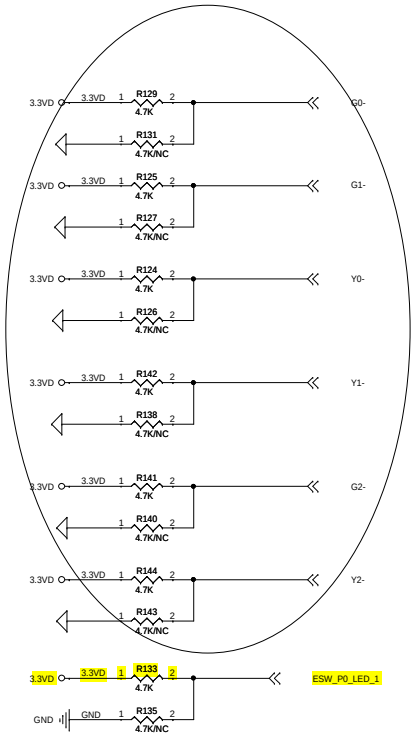


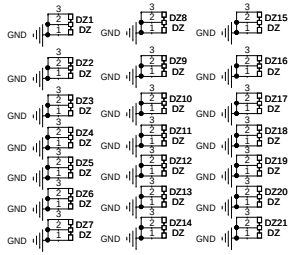












T-CHIP	Title: MT7612			
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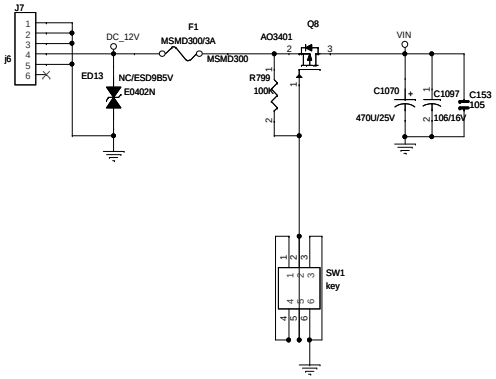
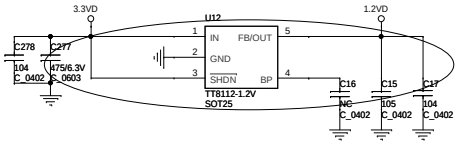
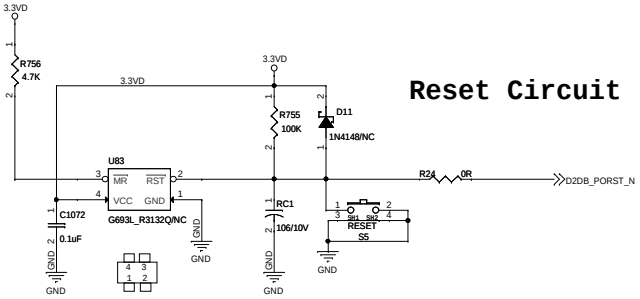
System Power

For USB/PCIe PHY Power (1.2V)

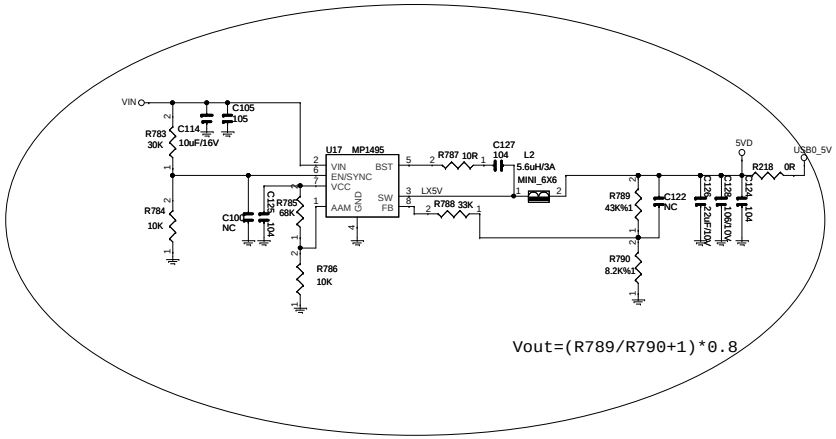
Current= 300mA



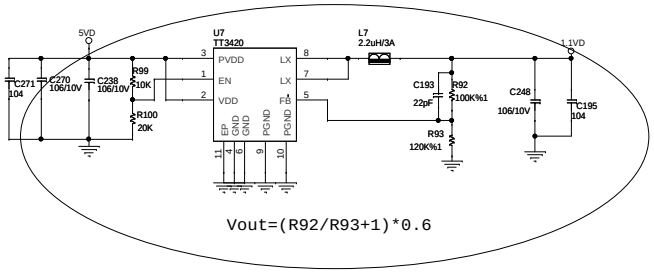




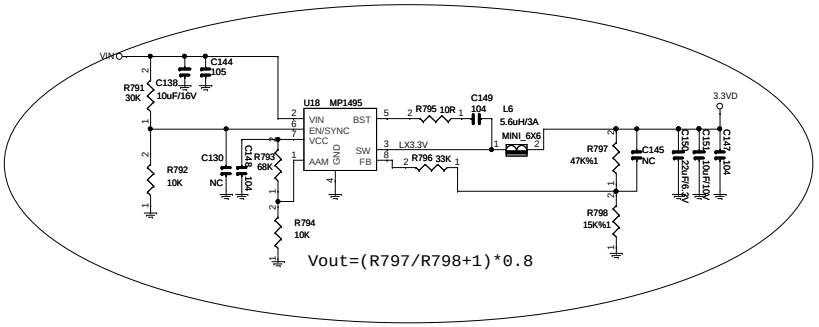
Reset Circuit



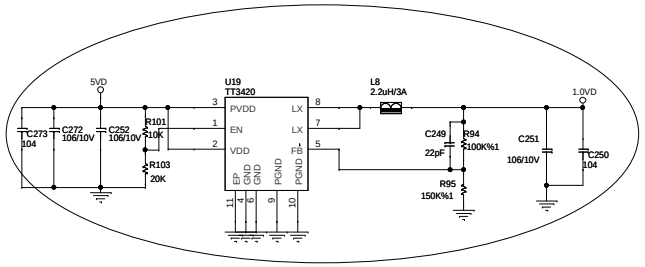
Vout=(R789/R790+1)*0.8



Vout=(R92/R93+1)*0.6



Vout=(R797/R798+1)*0.8



Vout=(R94/R95+1)*0.6

T-CHIP	Title: MT7612			
	Size: C	Document Number: MT7612	Drawn: CXL	Rev: V00
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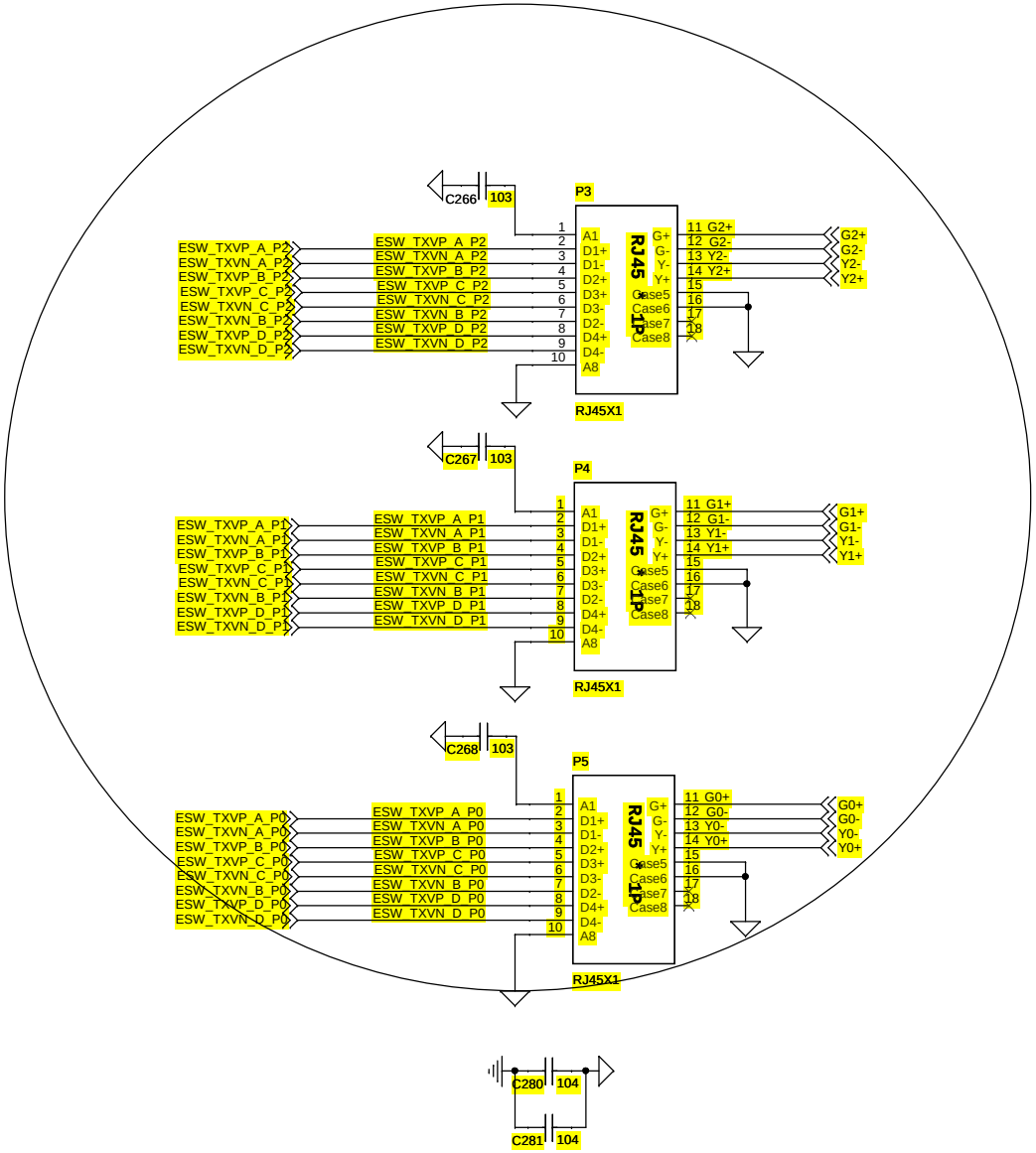

T-CHIP	Title: MT7612			
	Size: C	Document Number: MT7612	Drawn: CXL	Rev: V00
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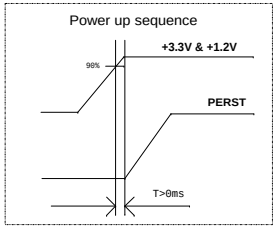
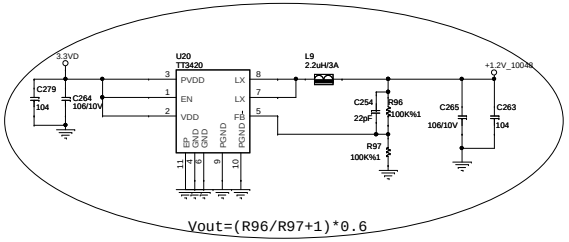
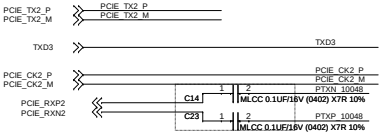
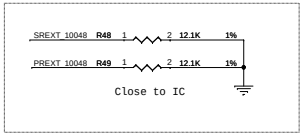
PCIe to SATA



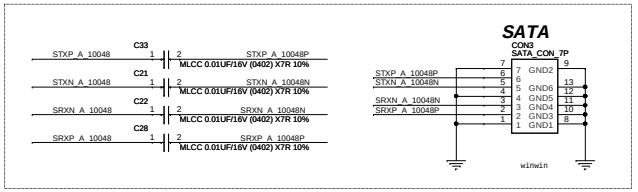


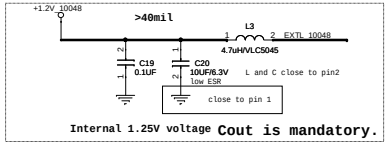


Close to PCIe Slot
X7R/0402 type

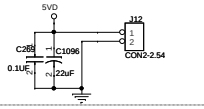


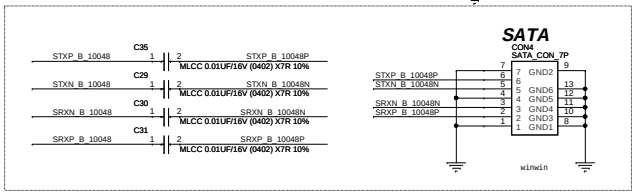
Close to IC

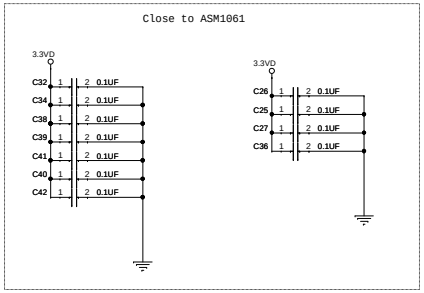


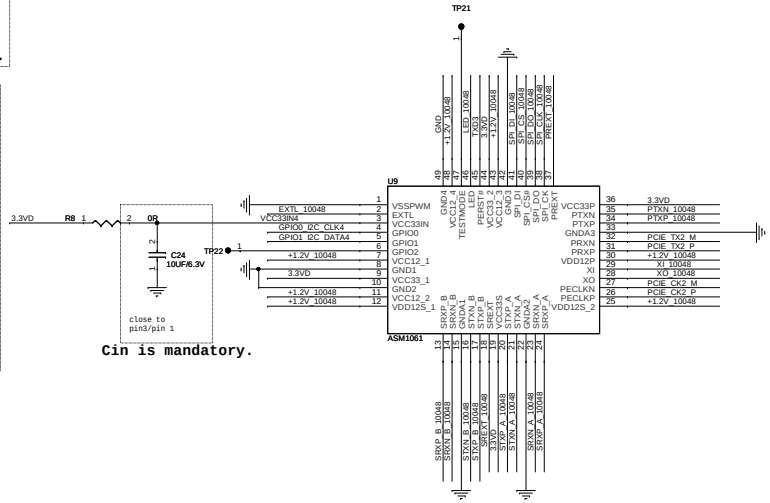


Internal 1.25V voltage **Cout is mandatory.**

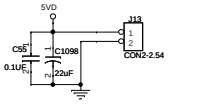


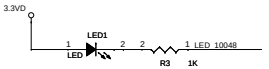


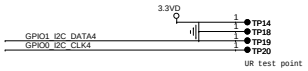




Cin is mandatory.



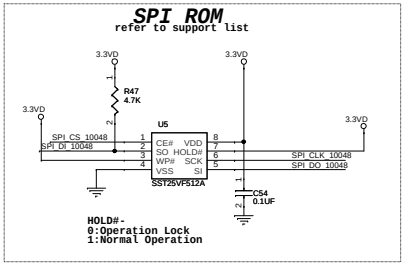


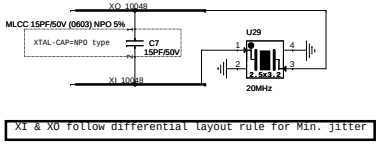


H/W Strapping

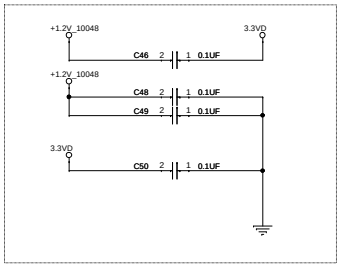
refer to datasheet:

SPI_DO
0: Spin up by H/W
1: Spin up by S/W

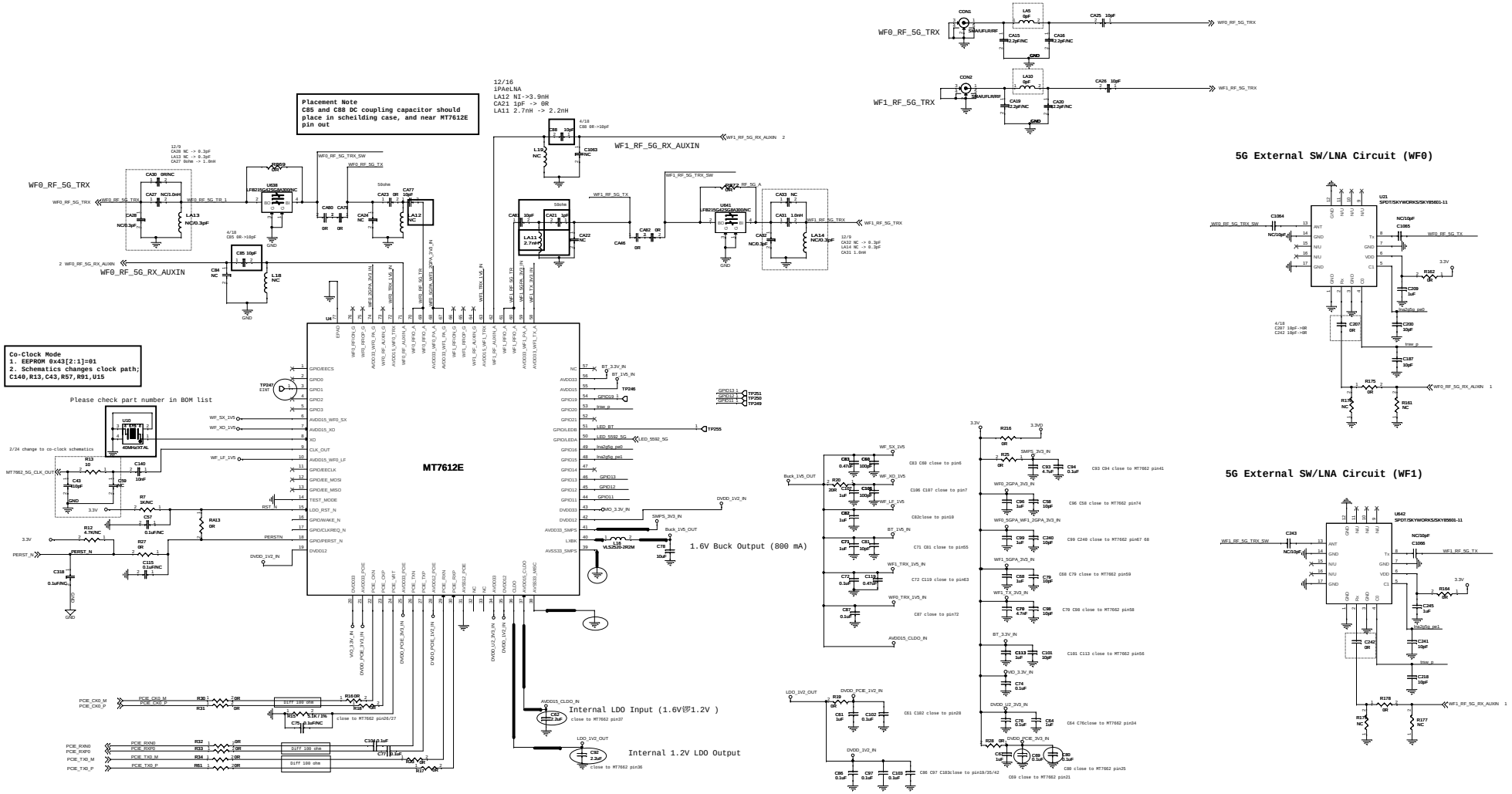




XI & XO follow differential layout rule for Min. jitter



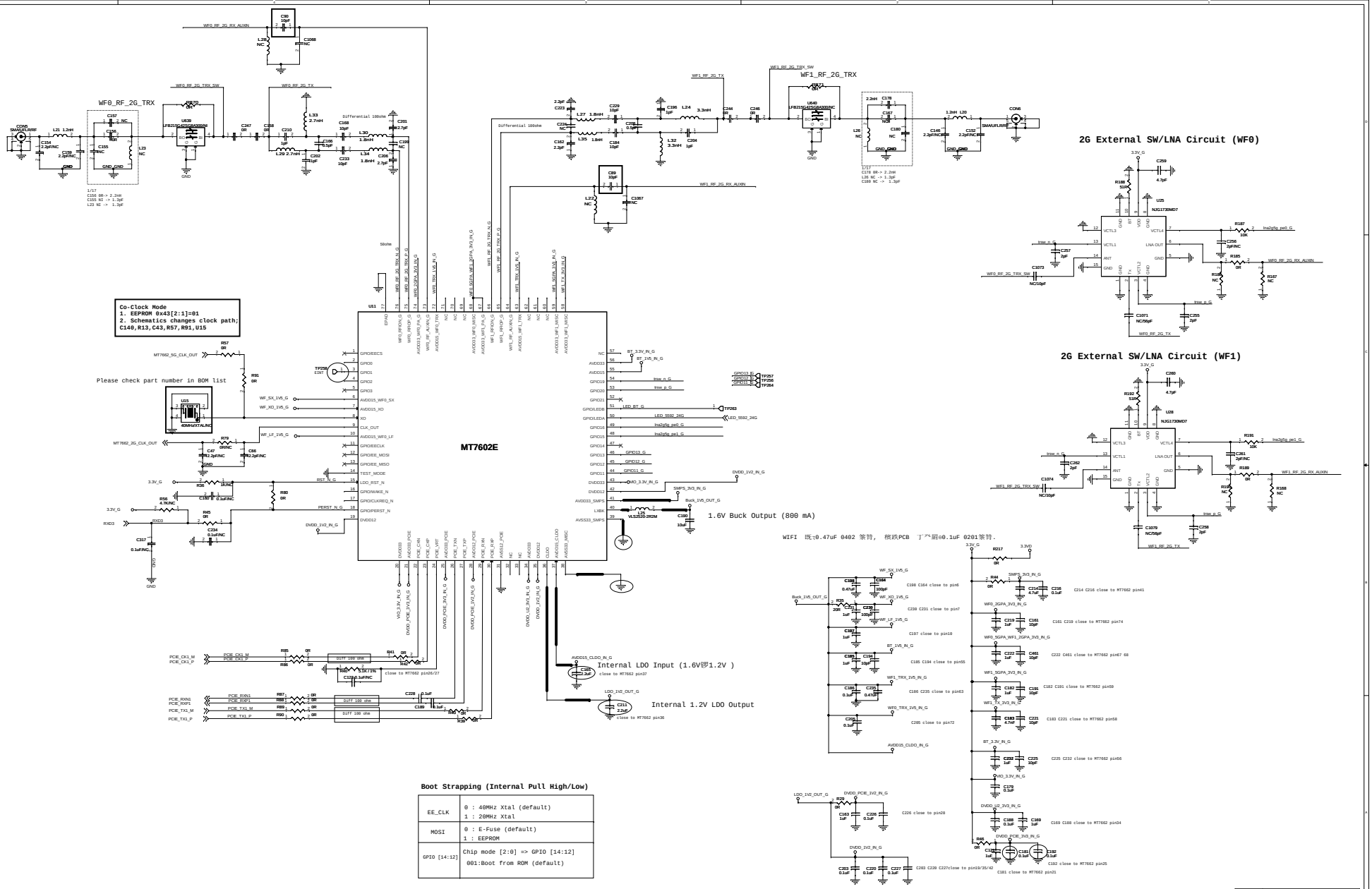
T-CHIP	Title: MT7612			
	Size: C	Document Number: MT7612	Drawn: CXL	Rev: V00
	Date: Friday, October 24, 2014	Sheet 11 of 14		



Boot Strapping (Internal Pull High/Low)

EE_CLK	0 : 40MHz Xtal (default) 1 : 20MHz Xtal
MOSI	0 : E-Fuse (default) 1 : EEPROM
GPIO [14:12]	Chip mode [2:0] => GPIO [14:12] 001:Boot from ROM (default)

T-CHIP	Title: MT7612			
	Size: C	Document Number: MT7612	Drawn: CYL	Rev: V00
	Date: Friday, October 24, 2014	Sheet 12 of 14		



Boot Strapping (Internal Pull High/Low)

EE_CLK	0 : 40MHz Xtal (default) 1 : 20MHz Xtal
MOSI	0 : E-Fuse (default) 1 : EEPROM
GPIO [14:12]	Chip mode [2:0] => GPIO [14:12] 001:Boot from ROM (default)

T-CHIP	Title: MT7612			
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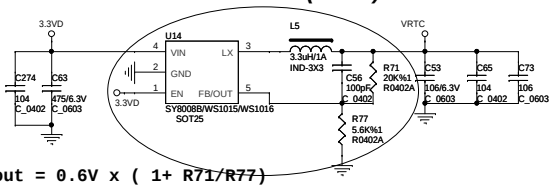
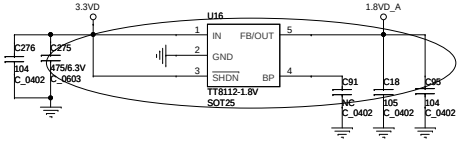
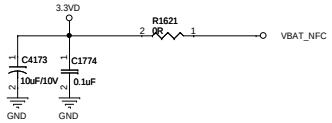
For VRTC Power (2.8V)

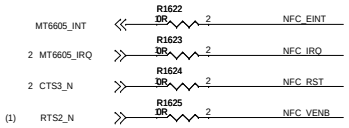


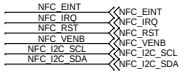
Vout = 0.6V x (1+ R71/R77)

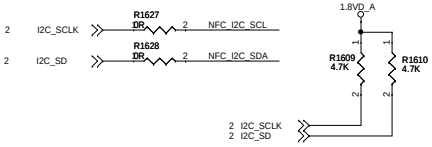
For DVDD_IO_NFC(1.8V)











T-CHIP	Title: MT7612		
	Size: C	Document Number: MT7612	Drawn: CXL / Rev: V00
	Date: Friday, October 24, 2014	Sheet 14 of 14	