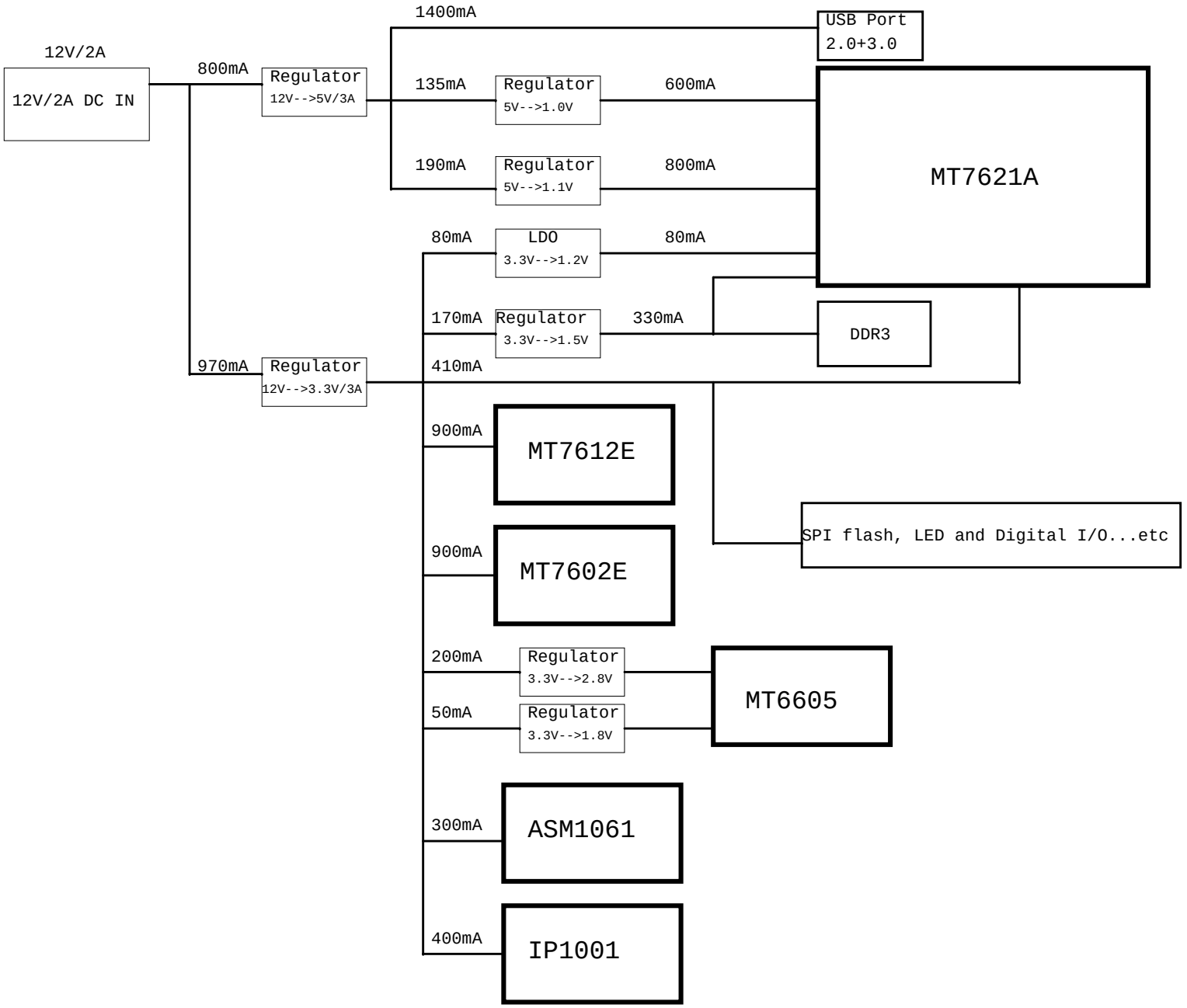
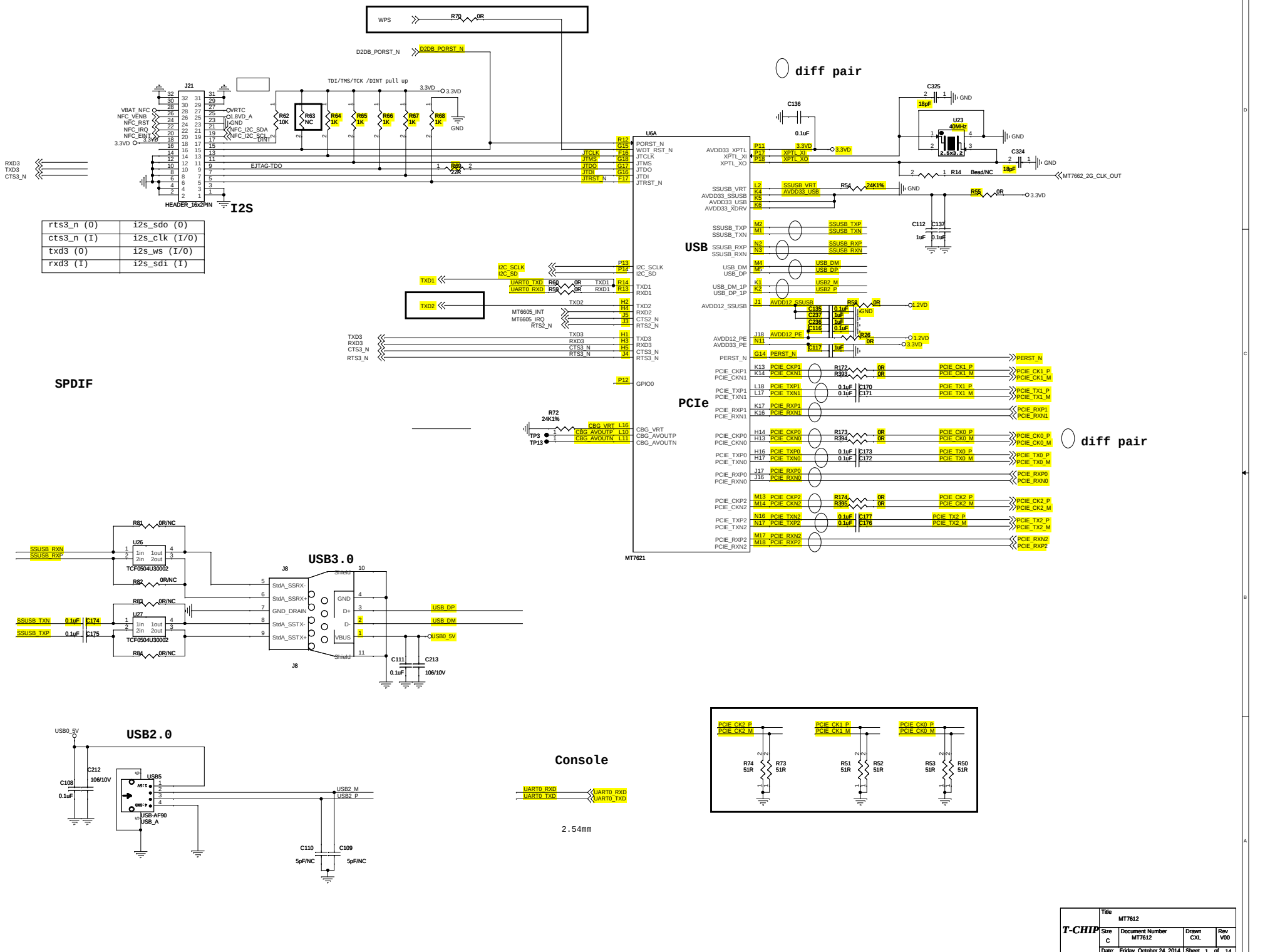

12V/2A
12V/2A DC IN
800mA
Regulator
12V-->5V/3A
1400mA
USB Port
2.0+3.0
135mA
Regulator
5V-->1.0V
600mA
190mA
Regulator
5V-->1.1V
800mA
MT7621A
80mA
LDO
3.3V-->1.2V
80mA
170mA
Regulator
3.3V-->1.5V
330mA
DDR3
970mA
Regulator
12V-->3.3V/3A
410mA
900mA
MT7612E
900mA
MT7602E
SPI flash, LED and Digital I/O...etc
200mA
Regulator
3.3V-->2.8V
50mA
Regulator
3.3V-->1.8V
MT6605
300mA
ASM1061
400mA
IP1001



rts3_n (O)	i2s_sdo (O)
cts3_n (I)	i2s_clk (I/O)
txd3 (O)	i2s_ws (I/O)
rxd3 (I)	i2s_sdi (I)

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DDR3/DDR2 Interface
The pinout is differenet
when use DDR3 and DDR2

diff pair

Test Pad for signal measurement

RDQM0	1	TP4
RDQM1	1	TP5
RDQS0	1	TP6
RDQS0	1	TP7
RDQS1	1	TP31
RDQS1	1	TP8
RRAS	1	TP9
RCS	1	TP10
RCAS	1	TP29
RWE_	1	TP30
RDQ2	1	TP32
RDQ7	1	TP33
RDQ9	1	TP34
RDQ12	1	TP35
RA4	1	TP37
RODT	1	TP36
RDQ15	1	TP38
RA6	1	TP39
RA8	1	TP40

RDQ[0:15] RDQ[0:15]

U6B

RDQ15 C8 RDQ15/RDQ14
RDQ14 C5 RDQ14/RDQ8
RDQ13 B9 RDQ13/RDQ9
RDQ12 A5 RDQ12/RDQ15
RDQ11 B10 RDQ11/RDQ12
RDQ10 B4 RDQ10/RDQ13
RDQ9 C10 RDQ9/RDQ11
RDQ8 A3 RDQ8/RDQ10
RDQ7 C2 RDQ7/RDQ5
RDQ6 C12 RDQ6/RDQ3
RDQ5 B2 RDQ5/RDQ2
RDQ4 B12 RDQ4/RDQ4
RDQ3 A2 RDQ3/RDQ0
RDQ2 A11 RDQ2/RDQ1
RDQ1 B3 RDQ1/RDQ7
RDQ0 C11 RDQ0/RDQ6

RA14 C17 RA14/RA6
RA13 B13 RA13/RBA2
RA12 D15 RA12/RCAS_
RA11 C18 RA11/RA11
RA10 E13 RA10/RA3
RA9 D13 RA9/RBA1
RA8 D16 RA8/RA13
RA7 E11 RA7/RWE_
RA6 D17 RA6/RA8
RA5 B16 RA5/RRAS_
RA4 E15 RA4/RA4
RA3 A16 RA3/RA12
RA2 D14 RA2/RA10
RA1 B18 RA1/RA0
RA0 E14 RA0/RA1

RDQM0 B5 RDQM0 RDQM0
RDQM1 B8 RDQM1 RDQM1
RDQS0 A7 RDQS0 RDQS0
RDQS0_ B7 RDQS0 RDQS0_
RDQS1 C7 RDQS1 RDQS1
RDQS1_ B6 RDQS1 RDQS1_
RBA0/RA9 C16 RBA0 RBA0
RBA1/RA2 B17 RBA1 RBA1
RBA2/RBA0 A13 RBA2 RBA2
RCLK C9 RCLK RCLK
RCLK_ D9 RCLK RCLK_
RCKE/RCKE A17 RCKE RCKE
RRAS_/RA5 C14 RRAS RRAS_
RCAS_/RA7 C15 RCAS RCAS_
RCS_/RCS_ B15 RCS RCS_
RODT/RODT B14 RODT RODT
RWE_/NC A15 RWE RWE_
DDR3RSTB/NC D11 DDR3RSTB DDR3RSTB

TN_MEMPLL E18 TN_MEMPLL
TP_MEMPLL E17 TP_MEMPLL
TP1
TP2
E16
AVDD33_MEMPLL B1 REXTDN
REXTDN C3 DVDD_VREF_A R102 0R DDRVREF DDRVREF
DVDD_VREF J6
DVDD33_IO_1 G2 ND_CS_N ND_CS_N
ND_CS_N F1 ND_RB_N ND_RB_N
ND_RB_N F3 ND_RE_N ND_RE_N
ND_RE_N G3 ND_CLE ND_CLE
ND_CLE F4 ND_WP ND_WP
ND_WP G5 ND_ALE ND_ALE
ND_ALE G4 ND_WE_N ND_WE_N
ND_WE_N F2 ND_D0 ND_D0
ND_D0 E3 ND_D1 ND_D1
ND_D1 E2 ND_D2 ND_D2
ND_D2 E4 ND_D3 ND_D3
ND_D3 D1 ND_D4 ND_D4
ND_D4 D2 ND_D5 ND_D5
ND_D5 C1 ND_D6 ND_D6
ND_D6 D3 ND_D7 ND_D7
ND_D7

MT7621

3.3VD
R436 NC
R435 10K
R408 240R

spi_cs0 (I/O)	nd_cs_n (O)
spi_cs1 (I/O)	nd_we_n (O)
spi_clk (I/O)	nd_re_n (O)
spi_miso (I/O)	nd_d[4] (I/O)
spi_mosi (I/O)	nd_d[5] (I/O)
spi_wp (I/O)	nd_d[6] (I/O)
spi_hold (I/O)	nd_d[7] (I/O)

SPI Flash

3.3VD
R11 4.7K
R9 4.7K
R10 4.7K
R1 NC
U8
ND_CS_N 1 /CS
ND_D4 2 DO
ND_D6 3 /WP
4 GND
VCC 8
/HOLD 7 ND_D7
CLK 6 ND_RE_N
DI 5 ND_D5
MX25L6406EM2I

3.3VD
R414 10K
R429 10K
R430 10K
R431 10K
R432 10K
R433 10K
ND_CLE
ND_D3
ND_D2
ND_D1
ND_D0
ND_ALE

TF/SPI Flash

3.3VD
C1099 22uF/6.3V
C253 105
R76 0R R0402A
ND_RB_N
ND_D2
ND_D3
ND_ALE
ND_D0
ND_D1
ND_CLE

J5
1 DATA2
2 CD/DATA3
3 CMD
4 VDD
5 CLK
6 VSS
7 DATA0
8 DATA1
9 CD
10 G1
11 G2
12 G3
13 G4
TF_SOCKET
MICRO-SD-YST

TF_wp (I)	nd_wp (O)
TF_clk (I/O)	nd_rb_n (I)
TF_cd (I)	nd_cle (O)
TF_cmd (I/O)	nd_ale (O)
TF_data[0] (I/O)	nd_d[0] (I/O)
TF_data[1] (I/O)	nd_d[1] (I/O)
TF_data[2] (I/O)	nd_d[2] (I/O)
TF_data[3] (I/O)	nd_d[3] (I/O)

OPTION

ED6	NC/ESD9B5V	E0402N
ED7	NC/ESD9B5V	E0402N
ED8	NC/ESD9B5V	E0402N
ED9	NC/ESD9B5V	E0402N
ED10	NC/ESD9B5V	E0402N
ED11	NC/ESD9B5V	E0402N
ED12	NC/ESD9B5V	E0402N

T-CHIP

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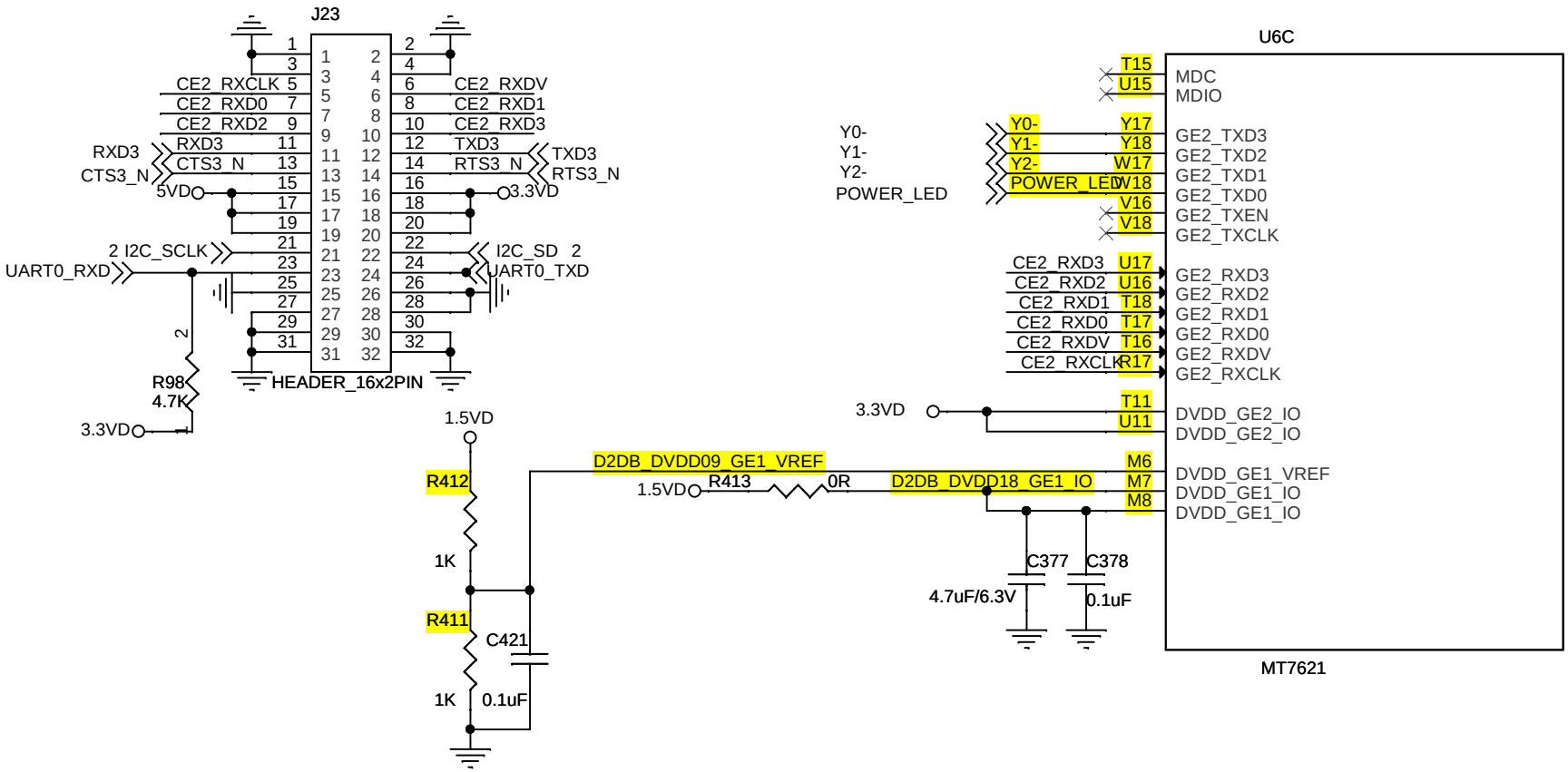
RGMII Interface



T-CHIP	Title: MT7612			
	Size: C	Document Number: MT7612	Drawn: CXL	Rev: V00
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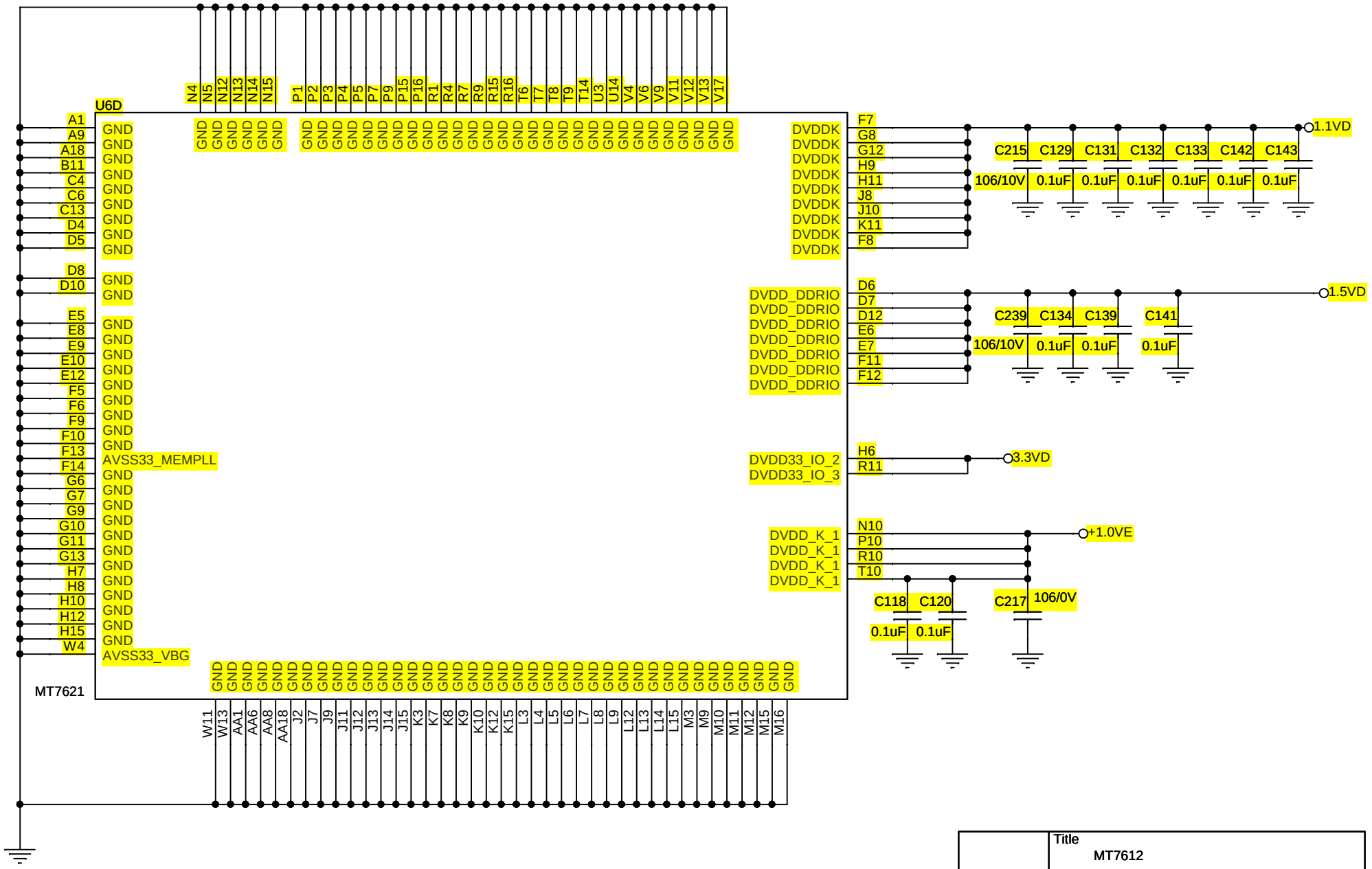
MT7621 Power



T-CHIP	Title: MT7612		
	Size: C	Document Number: MT7612	Drawn: CXL / Rev: V00
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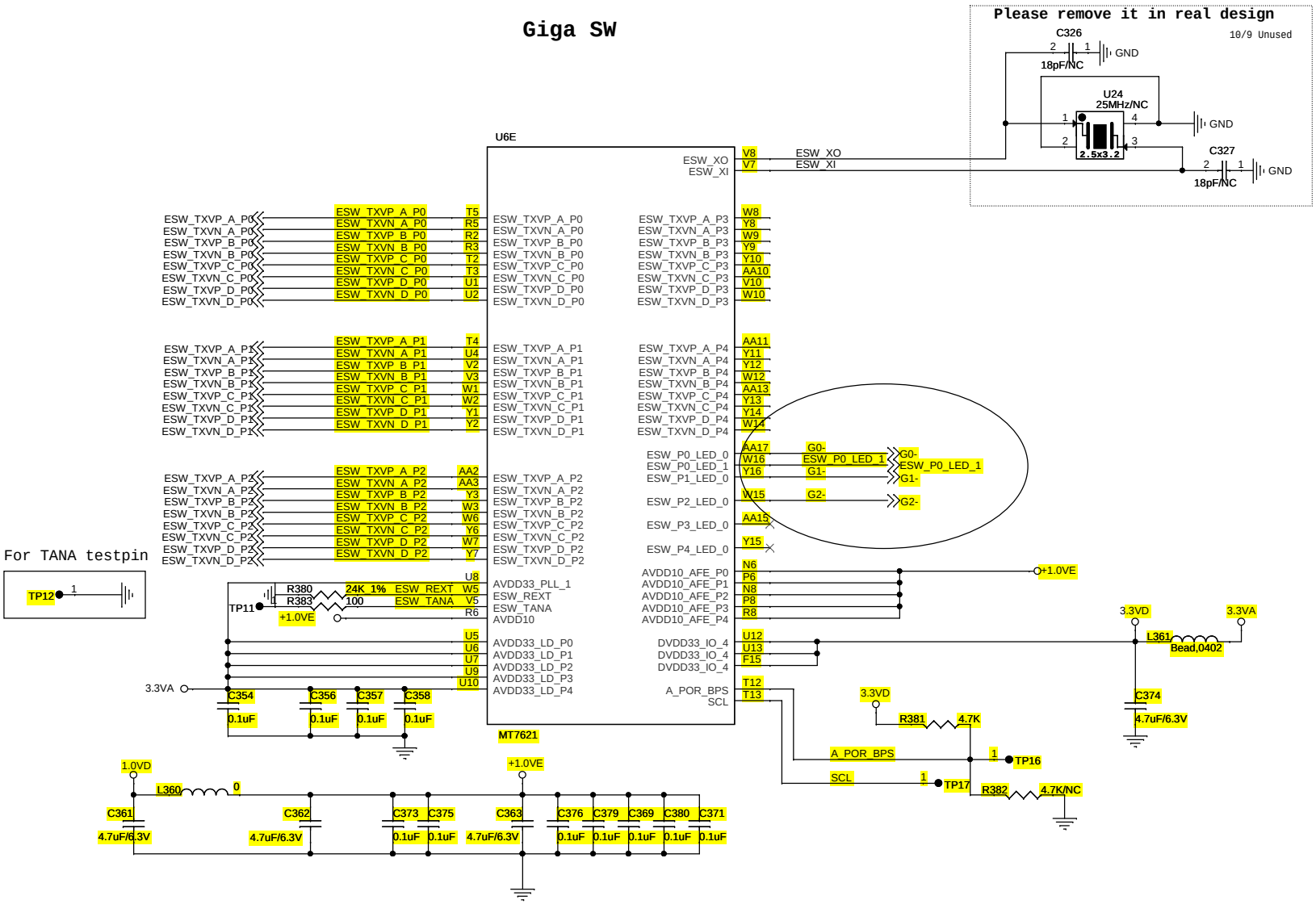
Giga SW



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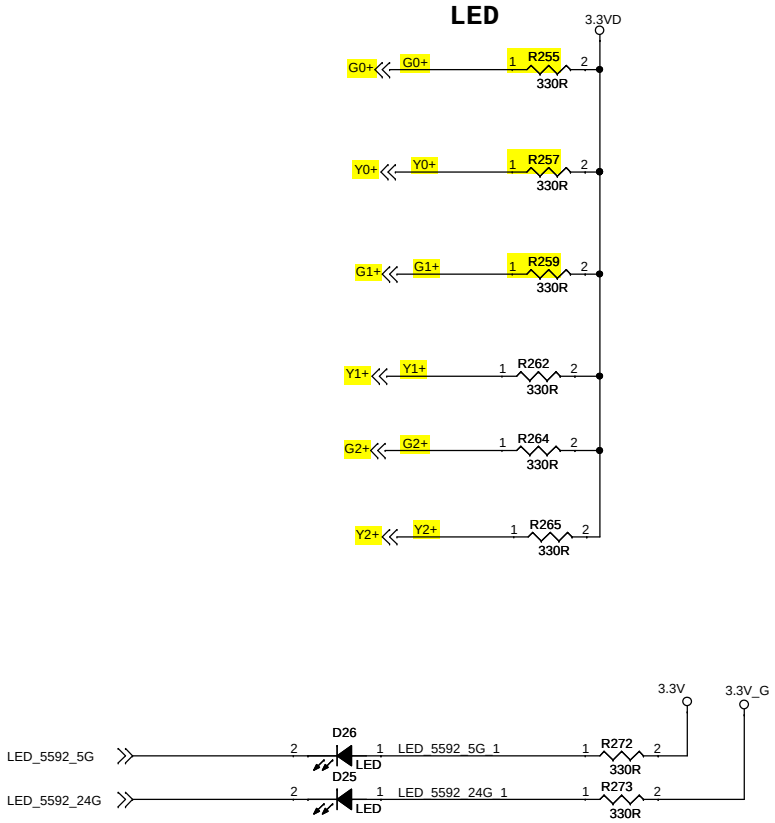
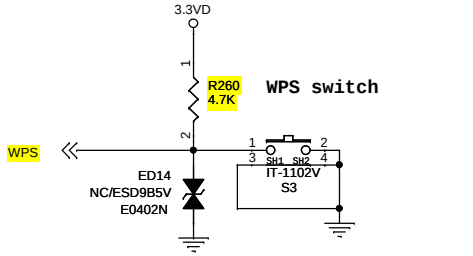
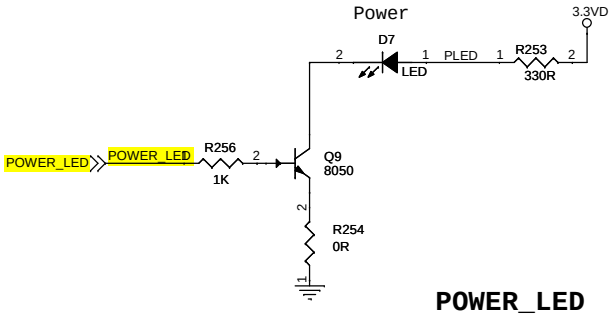
	Size: C	Document Number: MT7612	Drawn: CXL	Rev: V00
	Date: Friday, October 24, 2014	Sheet 5 of 14		







T-CHIP	Title: MT7612			
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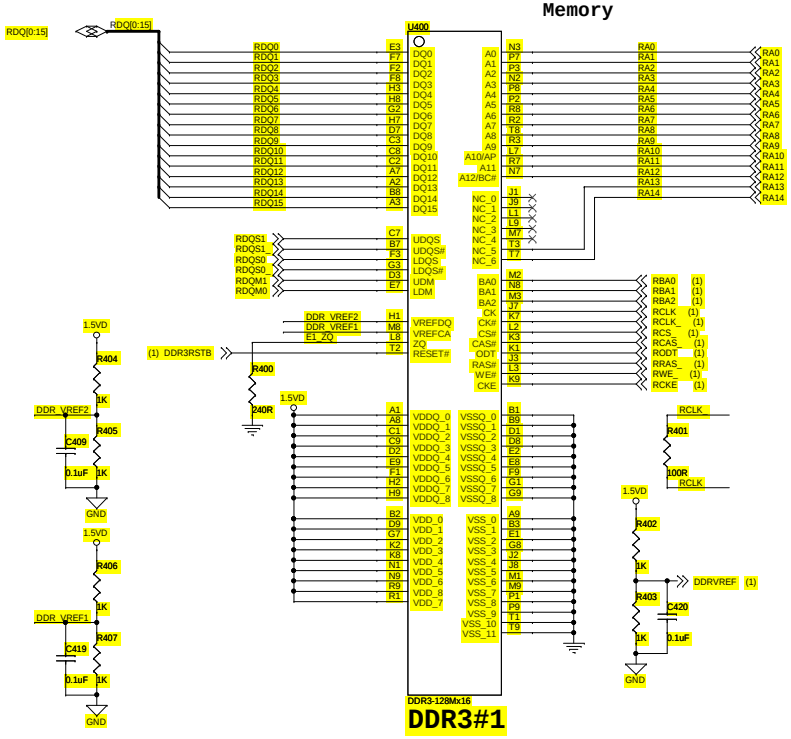
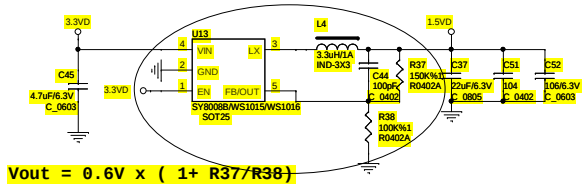
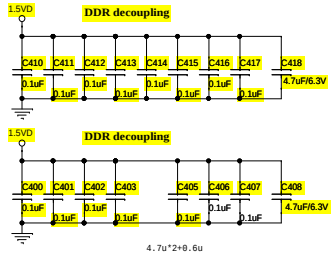
Memory







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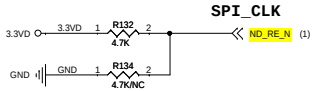
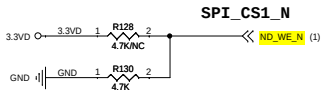
Boot Strapping

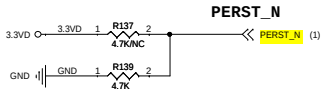
Pin Name	Description	Value	
SPI_CLK	DRAM_FROM_EE	For non scan mode: 0: DRAM/PLL configuration from EEPROM **1: DRAM configuration from Auto Detect**	For FT mode: 0: SUTIF 1: 3-wire SPI
{SPI_CS1_N, SPI_CS0_N, MDC }	XTAL_MODE	000: 20 MHz, Self Oscillation mode 001: 20 MHz, Single end input 010: 20 MHz, differential input **011: 40 MHz, Self Oscillation mode**	100: 40 MHz, Single end input 101: 40 MHz, differential input 110: 25 MHz, Self Oscillation mode 111: 25 MHz, Single end input
PERST_N	OCP_RATIO	**0: 1:3** 1: 1:4	
TXD2	DRAM_TYPE	**0: DDR3** 1: DDR2	
{RTS2_N, RTS3_N, TXD1, GPIO0}	CHIP_MODE[3:0]	0000: Normal / Boot from SPI 4-byte address and XTAL clock 0001: Normal / Boot from ROM (NAND page 2k+64 bytes) **0010: Normal / Boot from SPI 3-byte address** 0011: Normal / Boot from SPI 4-byte address 0100: iNIC RGMI / Boot from ROM 0101: iNIC MII / Boot from ROM 0110: iNIC RVMII / Boot from ROM 0111: iNIC PHY / Boot from ROM 1000: iNIC RGMII / Boot from ROM and XTAL clock 1001: Normal / Boot from internal SRAM 1010: Normal / Boot from ROM (NAND page 2k+128 bytes) 1011: Normal / Boot from ROM (NAND page 4k+128 bytes) 1100: Normal / Boot from ROM (NAND page 4k+224 bytes) 1101: Debug mode 1110: Scan mode 1111: Final Test	

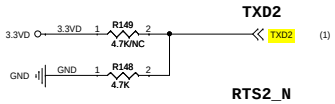
Giga Switch Hardware Trap

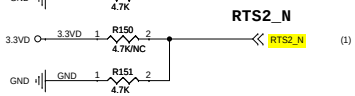
Pin Name	Trap	Fuction	Description	Default
P0_LED_0	HWTRAP[0]	HT_CHIP_MODE[0]	chip_mode[3:0] 4'b0000: IDDQ mode 4'b0001: IOTEST mode 4'b0010: NANDTREE mode 4'b0011: RING mode (both IO and std-cell) 4'b0100: MBIST 4'b0101: SCAN mode (internal) 4'b0110: SCAN-COMP mode (compression) 4'b0111: SCAN-MBIST-OLT mode 4'b1000: AFE-OLT mode 4'b1001: GPHY ATE mode 4'b1010: GPHY ADUMP mode 4'b1011: GPHY ADUMP probe mode 4'b1100: Reserved 4'b1101: Reserved 4'b1110: bootup probe mode 4'b1111: normal mode	4'b1111
P1_LED_0	HWTRAP[1]	HT_CHIP_MODE[1]		
P2_LED_0	HWTRAP[2]	HT_CHIP_MODE[2]		
P0_LED_1	HWTRAP[3]	HT_CHIP_MODE[3]		
P3_LED_0	HWTRAP[9]	HT_XTAL_FSEL[0]	External Crystal Frequency Selection xtal_freq_sel[1:0] 2'b01: 20MHz 2'b10: 40MHz 2'b11: 25MHz	2'b10
P4_LED_0	HWTRAP[10]	HT_XTAL_FSEL[1]		

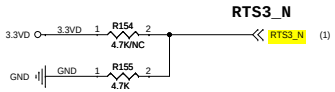


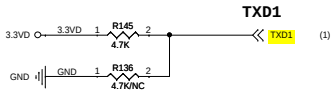


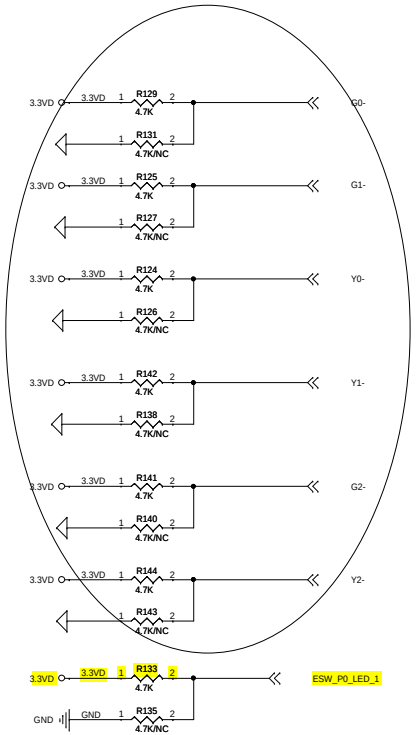


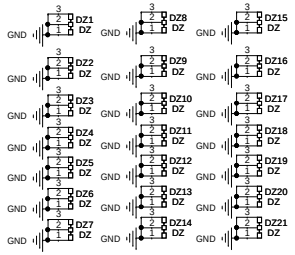












T-CHIP	Title: MT7612			
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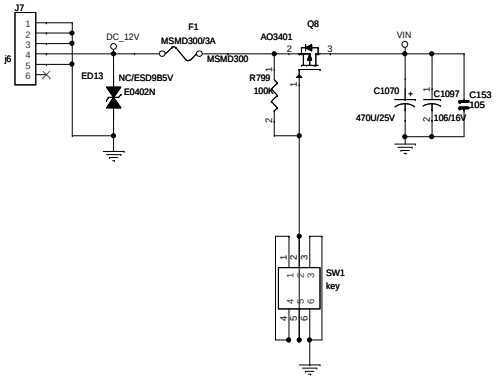
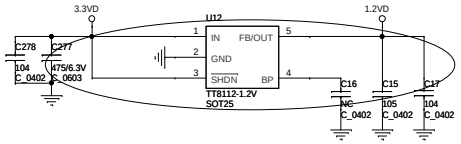
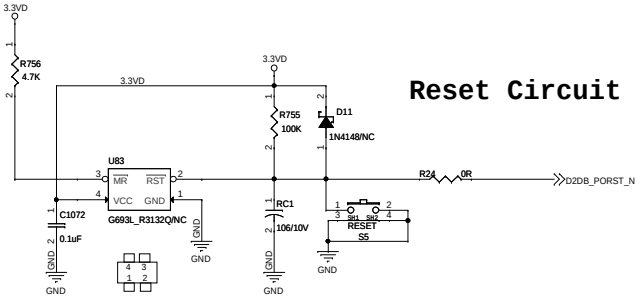
System Power

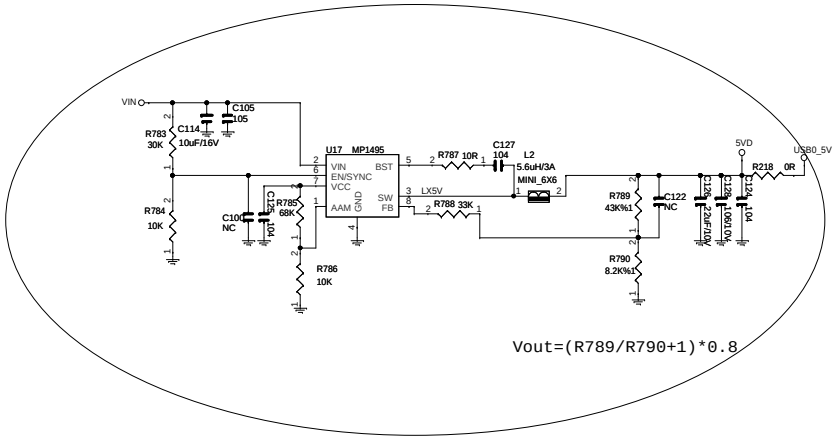
For USB/PCIe PHY Power (1.2V)
Current= 300mA



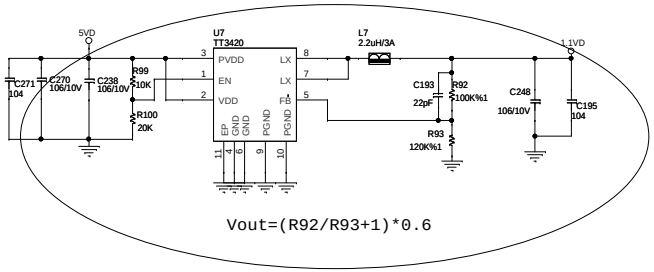




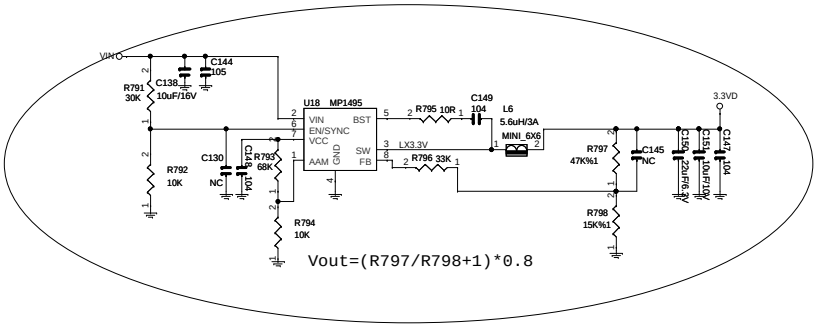
Reset Circuit



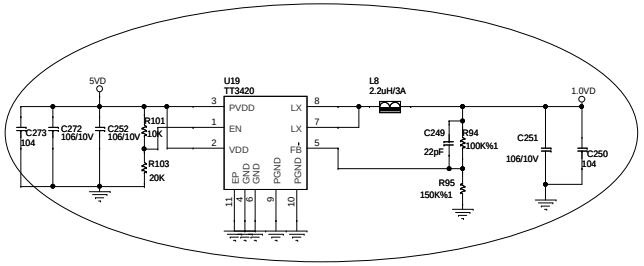
Vout=(R789/R790+1)*0.8



Vout=(R92/R93+1)*0.6



Vout=(R797/R798+1)*0.8



Vout=(R94/R95+1)*0.6

T-CHIP	Title: MT7612			
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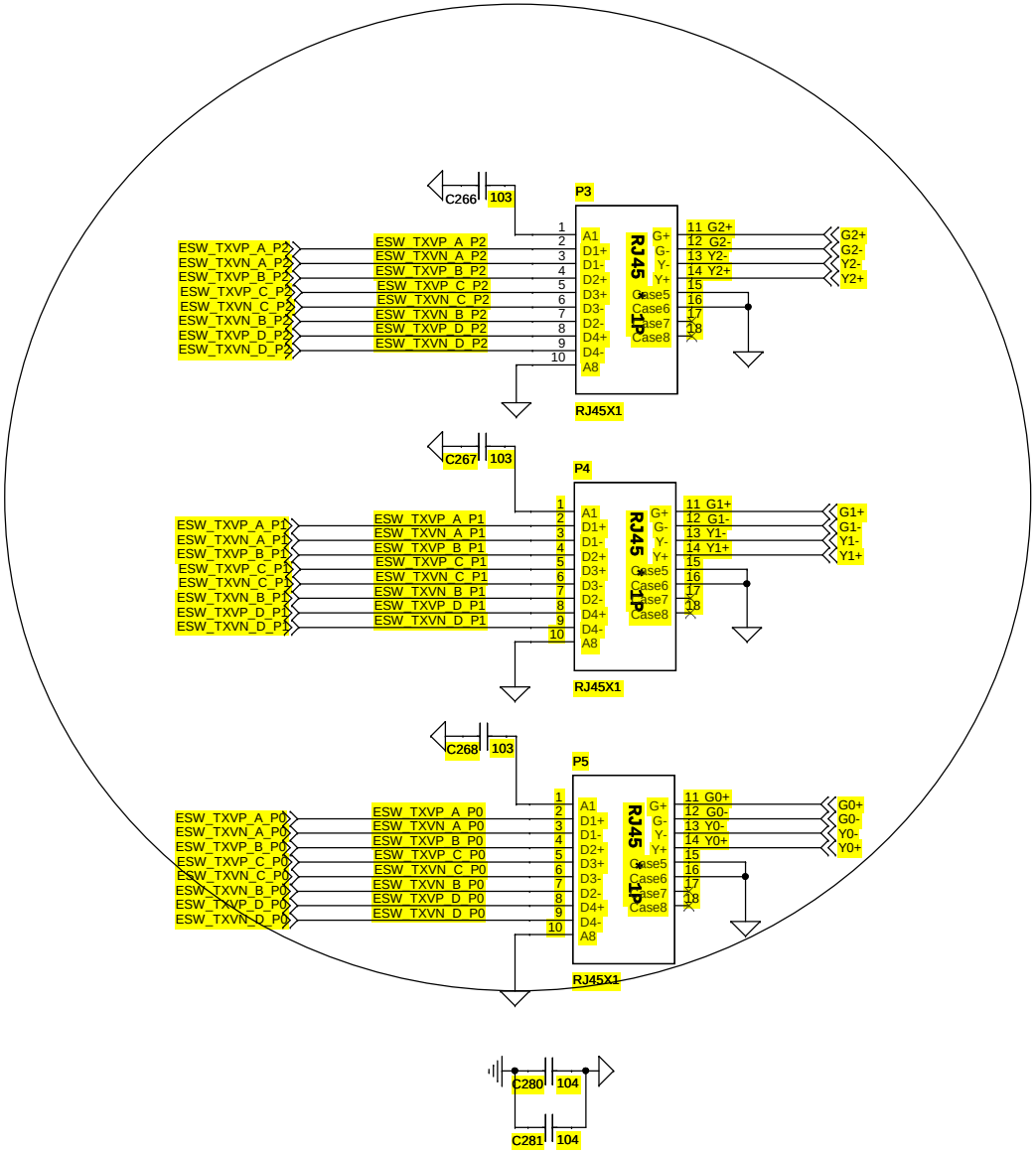

T-CHIP	Title: MT7612			
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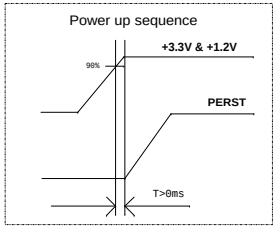
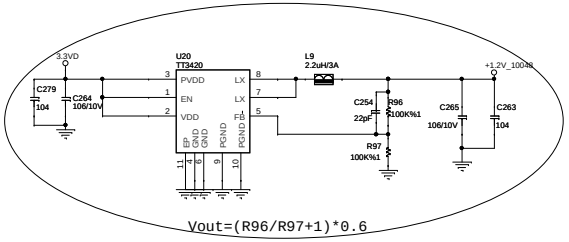
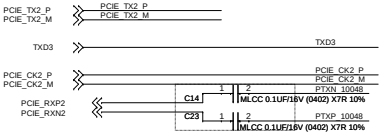
PCIe to SATA

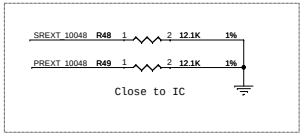




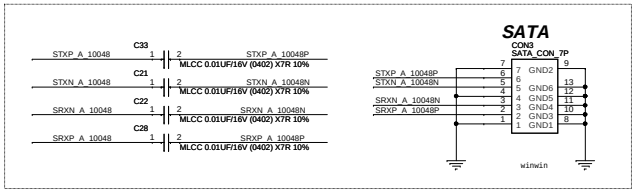
Vout=(R96/R97+1)*0.6

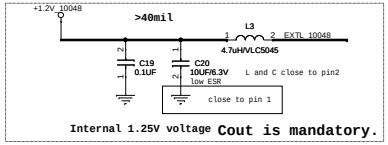


Close to PCIe Slot
X7R/0402 type

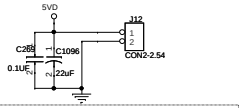


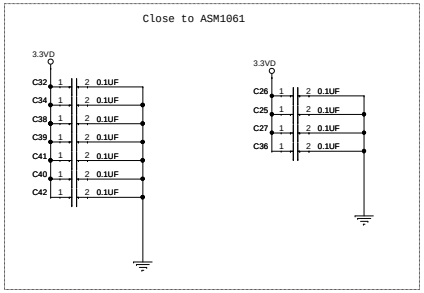
Close to IC

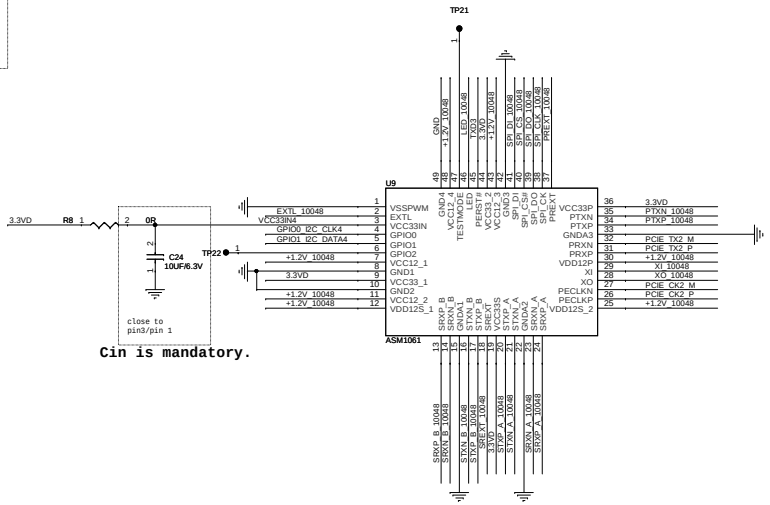




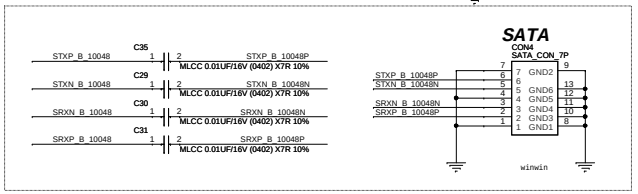
Internal 1.25V voltage **Cout is mandatory.**

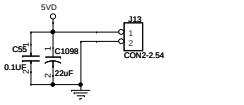


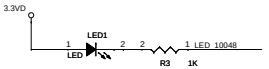


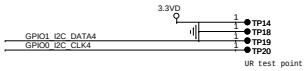


Cin is mandatory.







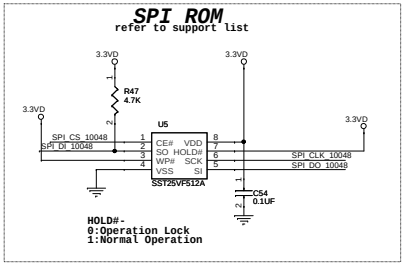


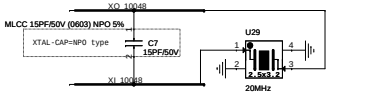
UR test point

H/W Strapping

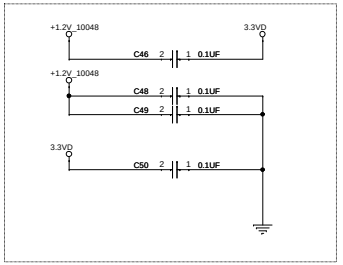
refer to datasheet:

SPI_DO
0: Spin up by H/W
1: Spin up by S/W





XI & XO follow differential layout rule for Min. jitter



T-CHIP	Title: MT7612			
	Size: C	Document Number: MT7612	Drawn: CXL	Rev: V00
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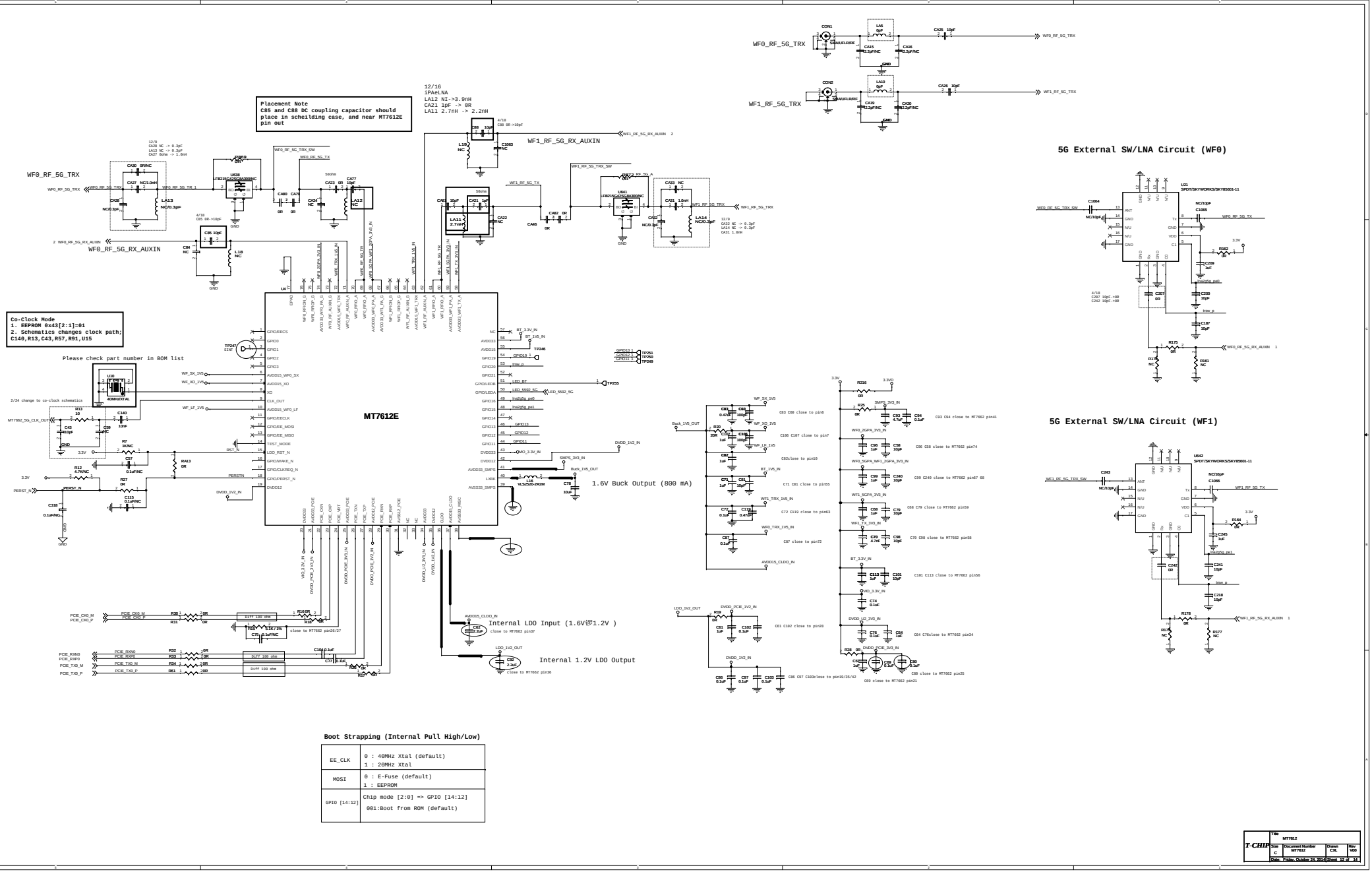
Placement Note
C85 and C88 DC coupling capacitor should place in scheilding case, and near MT7612E pin out
12/16
1PAeLNA
LA12 NI->3.9nH
CA21 1pF -> 0R
LA11 2.7nH -> 2.2nH
Co-Clock Mode
1. EEPROM 0x43[2:1]=01
2. Schematics changes clock path; C140,R13,C43,R57,R91,U15
Please check part number in BOM list
MT7612E
1.6V Buck Output (800 mA)
Internal LDO Input (1.6V或1.2V)
Internal 1.2V LDO Output
5G External SW/LNA Circuit (WF0)
5G External SW/LNA Circuit (WF1)
WF0_RF_5G_TRX
WF1_RF_5G_TRX
WF0_RF_5G_RX_AUXIN
WF1_RF_5G_RX_AUXIN
MT7662_5G_CLK_OUT
PERST_N
PCIE_CKP_M
PCIE_CKP_P
PCIE_TXP_M
PCIE_TXP_P
PCIE_RXP_M
PCIE_RXP_P
Boot Strapping (Internal Pull High/Low)
EE_CLK
0 : 40MHz Xtal (default)
1 : 20MHz Xtal
MOSI
0 : E-Fuse (default)
1 : EEPROM
GPIO [14:12]
Chip mode [2:0] => GPIO [14:12]
001:Boot from ROM (default)
T-CHIP
MT7612
C
Friday, October 24, 2014
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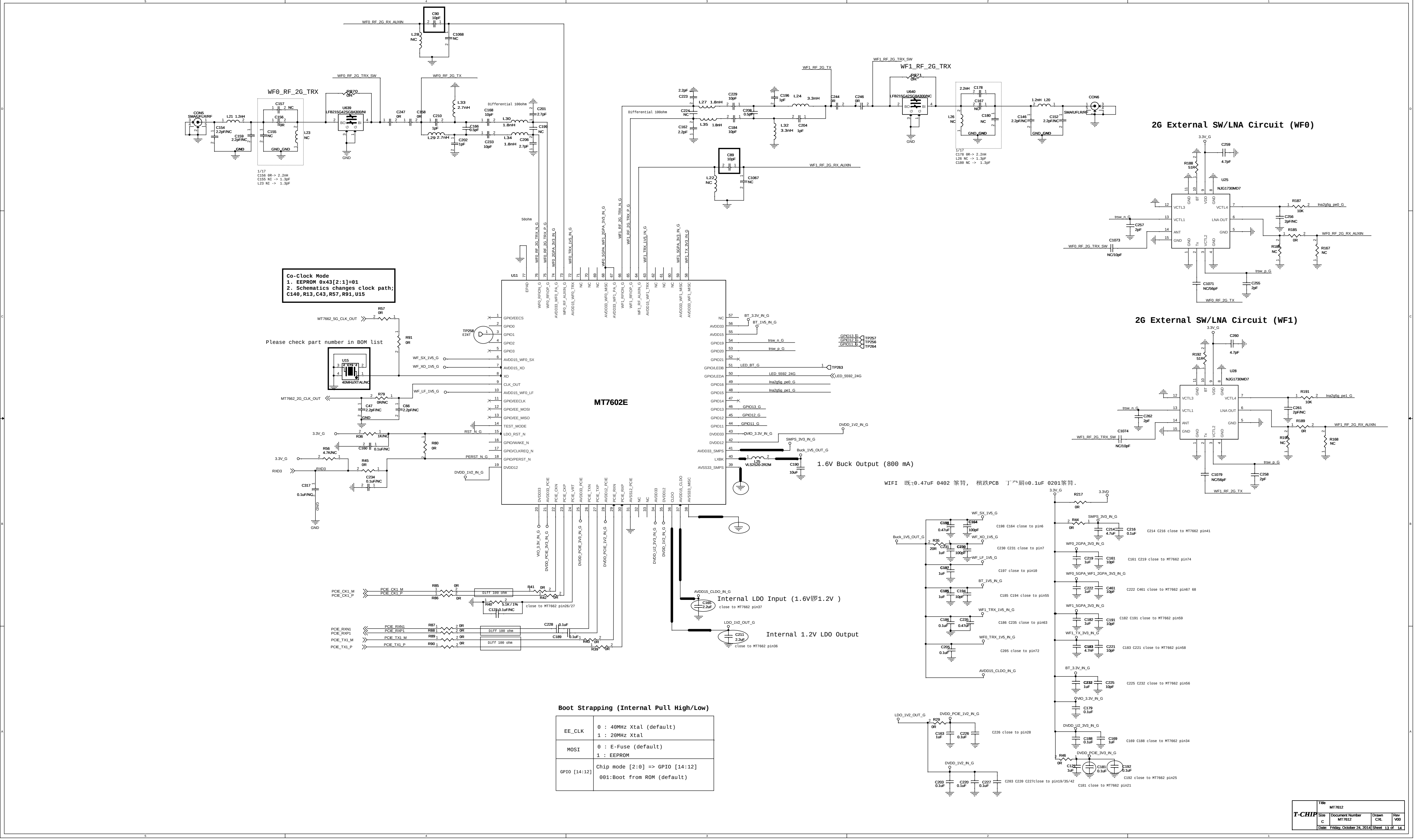

Boot Strapping (Internal Pull High/Low)

EE_CLK	0 : 40MHz Xtal (default) 1 : 20MHz Xtal
MOSI	0 : E-Fuse (default) 1 : EEPROM
GPIO [14:12]	Chip mode [2:0] => GPIO [14:12] 001:Boot from ROM (default)

T-CHIP	Title: MT7612
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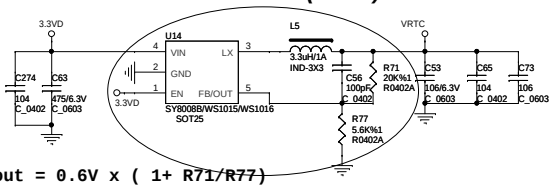
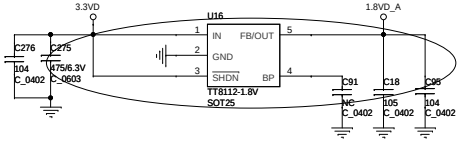
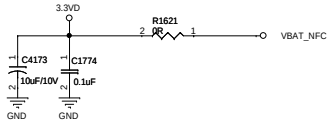
For VRTC Power (2.8V)

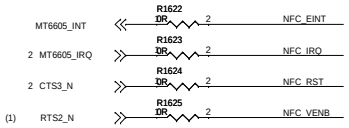


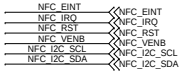
Vout = 0.6V x (1+ R71/R77)

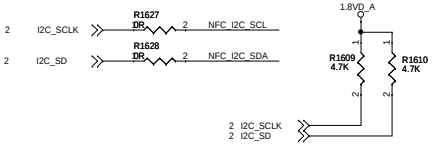
For DVDD_IO_NFC(1.8V)











T-CHIP	Title: MT7612		
	Size: C	Document Number: MT7612	Drawn: CXL / Rev: V00
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