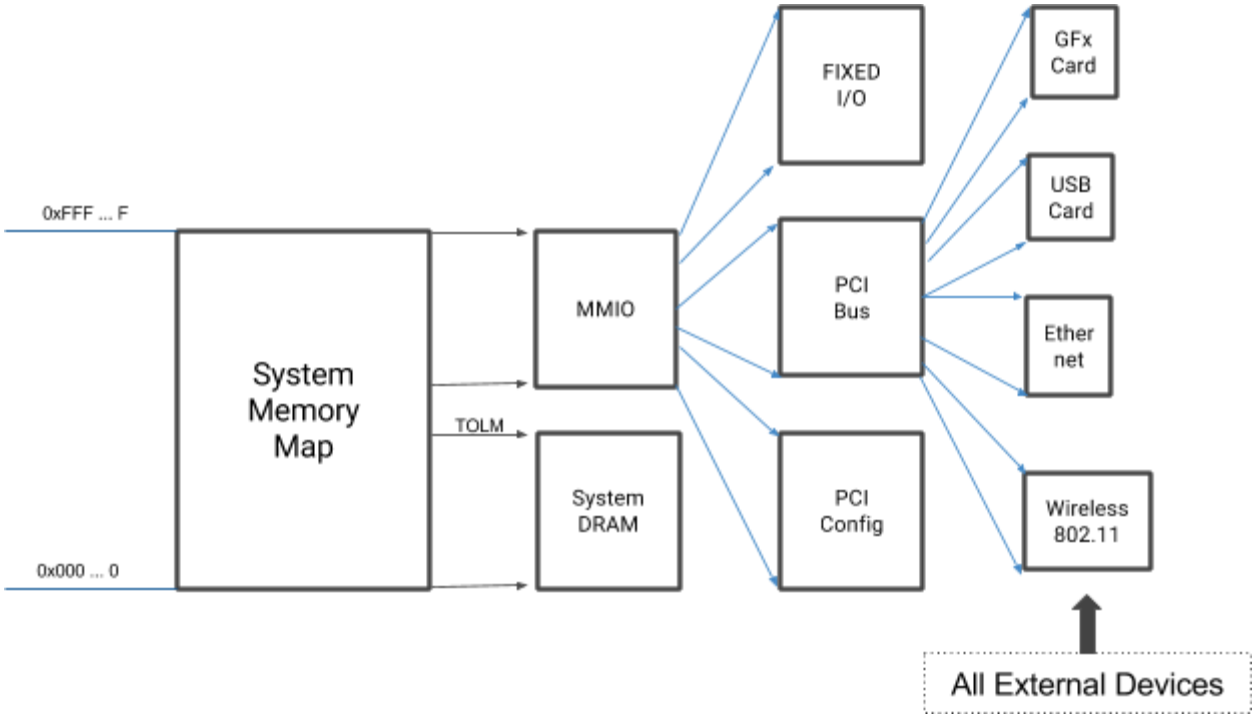
System Memory Map



PCI protocols that are used to identify external devices are often used to identify internal devices.

The PCIe bus portion of the the memory map (for the Intel Architecture) is not fixed.

The BIOS / firmware / OS write to the BAR (Base Address Register) at system initialization to determine the map dynamically.

In other systems designs this information is static and devices are assigned ranges at system on a chip (SOC) design time.

Intel Architecture is a lot more flexible regarding what can be connected to it , E.g. Intel Atom

Interrupt Controller (Another important concept for multitasking)

Typically and varying between manufacturers, the whole concept is asynchronously set on the chip for parallelization, on the device internally at SOC level. The attention of the processor is grabbed / peaked and it is interrupted to do another job.

This is a process queue and each process runs a little and then the cpu does something else.

We don't wait for the information from the disc, when the disk arm is ready it will send an interrupt to stop whatever the cpu is doing and say hey , I need you now.

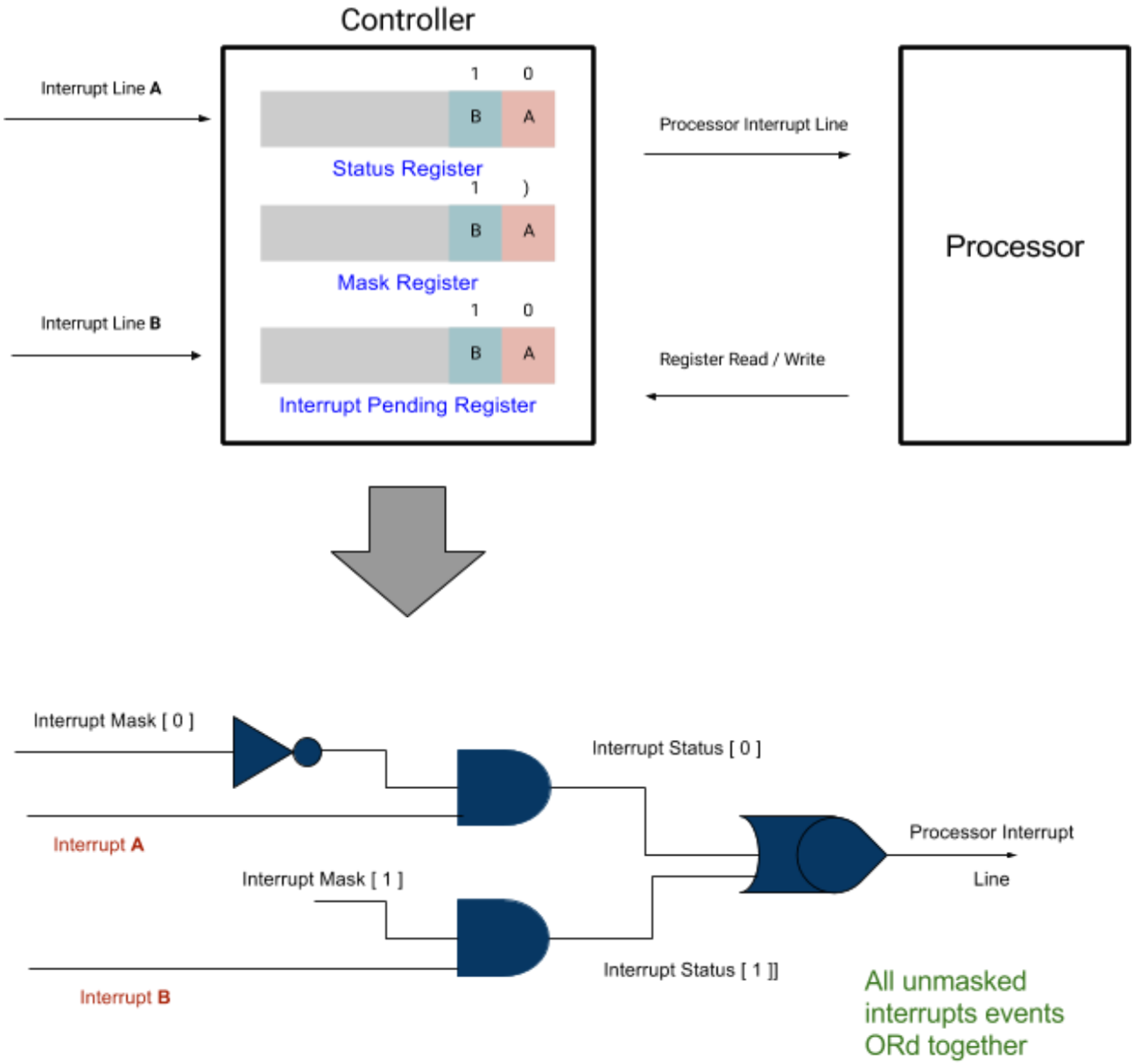
Sensors from the environment or real world can also change the state of exposed pins and act as interrupts.

With all these simultaneous interrupts occurring we need something to control them all hence

Interrupt Controller

- Enables the processors to interact with its environment
- Mechanism used by devices to indicate the need for the processors attention
- Avoids polling (devices checking another device to see what state a device changes to)
- There are usually multiple sources of interrupts hence the need for a controller

The interrupt controller gathers all the hardware interrupts event , identifies them and presents them to the processor in a well defined manner.



Each bit in the above interrupt controller register is dedicated to a specific interrupt source.

When the processor interrupt line becomes active, the processor saves its state and transfers control to the vector (interrupt handler) for external processor interrupts.

The interrupt handler reads the interrupt status register bits from the least significant bit (There is an implicit priority here which may be changed since its under software control)

PIC (Programmers Interrupts Controller).

8 input lines is not enough so we cascade to 16 which itself is becoming inadequate.