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| **Course Title** | Computer Organization | **CSC 322** |
| **Semester** | Spring 2022 |
| **Course Coordinator** | Haidar Harmanani |
| **Class Time and location** |  | |
|  | *Classes will be held from January 18, 2022 until April 29, 2022* | |
| **Last Revised on** | January 10, 2022 | |

Instructor

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***Course Page*:** <http://vlsi.byblos.lau.edu.lb/courses/csc322/>

***Office:*** *812 Block A*

***Office Hours:*** *By Appointment*

**Current Catalog Description**

Students gain experience with computer organization techniques by designing and implementing actual circuits using a high-level language, Verilog HDL and FPGAs. Course culminates in the design and simulation of a complete pipelined CPU.

Course Prerequisite/Co-requiste

Co-requisites: CSC 322: Computer Organization.

**References**

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| 1. S. Brown and Z. Vranesic, *Fundamentals of Digital Logic with Verilog Design*, 3rd Edition, McGraw Hill, 2014. 2. D. Patterson and J. Hennessy, *Computer Organization and Design: The Hardware/Software Interface,* 5th Edition, Morgan Kaufman. |

**Course Type**

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| **R**equired |  | **E**lective |  | **S**elective **E**lective |  |

**Course Learning Outcomes**

1. Students should be able to describe analytically combinational and sequential circuits functions.
2. Students shall demonstrate the ability to use FPGAs in order to implement combinational and sequential circuits.
3. Students shall demonstrate the ability to use CAD tools such as Altera or Xilinx in order to implement and simulate circuits.
4. Students shall demonstrate the ability to design, implement, and simulate, a given system with constraints, and to evaluate the system in terms of general quality attributes and possible tradeoffs.

**Student Outcomes Addressed in this Course**

Outcome 1 contributes to SO.1, and SO.10

Outcome 2 contributes to SO.3 and SO.9

Outcome 3 contributes to SO.9

Outcome 4 contributes to SO.3 and SO.9

**Topics Covered in the Course**

1. Fundamentals of logic design principles
2. Introduction to C/C++ and architectural modeling
3. Introduction to Verilog programming
4. Using Quartus II and FPGA prototyping
5. Design and implementation of combinational and sequential circuits
6. Creating and building the different components to build a simple computer system

Course Grading and Performance Criteria

Laboratory exercises consist of hands-on assignments that illustrate concepts discussed in the course (CSC 320). Lab problems are based on C and FPGA related designs using Verilog. We will be using Altera Boards as well as the Altera Quartus II Design Automation tools. The system consists of an integrated set of tools that allow one to capture designs (with schematics entry or a Hardware Description Language), simulate, and implement and test them. You will be also required to complete two design projects that complement each other. The first project will model an Instruction Set Architecture using C while the second will implement it using Verilog. The Hardware project must be downloaded to the FPGA board and tested for functional correctness. Since the class is relatively small, you are required to orally present your projects.

Exams 15%

Labs 85%

All labs should be submitted along with a report should typically be 1-2 pages long.

**Assessment Plan for the Course**

End of semester self-assessment. Embedded Assessment. Systematic Progression of Assignments. Reviewed every Spring semester by the coordinators for possible updates in the following Fall. Detailed review of all materials of the course once every three years by the CSC Curriculum Committee.

#### **Policy on Cheating and Plagiarism**

Students caught cheating on an exam receive a grade of zero on the exam in their first cheating attempt and receive a warning. Students caught cheating for the second time will receive a grade of “F” in the course and another warning. Plagiarism on assignments and project work is a serious offense. If plagiarism is detected, a student will be subject to penalty, similar to the cheating case, which ranges from receiving a zero on the assignment concerned to an “F” in the course in addition to a warning.

#### **University Attendance Policy**

Missing one third of classes implies that a student has to drop the course. (or alternative policy, provided that the number of missed classes is not less than 2 weeks of classes)

**Withdrawal policy**

Students are advised to consult the University Official Policy regarding courses withdrawal at the following link: <http://www.lau.edu.lb/academics/arp/u/withdrawal-from-university.php>. In specific:

* WI (Early Withdrawal) Indicates withdrawal from the course, after the Late Registration Period and until the end of the 5th week of the Fall and Spring semesters, and until the 10th day of the Summer modules. It has no quality points. It does not count in the GPA, and no credits will be added to the student’s record.
* WP (Withdrawal Pass) indicates withdrawal from the course, after the 5th week and until the end of the 10th week of the Fall and Spring semesters, and from the 11th day of classes until 18th day of the Summer modules. It has no quality points. It does not count in the GPA, and no credits will be added to the student’s record.
* WF (Withdrawal Fail) indicates withdrawal from the course, after the 5th week and until the end of the 10th week of the Fall and Spring semesters, and from the 11th day of classes until 18th day of the Summer modules. It has no quality points. It does not count in the GPA, and no credits will be added to the student’s record, but is counted as repeat.

A Withdrawal Form must be submitted to the Registrar’s Office.

*Deadline for withdrawal from courses with a WI is* **February 21, 2022** and **March 29, 2022** for withdrawal with a WP/WF (It is the student’s responsibility to drop the course).