同济大学计算机系

计算机组成原理实验报告

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一、实验内容

学习了解除法器的原理，实现一个 32 位无符号除法器和一个 32 位带符号除法器

二、模块建模

32 位无符号除法器：

功能描述：将两个 32 位无符号数相除，得到一个 32 位商和 32 位余数。

verilog 代码：

```
module DIVU(
input [31:0]dividend,
input [31:0]divisor,
input start,
input clock,
input reset,
output [31:0]q,
output [31:0]r,
output reg busy
);
reg[4:0]count;
reg [31:0] reg_q;
reg [31:0] reg_r;
reg [31:0] reg_b;
reg r_sign;
wire [32:0] sub_add=r_sign?({reg_r,reg_q[31]}+{1'b0,reg_b}):({reg_r,reg_q[31]}-{1'b0,reg_b});
assign r = r_sign? reg_r + reg_b : reg_r;
assign q = reg_q;
always @ (posedge clock or posedge reset)
begin
  if(reset == 1)
  begin
    count <=5'b0;
    busy <= 0;
  end
  else
  begin
    if (start)
    begin
      reg_r <= 32'b0;
      r_sign <= 0;
      reg_q <= dividend;
      reg_b <= divisor;
      count <= 5'b0;
```

```
            busy <= 1'b1;
        end
        else if (busy)
        begin
            reg_r <= sub_add[31:0];
            r_sign <= sub_add[32];
            reg_q <= {reg_q[30:0],~sub_add[32]};
            count <= count +5'b1;
            if (count == 5'h1f)
                busy <= 0;
        end
    end
end
endmodule
```

32 位带符号除法器：

功能描述：将两个 32 位带符号数相除，得到带符号的 32 位商和 32 位余数

verilog 代码：

```
module DIV(
input [31:0] dividend,
input [31:0] divisor,
input start,
input clock,
input reset,
output [31:0] q,
output [31:0] r,
output reg busy
);
reg[4:0]count;
reg [31:0] reg_q;
reg [31:0] reg_r;
reg [31:0] reg_b;
reg r_sign;
reg sign_d,sign_r;
wire [31:0] mid_q;
wire [31:0] mid_r;
wire [32:0] sub_add=r_sign?({reg_r,reg_q[31]}+{1'b0,reg_b}):({reg_r,reg_q[31]}-{1'b0,reg_b});
assign mid_r = r_sign? reg_r + reg_b : reg_r;
assign mid_q = reg_q;
assign r=sign_d?-mid_r:mid_r;
assign q=(sign_d^sign_r)?-mid_q:mid_q;
always @ (posedge clock or posedge reset)
begin
    if(reset == 1)
    begin
        count <=5'b0;
        busy <= 0;
    end
    else
    begin
        if (start)
        begin
            reg_r <= 32'b0;
            r_sign <= 0;
            if(dividend[31]==0)
                reg_q <= dividend;
            else
                reg_q<=-dividend;
            if(divisor[31]==0)
                reg_b <= divisor;
            else
                reg_b=-divisor;
            sign_d<=dividend[31];
            sign_r<=divisor[31];
            count <= 5'b0;
            busy <= 1'b1;
        end
        else if (busy)
        begin
            reg_r <= sub_add[31:0];
            r_sign <= sub_add[32];
            reg_q <= {reg_q[30:0],~sub_add[32]};
            count <= count +5'b1;
            if (count == 5'h1f)
            begin
                busy <= 0;
            end
        end
    end
end
endmodule
```

三、测试模块建模

32 位无符号除法器：

```
module DIVU_tb();
reg [31:0] dividend;
reg [31:0] divisor;
```

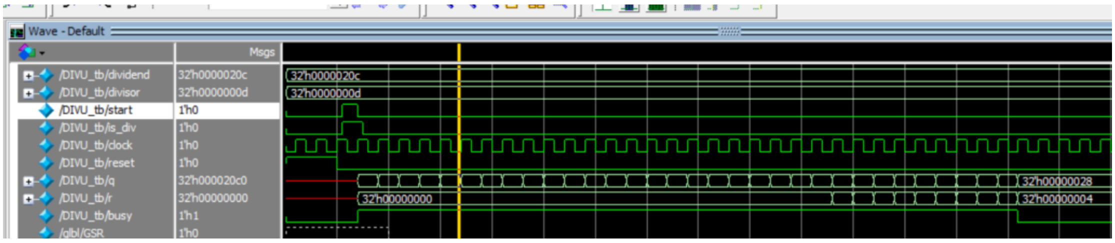
```
wire start;
reg is_div;
reg clock;
reg reset;
wire [31:0] q;
wire [31:0] r;
wire busy;
assign start=is_div&~busy;
DIVU DIVU_inst(dividend,divisor,start,clock,reset,q,r,busy);
initial
begin
    clock=0;
    reset=1;
    is_div=0;
    dividend=524;
    divisor=13;
    #50 reset=0;
    #5 is_div=1;
    #20 is_div=0;
end
always
begin
    #10 clock=~clock;
end
endmodule
```

32 位带符号除法器：

```
module DIV_tb();
reg [31:0] dividend;
reg [31:0] divisor;
wire start;
reg is_div;
reg clock;
reg reset;
wire [31:0] q;
wire [31:0] r;
wire busy;
assign start=is_div&~busy;
DIV DIV_inst(dividend,divisor,start,clock,reset,q,r,busy);
initial
begin
    clock=0;
    reset=1;
    is_div=0;
    dividend=-5;
    divisor=-2;
    #50 reset=0;
    #5 is_div=1;
    #20 is_div=0;
end
always
begin
    #10 clock=~clock;
end
endmodule
```

四、实验结果

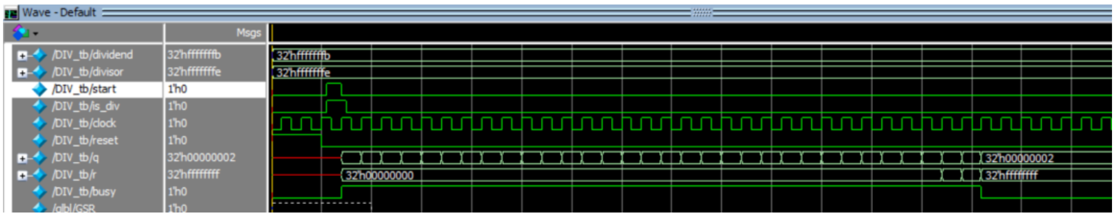
32 位无符号除法器：



Wave - Default

	Msgs
/DIVU_tb/dividend	32'h0000020c
/DIVU_tb/divisor	32'h0000000d
/DIVU_tb/start	1'h0
/DIVU_tb/is_div	1'h0
/DIVU_tb/clock	1'h0
/DIVU_tb/reset	1'h0
/DIVU_tb/q	32'h000020c0
/DIVU_tb/r	32'h00000000
/DIVU_tb/busy	1'h1
/glbl/GSR	1'h0

32 位带符号除法器：



Wave - Default

	Msgs
/DIV_tb/dividend	32'hfffffffb
/DIV_tb/divisor	32'hfffffffe
/DIV_tb/start	1'h0
/DIV_tb/is_div	1'h0
/DIV_tb/clock	1'h0
/DIV_tb/reset	1'h0
/DIV_tb/q	32'h00000002
/DIV_tb/r	32'hffffffff
/DIV_tb/busy	1'h0
/glbl/GSR	1'h0