Shri Vaishnav Vidyapeeth Vishwavidyalaya

A Presentation on

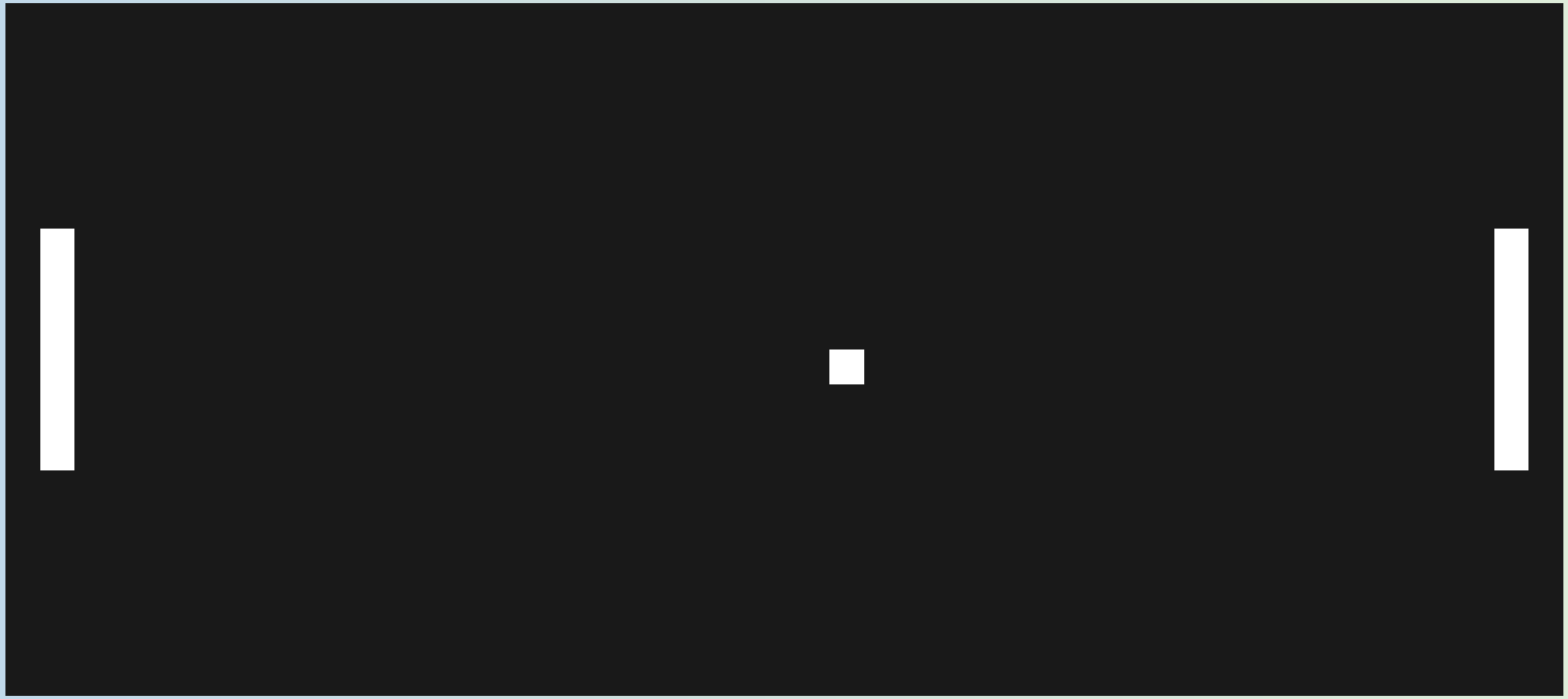
"PONG Game on FPGA"

Made by:

Rutuja Gogulwar (17010BTEC01840)

Hanshraj Rajput (17010BTEC01813)

PONG



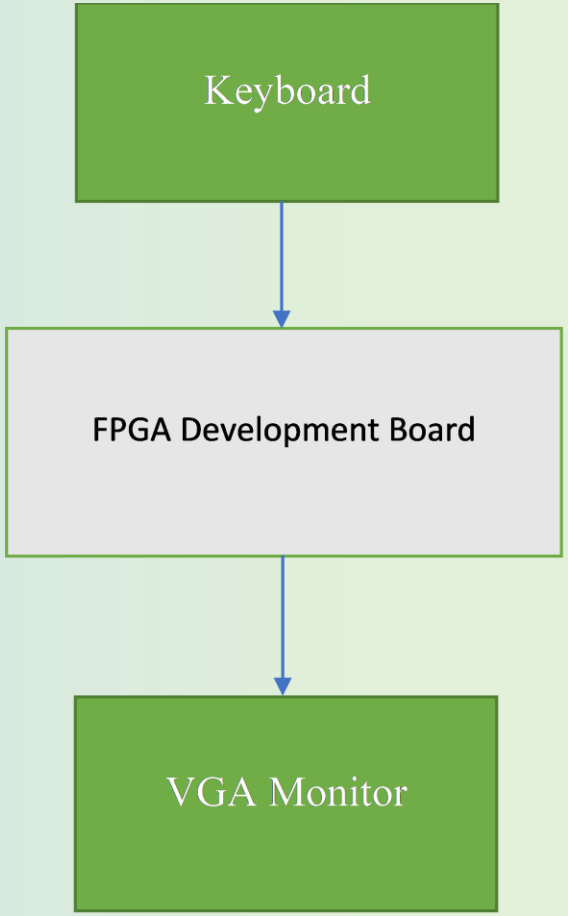
Introduction

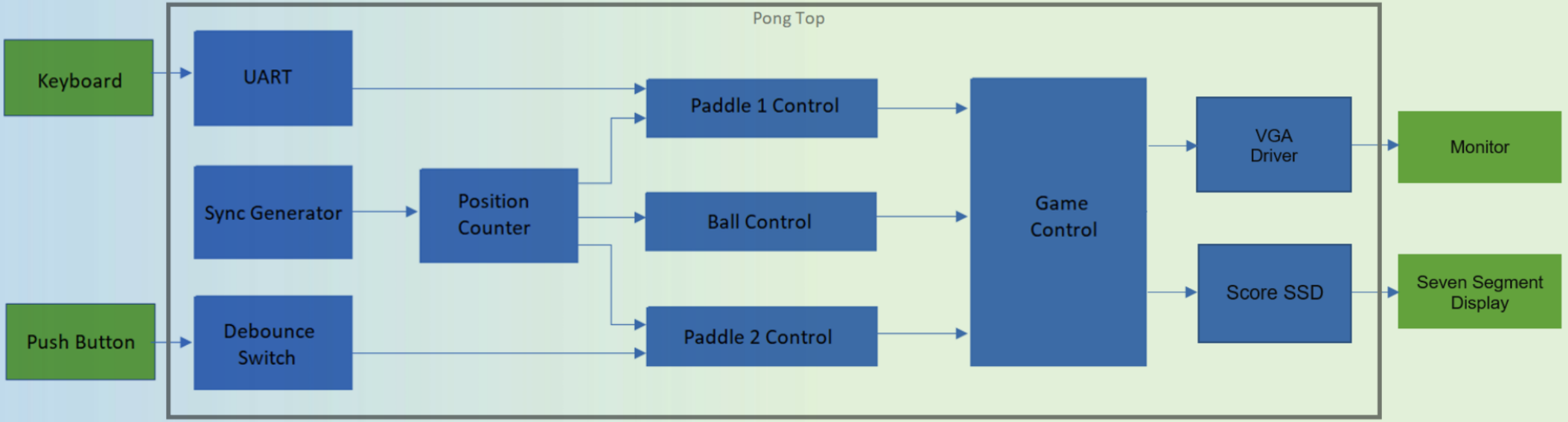
- The creation of games was always in the mind of the engineers
- In 1972, the first commercially successful arcade video game, "*Pong*" was released
- Pong is a two-dimensional which stimulates table tennis
- This project is the recreation of the same game on VGA monitor, using a FPGA development kit
- Pong and other early games were implemented largely with discrete TTL chips
- With advancement in technology, to conserve space power and increase reliability of design, it was designed on a single chip

Problem Definition

- A discrete circuit is constructed of components which are manufactured separately which are later connected together by using conducted wires on a PCB.
- Assembling and wiring of all individual discrete components take more time and occupies a larger space required
- All the elements are connected using soldering process so, that may have caused less reliability

Block Diagram





Detailed Block Diagram

Details of hardware

Sr. No.	Component	Specification
1.	FPGA Development Board	Altera DE0
2.	Monitor	LCD/CRT with VGA input
3.	Keyboard	USB port

Details of software used

- Altera Quartus II is used to program FPGA
- It is programmable logic device design software produced by Intel
- It is a multiplatform design environment that easily adapts to your specific needs in all phases of FPGA and CPLD design
- Quartus II enables analysis and synthesis of HDL designs, which enables the developer to compile their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer

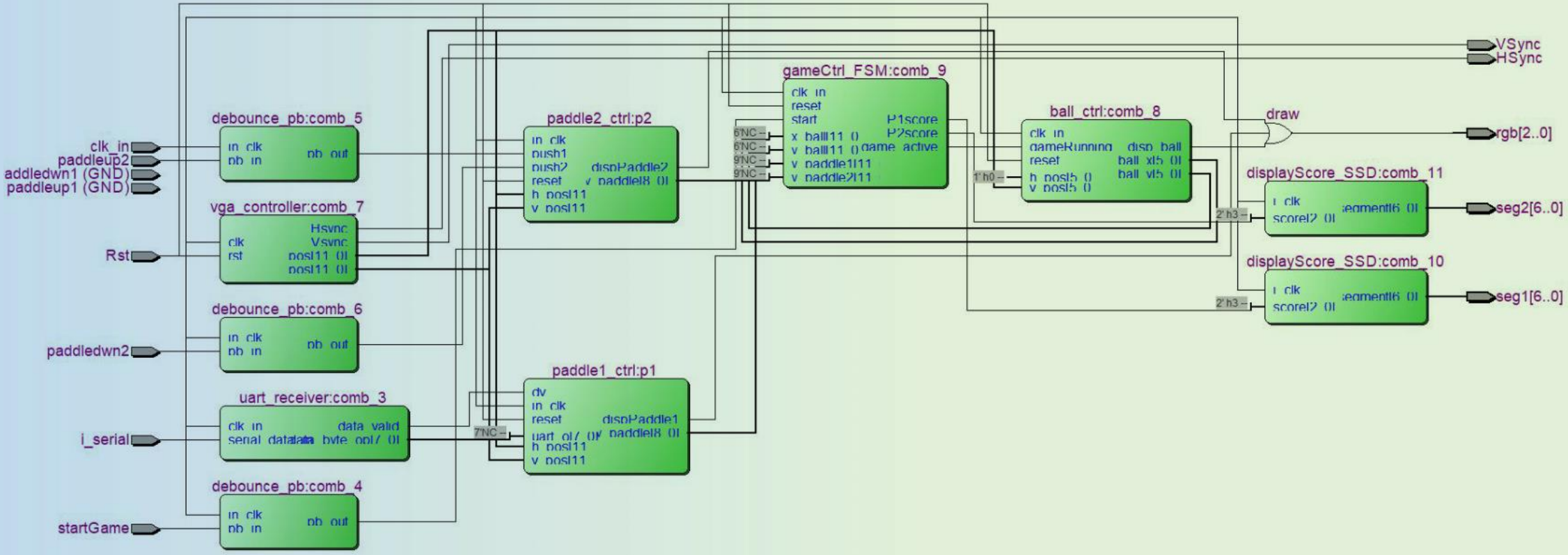
Working

- A dedicated circuit for the gameplay is designed inside the FPGA
- The system is divided in several modules, which are interconnected in top entity
- UART receiver, Debounce button, VGA controller, Paddle control, Ball control, Display score SSD, Game FSM. These are instantiated in top level module
- Push buttons mounted on the development board are used as input to control the player 1 paddle
- A UBS keyboard is connected to USB port of development board which would control the player 2 paddle
- A LCD monitor with VGA input will be used to display the graphics of the game

- **UART:** UART is a serial communication protocol with help of which, two devices can communicate without clock signal. UART receiver module receives data from the keyboard, converts input 8-bit serial data into 8 byte data and stores it.
- **Debounce Switch:** When a mechanical switch is toggled they create physical contact to terminal. The mechanical switch tend to bounce. To filter the glitchy button input debounce switch module is designed, which gives filtered output.
- **Paddle 1 control:** This module controls the position of paddle of player 1 based on the key pressed on the keyboard. It receives input from UART receiver and decides the position of paddle.
- **Paddle 2 control:** This module works similar to paddle 1 control except of the input. It receives input from the debounce switch and based on which switch is pressed, it will move paddle upwards or downwards.

- **Ball Control:** This module keeps track of the ball location in play area. The row/col that is being drawn on the VGA display is sent as an input to this module. If the current active pixel is the same pixel as where the ball is located, the output becomes a 1. Otherwise it's a 0.
- **Game Control:** This module is created by designing finite state machine which would control the gameplay. It will keep track of who scores the point and when the game will end.
- **Score SSD:** This module is responsible for displaying the scores of both the players on the seven segment display present on the FPGA board. It receives score of player as input from the game control module and displays it on SSD.
- **VGA Controller:** This module keeps track of position of pixel in 2d array and generates sync pulses
- **Pong Top:** All the submodules designed are instantiate in top entity to establish proper connection between them.

Circuit Diagram (RTL)



RTL diagram of top entity

Conclusion

- Our aim was to reconstruct one of the most popular games of computer game history
- It was a good decision to design it on FPGA because we had a suitable development the board which has a VGA port for interfacing a computer monitor, seven segment displays to display scores and push buttons for controls, and USB blaster for USB communication
- The advantage of designing this on FPGA was that the entire design was embedded inside the FPGA chip, because of which we did not have other dependencies

Future scope of work

- Score can be displayed on screen itself
- Speed ball can be changed dynamically with game running.
- Size of paddle can be set according to player’s choice
- Colors of paddle and ball can be changed dynamically
- After end of game, interesting graphics can be displayed
- Various game modes can be added like single-player mode, two-player mode, three-player mode and four-player mode

Thank You