Akhilesh Yadav
850 Sector 17 A Gurgaon – 122001
Email: akhil4yadav@gmail.com
Mobile: 09560587284

OBJECTIVE

To work in a growth oriented professional organization, where I can enhance my professional skills and hence be a valuable asset to the organization. It would be very satisfying to work in fields of Wireless telecommunication and Linux programming environment.

PROFESSIONAL PROFILE

- Result-oriented software developer with **6 years** of rich experience in wireless domain of Telecommunication Industry.
- Extensive experience of **Embedded C** with **Linux programming** environment.
- Experience in software development with various **RTOS** (ThreadX, TI BIOS).
- Strong development expertise in GSM **Layer 1** (Um interface) **scheduler** on DSP platform.
- Strong expertise in development and optimization of GSM Layer 2 **LAPDm**.
- Hands-on experience in development, optimization of GSM Layer3 (RR') protocols.
- Good understanding of GSM system clock and had developed **Clock Synchronization** algorithm in accordance with GSM G-823 specifications.
- Strong debugging ability of hardware and software related issues that occur in a **DSP** (BF54xx ADI DSP and TMS320C64x+ TI DSP) *based boards* and projects.
- Ability to acquire technical knowledge and skills rapidly.

TECHNICAL SKILLS

Protocols	GSM Layer-1 (Um Interface), LAPDm, RR' (Um), SCTP, RTP, FTP.
Hardware	TMS320C64x+ TI DSP, ADI DSP BF 547,AMR-9 based IMX27
Tools / IDEs	Lauterbach Debugger (ARM-9) ,GDB , Emacs , Wireshark , E1 Analyzer , ADI DSP BF54xx debugger
Languages	C , Unix Network and Socket Programming , UNIX shell scripting , Python3
Operating System	ThreadX (RTOS) ,TI BIOS 5.43, Ubuntu Kernel 3.2
Version control	SVN , CVS and GIT
Standards and Protocols	3GPP , ITU , LTE , SIP

PROFESSIONAL QUALIFICATION

- B.Tech in Electronics & Telecommunication during 2003-2007 with about 69% from **Uttar Pradesh Technical University, JSS-Academy of Technical Education, Noida**

PROFESSIONAL EXPERIENCE

Organization	Vihaan Networks Ltd.
Duration	July 2007 – Till Date
Profile	Technical Lead in Team BTS Layer 1 controller.

PROJECTS DETAILS

- **Project: Development and integration of Multi Carrier MACRO BTS**
  - Objective was to develop MC (Multi carrier) BTS supporting 6 carriers (6 TRXs) on multi core TI DSP 6487 with DSP BIOS-5.43 platform, Implementation and porting of L1 code and develop profiling frame work for debugging performance issues .

Role: Design Engineer, Developer .
Responsibilities:

- Feasibility analysis of MC BTS with **TI (6487 DSP)** 3 core processor architecture.
- Design and develop **EXTENDED CELL** feature .
- Design and develop **REPEATED FACCH** in down link of physical layer on BTS.
- Debug and optimize **AMR** (UL/DL) **DTX** state machine.
- Debug and enhance of **IPC** frame work on (Multi Core DSP) MC BTS.
- Develop **BIOS TASK PROFILING** frame work on TI processor to debug/enhance Layer1 controller scheduling of Um interface.
- Debugging and enhancement of Macro BTS.

Team Size : 4
Duration : August 2011 – August 2013
Platfrom : C on TI (6487 DSP) BIOS , TEMS , CMU-300.

- **Project: Designing, development of CSD (Circuit Switched Data) in PICO BTS**.
  - Objective was to design and develop CSD full rate and half rate in PICO BSTS, this feature is required to make data call (FAX) in GSM system with up to 9.6 Kbps data rate.

Role: Design Engineer, Developer .
Responsibilities:

- Study of 3GPP specification **45.002, 45.003** related to CSD development.
- Prepare requirement and High Level Design document for CSD FR/HR.
- Prepare Low Level Design and interface change document with BB (base band) and Media-gateway.
- Design and Implement CSD FR/HR feature and Integrate with baseband.
- Unit test on host and to test air interface scheduling with CMU-300.

Team Size : 3
Duration : April 2011 – August 2011
Platfrom : C on TI (6482 DSP) BIOS , CMU-300 , TEMS .

- **Project: Design, development of REPEATED SACCH feature in UL/DL.**
  - Objective was to develop this feature in order to repeat SACCH (UL/DL for SAPI 0 only) transmissions to increase the likelihood of a successful decode.

Role: Design Engineer, Developer .
Responsibilities:
- Study of 3GPP specification for LAPDm **44.006 and 45.002.**
- Prepare requirement and HLD document for REPEATED SACCH.
- Prepare LLD and interface change document with BB and LAPDm.
- Design and Implement changes in Layer 2 LAPDm.
- Design and Implement changes in Layer 1 (PHY CONTROLLER).
- Enhance and debug fixing of module after integration.
- Prepare unit test cases for testing of repeated SACCH mainly Um interface with TEMS.

Team Size : 4
Duration : January 2011 – April 2011
Platfrom : C on TI (6482 DSP)BIOS , CMU-300 , TEMS .

- **Project: Design and development of MULTIPLE PAGING CAPACITY feature in BTS**.
  - Objective was to design and develop Multiple Paging Capacity by implementing Paging Request 2 and Paging Request 3 in DL-CCCH module on BTS. This feature is required to solve sudden paging load in BTS during peak hour.

Role: Design Engineer, Developer .
Responsibilities:
- Study of 3GPP specification **44.018, 24.008.**
- Prepare HLD and requirement document for MULTIPLE PAGING CAPACITY.
- Prepare LLD and interface change document in BTS RR' Layer 3.
- Design and implement multiple paging capacities in DL-CCCH module.
- Development of test frame work, paging load generator stub.
- Integration testing of Multiple Paging Capacity with VNL BSC.

Team Size : 2
Duration : October 2010 – December 2011
Platfrom : C on (TI 6482 DSP) BIOS , CMU-300 , TEMS .

- **Project: Design and develop inter processor communication frame work between ADI-DSP Blackfin BF547.**
  - Objective was to design blackfin – blackfin (ADI DSP) inter processor communication framework .Which will be used further for frame number synchronization between DSPs and asynchronous data transfer between DSPs .

Role: Design Engineer, Developer .

Responsibilities:

- Prepare HLD and requirement document for BF-BF communication frame work.
- Prepare LLD and interface change document in BF-BF communication frame work.
- Study of HOST-DMA PORT interface configuration of BF-547 DSP .
- Develop and design frame software module for BF-BF communication frame work using ADI - DSP SPORT configuration .
- Unit testing of module with all possible scenarios .

Team Size : 2
Duration : June 2010 – September 2010
Platfrom : C on (ThreadX) ADI BF547 , MSO.

- **Project: Designing and development of VNL NIB (Network In Box) .**
  - Objective was to prototyping of complete GSM Network including SIP in one Box called NIB. Prototyping and feasibility analysis with GNU OpenBSC and PJ-SIP with VNL PICO BTS and develop an integrated system.

Role: Design Engineer, Developer .
Responsibilities:

- Study of **RFC 3261** and prepare requirement for integration of GSM network simulator (OpenBSC) with VNL – PICO BTS on TARGET ARM IMX-27.
- Prepare shared library of all required packages for OpenSource on ARM-9 .
- Develop and modify GSM messages to make call between GSM and SIP (VOIP), develop a protocol conversion layer to convert GSM message into SIP.
- Study and modification in OpenSource SIP and integration with PICO BTS.
- Develop server client base configuration frame work for NIB.
- Unit test cases for NIB and integration with Asterisk.

Team Size : 6
Duration : March 2010 – June 2010
Platfrom : C on Linux 3.2 ,ARM IMX 27, Ubuntu 10.04 , TEMS , Asterisk .

- **Project: Designing, development IP based R-BTS (Replace LAPD with SCTP).**
  - Objective was to convert VNL R2 TDM (E1 2Mbps) BTS into IP based BTS and in order to make IP BTS , replace GSM Layer-2 LAPD with SCTP.

Role: Design Engineer, Developer .
Responsibilities:

- Study and to prepare requirements of A-bis interface of VNL R-BTS and BSC.
- Study of **SIGTRAN SCTP** source code and **RFC-4096**.
- Replace LAPD on R2 TDM BTS with SCTP using CSPL framework.
- Modify and develop **THREADX** ip-stack **NetX** for SCTP and RTP implementation.
- Enhance SCTP SYS-CTL parameters and optimize for SATELLITE Abis interface.
- Debug and enhance SIGTRAN stack for VNL RBTS/VBTS.
- Integration testing of (SCTP) IP BTS with VNL BSC.

Team Size : 2
Duration : December 2009 – February 2010
Platfrom : C on ThreadX-RTOS , Wireshark .

- **Project: Design and develop GSM Network Simulator to test A-bis , Um Interface of PCIO BTS .**
  - Objective was to develop GSM Network Simulator based on GNU OpenSource as a test tool that can be used to test basic GSM functionalities of BTS.

Role: Design Engineer, Developer .
Responsibilities:

- Preparation of requirements and HLD document of GSM BTS protocol tester.
- Preparation of LLD document of GSM BTS protocol tester.
- Study of open source **GNU OpenBSC** to develop GSM BTS protocol tester.
- Study of 3GPP specs **48.058, 44.018** GSM TS 08.58 (RSL), GSM TS 08.59 (OML), **04.11**.
- Implemented **EARLY ASSIGNMENT** (implemented SDCCH resource handling) in OpenBSC as per 3GPP **24.08** and shared with OpenBSC Source.
- Implemented TCH/H resource allocation frame work in OpenBSC.
- Implemented/added Multiple CCCH,SCTP as Layer 2 A-bis interface, RTP frame work (Not Media gateway), and multiple voice codec AMR/FR/EFR support to GSM BTS protocol tester.
- Implemented **Python3 based user interface** to configure GSM Simulator.

Team Size : 2
Duration : June 2009 – December 2009
Platfrom : C on Linux 2.6 , Wireshark , TEMS , Python3 , Ubuntu .

- **Project: Development of CLOCK SYCHRONIZATION algorithm .**
  - Objective was to develop clock synchronization algorithm on BTS to meet GSM G-823 requirement for TDM BTS.

Role: Design Engineer, Developer .
Responsibilities:

- Prepare requirement document for clock synchronization on Maxim TDMoIP chip.
- Develop a software module that provides reference clock frequency of absolute accuracy better than 0.05 ppm (50 ppb), and meet the requirements of jitter and wander specification **G-823.**
- Study of tracking mode and configuration of Maxim **TDMoIP DS34S108**.
- Study and preparation of requirements for calibration of **OCXO** using DAC, and to study the behavior of OCXO, VCXO in different physical parameter.
- Prepared clock wander test setup using stable clock source RUBIDIUM (1 ppb stability) and ANT20.
- Unit test and integration of developed module with various other available platforms (BLACKFIN BF-547).

Team Size : 2
Duration : September 2008 – May 2009
Platfrom : C on ThreadX-RTOS ,ARM IMX27 , ANT-20 , Rubidium clock source .

- **Project: Maintenance and feature development of BIC (BTS interface card) .**
  - Objective was to provide backhaul connectivity to VNL Rural BTS and Village BTS to control BTS power supply and to provide synchronized clock to BTS.

Role: Design Engineer, Developer .
Responsibilities:
- Understand the architecture of VNL **BTS interface card**.
- Study of changes required and control registers of power supply card .
- Develop software module to handle alarms and control BTS power from OMC.
- Develop a basic clock synchronization algorithm that will synchronize (adjust DAC voltage) BIC clock with core network clock.
- Test and collect experimental data for VCXO and core network clock drift.

Team Size : 2
Duration : February 2008 – August 2008
Platfrom : C on ThreadX-RTOS , E1 analyzer ,NET HAWK.

- **Project: Development and integration of INFRAME TRX with VNL WorldGSM System.**
  - Objective was to learn and understand VNL WorldGSM system , integrate and test In frame S-TRX with VNL BSC.

Role: Design Engineer, Developer .
Responsibilities:
- Understand the architecture of VNL 12 TRX PABX WorldGSM product.
- Study on the various 3GPP core specifications mainly **48.058** , so as to thoroughly understand the criticality involved in the 2G BTS
- Isolating the problems faced via different configurations and analysys of problems with MSO and E1 PUMA analyzer.

Team Size : 5
Duration : July 2007 – January 2008
Platfrom : C on ThreadX-RTOS , E1 analyzer , RHEL.

PERSONAL DETAILS

- Father's Name : Mr. Awodh Nath Yadav .
- Mother's Name : Mrs. Savitri Devi Yadav .
- Date of Birth : 26th Aug 1984
- Marital Status : Married
- Nationality : Indian

I declare hereby, that all the information furnished above is true to the best of my knowledge and belief.

Place: Gurgaon **Akhilesh Yadav**