Curriculum Vitae

VINAY PANDEY

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Career Objective

To apply my acquired skills in a professional environment and to broaden my horizons, gain necessary exposure, for growth, both personally and professionally, with the organization.

Educational Qualification

S No.	Examination	Board/University	Year of Passing	Percentage
1	B. Tech(ECE)	GGSIPU	2010	70.21%
2	Senior Secondary	CBSE	2005	79.40%
3	Secondary	CBSE	2003	83.80%

B.Tech in Electronics and Communication Engineering from Ambedkar Institute of Technology affiliated to Guru Gobind Singh Indraprastha University.

Relevant Skills

Platforms: UNIX/LINUX, MS Windows
Programming: C/C++, Java, JEE, Struts, Hibernate, Spring MVC, JSP, Servlets, JSTL, JMS, JDBC, Jconsole, Jmap, Web Servers (Websphere, JBOSS), web containers(tomcat), EJBs, Shell Scripting, PL/SQL
Tools: OTM (Oracle Transportation Management), Eclipse (Indigo), SQL Developer
Other Technologies: DBMS, HTML, MS-Office

Professional Experience

Systems Engineer with Infosys Technologies Limited(Feb2011 - Present): Working on split of Kraft Foods into two new global companies, involves designing web interfaces to interact with OTM application to enable business process, creating scripts, database configurations using Java, Struts, Shell scripting and SQL.
Written logic that creates reports in pdf and xls formats from data read from database and sends the reports via email to concerned receivers. Written logic to format input files using File IO classes based on different business rules. Configured message queues to send and receive messages. Deployed web applications on web servers. Experience in testing and debugging of java code.

Projects and Training

1. **TCAD Project (6 months)** – Designed and simulated a SOI-MOSFET to investigate into the effect of variations in device dimensions on MOSFET characteristics. **Synopsys TCAD** tool set was used for this purpose. The exact procedure was as follows. A NMOS was designed using the **SDE** tool. After that the design was simulated with various transport models like drift-diffuison, hydrodynamic, thermodynamic models using **SDevice** tool to obtain various parameters like conduction current, diffusion current, electron density etc. Advanced transport models like **SPARTA** and **SMOCA** were also carried out on the design. The curves for various parameters were observed using the **Tecplot**

and **Inspect tools.** The findings were presented at the ICNB 2010 (International Conference on Nanotechnology and Biosensors).

2. Summer Training (June –July 2009, 6 weeks) D'gipro – Performed various steps present in an ASIC design flow like HDL description, placement and routing, etc using **Synopsys** tools. For this purpose, a memory module which is provided with the tool set was used. The design was verified using the VCS tool. For this a testbench was developed in Verilog HDL. After that optimization of the design, for size and operation speed, was done using DC (design compiler) tool. To set various design constraint, files were used which were written in TCL language. Then place and route was performed using the ICC compiler. Here the main aim was to put the various circuit elements on the silicon area for minimum timing delays and maximum speed of operation.

3. Automated Railway Crossing (Minor Project) – Developed an automated railway crossing prototype as the minor project. The design was based on **AT89C51** microcontroller. It employed **IR sensor** modules, **LM324** comparator ICs and **Geared DC Motors.** The coding for the design was done in C language using the **KEIL** software. The aim was to design such a railway crossing where no manual operation was required.

4. Project on RLE Design (6 weeks, Synopsys) – Designed the RLE (run length encoder) in **Verilog** HDL. The design contained components like FIFO, FSM, DMA, etc. Each component was verified for functionality with testbenches written in Verilog. After that all the modules were combined to form the RLE top level module. The top level design was verified using **System Verilog** on **VCS** tool of **Synopsys**. System Verilog features like interfaces, program block, classes, transactions, assertions, etc were used for writing the testbench for the top module.

Extra Curricular Activities & Achievements

1. Secured AIR **394** in the 5th **National Science Olympiad** organized by WIPRO.
2. Secured **1st** position in **football** in **KHEL'08** (AIT).
3. Secured **2nd** position in **cricket** in **KHEL'08** (AIT).
4. **Coordinated** the **Volley Ball** event in **KHEL'08** (AIT).
5. Attended **ROBOTACTICS Workshop** on 8051 microcontroller and Line Following Robot (IGIT).
6. **Event Head** for the event **Circuit Designing** in **DIGITALIS'09** (AIT).
7. Secured **3rd** position in Black box (**Circuit designing**) event in **INNOVISION'10** (NSIT).
8. Secured **3rd** position in **Linux Challenge** event in **INNOVISION'10** (NSIT).
9. Attended **TCAD Workshop** on VLSI design organized by Synopsys and IIT Bombay (AIT).
10. Secured **2nd** position in the 7th semester.
11. Secured **2nd** position in Mega Challenge (**Electronics Quiz**) event in **Proscenium'10** (AIT).
12. **Coordinated** the **Linux Challenge** event in **Proscenium'10** (AIT).