PANKAJ KUMAR

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PROFESSIONAL EXPERIENCE

- *Technical Leader (DSP-Firmware), Azcom India (May 2011-present)*
- *Technical Leader (DSP-Firmware, Aricent Technologies (Apr 2010 – Apr 2011)*
- *Senior Lead Firmware Engineer, DSP Firmware Group, Conexant Systems/Ikanos Communications (May 2006 – Mar 2010)*
- *Scientist, Advanced Communications Group, DRDO (Jan 1998 – April 2006)*

EDUCATIONAL QUALIFICATION

M.Tech. (Information Systems) CPI : 9.25out of 10
IIT, Kanpur 2002

B.E. (Electronics) 78.67% (Passed with distinction)
S.S.G.M. College of Engineering, Shegaon 1995

- Passed with Distinction
- First Rank

DOMAIN KNOWLEDGE

- Project management, Building and managing a team, Planning and Tracking, customer interaction and delivery management, Technical mentorship
- Wireless Communications: LTE R8 (FDD and TDD) (uplink and downlink), GSM, IS-95 and Satellite Communication
- Channel Coding: Convolution Encoding and Viterbi Decoding, Block Codes and Maximum Likelihood Decoding, Turbo Codes, Hybrid FEC-ARQ mechanisms.
- Modulation/Demodulation: BPSK/QPSK, PSK, QAM, Trellis Coded Modulation
- Spread Spectrum Systems: FHSS, DSSS
- Design and Realization of Embedded systems Hardware and Software.
- Broadband Communication: ADSL, ADSL2 and ADSL2+ with Annex A, B and M
- Validation and verification

TECHNICAL EXPERTISE

- Multiple Processors: TI's multi core DSP processor (6614 Appleton and 6618 Turbo Nyquist), Conexant Multi core proprietary DSP processor, ADI 21xx DSP processors and Intel's 87196KC Microcontroller.
- Defining system architecture, development of device drivers and firmware Modules using processor native language.
- Software Development Life-Cycle: Functional Specifications, High-Level-Low-Level Design, Coding and Unit Testing, Module Testing, Pre-integration and Integration Testing.
- Code composer studio, MATLAB, System View, LabView etc
- Integration and Testing/Debugging expertise on Target Platforms.
- Subversion, WinCVS, RSCCS Rational Clear-DDTS & DOXBOX Change Management Systems
- Lab instruments like Oscilloscopes, Logic Analyzer, Function Generator, Spectrum Analyzer Audio Analyzers, UE Emulators, JTAGs etc.

AWARDS AND ACCOMPLISHMENTS

- University Rank holder
- Merit Scholarships in Engineering for all four years.
- "**Laboratory Scientist of the Year** " award DRDO

PROJECT WORK

Physical layer for FAPI compliant Release 8 FDD/TDD-LTE enodeB on Texas Instruments DSP processor

Role Technical Architect
Team Strength Eleven

Overview

Leading engineering team for design and implementation of FAPI complaint LTE physical layer on Texas Instruments Appleton (TMS320TCI6614, running @ 1.2GHz) multi-core DSP processor using TI SYS/BIOS RTOS.Hardware platforms used for this development are 6614 EVM and small cell base station development platform (ngSCBP, developed at Azcom). Following are my major contributions

- Building and mentoring physical layer team, First person to join physical layer team @ Azcom, India. Single handedly formed a strongly contributing team of 11 members.
- Fully responsible for technical mentorship, planning and work assignment, tracking and delivery management, customer interaction, Integration, bugs resolution of PHY layer.
- Defined software architecture to make extensive use of hardware accelerators and on chip peripherals. This includes defining bit level and symbol level architectures and dividing functionality in multiple tasks, HWIs and SWIs. The clock cycles consumed in full downlink implementation are around 30% of total cycles available @1.2 GHz.
- Playing instrumental role in MAC-PHY integration and decisive role in locating the timing instants for L1-MAC message communication for FAPI compliance.
- Incorporated multilevel test strategy of Unit Testing, Module Testing, Integration testing and UE integration testing to allow bit exactness with MATLAB model and compatibility with test UEs and commercial dongles. Test pattern and expected output are generated using MATLAB and kept in external memory.
- For L1 development and testing, MAC Simulator is developed on test core to trigger PHY elaborations for LTE channels. Real time verification of LMP, FFTc and received TB and CB CRC is possible using this. All LTE channels implementation have been tested and verified using commercial UE emulators.
- Key role in deciding different code and data segment placement in hierarchical memory segments to optimize performance, cache coherency and acquire balance in memory usage and clock cycle consumption.
- Used BCP (Bit rate coprocessor) accelerator to implement the signal processing functionalities of channel encoding, rate matching, scrambling and modulation for PDSCH, PBCH and PDCCH channels. Used Ping pong buffers to keep TTI level modulated data for PDSCH and PDCCH channels.
- Used LTE library functions to implement the functionalities of Layer Map and pre-coding. Modified the library functions to adjust for power requirements of PDSCH as per FAPI procedures.
- For system insight and debug, implemented software profiling on Target Platforms using self developed code and using Unified Instrumentation Architecture tool of CCS. This enables the insight of start and duration of different tasks and interrupts.
- The software supports SISO, Tx/Rx-diversity and spatial multiplexing for 2x2 Antenna and is 3GPP R8 compliant.
- Contributed in generating related documentation of software architecture specification and test strategies.

Successful demonstration at MWC

- **Live Video Transfer to multiple commercial dongles**
- **DL data rate demonstration @150Mbps (OLSM 2x2)**

Design and development of channel decoding schemes for GSM and GPRS channels

Role Team Leader
Team Strength Three

Overview

Led engineering team to design and implement Viterbi decoding schemes for GSM and GPRS channels using VCP2 peripheral of TI Nyquist (6616) processor. This development is based on Chip support library functions of Nyquist and uses API functions to incorporate the decoding functionality. Following are my major contributions

- Implementation of test harness to independently verify the decoding functionality of TCH, CCH and PDTCH channels.
- Development of VCP2 driver to seamlessly interface with DSP cores, one VCP instance is dedicated for use by each C66x core
- Development of EDMA3 driver to pass branch metrics and decision data between VCP2 and DSP

Design and development of Universal Handshake on CPE-ADSL

Role Team Leader
Team Strength Five

Overview

Led engineering team to design and implement Universal Handshake to carry out initializations procedures for Annex A, B, and M modes for G.DMT, BIS and BIS-plus versions and their flavors of ADSL communication in a single session. This development is based on proprietary scheduler developed for Conexant DSP. Following are my major contributions

- Finite State Machine based design and implementation of Transmit- Receive states for handshake Message exchange
- Message Parser design and implementation of delimiting based parsing, Parameter extraction and their storage
- Message Composer design and implementation for dynamic message composing
- Reviewed engineering design releases and programs to make sure that design objectives are maintained.
- Successful IOL testing with all DSLAMS and provision for fallback for Legacy DSLAMS

Extended CPE-ADSL based handshake for modems supporting combined capabilities of A-VDSL.

Design and development of Universal Handshake on CO-ADSL Platforms

Role Team Leader
Team Strength Three

Overview

Besides differences in architectures and messages for CO and CPE platforms, there were challenges like CO being the leader of communication, ultimately governs the capability and parameters to be used over the link in Showtime. Following are my main contributions towards this activity

- Scheduler based design of Tx-Rx state machine for startup, handshake messaging and clear-down procedures
- Support for Legacy connection in T1.413 mode
- Successful Inter-compatibility tests with ADSL CPE
- Scheduling and planning engineering activities to meet program objectives
- Release Management and defect support

Customer Support, Defect Resolution, Release Management, Verification and Validation

Role Team Leader
Team Strength Five

Overview

These are ongoing activities to continuously support and improve the product. I contributed towards the following

- Lead support engineer for all external firmware defects
- Implemented Ethernet on first Mile (EFM) on CPE Platform
- Planning firmware release generation. Originating engineering changes and releases.
- Restructured/optimized code of two DSP engines (IPU and FDP) for automatic memory assignments and improved code/listing file generation
- Incorporated Trace dictionary and Trace Translation for on-field collection of vital debug information.
- Cabinet mode improvements, with priority to connect in Bisplus modes
- Incorporated G.Lite mode to connect in non splitter environment
- Verification and validation manager- Responsible for verification as per specifications, test cases execution and report generation, Enhancing testing scope by test cases addition and test instruments calibrations.
- DPM improvements: Enhanced test vectors to detect the faulty units during mass testing

Design and development of DSP module for Frequency Hopping Radio

Role Team Member
Team Strength Five

Overview

The module implements the functions of frequency hopping, modulation, demodulation, forward error correction, audio digitization and compression. It is designed around two high performance, 16-bit fixed point DSP (ADSP-2183) processors from Analog devices. Major peripherals used in the module are AMBE-2020 Vocoder, Xilinx FPGA, CVSD, DDFS, RTC, ADC and DAC.

- Hardware Design, testing and integration
- Software design and coding in ADSP-21xx assembly
- Design, development and testing of Device Drivers for CVSD, Vocoder, Codec, RTC, ADC and DAC
- Design and development of In system programming and IDMA Booting
- Asynchronous and Synchronous data communication

Design and development of Controller Module for Frequency Hopping Radio

Role Team Member
Team Strength Two

Overview

Controller module implements the Man-machine interface and acts as master controller of the radio. It is designed around Intel's 16-bit 87C196KC microcontroller. The other major peripherals used are Flash Memory, NVRAM, KBD controller, BCD switches and LCD display

- Hardware Design, testing and integration
- Software design and coding in Intel's 96 microcontroller assembly
- Designed and implemented Hybrid FEC-ARQ scheme for automatic data rate adaptation
- Design, development and testing of Device Drivers for FLASH, serial NVRAM, LCD display and KBD controller
- Designed and implemented DMA based Inter-processor communication
- Designed and implemented efficient CRC-16 computation algorithm for received message integrity

Processor subsystem design for Man-Pack Radio

Role Team Leader

Team Strength Four

Overview

To reduce power consumption, size and weight of radio, Processor subsystem is designed to implement the functions of signal processing, user interface and audio processing in a single board. It is designed around two ADSP-2189 DSP processors, DDFS, Voice-band modem, Audio processor, GPS Receiver, CPLD and Flash Memory.

- Hardware design, Component selection and interfacing with peripherals
- Finalized integration details with other subsystems
- Designed Voice-Band modem technology for Remote operation
- Designed and developed driver for AD-9954 DDFS for direct modulation generation at RF frequencies

Multiple Descriptive Coding

Completed M.Tech thesis on **"Frame Expansions Based on M-channel filter banks for robustness to erasures"**. In this work we obtained conditions for recovery from bursty erasures and bounds on maximum size of re-constructible erasures bursts for M-channel filter banks with decimation factor of M/2. We studied the effects of erasures and quantization noise on reconstructed signal.