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| EE464 HARDWARE PROJECT |
| Final Report |
| Formlar ve Görseller | ODTÜ ELEKTRİK - ELEKTRONİK MÜHENDİSLİĞİ |

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# Intro

This project is based on the need for an isolated DC-DC converter that takes an input voltage from 24V to 48V and gives a constant output of 15V at 45W with closed-loop control. The chosen converter design’s both lines, and load regulations, as well as the output voltage ripple, needs to be 3%. This final report will focus on the topology, our design choices, and its implementation results due to these constraints.

Table 1 Project Constrains

|  |  |
| --- | --- |
| Input Voltage Range | 24-48V |
| Output Voltage | 15V |
| Output Power | 45W |
| Line Regulation Percentage | 3% |
| Load Regulation Percentage | 3% |
| Output P-P Voltage Ripple | 3% |

# Topology Selection

The forward converter is also simple, like flyback, but instead of storing the energy, the transformer delivers the power via it. The output current is relatively more stable than some other isolated topologies, but the output inductor and other semiconductor devices highly affect the power loss, heating, and cost in our design. Also, this topology is very sensitive to load changes and is commonly used in high current applications, so in order to protect our load regulation constraints, and since our project is not in the high output current range, we did not choose to use this topology.

Push-pull and half/full-bridge topologies were considered since the core utilization is better and copper losses are less in these topologies, but these topologies are more applicable to high output power applications. Also, a small-scale project like ours did not need more components, hard switch control, and high switch stresses, so this is not the best option for us.

In this project, fundamental flyback topology is chosen. Flyback converters are used mostly in low to medium power applications, so this was the main reason why we tend to choose this topology. Also, this topology is chosen due to its simplicity in construct and control, especially in discontinuous conduction mode. It has a smaller number of circuit elements (mainly passive elements); also, no energy storage inductor is needed because of the transformer, and only one diode is used in the topology, which causes less loss in the system. Also, there are more minor EMI problems with respect to other isolated topologies.

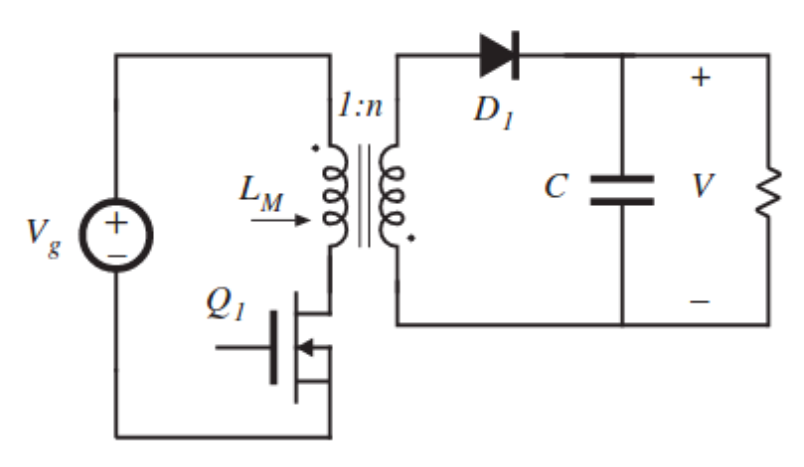


Figure 1 Flyback Converter Topology

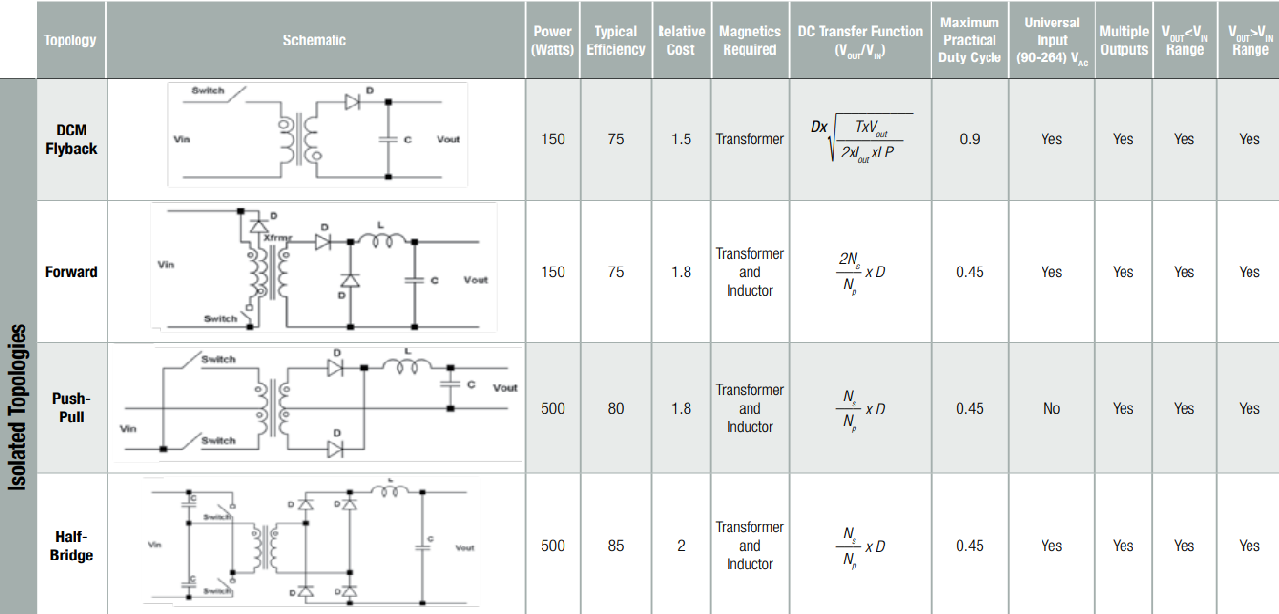


Figure 2 Isolated Converter Topologies Comparison (retrieved from Würth Elektronik)

# CONTROLLER DESIGN

There are different kinds of controllers we have found and implemented in LTspice. The first one is LT3751 which is a capacitor charger. The main advantage of the controller has UVLO/OVLO pins that are used for selecting the input voltage range. Another advantage of the controller is that two resistors which are RVout and RBG, are used to set up the output voltage.

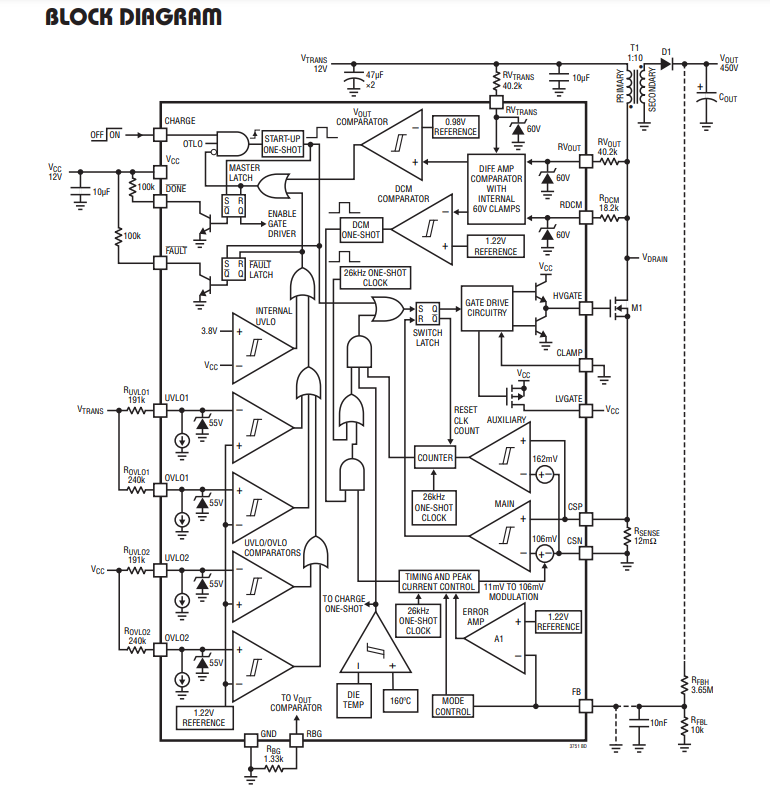


Figure 3 Block diagram of the LT3751

Also, this controller has the ability to operate in DCM operation, which increases the efficiency of the converter, which is really critical for the project. At that point, most of the requirements for the project are satisfied, whereas this controller is used for the capacitor charger, emphasized at the beginning. Because of that, when this controller was used with the load which is 5Ω in this project, the output voltage decreased to zero. In these controller applications, output voltage regulation resistors exist for high output values. On the other hand, we are trying to regulate the voltage at the 15V and 45W output. In this step, we could not reach the required voltage level because of the step size of the controller. The reason behind this is the controller, which is LT3751, is created for high voltage values. The digital voltage step size of the controller is higher than 15V.

After this controller, a lot of different kinds of controllers are implemented in LTspice and Simulink. Unfortunately, most of them could not reach the requirements that are specified in the project description. After the search step, we have found the LT3748, which is created by Linear technology. LT3748 is the isolated flyback converter controller. The advantages of this controller can be listed as:

-Wide input range and controllable lower threshold

-No transformer third winding or opto-isolator required for regulation

-Primary side winding feedback load regulation

-The LT3748 has different kinds of advantages besides those. The regulated output voltage can be decided as with the formula:

-Another advantage of the controller is indicating the inductance limitations, which are upper and lower bounds for the transformer design. This part will be explained in the transformer design step.

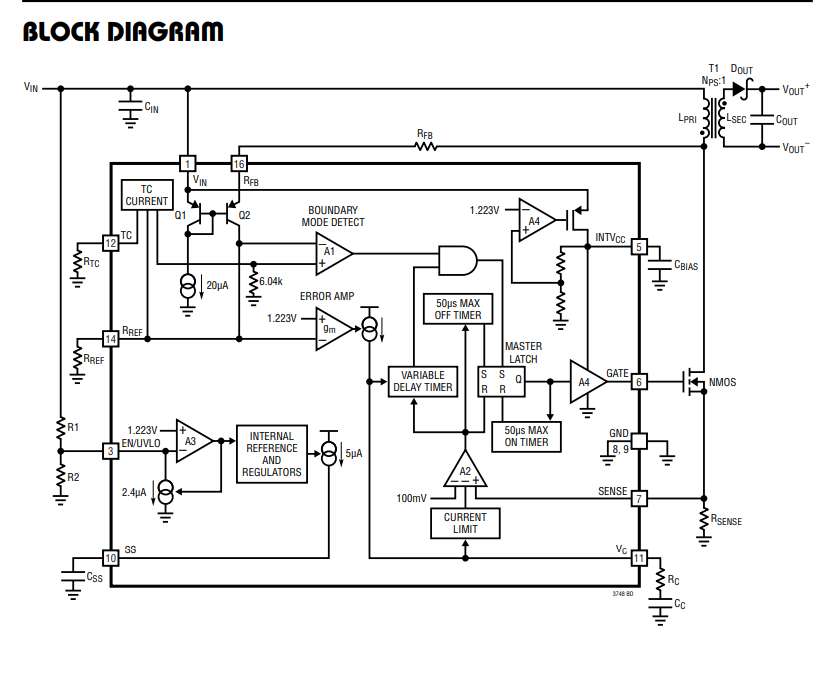


Figure 4 Block diagram of the LT3748

The manufacturer of this controller, which is Analog Devices, has created the LTspice models for this chip. Thanks to that, we have implemented the schematic of the flyback converter with LT3748.

Another chosen controller is LM51561 which is created by Texas Instruments. This controller is the second option for us. The advantages of this controller are wide and controllable input range, controllable output voltage, small size and low cost, and constant peak current limiting over input. The features of the LM51561 are similar to the LT3748. Both of them are ordered, and the applications will be started with the LT3748.

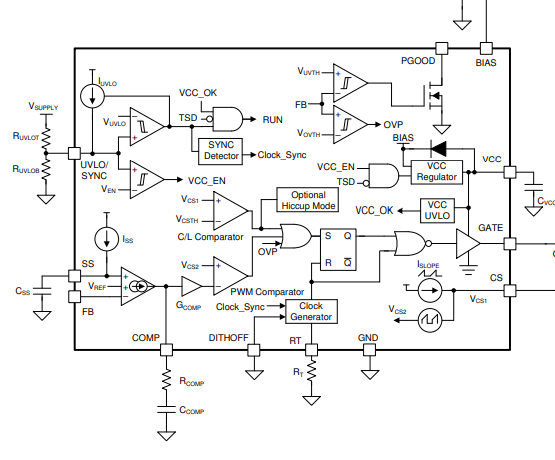


Figure 5 Block diagram of the LM56511

Our last option for the controller is using STM32 or Arduino to control the converter. At this point, the controller was designed to change the DON and Doff time.

# CONTROLLER CHOICE

For our last design, we have chosen LT3748. As we have explained in the controller selection part, there are too many advantages to choosing this controller. We have bought 3 of the controllers that are explained in the above part, which are LM51561, LT3748, and LT3751. On the other hand, LT3751, which is a high voltage capacitor charger, is not good enough to implement this project and, LM51561 was broken, and we could not try this controller. LT3748 was our last and most robust controller for this design. The advantages of this controller are listed as follows:

-Easy to implement

-Primary side winding feedback Load regulation

-Vout set by two external resistors

-INTVcc pin for the control of Gate Driver Voltage

-Capability to work with 5V to 100V input voltage Range

-1.9A Average Gate Drive Source and Sink Current

- No Transformer Third Winding or Opto-Isolator Required for Regulation

# SNUBBER DESIGN

The voltage increase at the drain side of the MOSFET when the switch is off, appearing because of the leakage inductance of the transformer. When the current at the input side is high enough, more stored energy needs to be dissipated. Because of that, leakage inductances of the transformer need to be minimized. Considering the inadequacy or failure of the snubber circuitry, the VDS voltage rating of the MOSFET can be chosen with the safety margin. There are different kinds of snubber circuit designs that exist. One of the popular ones is the RCD snubber circuit. Another one is the Zener snubber circuit. The advantage of the Zener suppressing circuit is dissipating the power when the voltage reaches the dangerous voltage level for the MOSFET.

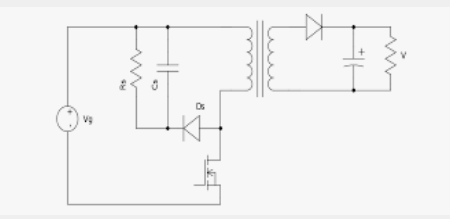


Figure 6 RCD Snubber circuitry

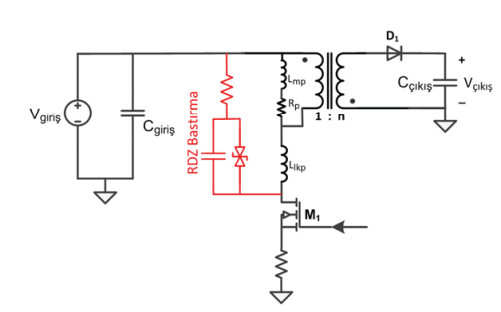


Figure 7 Snubber Circuit with Zener Diode

The advised approach for designing the snubber circuitry is measuring the period of the ringing when the switch is off without snubber circuitry. After that, the snubber capacitor needs to be added to the circuit starting from the feasible capacitance like 100pF. When the damping period reaches 1.5 -2 times longer, the capacitor is chosen. The change in period can determine the value of the parasitic capacitance, and the initial period of the damping can determine the leakage inductance. In addition to that, those values can be determined from the leakage inductance of the transformer and switch capacitance. When this inductance and capacitance value is determined, the resistance of the snubber needs to be decided.

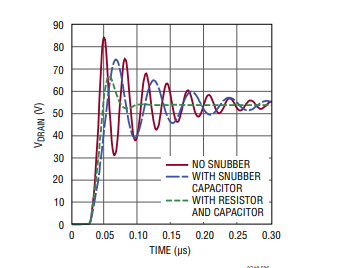


Figure 8 Effect of the Snubber taken from the Datasheet of the LT3748

Dissipated power will be equal to:

Another Snubber design for this design is implemented by those steps.

**Step 1)**

Measuring leakage inductance is calculated because of the eliminated parasitic element which is causing the ringing in the drain voltage of the MOSFET.

**Step 2)**

Snubber resistance and capacitance are calculated with those formulas:

As we have learned, the resistance on the snubber is handled with the overshoot of the drain voltage of the MOSFET, and the capacitor is working to eliminate the ringing on the drain voltage. Our ringing frequency was approximately equal to 1MHz, and leakage inductance on the transformer was equal to 2uH. According to this data, our resistance is equal to 40Ω, and the capacitance is equal to 11nF.

# TRANSFORMER DESIGN

For the transformer design, the start point was the controller’s limitations. According to the chosen IC LT3748, primary inductance has the following limitations:

The gain formula of the flyback converter is So, for the max Vin, D=0.27. For the min Vin, D=0.43. The operating frequency is chosen as 80 kHz. Hence, ton(min)=Dmin/f­sw=3.37 µs.

So .

LPRI is chosen as 55 µH inside these constraints. After this step, the core was chosen by the following step:

.

According to these, the most suitable core was KOOL MU 00K3515E090 since it has the lowest multiplication. Then, turn numbers found with the parameters of this core:

After finding the turns number, by using the RMS values of the primary and secondary side currents, cable selection was made:

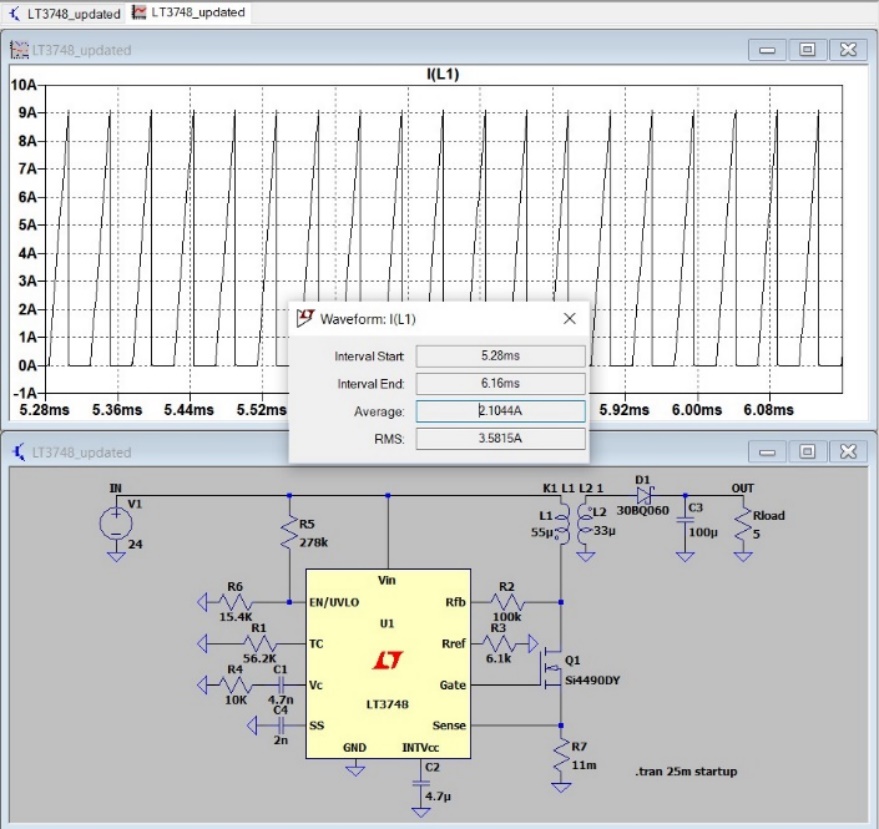


Figure 9 Primary side rms current

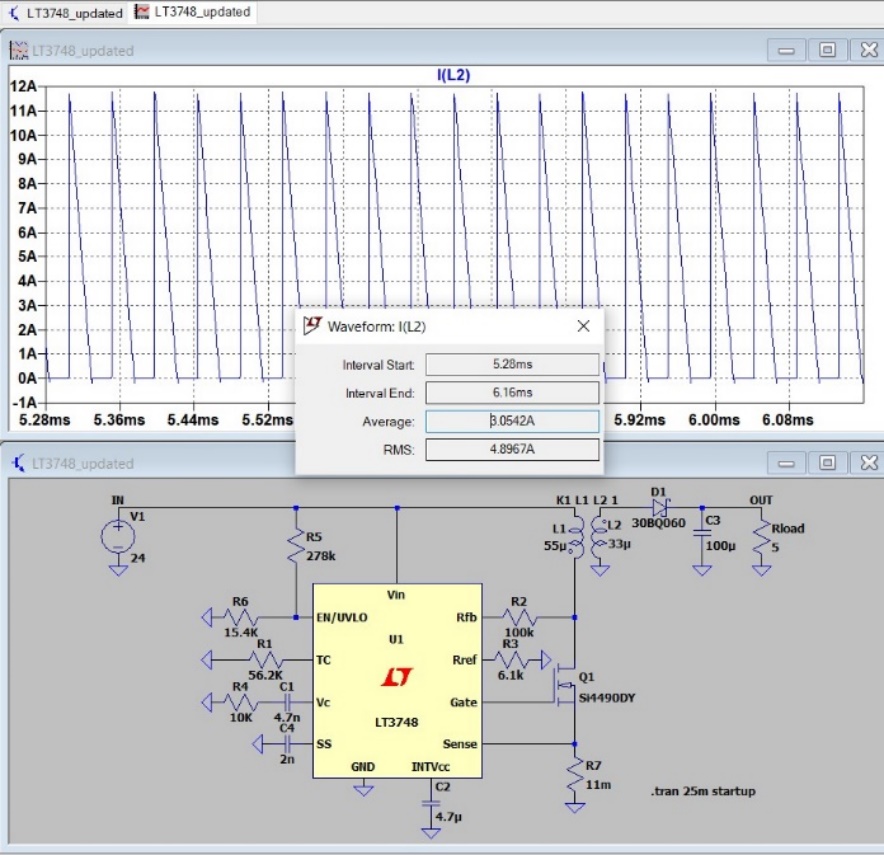


Figure 10 Secondary side RMS current

According to the simulations, the primary side voltage is a maximum 3.6 A. Secondary side voltage is a maximum 4.8 A. For a safety margin, the primary side current was chosen as 4A, and the secondary side voltage was chosen as 5A.

* For the primary side:
* For the secondary side:

For the cable selection, AWG 26 cable was chosen due to the high operating frequency margin. However, in the lab, there was AWG 25 cable with a 0.162 mm2 cross-section area and %100 skin depth at 85 kHz. Hence, we carried on with this cable.

* For the primary side:
* For the secondary side:

After we implemented the cables in the lab, they did not fit into the selected core. In real life, it showed us with these cable selections and turns number, and the fill factor must be higher than 1. So, the core selection is changed again.

After we searched the core inventory, the most suitable core was ferrite 0P44022EC core since, due to its material, leakage would be much less than the kool mu core. Also, its cross-section and window area is large enough to fit the cables. Then, all the calculations were made for this core. For the turn number, Al value of the core is important. So, if we change the A­l value of the core by adding an air gap to the core, we can acquire the desired turn numbers.

* Let’s assume the turn numbers as Npri = 12, Nsec = 9.5
* So,

So, by adding this air gap to the core, we can obtain the required reluctance value. If we calculate the magnetic flux density as

Hence, by this calculation, we can see that core is not saturated. It is not the expected value since we did all the calculations for B= 0.2 T. However, this result is close enough to the expected value, and it does not saturate the core. After that, the fill factor is calculated as follows:

It can be deducted that the fill factor is very small, and it shows that the core is overdesigned for this situation. However, since we built the transformer by hand, the fill factor is not high enough.

# COMPONENT CALCULATIONS

## Output Capacitor

From the voltage gain expression of the flyback converter, our duty cycle becomes

= N21 \* where N12 is chosen as 1.23

So, the duty limits become 0.44 for 24V input and 0.28 for 48V input.

= 0.03

D/(0.03\*5\*80kHz) = Co

Co has to be at least 36.7 µF (For 24 V input voltage) from the converter equations.

On the other hand, from the LT3748 datasheet output capacitor can be specified as

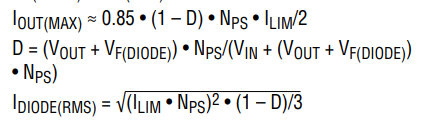


Figure 11 Output Voltage Equation with respect to Limiting Current

ILIM = = 8.62A (Duty approximated as 0.37)

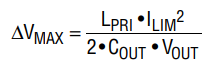


Figure 12 Output Capacitor Equation from the LT3748 Datasheet

0.03\*15 =

**Co = 302.72 µF**

## Diode and Switch

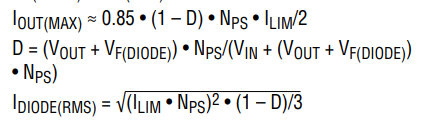


Figure 13 Diode RMS Current Equation from the Datasheet

ID(RMS) == 4.86A

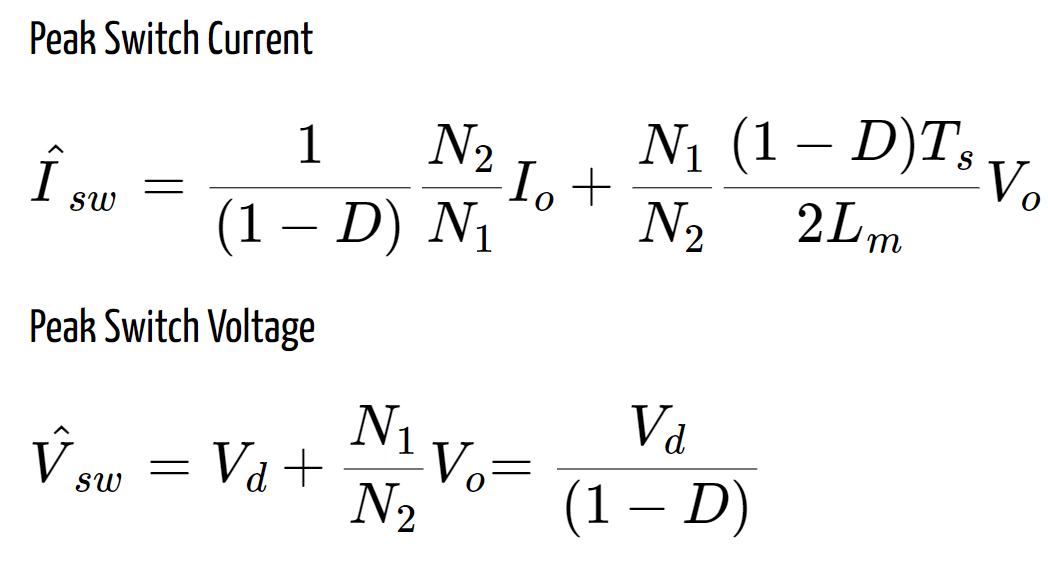


Figure 14 Peak Values for Switch

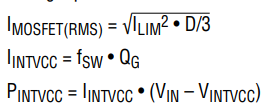


Figure 15 MOSFET RMS Current Equation from the Datasheet

IMOS(RMS) = = 3.03A

Vsw(max) = 48/(1-0.28) = 66.7V

Isw(max) = 3/0.8856+ 5.6 ≈ 12.07A (where Lm is 55 µH)

## Feedback and Reference Resistances

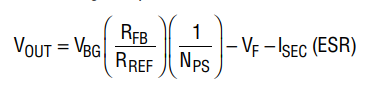


Figure 16 Output voltage equation from the datasheet

Where VBG bandgap voltage for a silicon switch is around 1.2 V,

NPS = N1/N2 = 1.23,

the forward voltage drop of the diode is 0.64V,

Equivalent series resistance on the secondary side is //ωL2//Ro ≈ 0

= 16.03

So, when RREF is given as 6.1kΩ (limited in the datasheet), RFB becomes around 97kΩ.

# SIMULATION RESULTS AND COMPONENT SELECTION

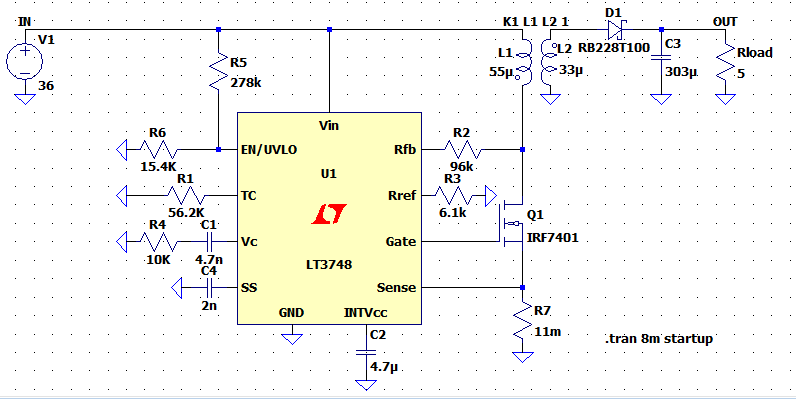


Figure 17 Circuit Diagram for the overall design with LT3748

Due to the above calculations in the previous section, the simulation circuit has been set, as seen in Figure 22.

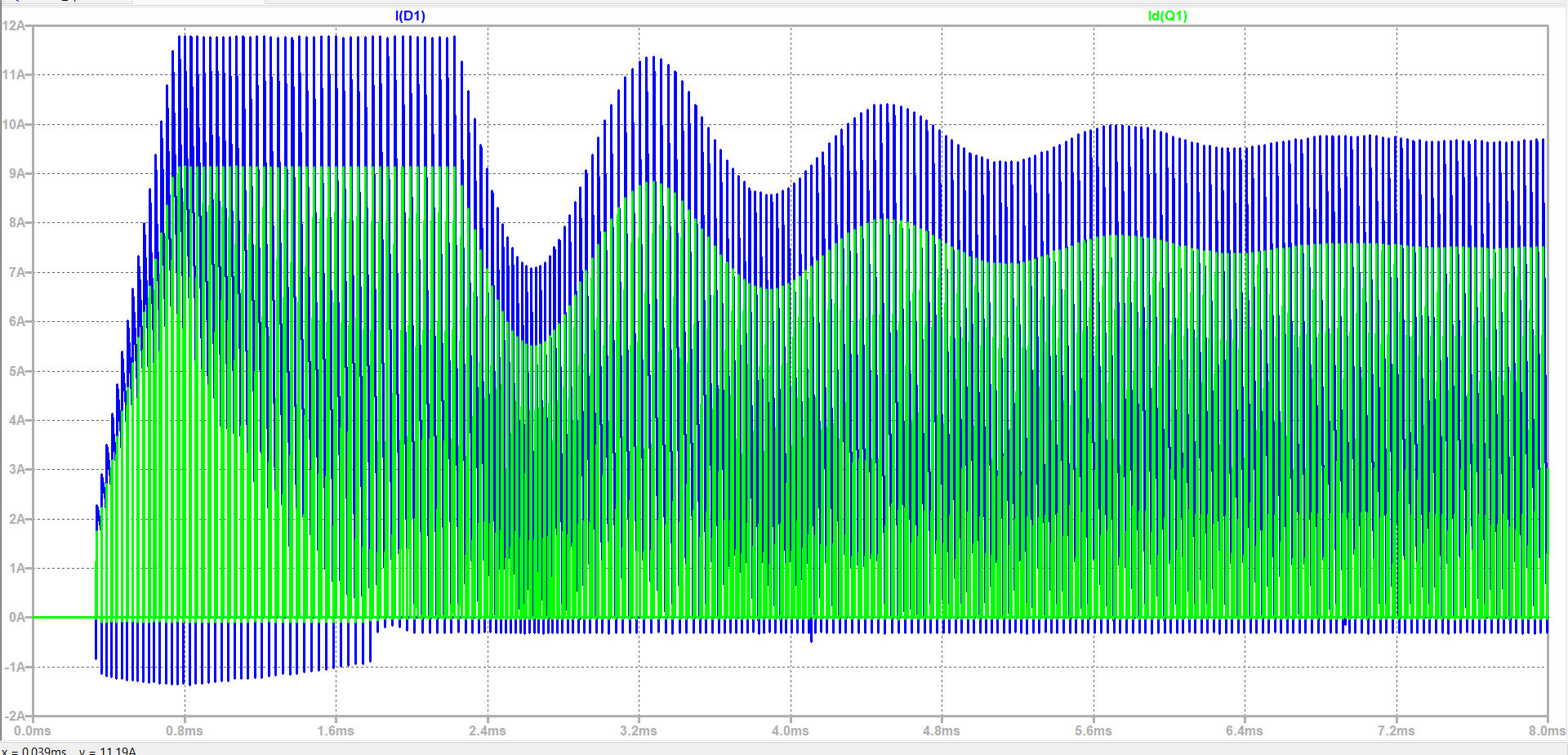


Figure 18 Diode and Switch Currents for the Transient Part

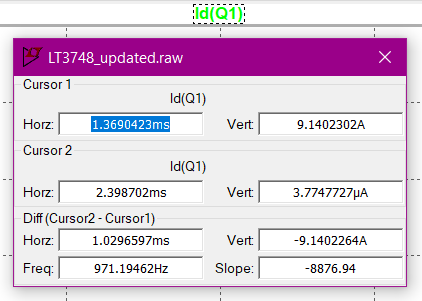
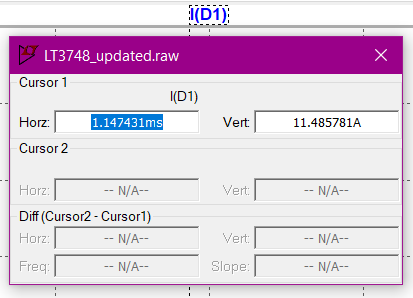


Figure 19 Diode and Switch Current Maxima



Figure 20 Diode and switch voltages

As seen in Figures 24 and 23, the diode selected must be able to handle at least 12 amperes, and the switch must handle 10 amperes. Also, Figure 25 shows that the switch must endure 60 volts, and the diode must handle at least 55 volts.

For simplicity, the switch is chosen from the lab inventory since the components match the ratings. IRF540 N-type MOSFET is chosen since it has 100V-27A ratings that can handle our circuit’s needs. For the diode, DS16-01AS-TRL with 100V-16A ratings is chosen.

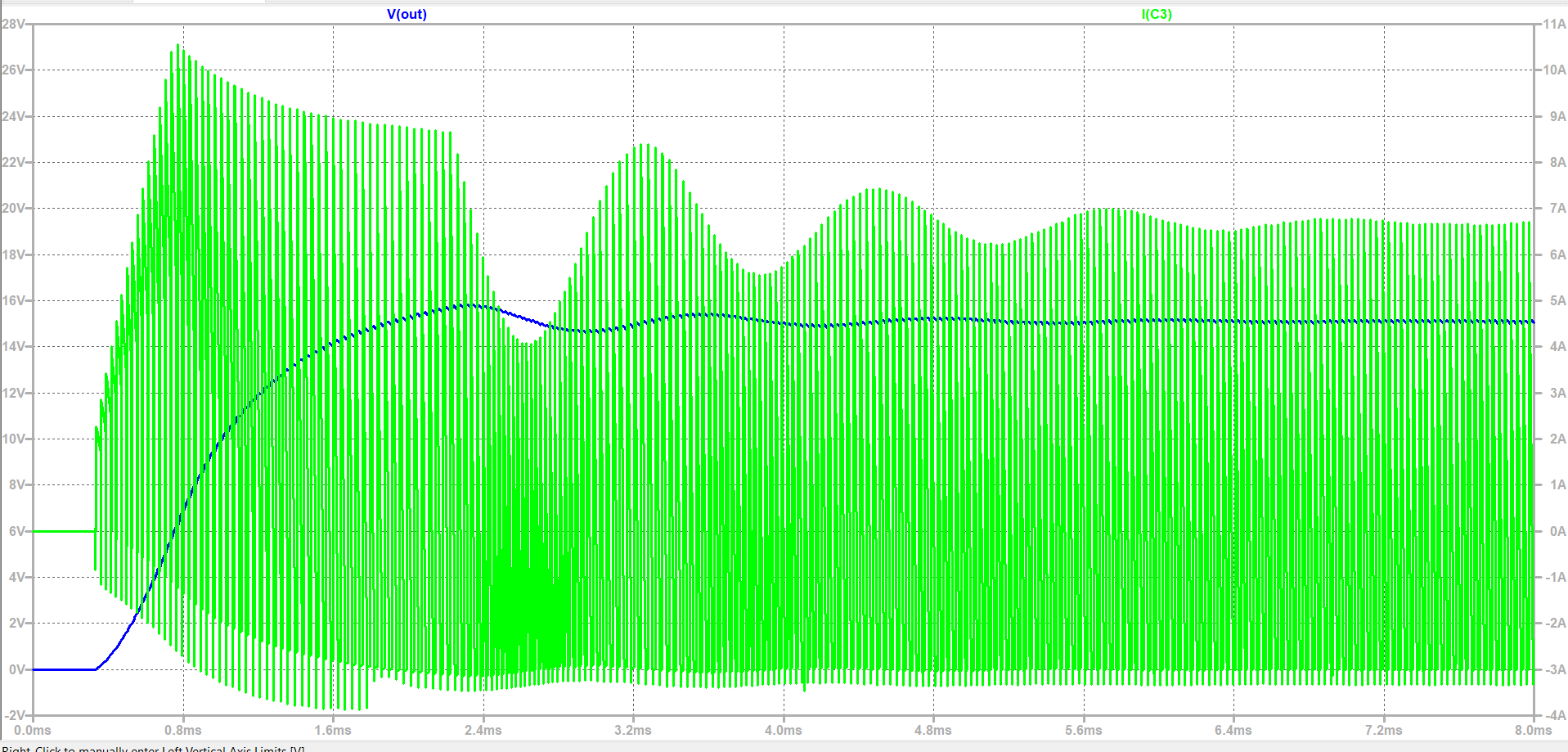


Figure 21 Output capacitor voltage and current for the transient interval

As obtained in Figure 26, the output voltage sees almost 16 volts in the transient time interval, so the output capacitor must bear this voltage. Also, the current seen by this capacitor reaches almost 11 amperes. After checking the most accessible stocks, the **SD1V337M1012MPA** capacitor has been our choice.This capacitor is 330µF and can handle 35V & 0.63A ripple current.

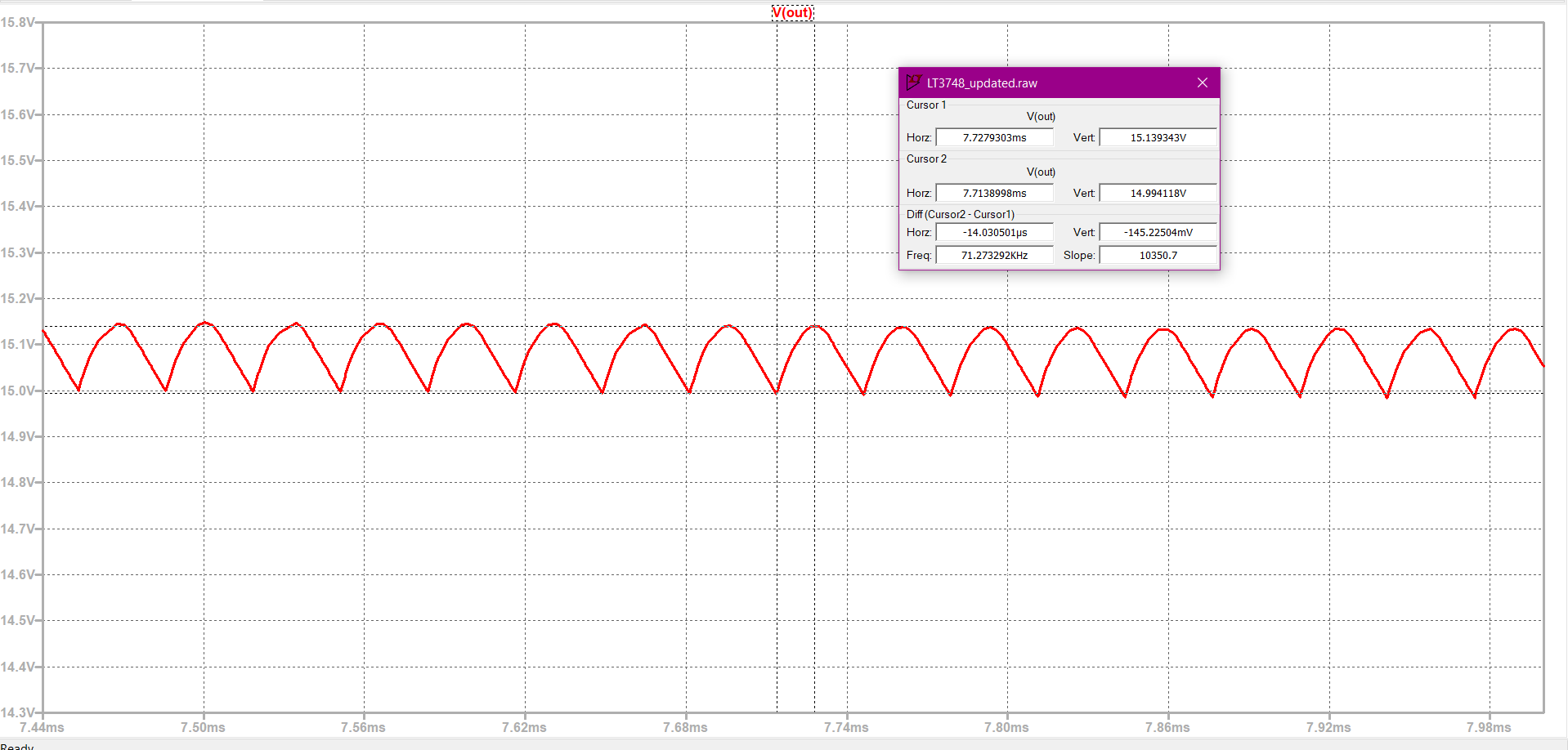


Figure 22 Output Voltage Ripple

As seen in Fig.27, the output ripple is around 0.15 Volts.

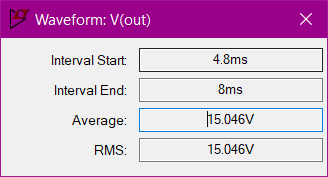
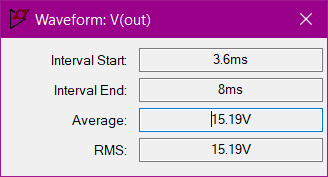


Figure 23 Vout deviation when the input goes from 24V to 48V

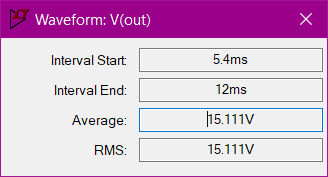
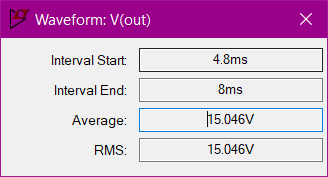


Figure 24 Vout deviation when Io changes from 100% to 10%

Line regulation from our simulation can be seen in Fig.27 as (15.19-15.046) \* 100/15.19 = 0.947 % and load regulation can be seen in Figure 28 as (15.111-15.046) \* 100/15.111 = 0.43%

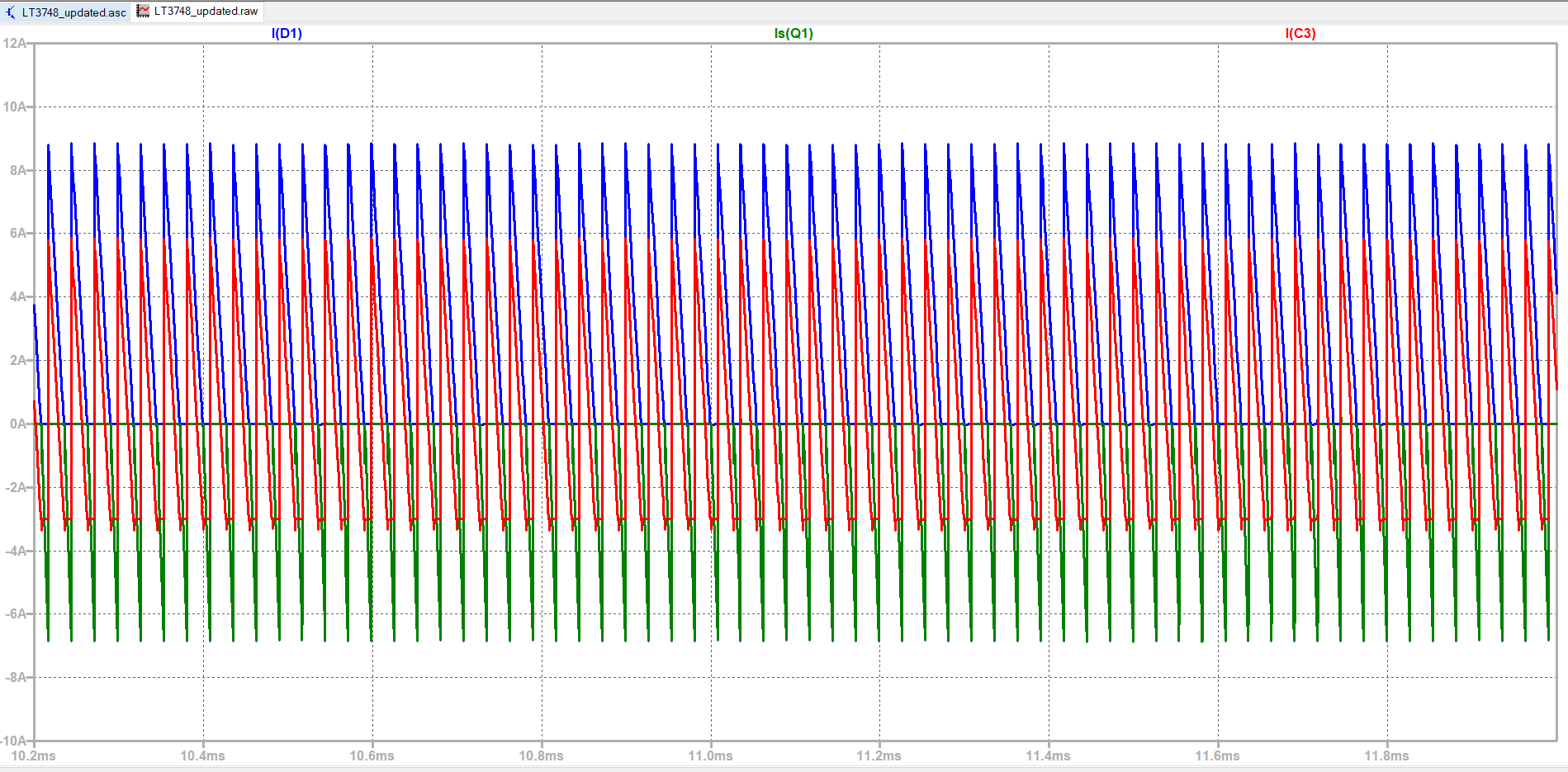


Figure 25 IDiode, IDS and IC at Steady State

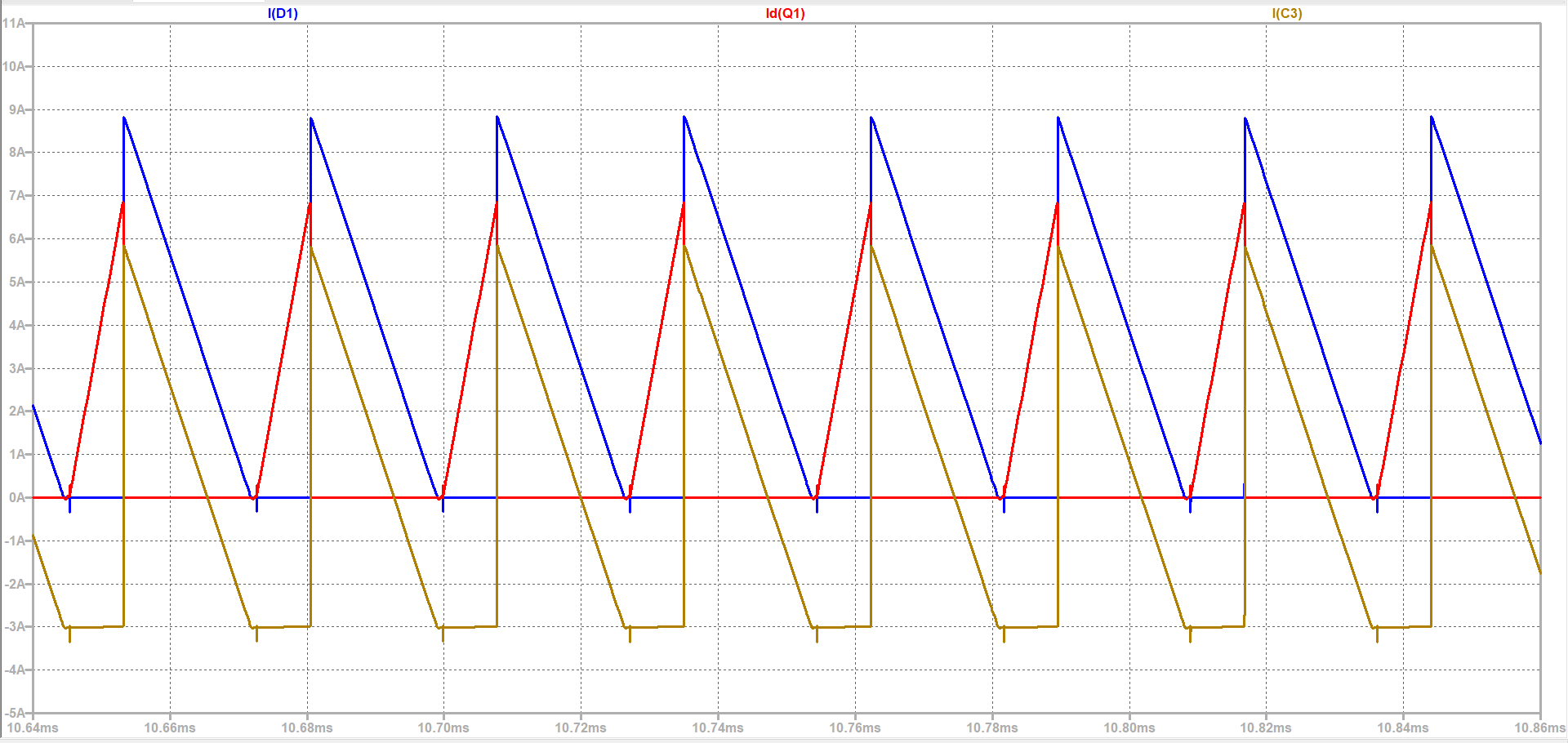


Figure 26 IDiode, IDS and IC waveforms

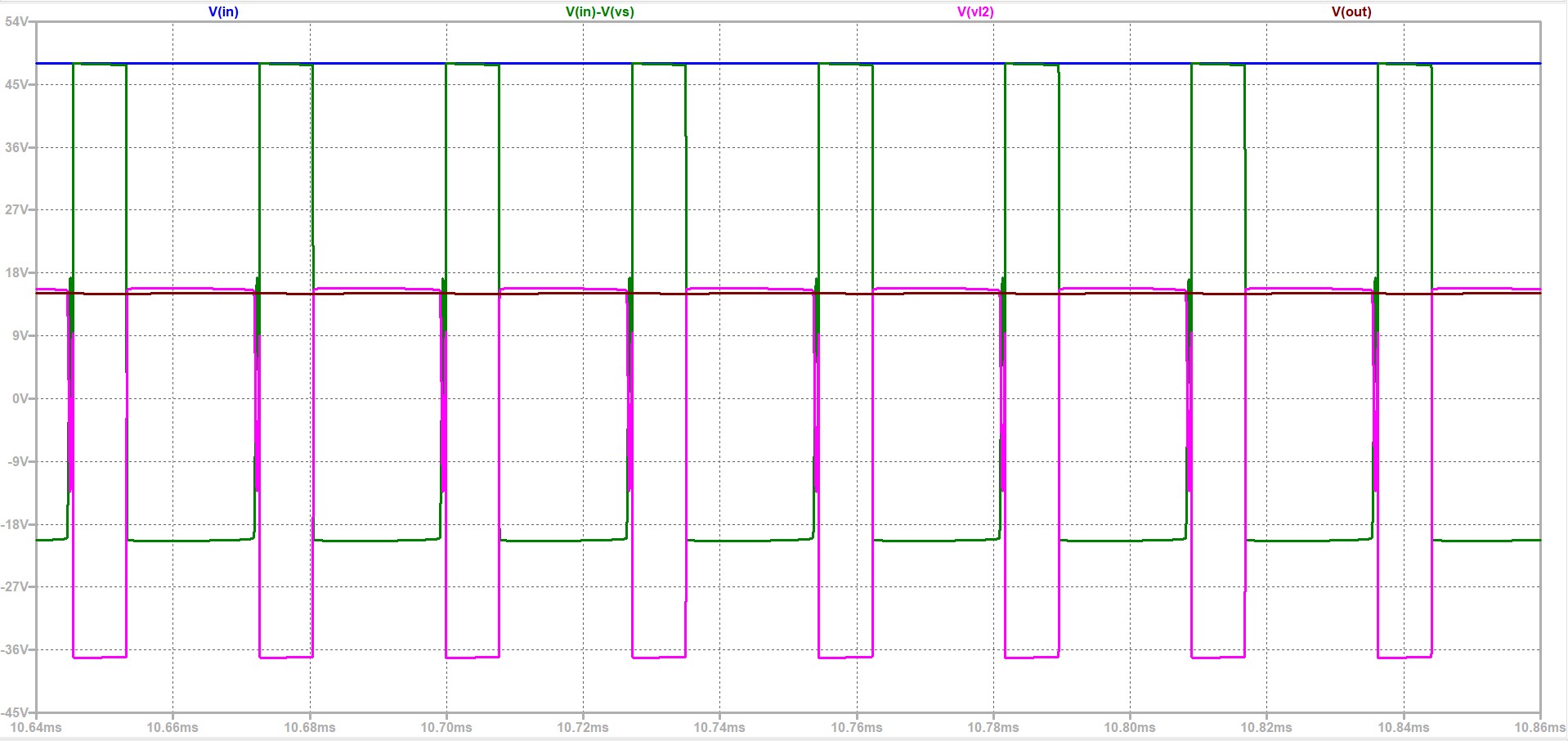


Figure 27 Vin, Vout, VL1, and VL2 voltage waveforms

# IMPLEMENTATION

The transformer was implemented according to calculations. However, as expected, real-life and theoretical calculations did not match exactly. After implementing the transformer, we did the measurements.

A picture containing text, indoor

Description automatically generated

Figure 28 Primary side inductance

For the primary side inductance measurement, which is magnetizing inductance, we left open the secondary side and connected the probes of the LCR meter to the primary side. The result of the measurement can be seen in Fig.11. The expected value was 55 µH, but it was measured as 53 µH. It is very close to the expected value.



Figure 29 Secondary side inductance

For the secondary side inductance measurement, we left open the primary side and connected the probes of the LCR meter to the secondary side. The result of the measurement can be seen in Figure 12. It was measured as 36 µH.

If the turns ratio is checked by the inductance values, the turns ratio can be found as

So, the turns ratio is satisfied by the inductance values.



Figure 30 Leakage inductance value

For the leakage inductance, we shorted the secondary side and connected the probes to the primary side. The connection can be seen in Figure 14. Since it was thought that we might change the turns in the future, excess cables did not cut out. Hence, resulted in more leakage inductance of 2.6 µH, which can be seen in Figure 13.

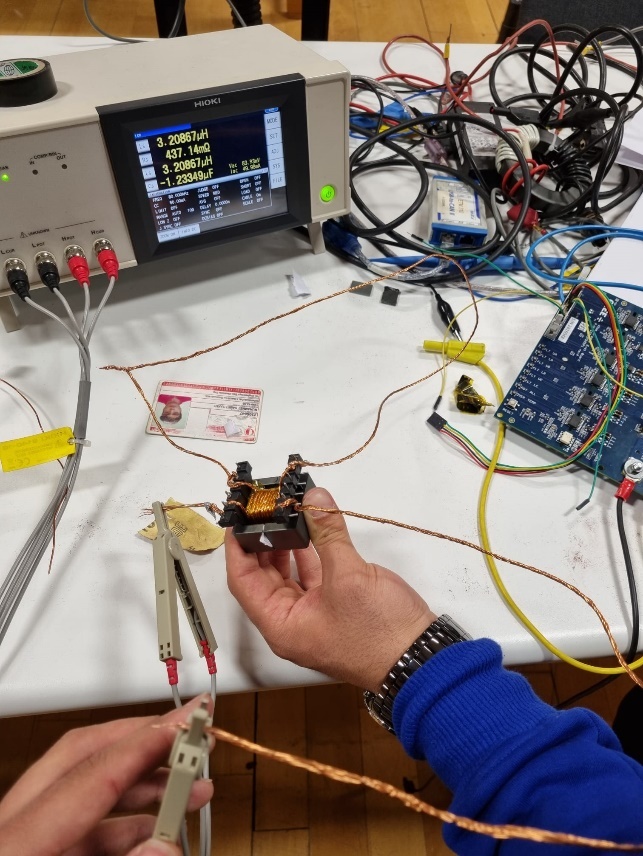


Figure 31 Leakage inductance measurement

## PCB Design

The controller LT3748 has an MSOP-16 package, so the pertinax test setup was impossible to use. In order to test out the simulated system, a printed circuit board design was a must. While designing the PCB, most SMD components were easily accessible to us for free or at very low prices; that is why very small packages like 0402 and 0603 were used in our design.

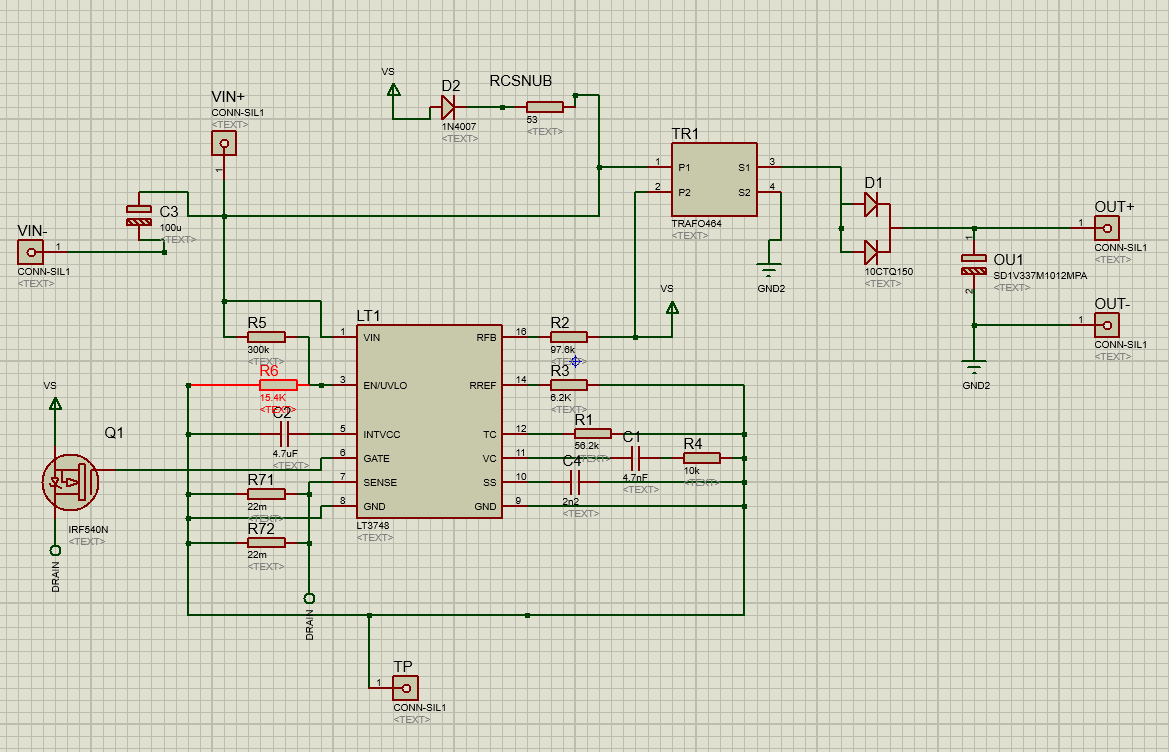


Figure 32 PCB Schematic

The initial schematic with the whole simulation components is shown in Figure 32. Other than 0402 and 0603 packages of controller resistances and capacitors, to change easily during test procedures, sense resistances were in 0805 packages, and snubber components were left as a large pad on the surface. The right side of the transformer has been connected to a ground isolated from the primary side via a secondary ground VIN- pin.

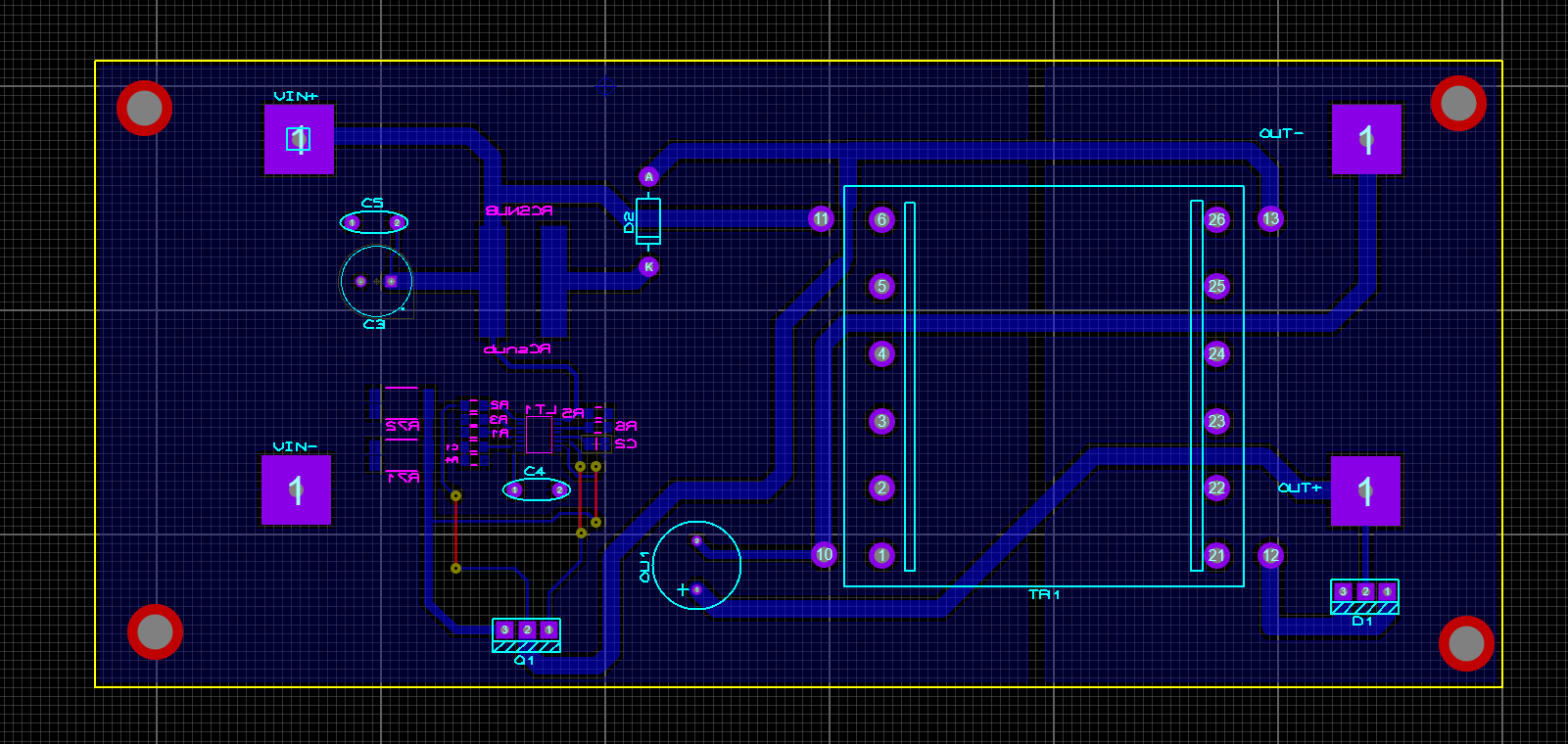


Figure 33 PCB Layout

The final layout is shown in Figure 33. Since our controller was very small and sensitive to any disturbances, reference, feedback, and sense resistances were placed really close, and no routes were passing under the controller. To make the board smaller and cheaper one-layer routes were inserted, and the components that affect another component the less were drawn closer. In the and a board with 160\*72 mm2 area has been printed. After final implementations, the circuitry seemed like Figures 34 and 35.



Figure 34 Top side of the circuitry

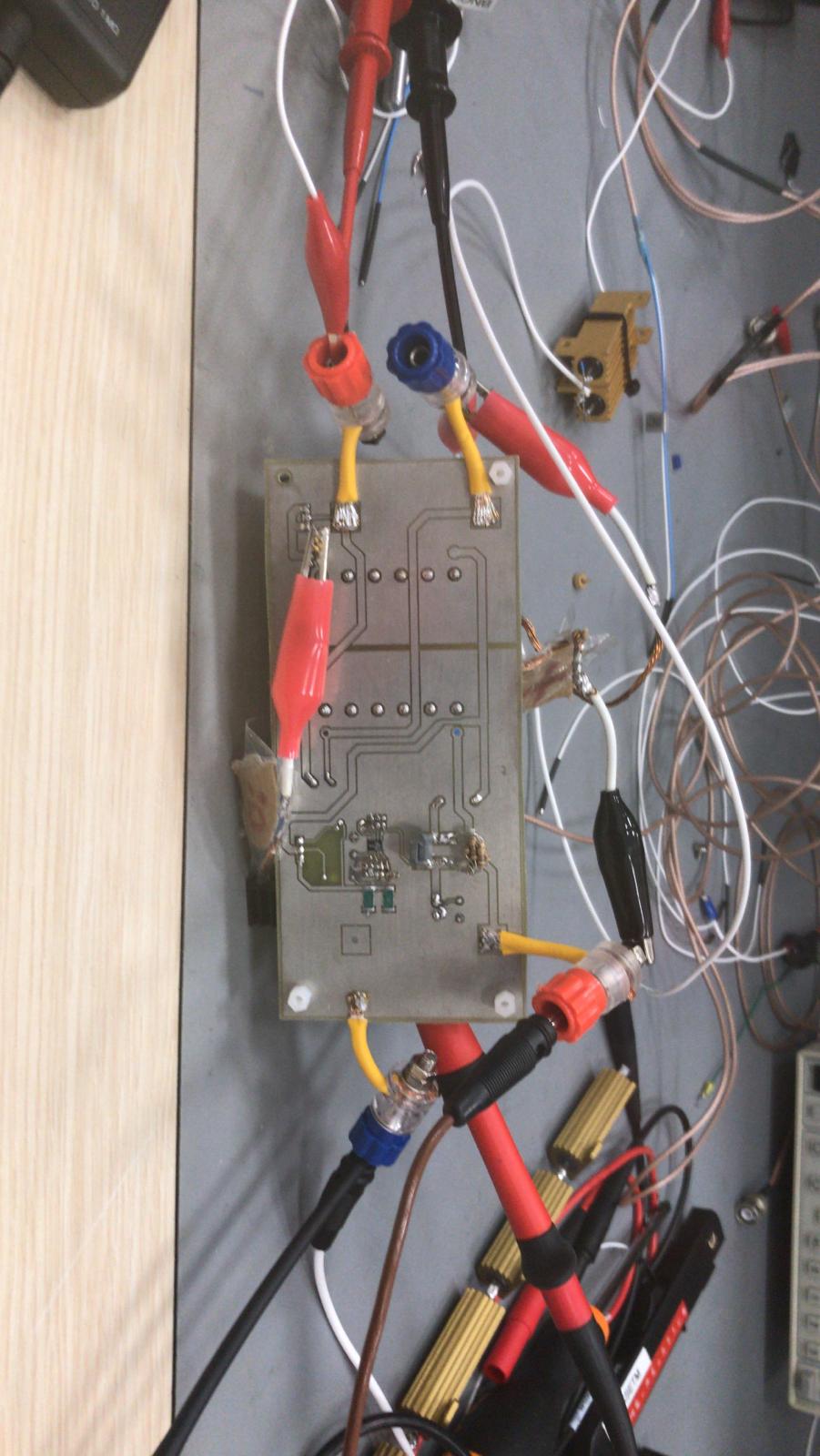


Figure 35 Bottom side of the circuitry



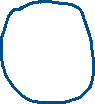


Figure 36 Snubber Circuit Implementation

In the figure above, you can see the controller (red circle) and the RCD snubber (blue circle). It was hard to implement the controller into the PCB since its size was extremely small, and the components connected to the controller were 0402 packages. Snubber is designed to dissipate the power stacked on the MOSFET. In order to do that, 11 nF ceramic capacitor and 40 ohm sand stone resistance. Initially, we implemented a through-hole 0.125 W resistor by paralleling 8 of them. However, in our first design, they burn out. Hence, we find the solution in paralleling three 120 ohm, 11 W sandstone resistors. We paralleled three of them to make a safety margin and dissipate more heat with more area.

## Line Regulation

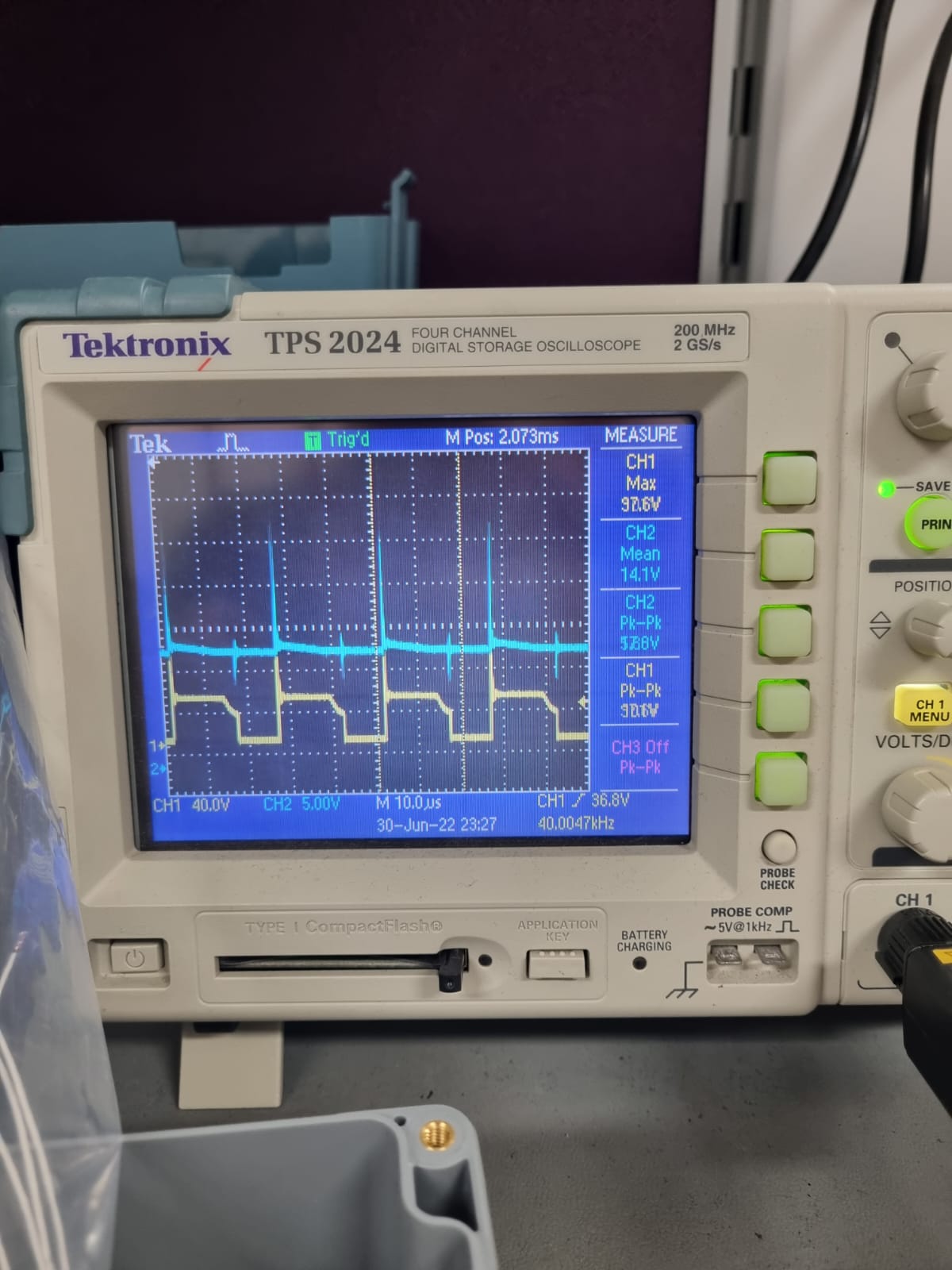
 

Figure 37 Line regulation input and output data for 32V input voltage

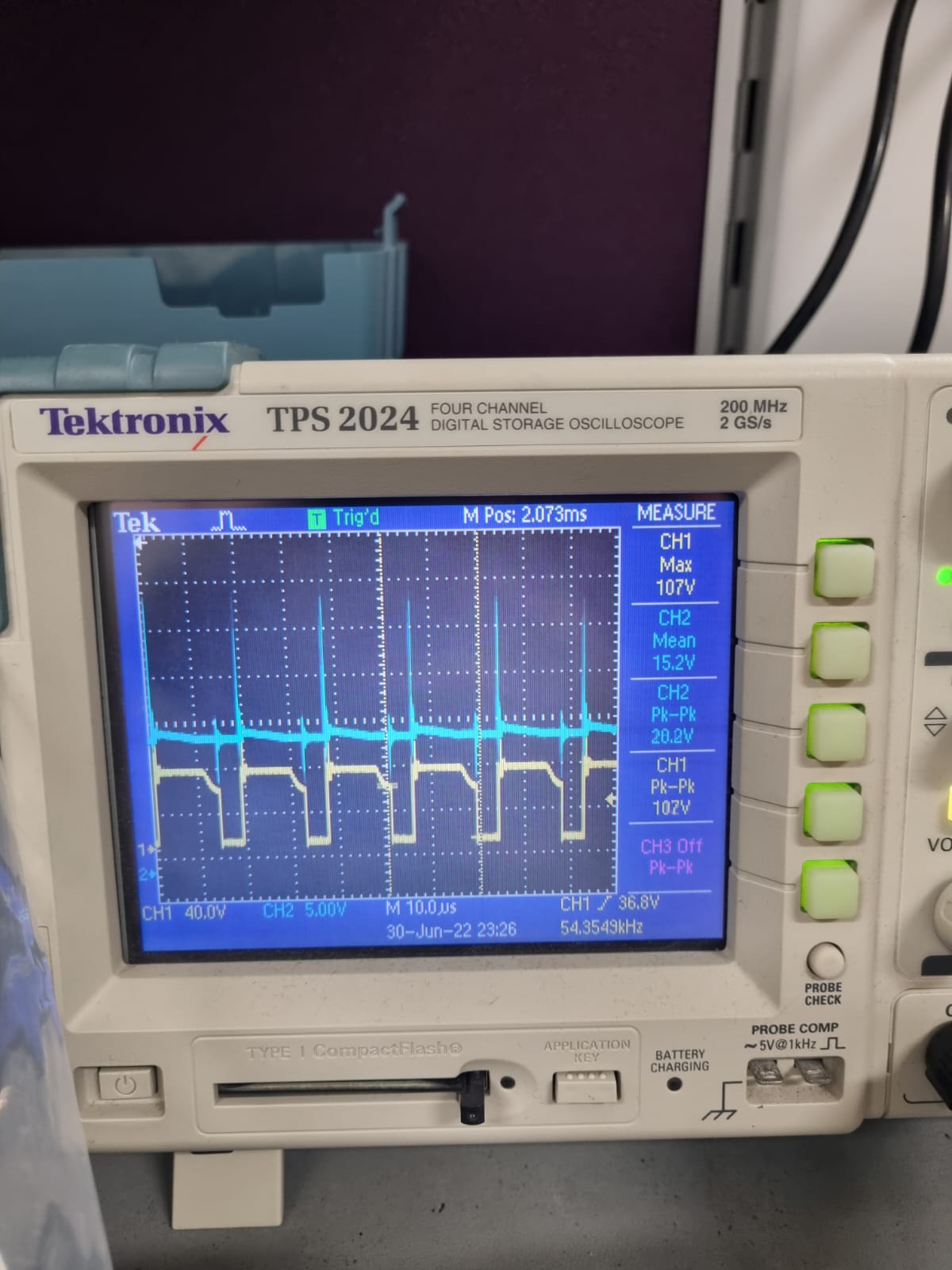
 

Figure 38 Line regulation input and output data for 48V input voltage

In the cases above, we’ve measured the line regulation while channel 1 gives the VDS voltage of the MOSFET and channel 2 gives the output. In order to do this, we’ve set our output voltage to 15 V by changing the load when the input voltage is 32 V. Then, we initially decreased our input voltage to 24 V and measured the output voltage. The output voltage was 14.1 V, as you can observe from Figure 37 above. After this, we set our input voltage to 48 V and measured the output voltage. The output voltage vas 15.2, as you can observe from Figure 38 above. So, if the line regulation is calculated:

This is higher than the required line regulation. The reason behind this can be the leakage inductance in the transformer. Due to the leakage inductance, controller cannot sense fully accurate current in the primary side, and cannot adapt the switching frequency and duty cycle appropriately.

## Load Regulation

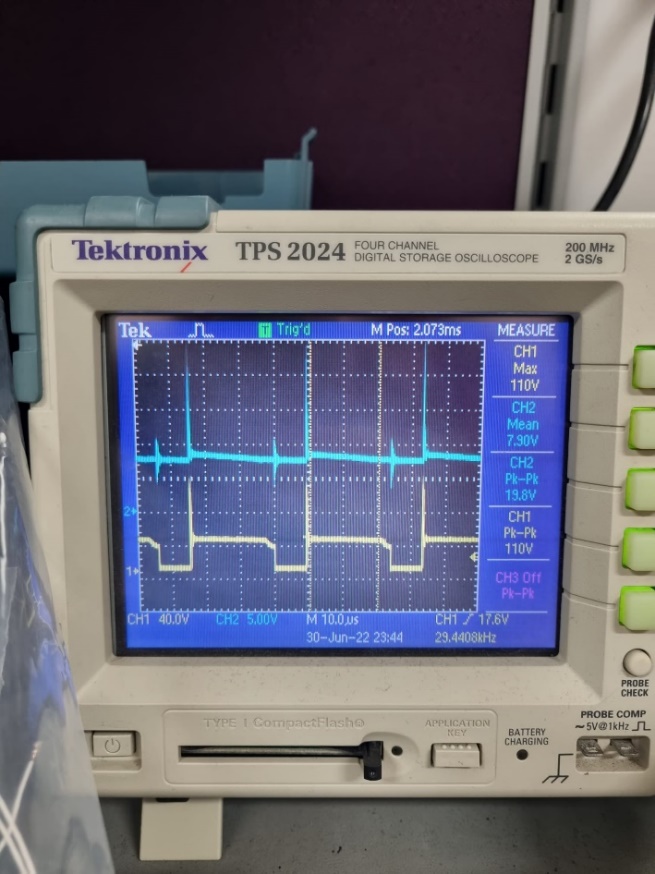
 

Figure 39 Load regulation input and output data for 5 ohm load

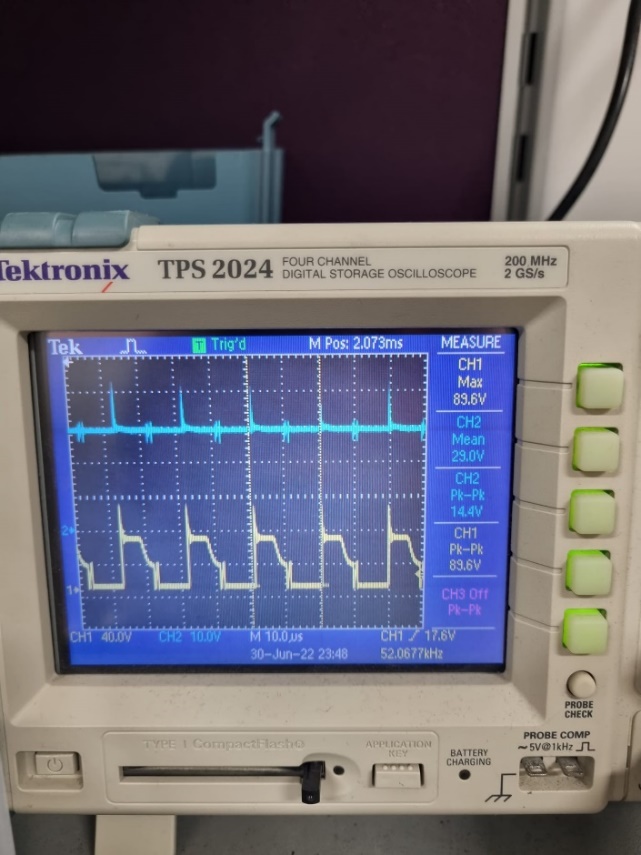
 

Figure 40 Load regulation input and output data for 50 ohm load

In the cases above, we’ve measured the load regulation while channel 1 gives the VDS voltage of the MOSFET and channel 2 gives the output. In order to do this, we’ve set our input voltage to 24 V and changed the load from 5 ohm to 50 ohm. In Figures 39.1 and 39.2, the results of the 5 ohm load case can be seen. The output voltage is approximately 8 V. On the other hand, in Figures 40.1 and 40.2, results of the 50 ohm load case can be seen. The output voltage is 29 V. So, if the load regulation is calculated:

In this design, the load regulation is awful, as we can see from the results. When the controller has no connection with the secondary side, the main problem is load regulation, as we have faced in our design. The way that our controller chooses the output voltage with two external resistors. It seems like an advantage, but the regulation is affected by other things. As the switch turns on, parasitic in the power stage, output rectifier reverse recovery characteristics, and high current gate drive pulses can create significant noise pulses on the leading edge of the current sense signal. This problem limits our current and results in load regulation problems. Because of that, we have designed an RC filter for the sense pin. In addition to that, these noise problems caused a premature, and the controller duty cycle became very low values that were not expected. After the demonstration, we handled this problem with the new RC filter and new sense resistor. We did not have enough time to test all the other things, whereas we put the simulation results below.

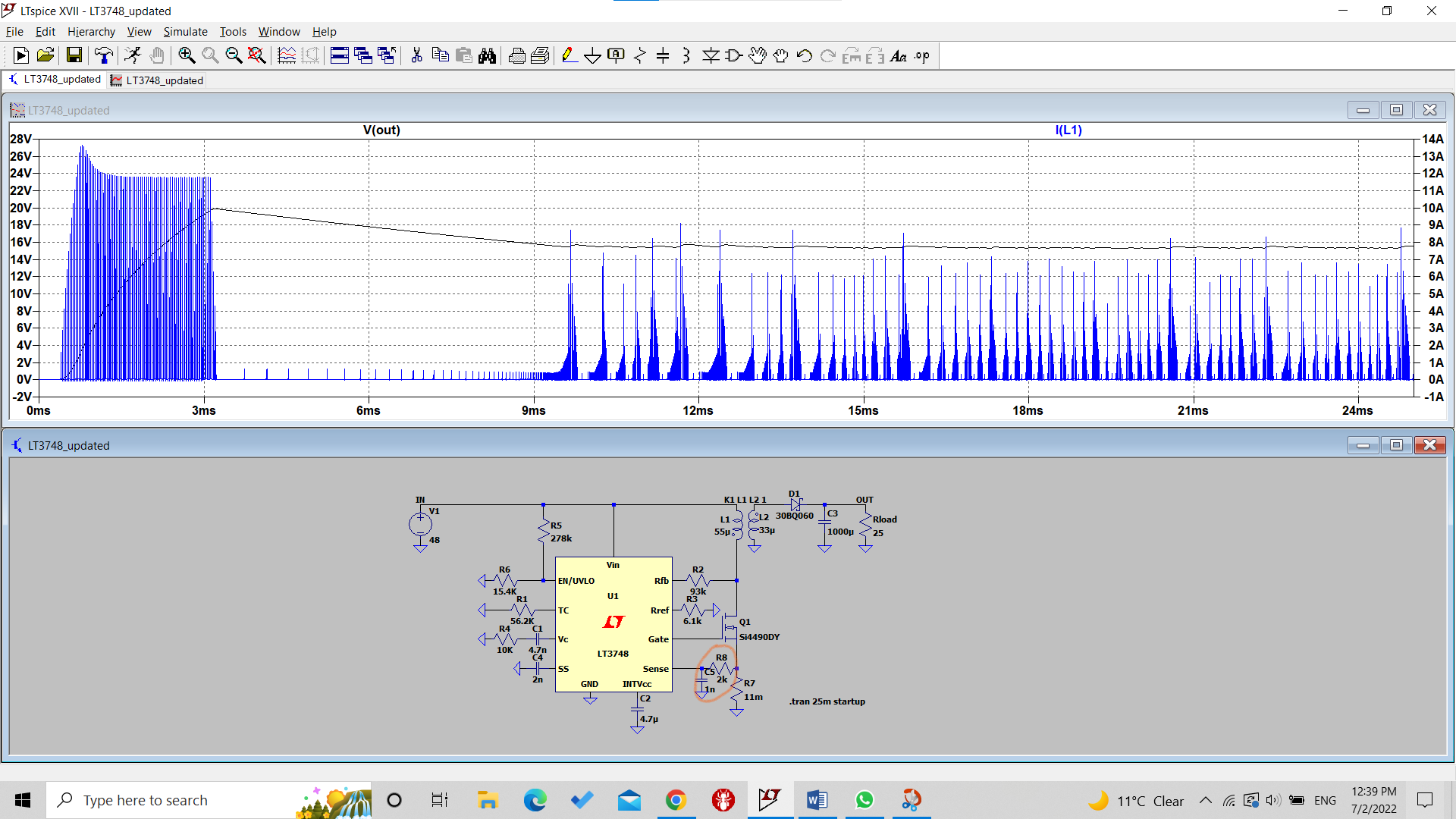


Figure 41 Input and output data for RC filter added simulation (Rsense = 11mOhm)

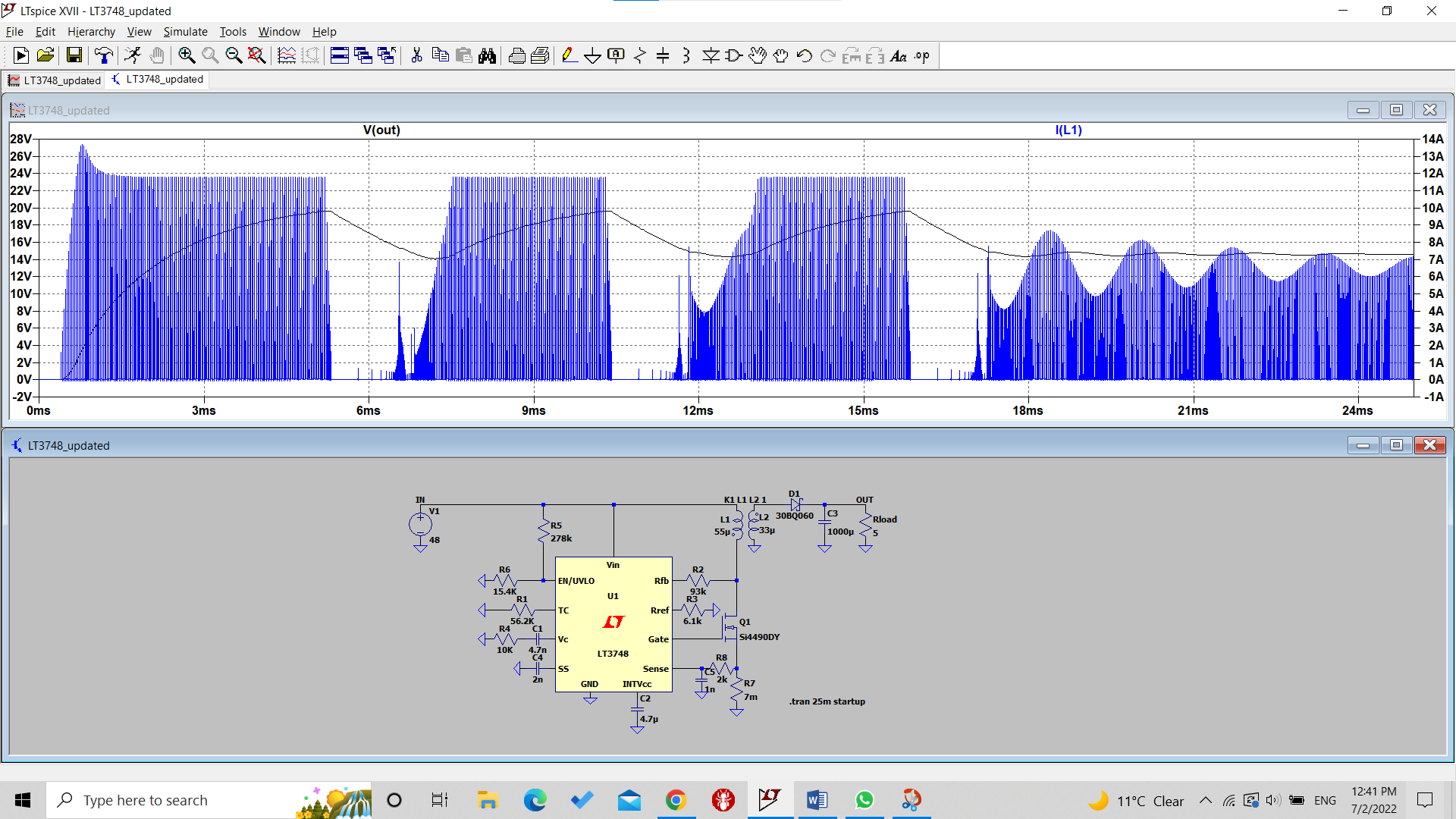


Figure 42 Input and output data for RC filter added simulation (Rsense = 7mOhm)

## Final Product Industrial Design

With respect to the borders of our board, the height of the semiconductors, size of the transformer, and the input-output cables outside the board, a simple IP-67 plastic box with 200\*120\*90 mm3 dimensions is added to the outside of the circuit to obtain a more industrial look and to give the “Blackbox” idea.



Figure 43 Industrial Design Casing

# LOSSES

### Copper Losses

For the copper losses, we need to find how much cable is used, and to obtain this information, the dimensions of the core must be known.

Diagram

Description automatically generated

Figure 44 Dimensions of the core

Dimensions of the core are represented in the figure above. According to this figure,

### Core Loss

According to the core loss per cm3 value of the core, approximate core loss is calculated as follows:

Since we are operating at high frequencies, core losses are much higher than the copper losses, and it is expected.

### Thermal Losses

Mosfet: Pcond = Rds\*I2ds(rms) = 0.04\*2.152 = 0.185W

Psw = Vin\*Io\*fsw\*(tr+tf) = 48\*3\*80kHz\*(55+57 ns) = 1.3W

Tjunc = Ta + Ploss \* Rja = 30+ (1.485\*62) = 122.07oC (Ambient temperature is taken as 30oC )

RHA = RJA – RCH – RJC = 62 -1.25

So, the heatsink thermal resistance must be less than 60.75oC/W.

Diode: Pcond = Vf\*If(avg) = 0.64\*3.18 = 2.04W

Psw = QR \* VRR\*fs where QR can be approximated as 0.5\*IRM\*tRR but since our diode is a Schottky diode, reverse recovery time is very small, thus switching losses can be ignored for now.

Assuming 100oC junction temperature and 30oC ambient,

RHA = (Tj-Ta)/Ploss – RCH – RJC

RHA = 70/2.04 – 0.5 - 1.4 = 32.5

So, the diode’s heatsink thermal resistance must be less than 32.5oC/W

## Real-Case Thermal Results



Figure 45 Thermal camera results of the circuit

As seen in Figure 45, unlike our expectations, the most heat-dissipating components were the snubber resistances. After almost 10 minutes of working, our output diode and MOSFET were still in good condition thermally. What we missed through ideal simulations was that more than the predicted simulation current was drawn by these snubber resistances from the input side since no transformer can work ideally and transfer all the current. In the end, we saw that our cooling choices were enough, and the thermal calculations did not fail us.

# EFFICIENCY

A picture containing text, device, control panel

Description automatically generated Graphical user interface

Description automatically generated

Figure 46 Data for efficiency calculation

Efficiency is calculated when the load is 5 ohm, and the input voltage is approximately 24 V. In these conditions, efficiency is

According to this calculation, the design has 4.3 Watts of loss. These losses are mostly due to the magnetic and copper losses calculated in the theoretical losses section and due to the snubber designed for the MOSFET.

# COST ANALYSIS

|  |  |
| --- | --- |
|  | **Price(TL)** |
| Diode | 29.0624 |
| MOSFET | 12.86 |
| Casing | 130 |
| PCB | 250 |
| 4.7nF capacitor | 1.2958 |
| 4.7µ capacitor | 0.4132 |
| 330µ capacitor | 1.8995 |
| 2.2n capacitor | 0.6157 |
|  | **Price(TL)** |
| 300k resistor | 0.2627 |
| 97.6k resistor | 0.0363 |
| 56.2k resistor | 0.0363 |
| 15.4k resistor | 0.0201 |
| 10k resistor | 0.0201 |
| 6.2k resistor | 0.0178 |
| 12 mΩ resistor | 21.58 |
| **Total** | **448.12 TL** |

# CONCLUSION

This report focused on designing an isolated 24-48V to 15V @45W DC-DC converter. As the chosen topology of the flyback converter, applicable controller LT3748, and components have been examined, outcomes of our design choices and design implementation have been argued. The reasons behind the failure of our design in some aspects have been discussed, and potential solutions were proposed. PCB design of the circuitry and the final schematic is shown. Thermal results of the circuit have been examined, cost of the project is calculated and the report is finalized.

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