EE464 HARDWARE PROJECT

Design Report

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Intro

This project is based on the need for an isolated DC-DC converter that takes an input voltage from 24V to 48V and gives a constant output of 15V at 45W with closed-loop control. The chosen converter design's both lines, and load regulations, as well as the output voltage ripple, needs to be 3%. This design report will focus on the topology and its component selections due to these constraints. Analytical calculations for electrical and magnetic design and overall simulation results will be discussed.

Table 1 Project Constrains

Input Voltage Range	24-48V
Output Voltage	15V
Output Power	45W
Line Regulation Percentage	3%
Load Regulation Percentage	3%
Output P-P Voltage Ripple	3%

Topology Selection

The forward converter is also simple like flyback but instead of storing the energy the transformer delivers the power via it. The output current is relatively more stable than some other isolated topologies but the output inductor and other semiconductor devices highly affect the power loss, heating and cost in our design. Also, this topology is very sensitive about load changes and commonly used in high current applications, so in order to protect our load regulation constraints and since our project is not in high output current range, we did not choose to use this topology.

Push-pull and half/full bridge topologies were considered since the core utilization is better and copper losses are less in these topologies, but these topologies are more applicable to high output power applications. Also, for a small scaled project like ours did not need more components, hard switch control and high switch stresses, so, this is not the best option for us.

In this project, fundamental flyback topology is chosen. Flyback converters are used mostly in low to medium power applications, so this was the main reason why we tend to choose this topology. Also, this topology is chosen due to its simplicity in construct and control, especially in discontinuous conduction mode. It has a smaller number of circuit elements (mainly passive elements); also, no energy storage inductor is needed because of the transformer, and only one diode is used in the topology, which causes less loss in the system. Also, there are more minor EMI problems with respect to other isolated topologies.

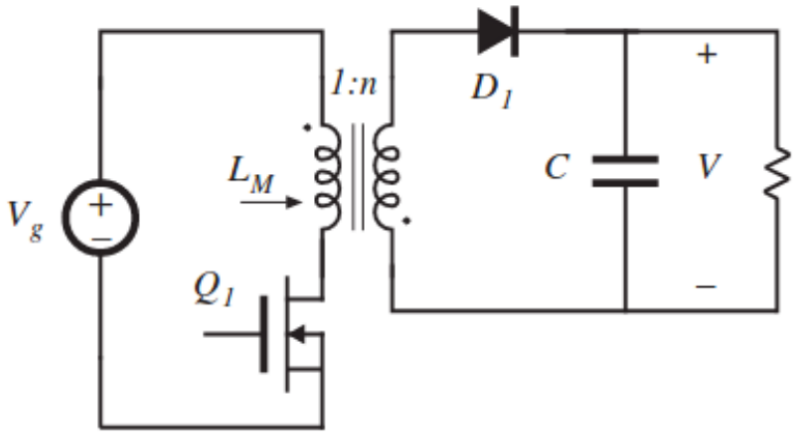


Figure 1 Flyback Converter Topology

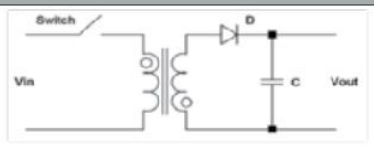
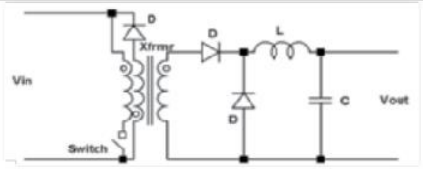
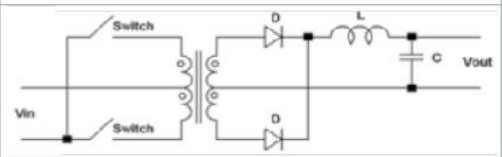
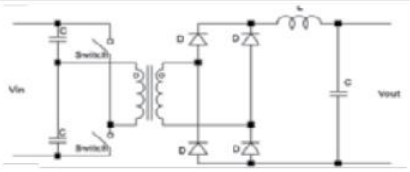
	Topology	Schematic	Power (Watts)	Typical Efficiency	Relative Cost	Magnetics Required	DC Transfer Function (V_{out}/V_{in})	Maximum Practical Duty Cycle	Universal Input (90-264) V_{AC}
Isolated Topologies	**DCM Flyback**		150	75	1.5	Transformer	$Dx\sqrt{\frac{TxV_{out}}{2xI_{out}xLP}}$	0.9	Yes
	Forward		150	75	1.8	Transformer and Inductor	$\frac{2N_s}{N_p} x D$	0.45	Yes
	Push-Pull		500	80	1.8	Transformer and Inductor	$\frac{N_s}{N_p} x D$	0.45	No
	Half-Bridge		500	85	2	Transformer and Inductor	$\frac{N_s}{N_p} x D$	0.45	Yes

Figure 2 Isolated Converter Topologies Comparison (retrieved from Würth Elektronik)

CONTROLLER DESIGN

There are different kinds of controllers we have found and implemented in LTspice. The first one is LT3751 which is a capacitor charger. The main advantage of the controller has UVLO/OVLO pins that are used for selecting the input voltage range. Another advantage of the controller is that two resistors which are RV_{out} and R_{BG}, are used to set up the output voltage.

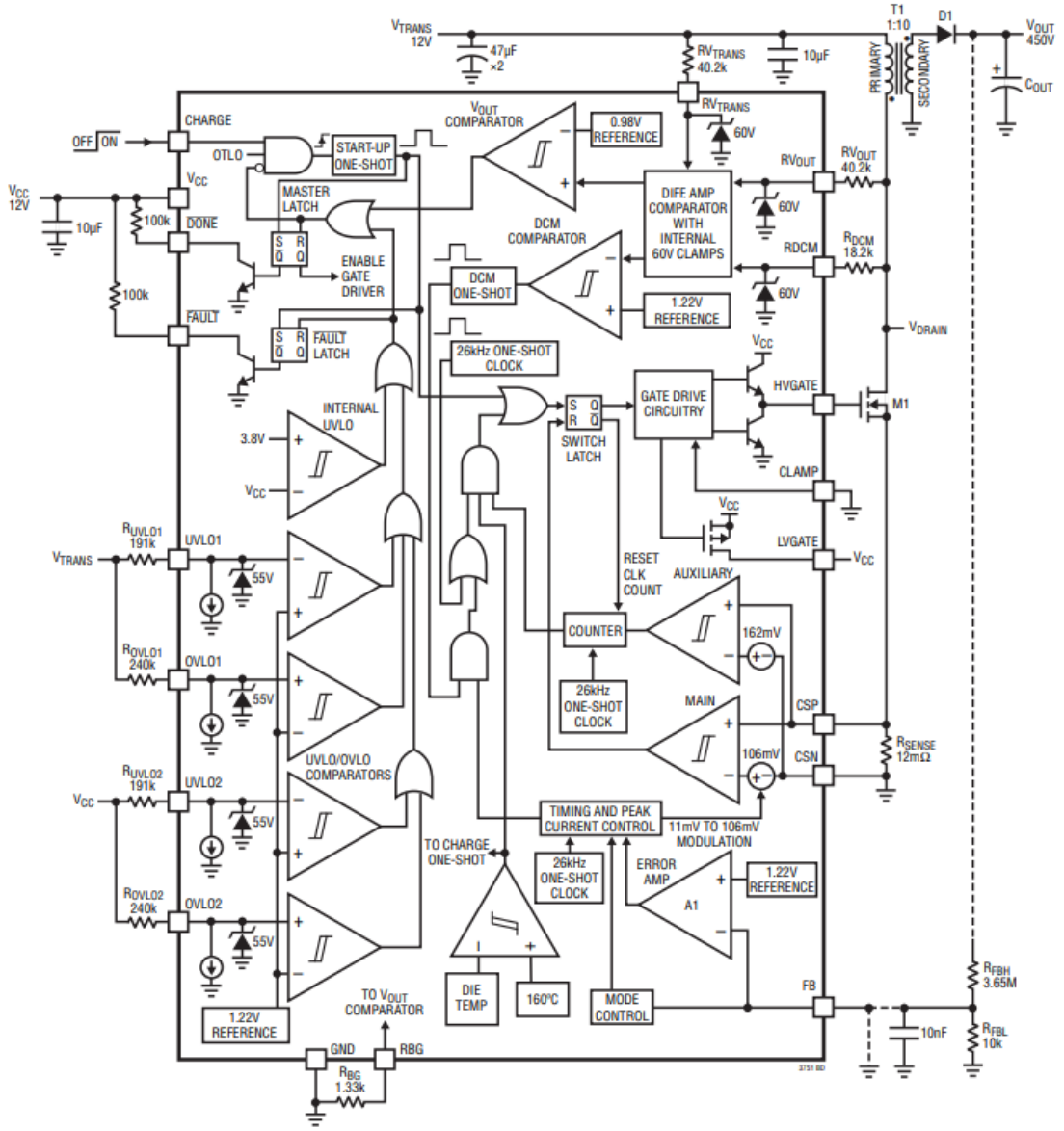


Figure 3 Block diagram of the LT3751

Also, this controller has the ability to operate in DCM operation, which increases the efficiency of the converter, which is really critical for the project. At that point, most of the requirements for the project are satisfied, whereas this controller is used for the capacitor charger, emphasized at the beginning. Because of that, when this controller was used with the load which is 5Ω in this project, the output voltage decreased to zero. In these controller applications, output

voltage regulation resistors exist for high output values. On the other hand, we are trying to regulate the voltage at the 15V and 45W output. In this step, we could not reach the required voltage level because of the step size of the controller. The reason behind this is the controller, which is LT3751, is created for high voltage values. The digital voltage step size of the controller is higher than 15V.

After this controller, a lot of different kinds of controllers are implemented in LTspice and Simulink. Unfortunately, most of them could not reach the requirements that are specified in the project description. After the search step, we have found the LT3748, which is created by Linear technology. LT3748 is the isolated flyback converter controller. The advantages of this controller can be listed as:

-Wide input range and controllable lower threshold

-No transformer third winding or opto-isolator required for regulation

-Primary side winding feedback load regulation

-The LT3748 has different kinds of advantages besides those. The regulated output voltage can be decided as with the formula:

$$V_{FLBK} = (V_{out} + V_F + I_{sec} * ESR) * N_{PS}$$

$$\frac{V_{FLBK}}{R_{FB}} = \frac{V_{BG}}{R_{REF}}$$

$$V_{out} = V_{BG} * \left(\frac{R_{FB}}{R_{REF}}\right) * \left(\frac{1}{N_{PS}}\right) - V_f - I_{sec} * ESR$$

-Another advantage of the controller is indicating the inductance limitations which are upper and lower bounds for the transformer design. This part will be explained in the transformer design step.

$$\frac{V_{IN(MAX)} * R_{SENSE} * t_{ON(MIN)}}{V_{SENSE(MIN)}} \leq L_{PRI} \leq \frac{V_{IN(MIN)} * (V_{OUT} + V_{F(DIODE)}) * N_{PS}}{f_{SW(MIN)} * I_{LIM} * ((V_{OUT} + V_{F(DIODE)}) * N_{PS} + V_{IN(MIN)})}$$

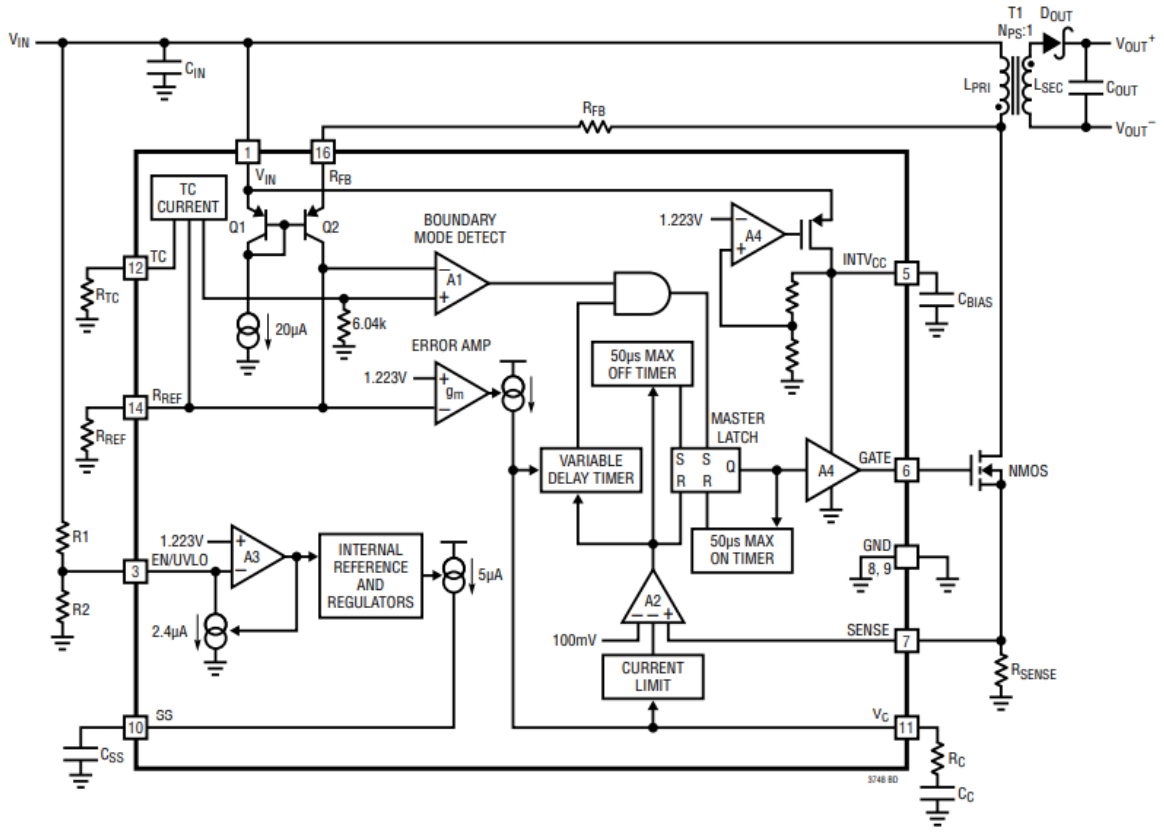


Figure 4 Block diagram of the LT3748

The manufacturer of this controller which is Analog Devices, has created the LTspice models for this chip. Thanks to that, we have implemented the schematic of the flyback converter with LT3748.

Another chosen controller is LM51561 which is created by Texas Instruments. This controller is the second option for us. The advantages of this controller are wide and controllable input range, controllable output voltage, small size and low cost, and constant peak current limiting over input. The features of the LM51561 are similar to the LT3748. Both of them are ordered and the applications will be started with the LT3748.

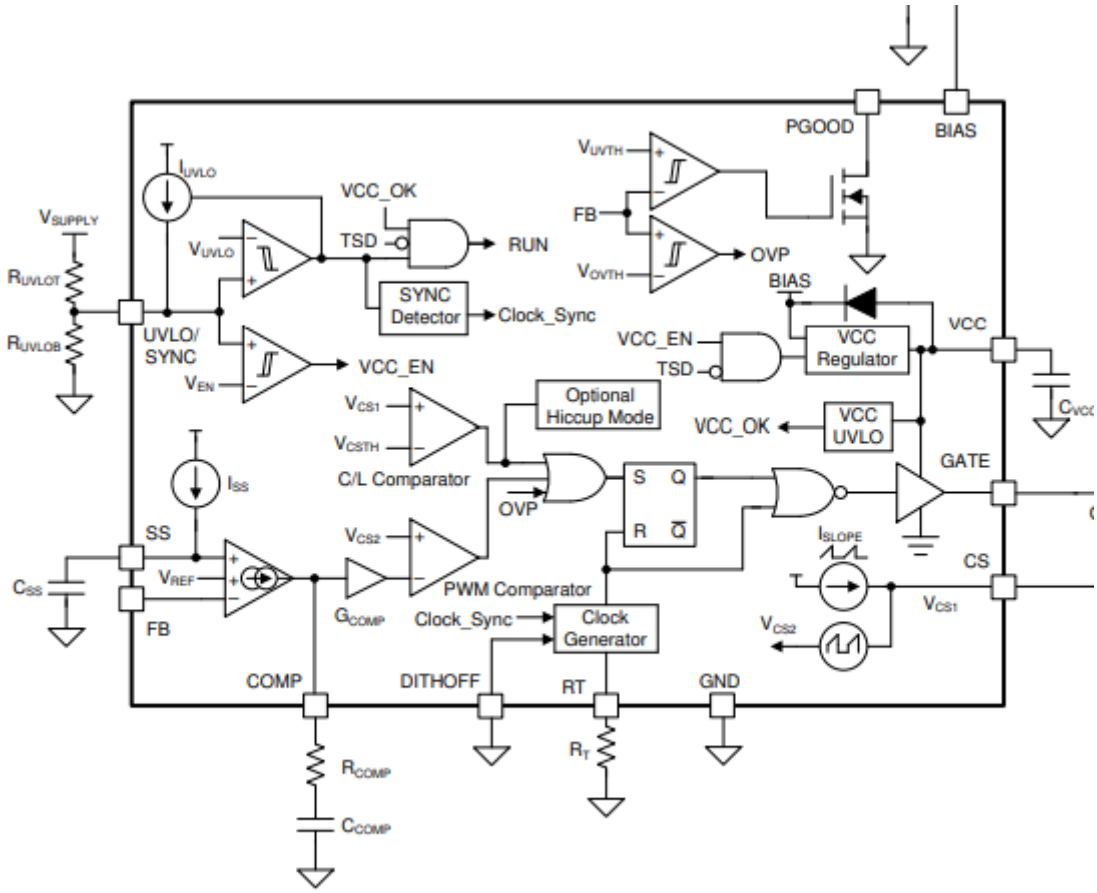


Figure 5 Block diagram of the LM56511

Our last option for the controller is using STM32 or Arduino to control the converter. At this point, the controller was designed to change the D_{ON} and D_{off} time.

SNUBBER DESIGN

The voltage increase at the drain side of the MOSFET, when the switch is off, appearing because of the leakage inductance of the transformer. When the current at the input side is high enough, more stored energy needs to be dissipated. Because of that, leakage inductances of the transformer need to be minimized. Considering the inadequacy or failure of the snubber circuitry, the V_{DS} voltage rating of the MOSFET can be chosen with the safety margin. There are different kinds of snubber circuit designs that exist. One of the popular ones is the RCD snubber circuit. Another one is the Zener snubber circuit. The advantage of the Zener suppressing circuit is dissipating the power when the voltage reaches the dangerous voltage level for the MOSFET.

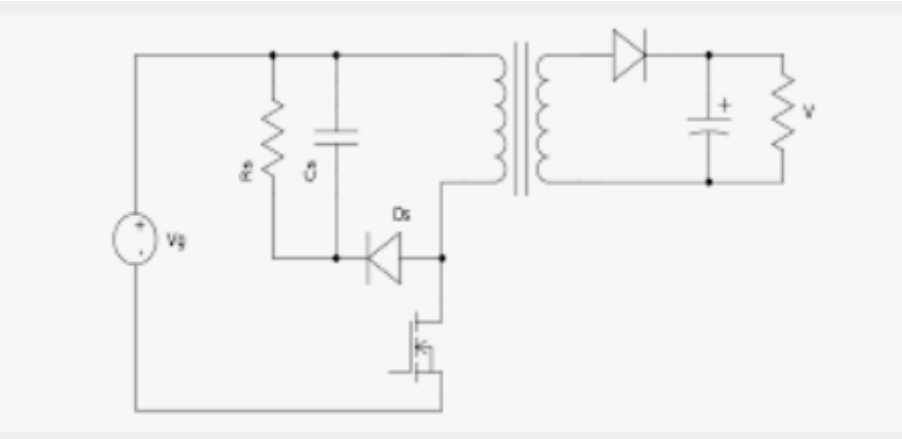


Figure 6 RCD Snubber circuitry

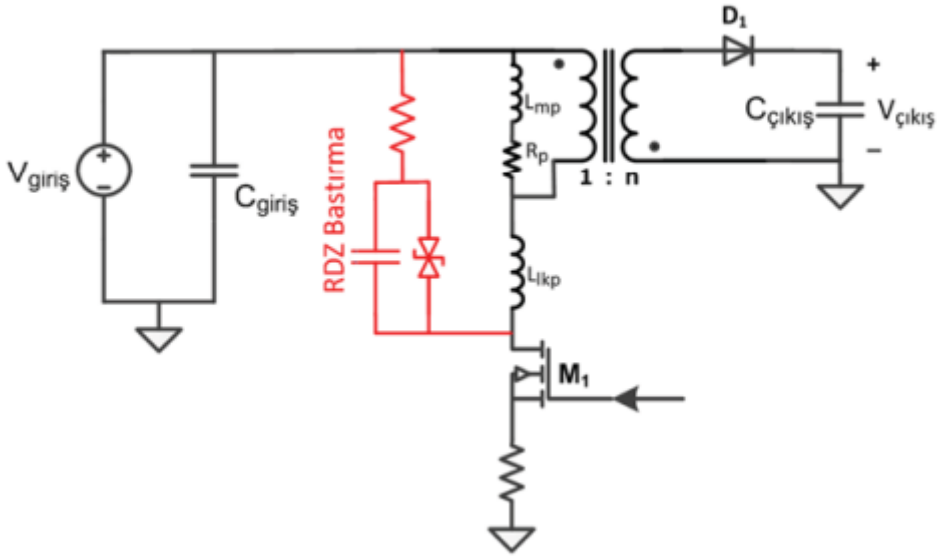


Figure 7 Snubber Circuit with Zener Diode

The advised approach for designing the snubber circuitry is measuring the period of the ringing when the switch is off without snubber circuitry. After that, the snubber capacitor needs to be added to the circuit starting from the feasible capacitance like 100pF. When the damping period reaches 1.5 -2 times longer, the capacitor is chosen. The change in period can determine the value of the parasitic capacitance, and the initial period of the damping can determine the leakage inductance. In addition to that, those values can be determined from the leakage inductance of the transformer and switch capacitance. When this inductance and capacitance value is determined, the resistance of the snubber needs to be decided.

$$C_{PAR} = \frac{C_{SNUBBER}}{\left(\frac{t_{PERIOD(SNUBBERED)}}{t_{PERIOD}}\right)^2 - 1}$$

$$L_{PAR} = \frac{t_{PERIOD}^2}{C_{PAR} * 4 * \pi^2}$$

$$R_{SNUBBER} = \sqrt{\frac{L_{PAR}}{C_{PAR}}}$$

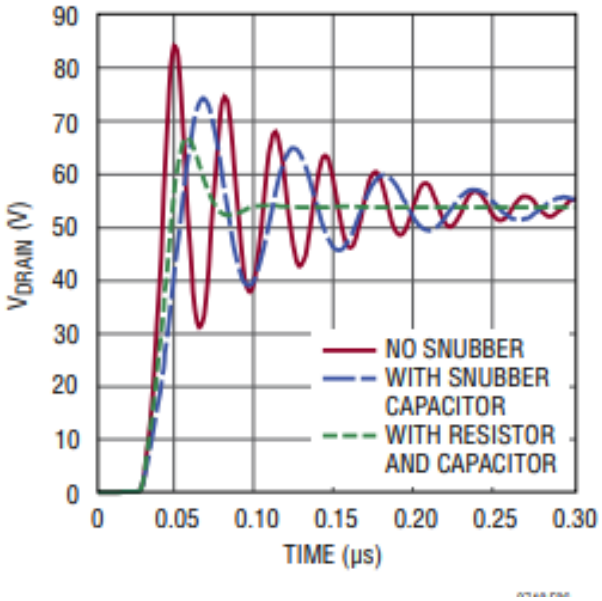


Figure 8 Effect of the Snubber taken from the Datasheet of the LT3748

Dissipated power will be equal to:

$$P_{SNUBBER} = f_{SW} * C_{SNUBBER} * \frac{V_{DRAIN}^2}{2}$$

TRANSFORMER DESIGN

For the transformer design, the start point was the controller's limitations. According to the chosen IC LT3748, primary inductance has the following limitations:

$$\frac{V_{IN(MAX)} * R_{SENSE} * t_{ON(MIN)}}{V_{SENSE(MIN)}} \leq L_{PRI} \leq \frac{V_{IN(MIN)} * (V_{OUT} + V_{F(DIODE)}) * N_{PS}}{f_{SW(MIN)} * I_{LIM} * ((V_{OUT} + V_{F(DIODE)}) * N_{PS} + V_{IN(MIN)})}$$

$$where\ V_{SENSE(MIN)} = 15mV, t_{ON(MIN)} = 250ns, N_{PS} = 1.2\ (chosen\ by\ us), R_{SENSE} = 11m\Omega,$$
$$I_{LIM} = \frac{100mV}{R_{SENSE}} = 9A, V_{F(DIODE)} = 0.7V$$

The gain formula of the flyback converter is $\frac{V_o}{V_{in}} = \frac{D}{(1-D)N_{PS}}$. So, for the max V_{in}, D=0.27. For the min V_{in}, D=0.43. The operating frequency is chosen as 80 kHz. Hence, $t_{on(min)}=D_{min}/f_{sw}$=3.37 µs.

So $8.8\ \mu H \leq L_{PRI} \leq 76.6\ \mu H$.

L_{PRI} is chosen as 55 µH inside these constraints. After this step, the core was chosen by the following step:

$$A_{core} * A_{window} = \frac{P_{out}}{2 * efficiency * k_{cu} * J * B * f} = 1953\ mm^4$$

$where\ parameters\ chosen\ as\ k_{cu} = 0.3, J = 3\frac{A}{mm^2}\ , B = 0.2\ T, f = 80\ kHz, efficiency = 0.8.$

According to these, the most suitable core was KOOL MU 00K3515E090 since it has the lowest $A_{core} * A_{window}$ multiplication. Then, turn numbers found with the parameters of this core:

$$L = 55\ \mu H = \frac{N^2}{R} where\ R = \frac{1}{A_l} and\ A_l = \frac{146nH}{T^2} \rightarrow N_{pri} = \sqrt{\frac{55\mu H}{A_l}} = 19 \rightarrow N_{sec} = 15.8$$

After finding the turns number, by using the RMS values of the primary and secondary side currents, cable selection was made:

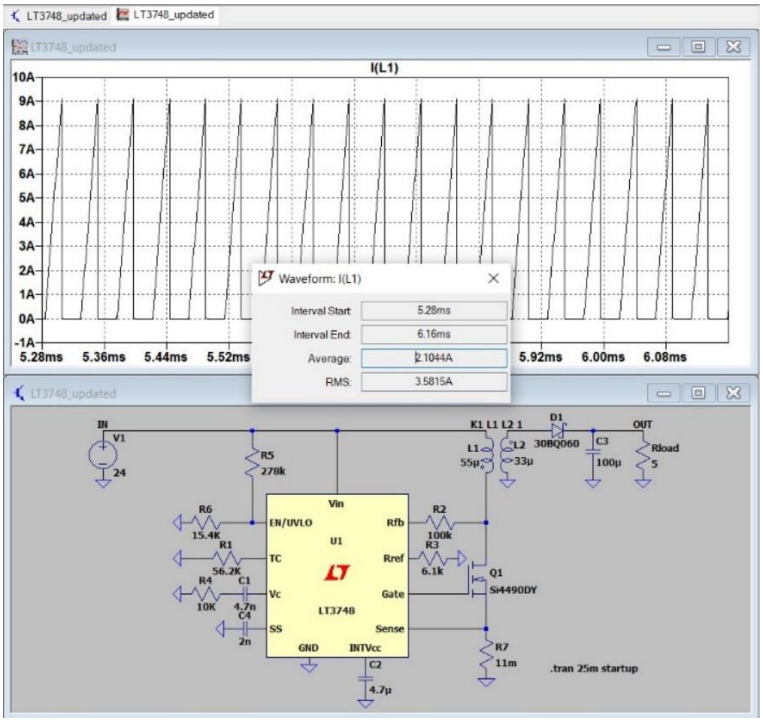


Figure 9 Primary side rms current

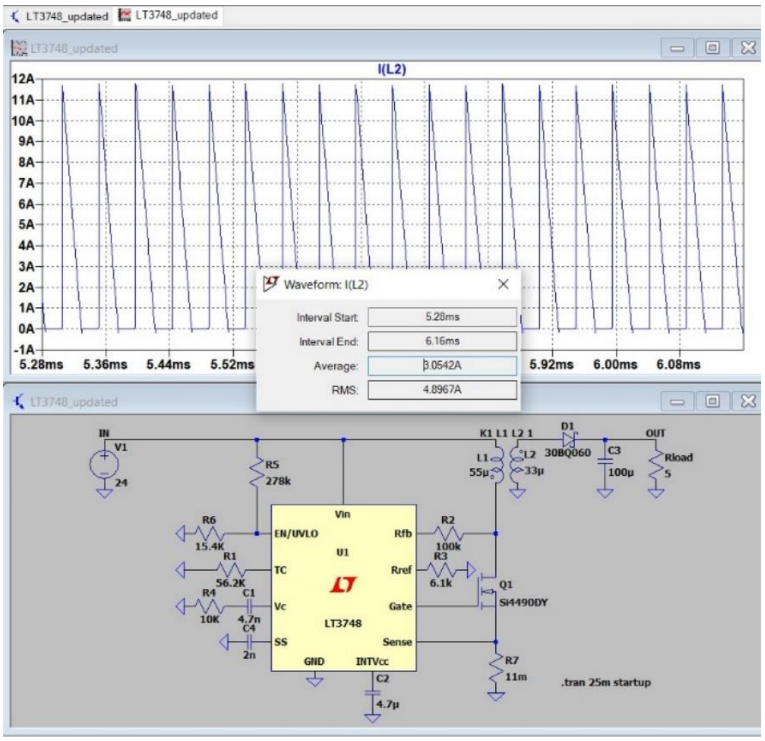


Figure 10 Secondary side RMS current

According to the simulations, the primary side voltage is a maximum 3.6 A. Secondary side voltage is a maximum 4.8 A. For a safety margin, the primary side current was chosen as 4A, and the secondary side voltage was chosen as 5A.

- For the primary side: $Cross\ section = \frac{4A}{\frac{3A}{mm^2}} = 1.33\ mm^2$
- For the secondary side: $Cross\ section = \frac{5A}{3A/mm\hat{}2} = 1.67\ mm^2$

For the cable selection, AWG 26 cable was chosen due to the high operating frequency margin. However, in the lab, there was AWG 25 cable with 0.162 mm^2 cross-section area and %100 skin depth at 85 kHz. Hence, we carried on with this cable.

- For the primary side: $\#\ of\ parallels = \frac{1.33mm^2}{0.162mm^2} = 8$
- For the secondary side: $\#\ of\ parallels = \frac{1.67mm^2}{0.162mm^2} \cong 11$

After we implemented the cables in the lab, they did not fit into the selected core. In real life, it showed us with these cable selections and turns number, the fill factor must be higher than 1. So, the core selection is changed again.

After we searched the core inventory, the most suitable core was ferrite 0P44022EC core since, due to its material, leakage would be much less than the kool mu core. Also, its cross-section and window area is large enough to fit the cables. Then, all the calculations were made for this core. For the turn number, A_l value of the core is important. So, if we change the A_l value of the core by adding an air gap to the core, we can acquire the desired turn numbers.

- Let's assume the turn numbers as N_{pri} = 12, N_{sec} = 9.5
- So, $A_l = \frac{L}{N_{pri}^2} = 382\,\frac{nH}{T^2}$

- $R_{new} = \frac{1}{A_l} = 2.62 * 10^6 H^{-1} = \frac{1}{A_{l(nominal)}} + \frac{l_{airgap}}{\mu_0 * A_{cross}} \rightarrow l_{airgap} = 0.72mm$

So, by adding this air gap to the core, we can obtain the required reluctance value. If we calculate the magnetic flux density as

$$B = \frac{N_{pri} * I_{peak}}{R_{new} * A_{cross}} = 0.18\,T \; where \; I_{peak} = 9A$$

Hence, by this calculation, we can see that core is not saturated. It is not the expected value since we did all the calculations for B= 0.2 T. However, this result is close enough to the expected value, and it does not saturate the core. After that, the fill factor is calculated as follows:

$$k_{cu} = \frac{N_{pri} * 8 * 0.162mm^2 + N_{sec} * 11 * 0.162mm^2}{A_{window}} = 0.12$$

It can be deducted that the fill factor is very small, and it shows that the core is overdesigned for this situation. However, since we built the transformer by hand, the fill factor is not high enough.

IMPLEMENTATION

The transformer was implemented according to calculations. However, as expected, real-life and theoretical calculations did not match exactly. After implementing the transformer, we did the measurements.

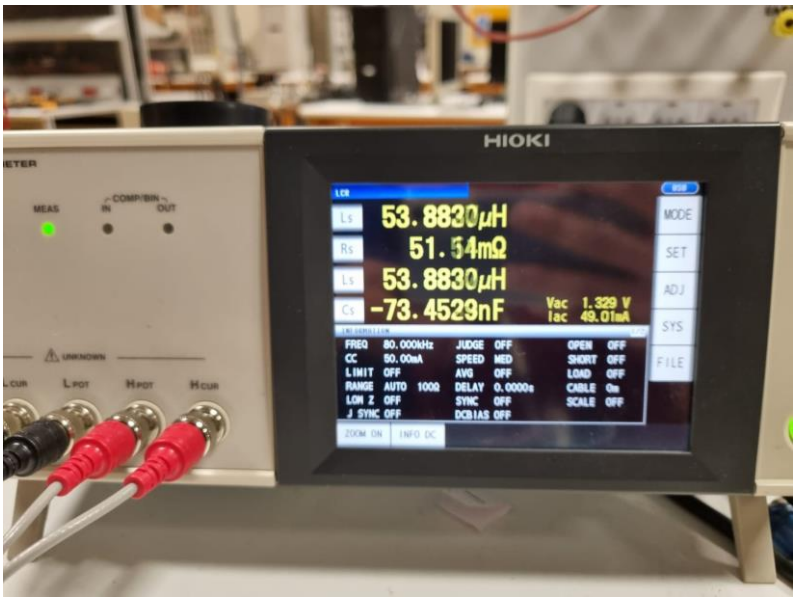


Figure 11 Primary side inductance

For the primary side inductance measurement, which is magnetizing inductance, we left open the secondary side and connected the probes of the LCR meter to the primary side. The result of the measurement can be seen in Fig.11. The expected value was 55 µH, but it was measured as 53 µH. It is very close to the expected value.

Figure 12 Secondary side inductance

For the secondary side inductance measurement, we left open the primary side and connected the probes of the LCR meter to the secondary side. The result of the measurement can be seen in Figure 12. It was measured as 36 µH.

If the turns ratio is checked by the inductance values, the turns ratio can be found as

$$N = \sqrt{\frac{55\ \mu\text{H}}{36\ \mu\text{H}}} = 1.23$$

So, the turns ratio is satisfied by the inductance values.

Figure 13 Leakage inductance value

For the leakage inductance, we shorted the secondary side and connected the probes to the primary side. The connection can be seen in Figure 14. Since it was thought that we might change the turns in the future, excess cables did not cut out. Hence, resulted in more leakage inductance of 2.6 µH, which can be seen in Figure 13.

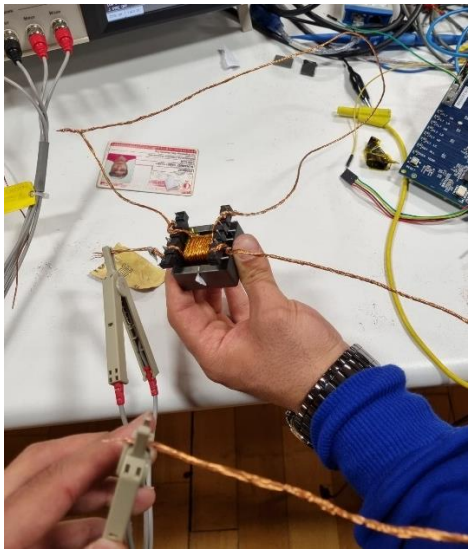


Figure 14 Leakage inductance measurement

LOSSES

Copper Losses

For the copper losses, we need to find how much cable is used. To obtain this information, dimensions of the core must be known

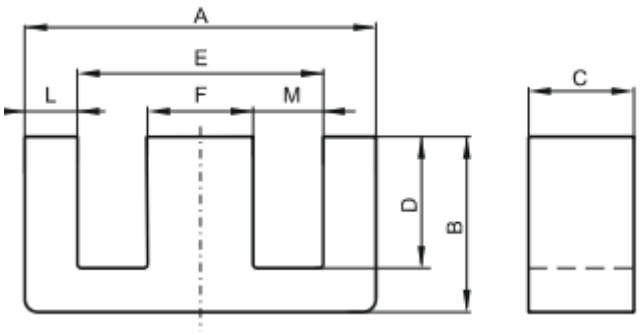


Figure 15 Dimensions of the core

Dimensions of the core are represented in the figure above. According to this figure,

$$MLT = 2\pi * \frac{E-F}{4} = 27\ mm, R = \ 106.2 * 10^{-6}\ \Omega/mm$$

$$R_{pri} = \frac{N_{pri} * MLT * R}{8} = 4.3m\Omega, R_{sec} = \frac{N_{sec} * MLT * R}{11} = 2.4m\Omega$$

$$P_{cu,total} = I_{pri,rms}^2 * R_{pri} + I_{sec,rms}^2 * R_{sec} = 0.49W$$

Core Loss

According to the core loss per cm^3 value of the core, approximate core loss is calculated as follows:

$$Core\ Loss = \frac{128mW}{cm^3} * 22.7cm^3 = 2.9\ W$$

Since we are operating at high frequencies, core losses are much higher than the copper losses, and it is expected.

COMPONENT CALCULATIONS

Output Capacitor

From the voltage gain expression of the flyback converter, our duty cycle becomes

$\frac{15}{Vin}$ = N_{21} * $\frac{D}{1-D}$ where N_{12} is chosen as 1.23

So, the duty limits become 0.44 for 24V input and 0.28 for 48V input.

$$\frac{\Delta Vo}{Vo} = \frac{D}{RCf} = 0.03$$

D/(0.03*5*80kHz) = C_o

C_o has to be at least 36.7 µF (For 24 V input voltage) from the converter equations.

On the other hand, from the LT3748 datasheet output capacitor can be specified as

$$I_{OUT(MAX)} \approx 0.85 \bullet (1 - D) \bullet N_{PS} \bullet I_{LIM}/2$$

Figure 16 Output Voltage Equation with respect to Limiting Current

$I_{LIM} = \frac{2*3}{1.3*0.85*(1-0.37)}$ = 8.62A (Duty approximated as 0.37)

$$\Delta V_{MAX} = \frac{L_{PRI} \bullet I_{LIM}^2}{2 \bullet C_{OUT} \bullet V_{OUT}}$$

Figure 17 Output Capacitor Equation from the LT3748 Datasheet

$$0.03*15 = \frac{55*10^{-6}*8.62^2}{2*C*15}$$

C_o = 302.72 µF

Diode and Switch

$$I_{DIODE(RMS)} = \sqrt{(I_{LIM} \bullet N_{PS})^2 \bullet (1 - D)/3}$$

Figure 18 Diode RMS Current Equation from the Datasheet

$I_{D(RMS)} = \sqrt{(8.62 * 1.23)^2(1 - 0.37)/3}$ = 4.86A

Peak Switch Current

$$\hat{I}_{sw} = \frac{1}{(1-D)} \frac{N_2}{N_1} I_o + \frac{N_1}{N_2} \frac{(1-D)T_s}{2L_m} V_o$$

Peak Switch Voltage

$$\hat{V}_{sw} = V_d + \frac{N_1}{N_2} V_o = \frac{V_d}{(1-D)}$$

Figure 19 Peak Values for Switch

$$I_{MOSFET(RMS)} = \sqrt{I_{LIM}^2 \bullet D/3}$$

Figure 20 MOSFET RMS Current Equation from the Datasheet

$I_{MOS(RMS)} = \sqrt{(0.37/3) * 8.62^2}$ = 3.03A

$V_{sw(max)}$ = 48/(1-0.28) = 66.7V

$I_{sw(max)}$ = 3/0.8856+ 5.6 ≈ 12.07A (where L_m is 55 µH)

Feedback and Reference Resistances

$$V_{OUT} = V_{BG}\left(\frac{R_{FB}}{R_{REF}}\right)\left(\frac{1}{N_{PS}}\right) - V_F - I_{SEC}\,(ESR)$$

Figure 21 Output voltage equation from the datasheet

Where V_{BG} bandgap voltage for a silicon switch is around 1.2 V,

$N_{PS} = N_1/N_2 = 1.23$,

the forward voltage drop of the diode is 0.64V,

Equivalent series resistance on the secondary side is $\frac{1}{\omega Co}$ //ωL_2//R_o ≈ 0

$\frac{R_{FB}}{R_{REF}}$ = 16.03

So, when R_{REF} is given as 6.1kΩ (limited in the datasheet) R_{FB} becomes around 97kΩ.

SIMULATION RESULTS AND COMPONENT SELECTION

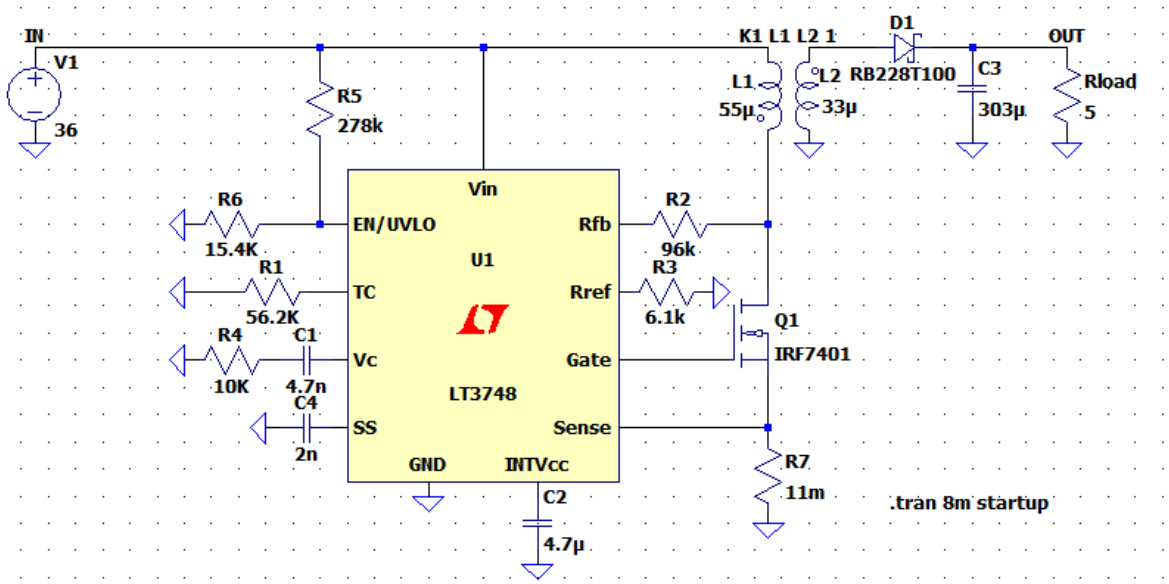


Figure 22 Circuit Diagram for the overall design with LT3748

Due to the above calculations in the previous section, the simulation circuit has been set, as seen in Figure 22.

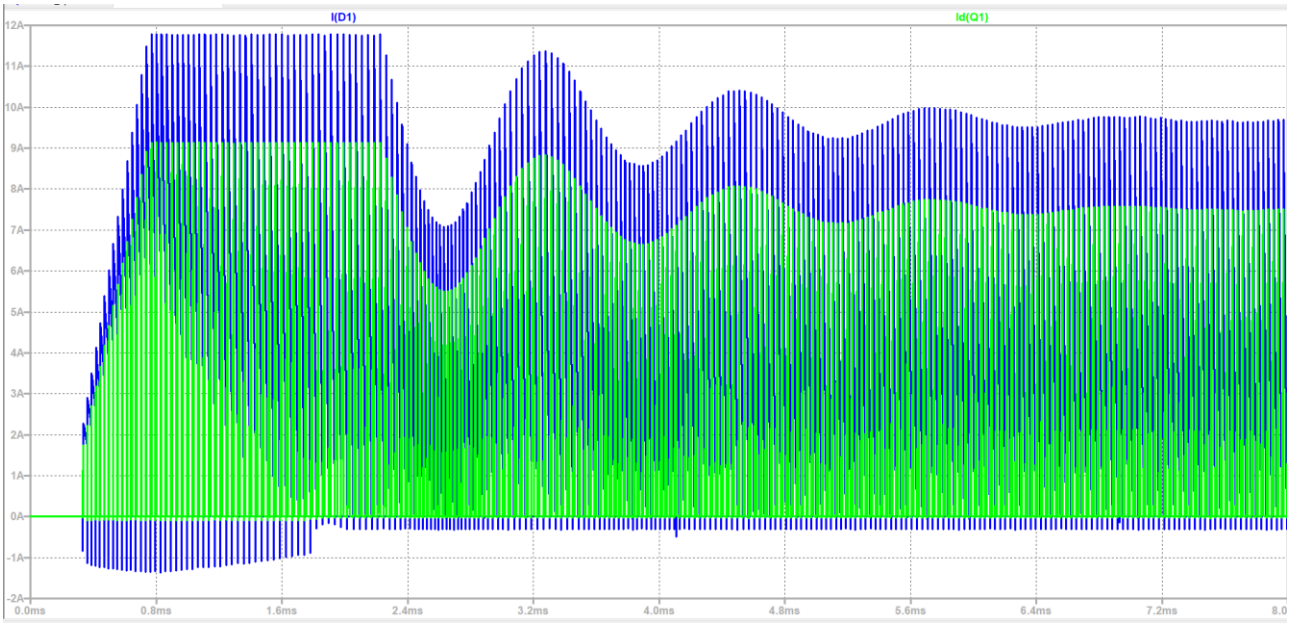


Figure 23 Diode and Switch Currents for the Transient Part

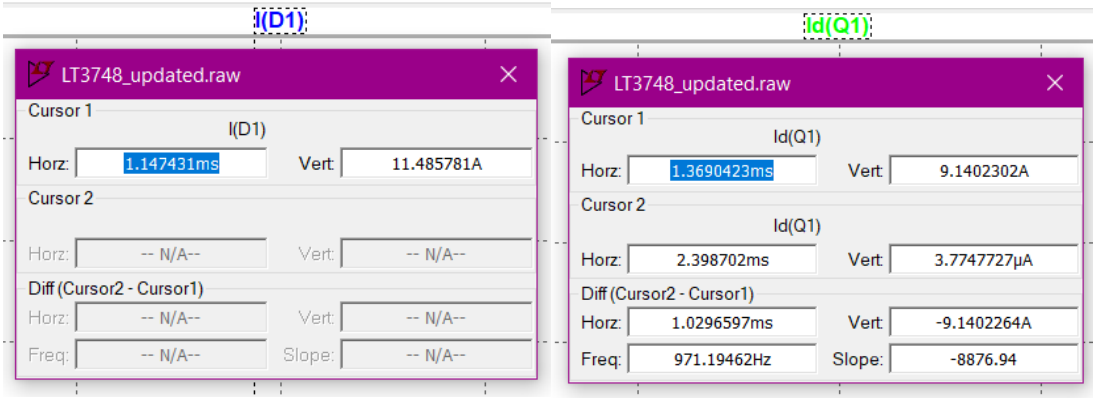


Figure 24 Diode and Switch Current Maxima

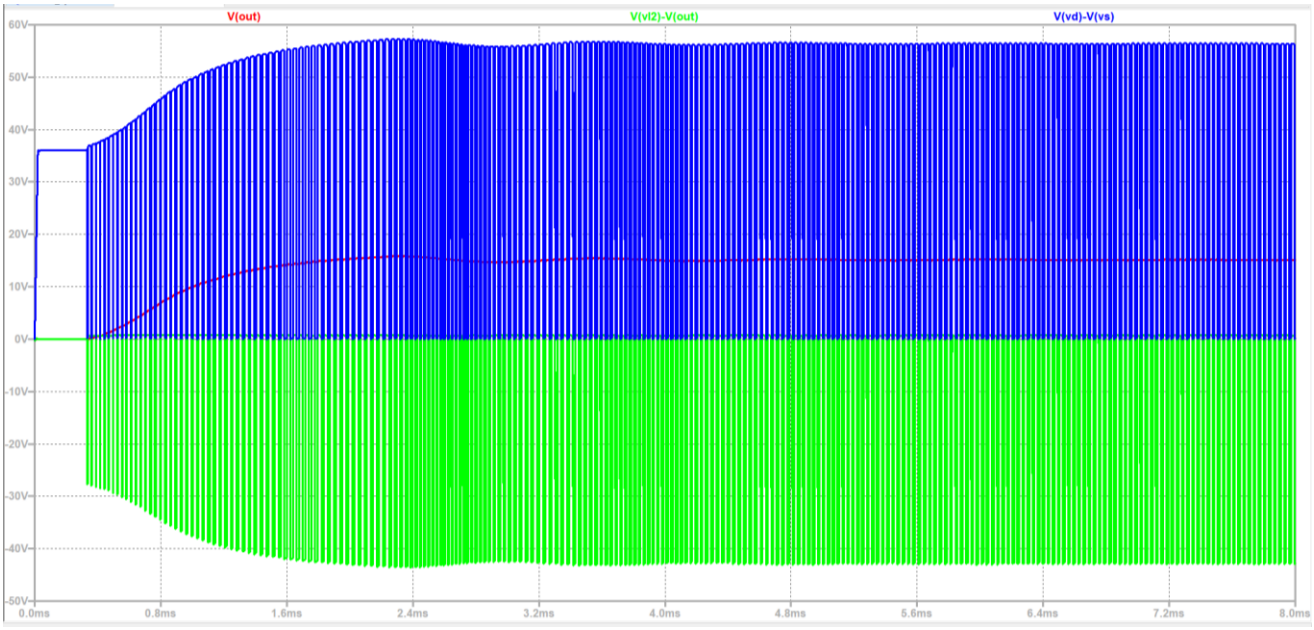


Figure 25 Diode and switch voltages

As seen in Figures 24 and 23, the diode selected must be able to handle at least 12 amperes, and the switch must handle 10 amperes. Also, Figure 25 shows that the switch must endure 60 volts, and the diode must handle at least 55 volts.

For simplicity, the switch is chosen from the lab inventory since the components match with the ratings. IRF540 N-type MOSFET is chosen since it has 100V-27A ratings that can handle our circuit's needs. For the diode, DS16-01AS-TRL with 100V-16A ratings is chosen.

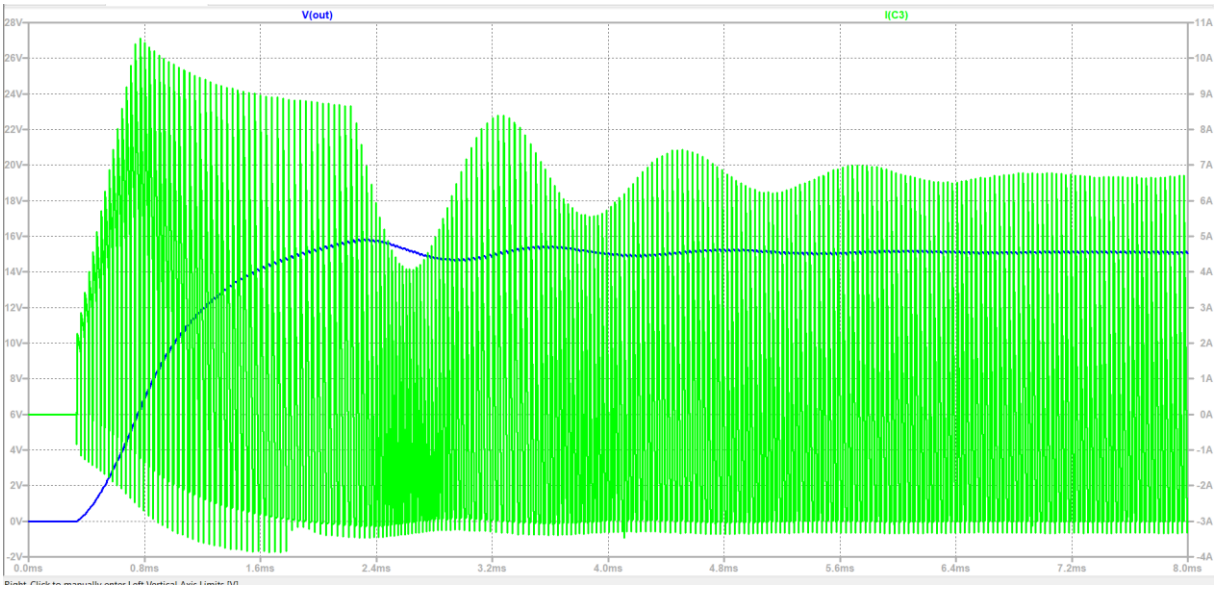


Figure 26 Output capacitor voltage and current for the transient interval

As obtained in Figure 26, the output voltage sees almost 16 volts in the transient time interval, so the output capacitor must bear this voltage. Also, the current seen by this capacitor reaches almost 11

amperes. After checking the most accessible stocks, the **SD1V337M1012MPA** capacitor has been our choice. This capacitor is 330µF and can handle 35V & 0.63A ripple current.

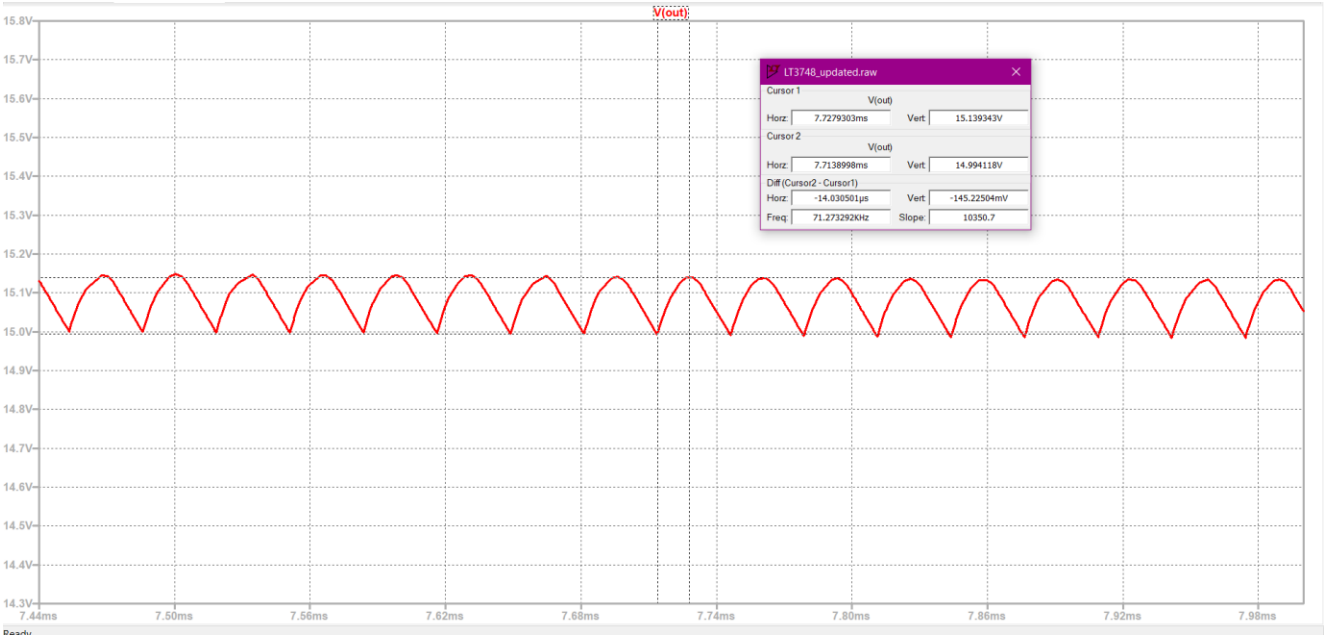


Figure 27 Output Voltage Ripple

As seen in Fig.27, the output ripple is around 0.15 Volts.

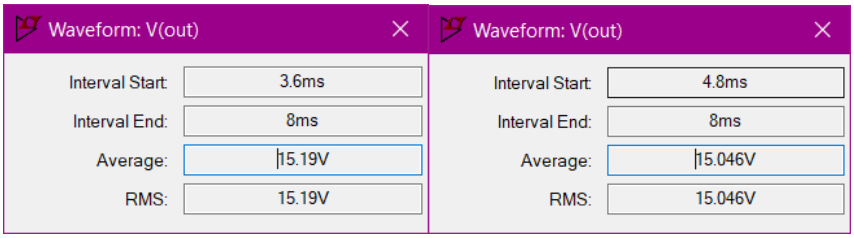


Figure 28 V_{out} deviation when the input goes from 24V to 48V

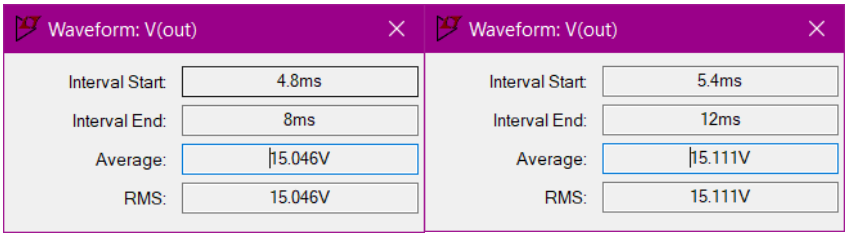


Figure 29 V_{out} deviation when I_o changes from 100% to 10%

Line regulation from our simulation can be seen in Fig.27 as (15.19-15.046) * 100/15.19 = 0.947 % and load regulation can be seen in Figure 28 as (15.111-15.046) * 100/15.111 = 0.43%

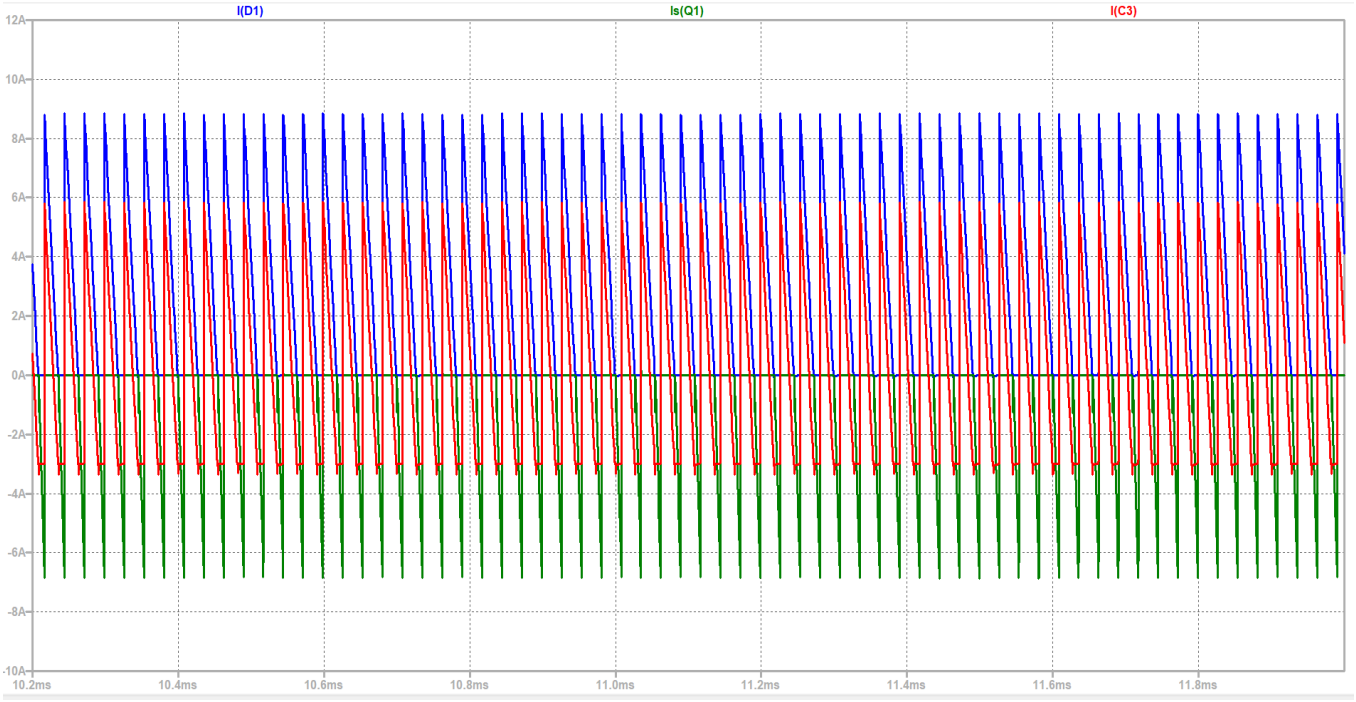


Figure 30 I_{Diode}, I_{DS} and I_C at Steady State

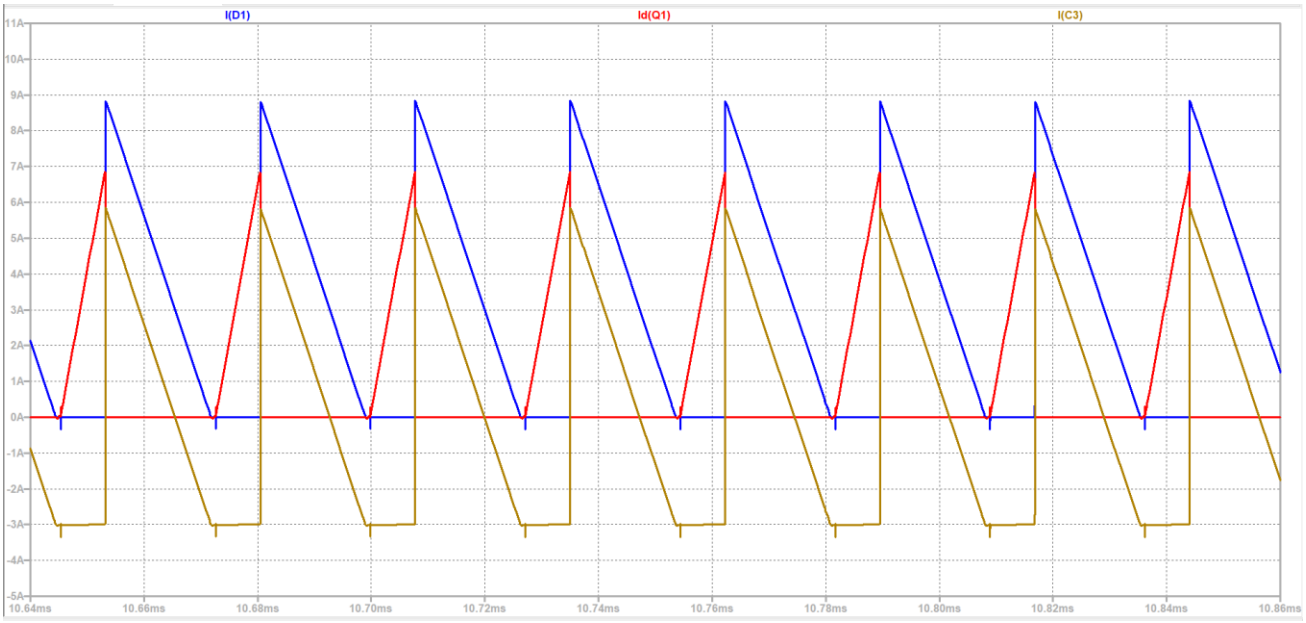


Figure 31 I_{Diode}, I_{DS} and I_C waveforms

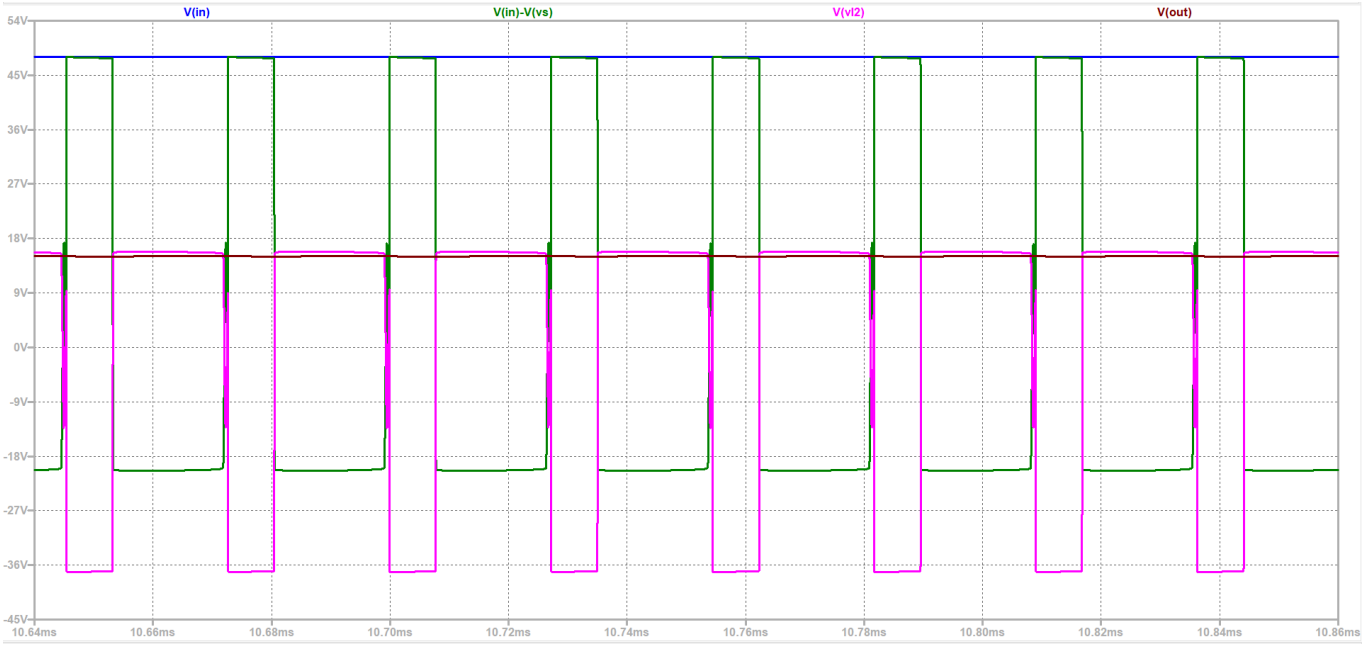


Figure 32 V_{in}, V_{out}, V_{L1} and V_{L2} voltage waveforms

THERMAL CALCULATIONS

Mosfet

$P_{cond} = R_{ds}*I^2_{ds(rms)} = 0.04*2.15^2 = 0.185W$

$P_{sw} = V_{in}*I_o*f_{sw}*(t_r+t_f) = 48*3*80kHz*(55+57\ ns) = 1.3W$

$T_{junc} = T_a + P_{loss} * R_{ja} = 30+ (1.485*62) = 122.07^oC$ (Ambient temperature is taken as 30^oC)

$R_{HA} = R_{JA} – R_{CH} – R_{JC} = 62 -1.25$

So, the heatsink thermal resistance must be less than $60.75^oC/W$.

Diode

$P_{cond} = V_f*I_{f(avg)} = 0.64*3.18 = 2.04W$

$P_{sw} = Q_R * V_{RR}*f_s$ where Q_R can be approximated as $0.5*I_{RM}*t_{RR}$ but since our diode is a Schottky diode, reverse recovery time is very small, thus switching losses can be ignored for now.

Assuming 100^oC junction temperature and 30^oC ambient,

$R_{HA} = (T_j-T_a)/P_{loss} – R_{CH} – R_{JC}$

$R_{HA} = 70/2.04 – 0.5 - 1.4 = 32.5$

So, the diode's heatsink thermal resistance must be less than $32.5^oC/W$

CONCLUSION

This report focused on the design of an isolated 24-48V to 15V @45W DC-DC converter. The chosen topology of flyback converter is discussed and applicable controller options has been examined. LT3748 isolated flyback controller has been chosen. An appropriate magnetic core has been chosen and magnetic design is done and implemented on the core. Analytical calculations for controller needed components and flyback components are done, and appropriate connections has been made in LTSPICE environment. After observing the ratings of the simulations, appropriate semiconductors and other passive components have been chosen. Thermal calculations for semiconductor devices have been done and design report is finalized.

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